

Welcome to E-XFL.COM

#### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

#### Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

E·XFI

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	-
Connectivity	CANbus, I <sup>2</sup> C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I <sup>2</sup> S, Motor Control PWM, POR, PWM, WDT
Number of I/O	35
Program Memory Size	256КВ (85.5К х 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	-
Data Converters	A/D 18x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep256gm604-h-ml

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

## 4.2 Data Address Space

The dsPIC33EPXXXGM3XX/6XX/7XX CPU has a separate 16-bit wide data memory space. The Data Space is accessed using separate Address Generation Units (AGUs) for read and write operations. The data memory maps, which are presented by device family and memory size, are shown in Figure 4-5 through Figure 4-7.

All Effective Addresses (EAs) in the data memory space are 16 bits wide and point to bytes within the Data Space. This arrangement gives a Base Data Space address range of 64 Kbytes or 32K words.

The Base Data Space address is used in conjunction with a Data Space Read or Write Page register (DSRPAG or DSWPAG) to form an Extended Data Space, which has a total address range of 16 Mbytes.

dsPIC33EPXXXGM3XX/6XX/7XX devices implement up to 52 Kbytes of data memory (4 Kbytes of data memory for Special Function Registers and up to 48 Kbytes of data memory for RAM). If an EA points to a location outside of this area, an all zero word or byte is returned.

#### 4.2.1 DATA SPACE WIDTH

The data memory space is organized in byteaddressable, 16-bit wide blocks. Data is aligned in data memory and registers as 16-bit words, but all Data Space EAs resolve to bytes. The Least Significant Bytes (LSBs) of each word have even addresses, while the Most Significant Bytes (MSBs) have odd addresses.

#### 4.2.2 DATA MEMORY ORGANIZATION AND ALIGNMENT

To maintain backward compatibility with PIC<sup>®</sup> MCU devices and improve Data Space memory usage efficiency, the dsPIC33EPXXXGM3XX/6XX/7XX instruction set supports both word and byte operations. As a consequence of byte accessibility, all Effective Address calculations are internally scaled to step through word-aligned memory. For example, the core recognizes that Post-Modified Register Indirect Addressing mode [Ws++] results in a value of Ws + 1 for byte operations and Ws + 2 for word operations.

A data byte read, reads the complete word that contains the byte, using the LSb of any EA to determine which byte to select. The selected byte is placed onto the LSB of the data path. That is, data memory and registers are organized as two parallel, byte-wide entities with shared (word) address decode but separate write lines. Data byte writes only write to the corresponding side of the array or register that matches the byte address. All word accesses must be aligned to an even address. Misaligned word data fetches are not supported, so care must be taken when mixing byte and word operations, or translating from 8-bit MCU code. If a misaligned read or write is attempted, an address error trap is generated. If the error occurred on a read, the instruction underway is completed. If the error occurred on a write, the instruction is executed but the write does not occur. In either case, a trap is then executed, allowing the system and/or user application to examine the machine state prior to execution of the address Fault.

All byte loads into any W register are loaded into the LSB; the MSB is not modified.

A Sign-Extend (SE) instruction is provided to allow user applications to translate 8-bit signed data to 16-bit signed values. Alternatively, for 16-bit unsigned data, user applications can clear the MSB of any W register by executing a Zero-Extend (ZE) instruction on the appropriate address.

#### 4.2.3 SFR SPACE

The first 4 Kbytes of the Near Data Space, from 0x0000 to 0x0FFF, is primarily occupied by Special Function Registers (SFRs). These are used by the dsPIC33EPXXXGM3XX/6XX/7XX core and peripheral modules for controlling the operation of the device.

SFRs are distributed among the modules that they control and are generally grouped together by module. Much of the SFR space contains unused addresses; these are read as '0'.

**Note:** The actual set of peripheral features and interrupts varies by the device. Refer to the corresponding device tables and pinout diagrams for device-specific information.

#### 4.2.4 NEAR DATA SPACE

The 8-Kbyte area, between 0x0000 and 0x1FFF, is referred to as the Near Data Space. Locations in this space are directly addressable through a 13-bit absolute address field within all memory direct instructions. Additionally, the whole Data Space is addressable using MOV instructions, which support Memory Direct Addressing mode with a 16-bit address field, or by using Indirect Addressing mode using a Working register as an Address Pointer.

## 4.2.5 X AND Y DATA SPACES

The dsPIC33EP core has two Data Spaces: X and Y. These Data Spaces can be considered either separate (for some DSP instructions) or as one unified linear address range (for MCU instructions). The Data Spaces are accessed using two Address Generation Units (AGUs) and separate data paths. This feature allows certain instructions to concurrently fetch two words from RAM, thereby enabling efficient execution of DSP algorithms, such as Finite Impulse Response (FIR) filtering and Fast Fourier Transform (FFT).

The X Data Space is used by all instructions and supports all addressing modes. The X Data Space has separate read and write data buses. The X read data bus is the read data path for all instructions that view Data Space as combined X and Y address space. It is also the X data prefetch path for the dual operand DSP instructions (MAC class).

The Y Data Space is used in concert with the X Data Space by the MAC class of instructions (CLR, ED, EDAC, MAC, MOVSAC, MPY, MPY. N and MSC) to provide two concurrent data read paths.

Both the X and Y Data Spaces support Modulo Addressing mode for all instructions, subject to addressing mode restrictions. Bit-Reversed Addressing mode is only supported for writes to X Data Space.

All data memory writes, including in DSP instructions, view Data Space as combined X and Y address space. The boundary between the X and Y Data Spaces is device-dependent and is not user-programmable.

IADLL	<b>-</b> -J.																	
SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
IC1CON1	0140		—	ICSIDL	ICTSEL2	ICTSEL1	ICTSEL0	_	_	—	ICI1	ICI0	ICOV	ICBNE	ICM2	ICM1	ICM0	0000
IC1CON2	0142	_	_	-	_	—	_	_	IC32	ICTRIG	TRIGSTAT	—	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0	000D
IC1BUF	0144								Input Cap	ture 1 Buff	er Register							xxxx
IC1TMR	0146								Input Cap	ture 1 Tim	er Register							0000
IC2CON1	0148	_	_	ICSIDL	ICTSEL2	ICTSEL1	ICTSEL0	_	-	_	ICI1	ICI0	ICOV	ICBNE	ICM2	ICM1	ICM0	0000
IC2CON2	014A	_	_	-	_	_	_	_	IC32	ICTRIG	TRIGSTAT	_	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0	000D
IC2BUF	014C								Input Cap	ture 2 Buff	er Register							xxxx
IC2TMR	014E								Input Cap	ture 2 Tim	er Register							0000
IC3CON1	0150	_	_	ICSIDL	ICTSEL2	ICTSEL1	ICTSEL0	_	-	_	ICI1	ICI0	ICOV	ICBNE	ICM2	ICM1	ICM0	0000
IC3CON2	0152	_	_	-	_	_	_	_	IC32	ICTRIG	TRIGSTAT	_	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0	000D
IC3BUF	0154								Input Cap	ture 3 Buff	er Register							xxxx
IC3TMR	0156								Input Cap	ture 3 Tim	er Register							0000
IC4CON1	0158		—	ICSIDL	ICTSEL2	ICTSEL1	ICTSEL0		—	—	ICI1	ICI0	ICOV	ICBNE	ICM2	ICM1	ICM0	0000
IC4CON2	015A		—	—	—	—	—		IC32	ICTRIG	TRIGSTAT	—	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0	000D
IC4BUF	015C								Input Cap	ture 4 Buff	er Register							xxxx
IC4TMR	015E								Input Cap	ture 4 Tim	er Register							0000
IC5CON1	0160	_	—	ICSIDL	ICTSEL2	ICTSEL1	ICTSEL0	_	—	—	ICI1	ICI0	ICOV	ICBNE	ICM2	ICM1	ICM0	0000
IC5CON2	0162	_	—	—	—	—	—	_	IC32	ICTRIG	TRIGSTAT	—	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0	000D
IC5BUF	0164								Input Cap	ture 5 Buff	er Register							xxxx
IC5TMR	0166								Input Cap	ture 5 Tim	er Register							0000
IC6CON1	0168	_	—	ICSIDL	ICTSEL2	ICTSEL1	ICTSEL0	_	—	—	ICI1	ICI0	ICOV	ICBNE	ICM2	ICM1	ICM0	0000
IC6CON2	016A	_	_	-	_	—	_	—	IC32	ICTRIG	TRIGSTAT	_	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0	000D
IC6BUF	016C								Input Cap	ture 6 Buff	er Register							xxxx
IC6TMR	016E			_					Input Cap	ture 6 Tim	er Register	-	-		-			0000
IC7CON1	0170	_	—	ICSIDL	ICTSEL2	ICTSEL1	ICTSEL0		—	—	ICI1	ICI0	ICOV	ICBNE	ICM2	ICM1	ICM0	0000
IC7CON2	0172	_	—	—	—	—	—	_	IC32	ICTRIG	TRIGSTAT	—	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0	000D
IC7BUF	0174	Input Capture 7 Buffer Register xxxx																
IC7TMR	0176	6 Input Capture 7 Timer Register 0000																
IC8CON1	0178			ICSIDL	ICTSEL2	ICTSEL1	ICTSEL0		—	_	ICI1	ICI0	ICOV	ICBNE	ICM2	ICM1	ICM0	0000
IC8CON2	017A	_	—	—	—	—	—	—	IC32	ICTRIG	TRIGSTAT	—	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0	000D
IC8BUF	017C Input Capture 8 Buffer Register xxxx											xxxx						
IC8TMR	017E								Input Cap	ture 8 Tim	er Register							0000

#### TABLE 4-5: INPUT CAPTURE 1 THROUGH INPUT CAPTURE 8 REGISTER MAP

Legend: x = unknown value on Reset; -- = unimplemented, read as '0'. Reset values are shown in hexadecimal.

## TABLE 4-19: UART3 AND UART4 REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
U3MODE	0250	UARTEN		USIDL	IREN	RTSMD		UEN1	UEN0	WAKE	LPBACK	ABAUD	URXINV	BRGH	PDSEL1	PDSEL0	STSEL	0000
U3STA	0252	UTXISEL1	UTXINV	UTXISEL0	_	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL1	URXISEL0	ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
<b>U3TXREG</b>	0254	_	_	_	_	_	_	_				UART3 T	ransmit Re	gister				xxxx
U3RXREG	0256	_	_	_	_	_	_	_	UART3 Receive Register 0							0000		
U3BRG	0258							Baud	Rate Gene	erator Presca	ler							0000
U4MODE	02B0	UARTEN	_	USIDL	IREN	RTSMD	_	UEN1	UEN0	WAKE	LPBACK	ABAUD	URXINV	BRGH	PDSEL1	PDSEL0	STSEL	0000
U4STA	02B2	UTXISEL1	UTXINV	UTXISEL0	_	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL1	URXISEL0	ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
U4TXREG	02B4	_	_	_	_	_	_	_				UART4 T	ransmit Re	gister				xxxx
U4RXREG	02B6	_	_	_	_	_	_	_	UART4 Receive Register 00								0000	
U4BRG	02B8							Baud	Rate Gene	erator Presca	ler							0000
			<b>D</b> (			( .) D												

Legend: x = unknown value on Reset; - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

## TABLE 4-20: SPI1, SPI2 AND SPI3 REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
SPI1STAT	0240	SPIEN	—	SPISIDL	—	—	SPIBEC2	SPIBEC1	SPIBEC0	SRMPT	SPIROV	SRXMPT	SISEL2	SISEL1	SISEL0	SPITBF	SPIRBF	0000
SPI1CON1	0242	—	—	—	DISSCK	DISSDO	MODE16	SMP	CKE	SSEN	CKP	MSTEN	SPRE2	SPRE1	SPRE0	PPRE1	PPRE0	0000
SPI1CON2	0244	FRMEN	SPIFSD	FRMPOL	—	—		—	—	—	—	—		—	—	FRMDLY	SPIBEN	0000
SPI1BUF	0248							SPI1 Trar	nsmit and Re	ceive Buffe	er Register							0000
SPI2STAT	0260	SPIEN	—	SPISIDL	—	—	SPIBEC2	SPIBEC1	SPIBEC0	SRMPT	SPIROV	SRXMPT	SISEL2	SISEL1	SISEL0	SPITBF	SPIRBF	0000
SPI2CON1	0262	—	—	—	DISSCK	DISSDO	MODE16	SMP	CKE	SSEN	CKP	MSTEN	SPRE2	SPRE1	SPRE0	PPRE1	PPRE0	0000
SPI2CON2	0264	FRMEN	SPIFSD	FRMPOL	—	—	_	—	—	—	—	—	-	—	—	FRMDLY	SPIBEN	0000
SPI2BUF	0268							SPI2 Trar	nsmit and Re	ceive Buffe	er Register							0000
SPI3STAT	02A0	SPIEN	—	SPISIDL	_	—	SPIBEC2	SPIBEC1	SPIBEC0	SRMPT	SPIROV	SRXMPT	SISEL2	SISEL1	SISEL0	SPITBF	SPIRBF	0000
SPI3CON1	02A2	_	_	_	DISSCK	DISSDO	MODE16	SMP	CKE	SSEN	CKP	MSTEN	SPRE2	SPRE1	SPRE0	PPRE1	PPRE0	0000
SPI3CON2	02A4	FRMEN	SPIFSD	FRMPOL	_	_	_	_	_	_	_	_	_	_	_	FRMDLY	SPIBEN	0000
SPI3BUF	02A8	SPI3 Transmit and Receive Buffer Register 0000																

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

# TABLE 4-23: CAN1 REGISTER MAP WHEN WIN (C1CTRL<0>) = 0 OR 1 FOR dsPIC33EPXXXGM60X/7XX DEVICES<sup>(1)</sup>

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
C1CTRL1	0400	—	-	CSIDL	ABAT	CANCKS	REQOP2	REQOP1	REQOP0	OPMODE2	OPMODE1	OPMODE0	-	CANCAP	—	-	WIN	0480
C1CTRL2	0402	—	—	—	_	—	—	—	_	_	_	_			DNCNT<4:0>			0000
C1VEC	0404	_	_	_	FILHIT4	FILHIT3	FILHIT2	FILHIT1	FILHIT0	_	ICODE6	ICODE5	ICODE4	ICODE3	ICODE2	ICODE1	ICODE0	0040
C1FCTRL	0406	DMABS2	DMABS1	DMABS0	—	—	—	—	—	_	_	_	FSA4	FSA3	FSA2	FSA1	FSA0	0000
C1FIFO	0408	—	_	FBP5	FBP4	FBP3	FBP2	FBP1	FBP0	_	-	FNRB5	FNRB4	FNRB3	FNRB2	FNRB1	FNRB0	0000
C1INTF	040A	_	_	TXBO	TXBP	RXBP	TXWAR	RXWAR	EWARN	IVRIF	WAKIF	ERRIF	_	FIFOIF	RBOVIF	RBIF	TBIF	0000
C1INTE	040C	—	_	—	—	—	—	—	_	IVRIE	WAKIE	ERRIE	-	FIFOIE	RBOVIE	RBIE	TBIE	0000
C1EC	040E	TERRCNT7	TERRCNT6	TERRCNT5	TERRCNT4	TERRCNT3	TERRCNT2	TERRCNT1	TERRCNT0	RERRCNT7	RERRCNT6	RERRCNT5	RERRCNT4	RERRCNT3	RERRCNT2	RERRCNT1	RERRCNT0	0000
C1CFG1	0410	_	_	_	_	—	_	_	_	SJW1	SJW0	BRP5	BRP4	BRP3	BRP2	BRP1	BRP0	0000
C1CFG2	0412	—	WAKFIL	—	—	—	SEG2PH2	SEG2PH1	SEG2PH0	SEG2PHTS	SAM	SEG1PH2	SEG1PH1	SEG1PH0	PRSEG2	PRSEG1	PRSEG0	0000
C1FEN1	0414								FLTE	N<15:0>								FFFF
C1FMSKSEL1	0418	F7MSK1	F7MSK0	F6MSK1	F6MSK0	F5MSK1	F5MSK0	F4MSK1	F4MSK0	F3MSK1	F3MSK0	F2MSK1	F2MSK0	F1MSK1	F1MSK0	F0MSK1	F0MSK0	0000
C1FMSKSEL2	041A	F15MSK1	F15MSK0	F14MSK1	F14MSK0	F13MSK1	F13MSK0	F12MSK1	F12MSK0	F11MSK1	F11MSK0	F10MSK1	F10MSK0	F9MSK1	F9MSK0	F8MSK1	F8MSK0	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: These registers are not present on dsPIC33EPXXXGM3XX devices.

# TABLE 4-24: CAN1 REGISTER MAP WHEN WIN (C1CTRL<0>) = 0 FOR dsPIC33EPXXXGM60X/7XX DEVICES<sup>(1)</sup>

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
	0400- 041E							Se	e definition	when WIN =	<b>-</b> x							
C1RXFUL1	0420								RXFUL	.<15:0>								0000
C1RXFUL2	0422			RXFUL<31:16> 0000														
C1RXOVF1	0428			RXOVF<15:0> 0000														
C1RXOVF2	042A								RXOVF	<31:16>								0000
C1TR01CON	0430	TXEN1	TXABT1	TXLARB1	TXERR1	TXREQ1	RTREN1	TX1PRI1	TX1PRI0	TXEN0	TXABAT0	TXLARB0	TXERR0	TXREQ0	RTREN0	TX0PRI1	TX0PRI0	0000
C1TR23CON	0432	TXEN3	TXABT3	TXLARB3	TXERR3	TXREQ3	RTREN3	TX3PRI1	TX3PRI0	TXEN2	TXABAT2	TXLARB2	TXERR2	TXREQ2	RTREN2	TX2PRI1	TX2PRI0	0000
C1TR45CON	0434	TXEN5	TXABT5	TXLARB5	TXERR5	TXREQ5	RTREN5	TX5PRI1	TX5PRI0	TXEN4	TXABAT4	TXLARB4	TXERR4	TXREQ4	RTREN4	TX4PRI1	TX4PRI0	0000
C1TR67CON	0436	TXEN7	TXABT7	TXLARB7	TXERR7	TXREQ7	RTREN7	TX7PRI1	TX7PRI0	TXEN6	TXABAT6	TXLARB6	TXERR6	TXREQ6	RTREN6	TX6PRI1	TX6PRI0	xxxx
C1RXD	0440		CAN1 Receive Data Word xxxx															
C1TXD	0442		CAN1 Transmit Data Word xxxx															

Legend: x = unknown value on Reset; - = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** These registers are not present on dsPIC33EPXXXGM3XX devices.

#### 4.3.4 SOFTWARE STACK

The W15 register serves as a dedicated Software Stack Pointer (SSP) and is automatically modified by exception processing, subroutine calls and returns; however, W15 can be referenced by any instruction in the same manner as all other W registers. This simplifies reading, writing and manipulating of the Stack Pointer (for example, creating stack frames).

Note:	То	protec	ct	agains	misa	ned	stack			
	acc	esses,	W	/15<0>	is	fixed	to	'0'	by	the
	har	dware.								

W15 is initialized to 0x1000 during all Resets. This address ensures that the SSP points to valid RAM in all dsPIC33EPXXXGM3XX/6XX/7XX devices and permits stack availability for non-maskable trap exceptions. These can occur before the SSP is initialized by the user software. You can reprogram the SSP during initialization to any location within Data Space.

The Software Stack Pointer always points to the first available free word and fills the software stack, working from lower toward higher addresses. Figure 4-13 illustrates how it pre-decrements for a stack pop (read) and post-increments for a stack push (writes).

When the PC is pushed onto the stack, PC<15:0> are pushed onto the first available stack word, then PC<22:16> are pushed into the second available stack location. For a PC push during any CALL instruction, the MSB of the PC is zero-extended before the push, as shown in Figure 4-13. During exception processing, the MSB of the PC is concatenated with the lower 8 bits of the CPU STATUS Register, SR. This allows the contents of SRL to be preserved automatically during interrupt processing.

- **Note 1:** To maintain the Software Stack Pointer (W15) coherency, W15 is never subject to (EDS) paging, and is therefore, restricted to an address range of 0x0000 to 0xFFFF. The same applies to the W14 when used as a Stack Frame Pointer (SFA = 1).
  - 2: As the stack can be placed in, and can access X and Y spaces, care must be taken regarding its use, particularly with regard to local automatic variables in a 'C' development environment

#### FIGURE 4-13: C.

#### CALL STACK FRAME



## 4.4 Instruction Addressing Modes

The addressing modes shown in Table 4-66 form the basis of the addressing modes optimized to support the specific features of the individual instructions. The addressing modes provided in the MAC class of instructions differ from those in the other instruction types.

#### 4.4.1 FILE REGISTER INSTRUCTIONS

Most file register instructions use a 13-bit address field (f) to directly address data present in the first 8192 bytes of data memory (Near Data Space). Most file register instructions employ a Working register, W0, which is denoted as WREG in these instructions. The destination is typically either the same file register or WREG (with the exception of the MUL instruction), which writes the result to a register or register pair. The MOV instruction allows additional flexibility and can access the entire Data Space.

#### 4.4.2 MCU INSTRUCTIONS

The three-operand MCU instructions are of the form:

Operand 3 = Operand 1 <function> Operand 2

where Operand 1 is always a Working register (that is, the addressing mode can only be Register Direct), which is referred to as Wb. Operand 2 can be a W register fetched from data memory or a 5-bit literal. The result location can be either a W register or a data memory location. The following addressing modes are supported by MCU instructions:

- Register Direct
- Register Indirect
- · Register Indirect Post-Modified
- · Register Indirect Pre-Modified
- 5-Bit or 10-Bit Literal

Note: Not all instructions support all of the addressing modes given above. Individual instructions can support different subsets of these addressing modes.

## **10.0 POWER-SAVING FEATURES**

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGM3XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To \_complement the information in this data sheet, refer to the "dsPIC33/PIC24 Family Reference Manual", "Watchdog Timer and Power-Saving Modes" (DS70615), which is available from the Microchip web site (www.microchip.com).
  - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGM3XX/6XX/7XX devices provide the ability to manage power consumption by selectively managing clocking to the CPU and the peripherals. In general, a lower clock frequency and a reduction in the number of peripherals being clocked constitutes lower consumed power.

The dsPIC33EPXXXGM3XX/6XX/7XX devices can manage power consumption in four ways:

- Clock Frequency
- Instruction-Based Sleep and Idle modes
- · Software-Controlled Doze mode
- · Selective Peripheral Control in Software

Combinations of these methods can be used to selectively tailor an application's power consumption while still maintaining critical application features, such as timing-sensitive communications.

#### EXAMPLE 10-1: PWRSAV INSTRUCTION SYNTAX

PWRSAV #SLEEP\_MODE ; Put the device into Sleep mode
PWRSAV #IDLE\_MODE ; Put the device into Idle mode

## 10.1 Clock Frequency and Clock Switching

The dsPIC33EPXXXGM3XX/6XX/7XX devices allow a wide range of clock frequencies to be selected under application control. If the system clock configuration is not locked, users can choose low-power or high-precision oscillators by simply changing the NOSCx bits (OSCCON<10:8>). The process of changing a system clock during operation, as well as limitations to the process, are discussed in more detail in **Section 9.0 "Oscillator Configuration"**.

### 10.2 Instruction-Based Power-Saving Modes

The dsPIC33EPXXXGM3XX/6XX/7XX devices have two special power-saving modes that are entered through the execution of a special PWRSAV instruction. Sleep mode stops clock operation and halts all code execution. Idle mode halts the CPU and code execution, but allows peripheral modules to continue operation. The assembler syntax of the PWRSAV instruction is shown in Example 10-1.

Note: SLEEP\_MODE and IDLE\_MODE are constants defined in the Assembler Include file for the selected device.

Sleep and Idle modes can be exited as a result of an enabled interrupt, WDT time-out or a device Reset. When the device exits these modes, it is said to "wake-up".

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_				IC6R<6:0>			
bit 15							bit 8
U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
_				IC5R<6:0>			
bit 7							bit C
Legend:							
R = Readat	ole bit	W = Writable	bit	U = Unimplen	nented bit, rea	ad as '0'	
-n = Value a	at POR	'1' = Bit is set		'0' = Bit is clea	ared	x = Bit is unkı	nown
bit 15	Unimpleme	ented: Read as '	0'				
bit 14-8	IC6R<6:0>: (see Table 1	Assign Input Ca 11-2 for input pin	apture 6 (IC6) selection nu	) to the Correspo mbers)	onding RPn P	in bits	
	1111100 =	Input tied to RPI	1124				
	•						
	•						
	0000001 = 0000000 =	Input tied to CM Input tied to Vss	P1				
bit 7	Unimpleme	ented: Read as '	0'				
bit 6-0	IC5R<6:0>: (see Table ?	Assign Input Ca 11-2 for input pin	apture 5 (IC5) selection nu	) to the Correspo mbers)	onding RPn P	in bits	
	1111100 =	Input tied to RP	1124				
	•						
	•						
	0000001 =	Input tied to CM	P1				
	0000000 =	Input tied to Vss	3				

#### REGISTER 11-6: RPINR9: PERIPHERAL PIN SELECT INPUT REGISTER 9

#### REGISTER 11-36: RPOR6: PERIPHERAL PIN SELECT OUTPUT REGISTER 6

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0					
_				RP55	R<5:0>							
bit 15							bit 8					
U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0					
_	—			RP54	R<5:0>							
bit 7							bit 0					
Legend:												
R = Readabl	e bit	W = Writable	bit	U = Unimplen	nented bit, rea	d as '0'						
-n = Value at	POR	'1' = Bit is set		'0' = Bit is clea	ared	ed x = Bit is unknown						
bit 15-14	Unimplemen	ted: Read as '	0'									
bit 13-8	<b>RP55R&lt;5:0&gt;</b> (see Table 11	: Peripheral Ou -3 for periphera	Itput Functior al function nu	i is Assigned to mbers)	RP55 Output	Pin bits						
bit 7-6	Unimplemen	ted: Read as '	0'									
bit 5-0	RP54R<5:0>: Peripheral Output Function is Assigned to RP54 Output Pin bits											

(see Table 11-3 for peripheral function numbers)

#### REGISTER 11-37: RPOR7: PERIPHERAL PIN SELECT OUTPUT REGISTER 7

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
	—			RP57R	<5:0>		
bit 15	·						bit 8
U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	_			RP56R	<5:0>		
bit 7							bit 0
Legend:							
R = Readabl	le bit	W = Writable	bit	U = Unimpleme	ented bit, rea	d as '0'	
-n = Value at	t POR	'1' = Bit is set		'0' = Bit is clear	ed	x = Bit is unkr	nown
bit 15-14	Unimplemen	ted: Read as '	0'				
bit 12 0		. Dorinhoral Ou	tout Eurotion	n in Annianad to D		Din hita	

bit 13-8 **RP57R<5:0>:** Peripheral Output Function is Assigned to RP57 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-6 Unimplemented: Read as '0'

bit 5-0 **RP56R<5:0>:** Peripheral Output Function is Assigned to RP56 Output Pin bits (see Table 11-3 for peripheral function numbers)

#### REGISTER 15-2: OCxCON2: OUTPUT COMPARE x CONTROL REGISTER 2 (CONTINUED)

- bit 4-0 SYNCSEL<4:0>: Trigger/Synchronization Source Selection bits 11111 = OCxRS compare event is used for synchronization 11110 = INT2 is the source for compare timer synchronization 11101 = INT1 is the source for compare timer synchronization 11100 = CTMU trigger is the source for compare timer synchronization 11011 = ADC1 interrupt is the source for compare timer synchronization 11010 = Analog Comparator 3 is the source for compare timer synchronization 11001 = Analog Comparator 2 is the source for compare timer synchronization 11000 = Analog Comparator 1 is the source for compare timer synchronization 10111 = Input Capture 8 interrupt is the source for compare timer synchronization 10110 = Input Capture 7 interrupt is the source for compare timer synchronization 10101 = Input Capture 6 interrupt is the source for compare timer synchronization 10100 = Input Capture 5 interrupt is the source for compare timer synchronization 10011 = Input Capture 4 interrupt is the source for compare timer synchronization 10010 = Input Capture 3 interrupt is the source for compare timer synchronization 10001 = Input Capture 2 interrupt is the source for compare timer synchronization 10000 = Input Capture 1 interrupt is the source for compare timer synchronization 01111 = GP Timer5 is the source for compare timer synchronization 01110 = GP Timer4 is the source for compare timer synchronization 01101 = GP Timer3 is the source for compare timer synchronization 01100 = GP Timer2 is the source for compare timer synchronization 01011 = GP Timer1 is the source for compare timer synchronization 01010 = PTGx trigger is the source for compare timer synchronization<sup>(3)</sup> 01001 = Compare timer is unsynchronized 01000 = Output Compare 8 is the source for compare timer synchronization<sup>(1,2)</sup> 00111 = Output Compare 7 is the source for compare timer synchronization<sup>(1,2)</sup> 00110 = Output Compare 6 is the source for compare timer synchronization<sup>(1,2)</sup> 00101 = Output Compare 5 is the source for compare timer synchronization<sup>(1,2)</sup> 00100 = Output Compare 4 is the source for compare timer synchronization<sup>(1,2)</sup> 00011 = Output Compare 3 is the source for compare timer synchronization<sup>(1,2)</sup> 00010 = Output Compare 2 is the source for compare timer synchronization<sup>(1,2)</sup> 00001 = Output Compare 1 is the source for compare timer synchronization<sup>(1,2)</sup> 00000 = Compare timer is unsynchronized
- Note 1: Do not use the OCx module as its own synchronization or trigger source.
  - 2: When the OCy module is turned off, it sends a trigger out signal. If the OCx module uses the OCy module as a trigger source, the OCy module must be unselected as a trigger source prior to disabling it.
  - 3: Each Output Compare x module (OCx) has one PTG Trigger/Sync source. See Section 25.0 "Peripheral Trigger Generator (PTG) Module" for more information.

PTGO4 = OC1, OC5 PTGO5 = OC2, OC6 PTGO6 = OC3, OC7 PTGO7 = OC4, OC8

#### 16.1.2 WRITE-PROTECTED REGISTERS

On dsPIC33EPXXXGM3XX/6XX/7XX devices, write protection is implemented for the IOCONx and FCLCONx registers. The write protection feature prevents any inadvertent writes to these registers. This protection feature can be controlled by the PWMLOCK Configuration bit (FOSCSEL<6>). The default state of the write protection feature is enabled (PWMLOCK = 1). The write protection feature can be disabled by configuring: PWMLOCK = 0.

To gain write access to these locked registers, the user application must write two consecutive values of 0xABCD and 0x4321 to the PWMKEY register to perform the unlock operation. The write access to the IOCONx or FCLCONx registers must be the next SFR access following the unlock process. There can be no other SFR accesses during the unlock process and subsequent write access. To write to both the IOCONx and FCLCONx registers requires two unlock operations.

The correct unlocking sequence is described in Example 16-1.

#### EXAMPLE 16-1: PWM1 WRITE-PROTECTED REGISTER UNLOCK SEQUENCE

; FLT32 pin must be pulle	d high externally in order to clear and disable the fault
; Writing to FCLCON1 regi	ster requires unlock sequence
<pre>mov #0xabcd, w10 mov #0x4321, w11 mov #0x0000, w0 mov w10, PWMKEY mov w11, PWMKEY mov w0, FCLCON1</pre>	<pre>; Load first unlock key to w10 register ; Load second unlock key to w11 register ; Load desired value of FCLCON1 register in w0 ; Write first unlock key to PWMKEY register ; Write second unlock key to PWMKEY register ; Write desired value to FCLCON1 register</pre>
; Set PWM ownership and p	olarity using the IOCON1 register
; Writing to IOCON1 regis	ter requires unlock sequence
<pre>mov #0xabcd, w10 mov #0x4321, w11 mov #0xF000, w0 mov w10, PWMKEY mov w11, PWMKEY mov w0, IOCON1</pre>	<pre>; Load first unlock key to w10 register ; Load second unlock key to w11 register ; Load desired value of IOCON1 register in w0 ; Write first unlock key to PWMKEY register ; Write second unlock key to PWMKEY register ; Write desired value to IOCON1 register</pre>

# 19.0 INTER-INTEGRATED CIRCUIT<sup>™</sup> (I<sup>2</sup>C<sup>™</sup>)

- Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGM3XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the "dsPIC33/PIC24 Family Reference Manual", "Inter-Integrated Circuit™ (I<sup>2</sup>C™)" (DS70000195), which is available from the Microchip web site (www.microchip.com).
  - 2: Some registers and associated bits described in this section may not be available on all devices. Refer to Section 4.0 "Memory Organization" in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGM3XX/6XX/7XX family of devices contains two Inter-Integrated Circuit ( $I^2C$ ) modules: I2C1 and I2C2.

The  $I^2C$  module provides complete hardware support for both Slave and Multi-Master modes of the  $I^2C$  serial communication standard, with a 16-bit interface. The I<sup>2</sup>C module has a 2-pin interface:

- The SCLx pin is clock.
- The SDAx pin is data.

The  $I^2C$  module offers the following key features:

- I<sup>2</sup>C Interface Supporting both Master and Slave modes of Operation.
- I<sup>2</sup>C Slave mode Supports 7 and 10-Bit Addressing.
- I<sup>2</sup>C Master mode Supports 7 and 10-Bit Addressing.
- I<sup>2</sup>C Port Allows Bidirectional Transfers Between Master and Slaves.
- Serial Clock Synchronization for I<sup>2</sup>C Port can be used as a Handshake Mechanism to Suspend and Resume Serial Transfer (SCLREL control).
- I<sup>2</sup>C Supports Multi-Master Operation, Detects Bus Collision and Arbitrates Accordingly.
- Intelligent Platform Management Interface (IPMI)
   Support
- System Management Bus (SMBus) Support

#### BUFFER 21-5: CANx MESSAGE BUFFER WORD 4

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
			Byte	3<15:8>			
bit 15							bit 8
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
			Byte	2<7:0>			
bit 7							bit 0
Legend:							
R = Readable	bit	W = Writable b	bit	U = Unimpler	nented bit, rea	ad as '0'	
-n = Value at F	POR	'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unk	nown

bit 15-8 Byte 3<15:8>: CANx Message Byte 3

bit 7-0 Byte 2<7:0>: CANx Message Byte 2

#### BUFFER 21-6: CANx MESSAGE BUFFER WORD 5

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
			Byte	5<15:8>			
bit 15							bit 8
R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
			Byte	4<7:0>			
bit 7						bit 0	
Legend:							
R = Readable bit W = Writable bit			U = Unimplemented bit, read as '0'				
-n = Value at POR '1' = Bit is		'1' = Bit is set		'0' = Bit is cle	ared	x = Bit is unkr	nown
bit 15 9			ao Puto F				
01010-0	Dyte 5<15:0	>: CAINX Messa	уе Буlе 5				

bit 7-0 Byte 4<7:0>: CANx Message Byte 4

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	
ITRIM5	ITRIM4	ITRIM3	ITRIM2	ITRIM1	ITRIM0	IRNG1	IRNG0	
bit 15							bit 8	
U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0	
_	—	_	—	—	_	_	_	
bit 7							bit 0	
Logondi								
R = Reada	uhle hit	W = Writable	hit	II = I Inimplen	nented hit read	l as 'N'		
-n = Value	at POR	'1' = Rit is set	bit	$0^{\circ} = \text{Bit is clear}$	ared	x - Bit is unknown		
					area		lowin	
bit 15-10	ITRIM<5:0>:	Current Source	e Trim bits					
	011111 <b>= Ma</b>	iximum positive	e change from	nominal curren	t + 62%			
	011110 <b>= Ma</b>	iximum positive	e change from	nominal curren	t + 60%			
	•							
	•							
	000010 <b>= M</b> ir	nimum positive	change from r	nominal current	+ 4%			
	000001 = Mir	nimum positive	change from r	nominal current	+ 2%			
	1111111 = Mir	minal current o	e change from	nominal curren	t – 2%			
	111110 <b>= Mi</b> r	nimum negative	e change from	nominal curren	t – 4%			
	•							
	•							
	100010 <b>= Ma</b>	ximum negativ	e change from	nominal currer	nt – 60%			
	100001 <b>= Ma</b>	iximum negativ	e change from	nominal currer	nt – 62%			
bit 9-8	IRNG<1:0>: (	Current Source	Range Select	bits				
	11 = 100 × Ba	ase Current <sup>(2)</sup>						
	$10 = 10 \times Bas$	se Current <sup>(2)</sup>						
	$01 = Base Cu00 = 1000 \times E$	Base Current <sup>(1,</sup>	2)					
bit 7-0	Unimplemen	ted: Read as '	0'					
Note 1:	This current range	e is not availab	le for use with	the internal ten	nperature meas	surement diode	<u>,</u>	
2:	Refer to the CTM	U Current Sou	rce Specificatio	ons (Table 33-5	5) in <b>Section 3</b>	3.0 "Electrica		
	Characteristics"	for the current	range selectio	n values.	,			

## REGISTER 22-3: CTMUICON: CTMU CURRENT CONTROL REGISTER<sup>(3)</sup>

3: Current sources are not generated when 12-Bit ADC mode is chosen. Current sources are active only when 10-Bit ADC mode is chosen.

TABLE 33-4: DC TEMPERATURE AND VOLTAGE SPECIFICATION	TABLE 33-4:	DC TEMPERATURE AND VOLTAGE SPECIFICATIONS
--	-------------	---

DC CHARACTERISTICS			$\begin{array}{llllllllllllllllllllllllllllllllllll$						
Param No.	Symbol	Characteristic	Min.	Тур. <sup>(1)</sup>	Conditions				
Operati	Operating Voltage								
DC10	Vdd	Supply Voltage <sup>(3)</sup>	3.0	_	3.6	V			
DC12	Vdr	RAM Data Retention Voltage <sup>(2)</sup>	1.95	_		V			
DC16	VPOR	VDD Start Voltage to Ensure Internal Power-on Reset Signal	_	—	Vss	V			
DC17	Svdd	<b>VDD Rise Rate</b> to Ensure Internal Power-on Reset Signal	0.03	—	—	V/ms	0V-3.0V in 3 ms		
DC18	VCORE	VDD Core <sup>(3)</sup> Internal Regulator Voltage	1.62	1.8	1.98	V	Voltage is dependent on load, temperature and VDD		

**Note 1:** Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

2: This is the limit to which VDD may be lowered without losing RAM data.

**3:** Device is functional at VBORMIN < VDD < VDDMIN. Analog modules: ADC, op amp/comparator and comparator voltage reference will have degraded performance. Device functionality is tested but not characterized. Refer to Parameter BO10 in Table 33-12 for the minimum and maximum BOR values.

#### TABLE 33-5: FILTER CAPACITOR (CEFC) SPECIFICATIONS

				$\begin{array}{llllllllllllllllllllllllllllllllllll$				
Param No.	Symbol	Characteristics	Min.	Тур.	vp. Max. Units Comments		Comments	
	Cefc	External Filter Capacitor Value <sup>(1)</sup>	4.7	10	_	μF	Capacitor must have a low series resistance (< 1 Ohm)	

**Note 1:** Typical VCAP voltage = 1.8 volts when VDD  $\ge$  VDDMIN.

# dsPIC33EPXXXGM3XX/6XX/7XX

## FIGURE 33-8: OUTPUT COMPARE x (OCx) TIMING CHARACTERISTICS



#### TABLE 33-26: OUTPUT COMPARE x (OCx) TIMING REQUIREMENTS

AC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$						
Param No.	Symbol	Characteristic <sup>(1)</sup>	Min.	Тур.	Max.	Units	Conditions		
OC10	TccF	OCx Output Fall Time	_	_		ns	See Parameter DO32		
OC11	TccR	OCx Output Rise Time	—	—	— ns See Parameter DO31				

Note 1: These parameters are characterized but not tested in manufacturing.

#### FIGURE 33-9: OCx/PWMx MODULE TIMING CHARACTERISTICS



#### TABLE 33-27: OCx/PWMx MODE TIMING REQUIREMENTS

AC CHARACTERISTICS			$\begin{array}{l} \mbox{Standard Operating Conditions: 3.0V to 3.6V} \\ \mbox{(unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for Industrial} \\ & -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for Extended} \end{array}$				
Param No.	Symbol	Characteristic <sup>(1)</sup>	Min.	Тур.	Max.	Units	Conditions
OC15	Tfd	Fault Input to PWMx I/O Change	—	_	Tcy + 20	ns	
OC20	TFLT	Fault Input Pulse Width	Tcy + 20	_	—	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

## 100-Lead Plastic Thin Quad Flatpack (PT) – 12x12x1 mm Body, 2.00 mm [TQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



#### Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Chamfers at corners are optional; size may vary.

3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.

4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-100B

100-Lead Plastic Thin Quad Flatpack (PF) - 14x14x1 mm Body 2.00 mm Footprint [TQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



	MILLIMETERS			
Dimension	MIN	NOM	MAX	
Contact Pitch	Е		0.50 BSC	
Contact Pad Spacing	C1		15.40	
Contact Pad Spacing	C2		15.40	
Contact Pad Width (X100)	X1			0.30
Contact Pad Length (X100)	Y1			1.50
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2110B

# APPENDIX A: REVISION HISTORY

## **Revision A (February 2013)**

This is the initial released version of this document.

## Revision B (June 2013)

Changes to Section 5.0 "Flash Program Memory", Register 5-1. Changes to Section 6.0 "Resets", Figure 6-1. Changes to Section 26.0 "Op Amp/Comparator Module", Register 26-2. Updates to most of the tables in Section 33.0 "Electrical Characteristics". Minor text edits throughout the document.

#### **Revision C (September 2013)**

Changes to Figure 23-1. Changes to Figure 26-2. Changes to Table 30-2. Changes to Section 33.0 "Electrical Characteristics". Added Section 34.0 "High-Temperature Electrical Characteristics" to the data sheet. Minor typographical edits throughout the document.

#### **Revision D (August 2014)**

This revision incorporates the following updates:

- Sections:
  - Updated Section 2.0 "Guidelines for Getting Started with 16-Bit Digital Signal Controllers", Section 8.0 "Direct Memory Access (DMA)", Section 10.3 "Doze Mode", Section 21.0 "Controller Area Network (CAN) Module (dsPIC33EPXXXGM6XX/7XX Devices Only)", Section 23.0 "10-Bit/12-Bit Analog-to-Digital Converter (ADC)", Section 23.1.2 "12-Bit ADCx Configuration", Section 21.4 "CAN Message Buffers", Section 35.0 "Packaging Information"
- · Figures:
  - Updated **"Pin Diagrams"**, Figure 1-1, Figure 9-1
- · Registers:
  - Updated Register 5-1, Register 8-2, Register 21-1, Register 23-2
- · Tables:
  - Updated Table 1-1, Table 7-1, Table 8-1, Table 34-9, Table 1, Table 4-2, Table 4-3, Table 4-25, Table 4-33, Table 4-34, Table 4-39, Table 4-30, Table 4-46, Table 4-47, Table 33-16, Table 34-8

NOTES: