What is "**Embedded - Microcontrollers**"?

"**Embedded - Microcontrollers**" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "**Embedded - Microcontrollers**"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	CANbus, I²C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, Motor Control PWM, POR, PWM, WDT
Number of I/O	35
Program Memory Size	256KB (85.5K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	-
Data Converters	A/D 18x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep256gm604t-i-pt

dsPIC33EPXXXGM3XX/6XX/7XX

2.7 Oscillator Value Conditions on Device Start-up

If the PLL of the target device is enabled and configured for the device start-up oscillator, the maximum oscillator source frequency must be limited to 5 MHz < F_{IN} < 13.6 MHz to comply with device PLL start-up conditions. This means that if the external oscillator frequency is outside this range, the application must start up in the FRC mode first. The default PLL settings after a POR with an oscillator frequency outside this range will violate the device operating speed.

Once the device powers up, the application firmware can initialize the PLL SFRs, CLKDIV and PLLDBF to a suitable value, and then perform a clock switch to the Oscillator + PLL clock source. Note that clock switching must be enabled in the device Configuration Word.

2.8 Unused I/Os

Unused I/O pins should be configured as outputs and driven to a logic low state.

Alternatively, connect a 1k to 10k resistor between V_{SS} and unused pins, and drive the output to logic low.

2.9 Application Examples

- Induction heating
- Uninterruptable Power Supplies (UPS)
- DC/AC inverters
- Compressor motor control
- Washing machine 3-phase motor control
- BLDC motor control
- Automotive HVAC, cooling fans, fuel pumps
- Stepper motor control
- Audio and fluid sensor monitoring
- Camera lens focus and stability control
- Speech (playback, hands-free kits, answering machines, VoIP)
- Consumer audio
- Industrial and building control (security systems and access control)
- Barcode reading
- Networking: LAN switches, gateways
- Data storage device management
- Smart cards and smart card readers
- Dual motor control

Examples of typical application connections are shown in Figure 2-4 through Figure 2-8.
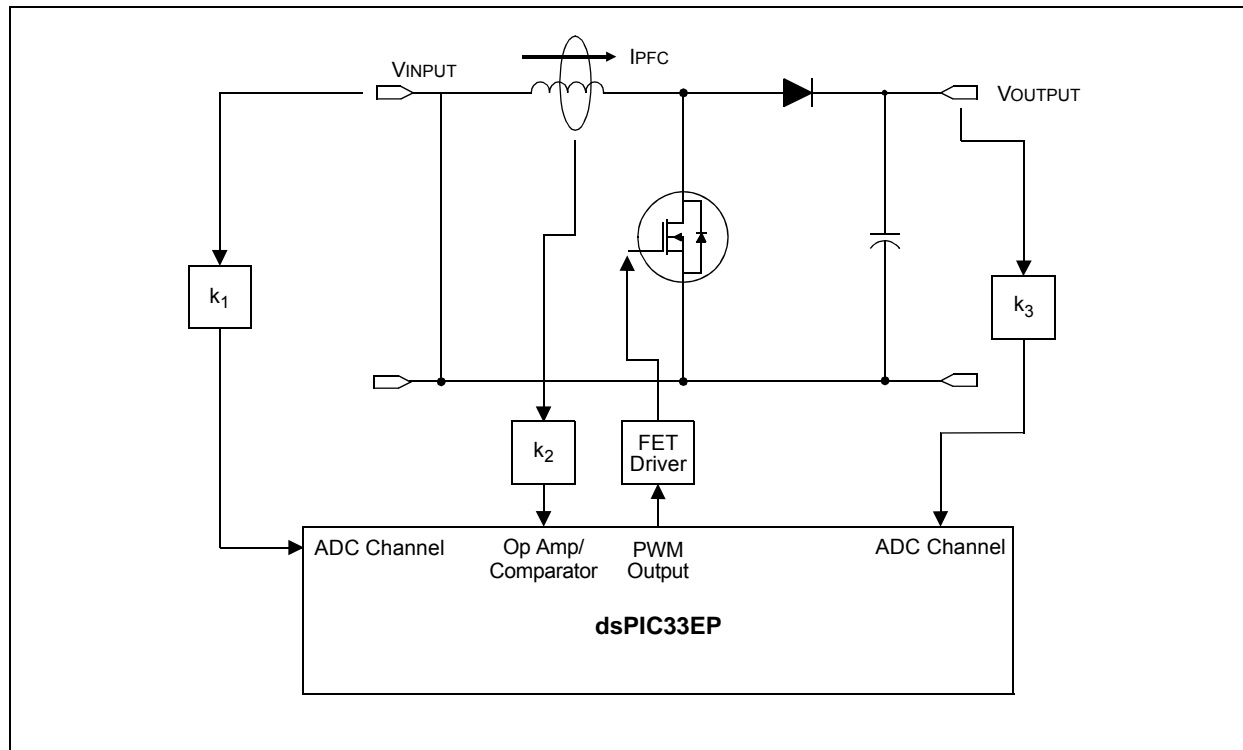
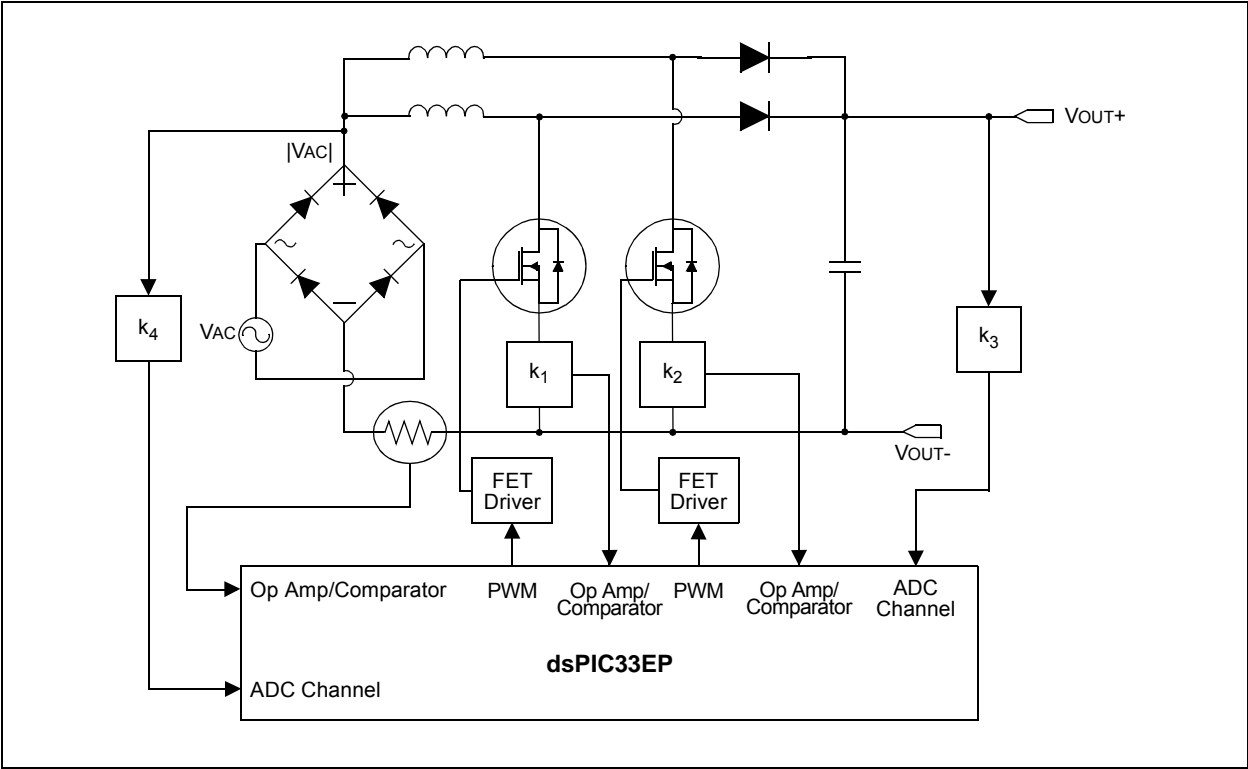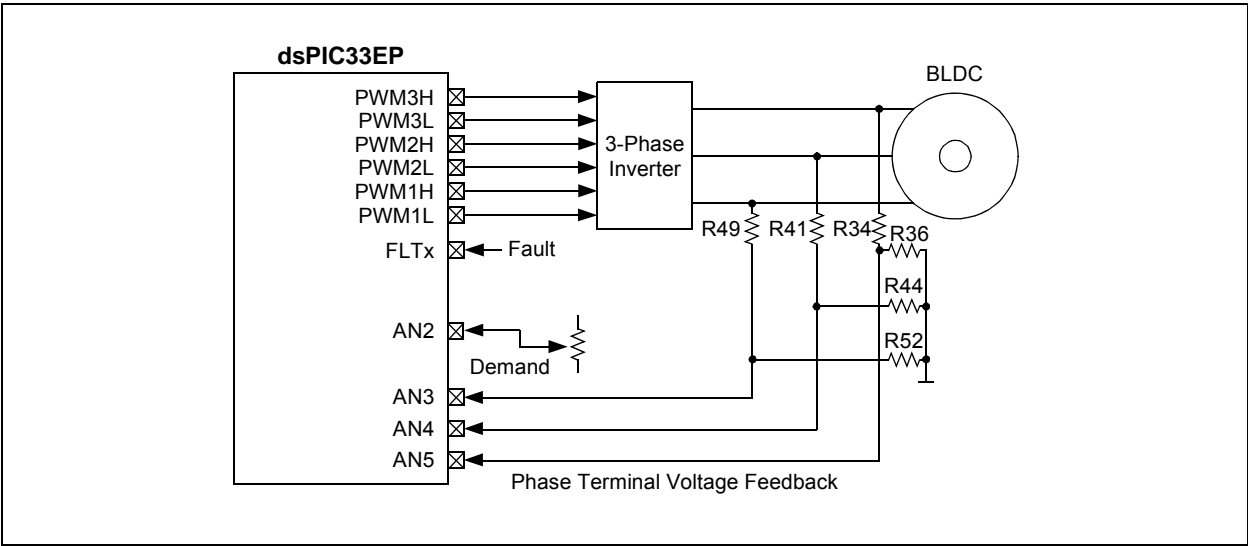**FIGURE 2-4: BOOST CONVERTER IMPLEMENTATION**

FIGURE 2-7: **INTERLEAVED PFC**

FIGURE 2-8: **BEMF VOLTAGE MEASURED USING THE ADC MODULE**

REGISTER 3-1:   SR: CPU STATUS REGISTER (CONTINUED)

bit 7-5   **IPL<2:0>:** CPU Interrupt Priority Level Status bits[1,2]

`111` = CPU Interrupt Priority Level is 7 (15); user interrupts are disabled
`110` = CPU Interrupt Priority Level is 6 (14)
`101` = CPU Interrupt Priority Level is 5 (13)
`100` = CPU Interrupt Priority Level is 4 (12)
`011` = CPU Interrupt Priority Level is 3 (11)
`010` = CPU Interrupt Priority Level is 2 (10)
`001` = CPU Interrupt Priority Level is 1 (9)
`000` = CPU Interrupt Priority Level is 0 (8)

bit 4   **RA:** `REPEAT` Loop Active bit

`1` = `REPEAT` loop is in progress
`0` = `REPEAT` loop is not in progress

bit 3   **N:** MCU ALU Negative bit

`1` = Result was negative
`0` = Result was non-negative (zero or positive)

bit 2   **OV:** MCU ALU Overflow bit

This bit is used for signed arithmetic (2's complement). It indicates an overflow of the magnitude that causes the sign bit to change state.
`1` = Overflow occurred for signed arithmetic (in this arithmetic operation)
`0` = No overflow occurred

bit 1   **Z:** MCU ALU Zero bit

`1` = An operation that affects the Z bit has set it at some time in the past
`0` = The most recent operation that affects the Z bit has cleared it (i.e., a non-zero result)

bit 0   **C:** MCU ALU Carry/$\overline{\text{Borrow}}$ bit

`1` = A carry-out from the Most Significant bit (MSb) of the result occurred
`0` = No carry-out from the Most Significant bit of the result occurred

Note 1:   The IPL<2:0> bits are concatenated with the IPL<3> bit (CORCON<3>) to form the CPU Interrupt Priority Level. The value in parentheses indicates the IPL, if IPL<3> = `1`. User interrupts are disabled when IPL<3> = `1`.

2:   The IPL<2:0> Status bits are read-only when the NSTDIS bit (INTCON1<15>) = `1`.

3:   A data write to the SR register can modify the SA and SB bits by either a data write to SA and SB or by clearing the SAB bit. To avoid a possible SA or SB bit write race condition, the SA and SB bits should not be modified using bit operations.

TABLE 4-25: CAN1 REGISTER MAP WHEN WIN (C1CTRL<0>) = 1 FOR dsPIC33EPXXXGM60X/7XX DEVICES[1] (CONTINUED)

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
C1RXF11SID	046C	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	EXIDE	—	EID17	EID16	xxxx
C1RXF11EID	046E	EID<15:0>																xxxx
C1RXF12SID	0470	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	EXIDE	—	EID17	EID16	xxxx
C1RXF12EID	0472	EID<15:0>																xxxx
C1RXF13SID	0474	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	EXIDE	—	EID17	EID16	xxxx
C1RXF13EID	0476	EID<15:0>																xxxx
C1RXF14SID	0478	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	EXIDE	—	EID17	EID16	xxxx
C1RXF14EID	047A	EID<15:0>																xxxx
C1RXF15SID	047C	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	EXIDE	—	EID17	EID16	xxxx
C1RXF15EID	047E	EID<15:0>																xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
Note 1: These registers are not present on dsPIC33EPXXXGM3XX devices.

TABLE 4-26: CAN2 REGISTER MAP WHEN WIN (C1CTRL<0>) = 0 OR 1 FOR dsPIC33EPXXXGM60X/7XX DEVICES[1]

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
C2CTRL1	0500	—	—	CSIDL	ABAT	CANCKS	REQOP2	REQOP1	REQOP0	OPMODE2	OPMODE1	OPMODE0	—	CANCAP	—	—	WIN	0480
C2CTRL2	0502	—	—	—	—	—	—	—	—	—	—	—	DNCNT<4:0>					0000
C2VEC	0504	—	—	FILHIT4	FILHIT3	FILHIT2	FILHIT1	FILHIT0	—	ICODE6	ICODE5	ICODE4	ICODE3	ICODE2	ICODE1	ICODE0		0040
C2FCTRL	0506	DMABS2	DMABS1	DMABS0	—	—	—	—	—	—	—	—	FSA4	FSA3	FSA2	FSA1	FSA0	0000
C2FIFO	0508	—	—	FBP5	FBP4	FBP3	FBP2	FBP1	FBP0	—	—	FNRB5	FNRB4	FNRB3	FNRB2	FNRB1	FNRB0	0000
C2INTF	050A	—	—	TXBO	TXBP	RXBP	TXWAR	RXWAR	EWARN	IVRIF	WAKIF	ERRIF	—	FIFOIF	RBOVIF	RBIF	TBIF	0000
C2INTE	050C	—	—	—	—	—	—	—	—	IVRIE	WAKIE	ERRIE	—	FIFOIE	RBOVIE	RBIE	TBIE	0000
C2EC	050E	TERRCNT7	TERRCNT6	TERRCNT5	TERRCNT4	TERRCNT3	TERRCNT2	TERRCNT1	TERRCNT0	RERRCNT7	RERRCNT6	RERRCNT5	RERRCNT4	RERRCNT3	RERRCNT2	RERRCNT1	RERRCNT0	0000
C2CFG1	0510	—	—	—	—	—	—	—	—	SJW1	SJW0	BRP5	BRP4	BRP3	BRP2	BRP1	BRP0	0000
C2CFG2	0512	—	WAKFIL	—	—	—	SEG2PH2	SEG2PH1	SEG2PH0	SEG2PHTS	SAM	SEG1PH2	SEG1PH1	SEG1PH0	PRSEG2	PRSEG1	PRSEG0	0000
C2FEN1	0514	FLTEN<15:0>																FFFF
C2FMSKSEL1	0518	F7MSK1	F7MSK0	F6MSK1	F6MSK0	F5MSK1	F5MSK0	F4MSK1	F4MSK0	F3MSK1	F3MSK0	F2MSK1	F2MSK0	F1MSK1	F1MSK0	F0MSK1	F0MSK0	0000
C2FMSKSEL2	051A	F15MSK1	F15MSK0	F14MSK1	F14MSK0	F13MSK1	F13MSK0	F12MSK1	F12MSK0	F11MSK1	F11MSK0	F10MSK1	F10MSK0	F9MSK1	F9MSK0	F8MSK1	F8MSK0	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
Note 1: These registers are not present on dsPIC33EPXXXGM3XX devices.

dsPIC33EPXXXGM3XX/6XX/7XX

TABLE 4-46: PORTA REGISTER MAP FOR dsPIC33EPXXXGM310/710 DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISA	0E00	TRISA<15:14>		—			TRISA<12:7>				—	—	TRISA4	—	—	TRISA<1:0>		DF9F
PORTA	0E02	RA<15:14>		—			RA<12:7>				—	—	RA4	—	—	RA<1:0>		0000
LATA	0E04	LATA<15:14>		—			LATA<12:7>				—	—	LATA4	—	—	LATA<1:0>		0000
ODCA	0E06	ODCA<15:14>		—			ODCA<12:7>				—	—	ODCA4	—	—	ODCA<1:0>		0000
CNENA	0E08	CNIEA<15:14>		—			CNIEA<12:7>				—	—	CNIEA4	—	—	CNIEA<1:0>		0000
CNPUA	0E0A	CNPUA<15:14>		—			CNPUA<12:7>				—	—	CNPUA4	—	—	CNPUA<1:0>		0000
CNPDA	0E0C	CNPDA<15:14>		—			CNPDA<12:7>				—	—	CNPDA4	—	—	CNPDA<1:0>		0000
ANSELA	0E0E	ANSA<15:14>		—	ANSA<12:11>		—	ANSA9	—	—	—	—	ANSA4	—	—	ANSA<1:0>		1813

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-47: PORTA REGISTER MAP FOR dsPIC33EPXXXGM306/706 DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISA	0E00	—	—	—			TRISA<12:7>				—	—	TRISA4	—	—	TRISA<1:0>		DF9F
PORTA	0E02	—	—	—			RA<12:7>				—	—	RA4	—	—	RA<1:0>		0000
LATA	0E04	—	—	—			LATA<12:7>				—	—	LATA4	—	—	LATA<1:0>		0000
ODCA	0E06	—	—	—			ODCA<12:7>				—	—	ODCA4	—	—	ODCA<1:0>		0000
CNENA	0E08	—	—	—			CNIEA<12:7>				—	—	CNIEA4	—	—	CNIEA<1:0>		0000
CNPUA	0E0A	—	—	—			CNPUA<12:7>				—	—	CNPUA4	—	—	CNPUA<1:0>		0000
CNPDA	0E0C	—	—	—			CNPDA<12:7>				—	—	CNPDA4	—	—	CNPDA<1:0>		0000
ANSELA	0E0E	—	—	—	ANSA<12:11>		—	ANSA9	—	—	—	—	ANSA4	—	—	ANSA<1:0>		1813

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-48: PORTA REGISTER MAP FOR dsPIC33EPXXXGM304/604 DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISA	0E00	—	—	—	—	—		TRISA<10:7>			—	—			TRISA<4:0>			DF9F
PORTA	0E02	—	—	—	—	—		RA<10:7>			—	—			RA<4:0>			0000
LATA	0E04	—	—	—	—	—		LATA<10:7>			—	—			LATA<4:0>			0000
ODCA	0E06	—	—	—	—	—		ODCA<10:7>			—	—			ODCA<4:0>			0000
CNENA	0E08	—	—	—	—	—		CNIEA<10:7>			—	—			CNIEA<4:0>			0000
CNPUA	0E0A	—	—	—	—	—		CNPUA<10:7>			—	—			CNPUA<4:0>			0000
CNPDA	0E0C	—	—	—	—	—		CNPDA<10:7>			—	—			CNPDA<4:0>			0000
ANSELA	0E0E	—	—	—	—	—	—	ANSA9	—	—	—	—	ANSA4	—	ANSA<2:0>			1813

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

4.7 Interfacing Program and Data Memory Spaces

The dsPIC33EPXXXGM3XX/6XX/7XX architecture uses a 24-bit-wide Program Space and a 16-bit-wide Data Space. The architecture is also a modified Harvard scheme, meaning that data can also be present in the Program Space. To use this data successfully, it must be accessed in a way that preserves the alignment of information in both spaces.

Aside from normal execution, the architecture of the dsPIC33EPXXXGM3XX/6XX/7XX devices provides two methods by which Program Space can be accessed during operation:
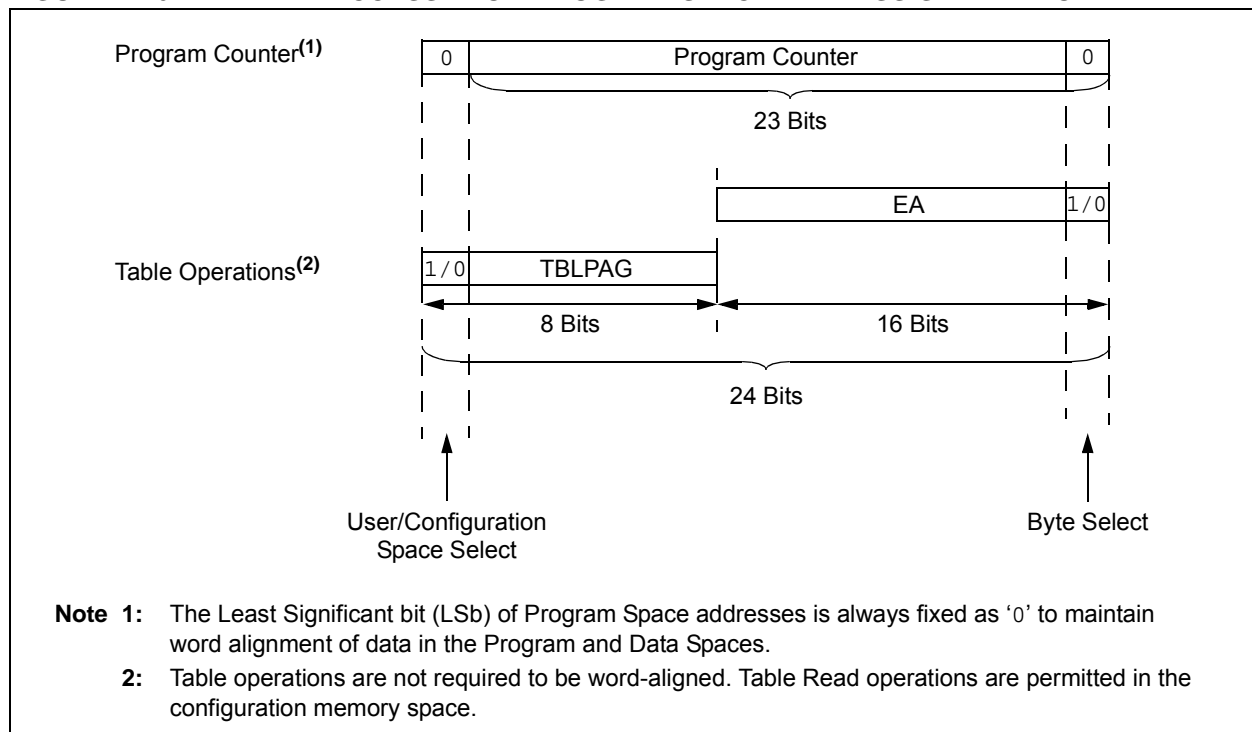
• Using table instructions to access individual bytes or words anywhere in the Program Space
• Remapping a portion of the Program Space into the Data Space (Program Space Visibility)

Table instructions allow an application to read or write to small areas of the program memory. This capability makes the method ideal for accessing data tables that need to be updated periodically. It also allows access to all bytes of the program word. The remapping method allows an application to access a large block of data on a read-only basis, which is ideal for look-ups from a large table of static data. The application can only access the least significant word of the program word.

TABLE 4-68: PROGRAM SPACE ADDRESS CONSTRUCTION

Access Type	Access Space	Program Space Address				
		<23>	**<22:16>**	**<15>**	**<14:1>**	**<0>**
Instruction Access (Code Execution)	User	0	PC<22:1>			0
		`0xx  xxxx  xxxx  xxxx  xxxx xxx0`				
`TBLRD/TBLWT` (Byte/Word Read/Write)	User	TBLPAG<7:0>		Data EA<15:0>		
		`0xxx xxxx    xxxx xxxx xxxx xxxx`				
	Configuration	TBLPAG<7:0>		Data EA<15:0>		
		`1xxx xxxx    xxxx xxxx xxxx xxxx`				

FIGURE 4-16: DATA ACCESS FROM PROGRAM SPACE ADDRESS GENERATION

Note 1: The Least Significant bit (LSb) of Program Space addresses is always fixed as '0' to maintain word alignment of data in the Program and Data Spaces.

2: Table operations are not required to be word-aligned. Table Read operations are permitted in the configuration memory space.

NOTES:

REGISTER 10-1: PMD1: PERIPHERAL MODULE DISABLE CONTROL REGISTER 1

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
T5MD	T4MD	T3MD	T2MD	T1MD	QEI1MD	PWMMD	DCIMD
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
I2C1MD	U2MD	U1MD	SPI2MD	SPI1MD	C2MD[1]	C1MD[1]	AD1MD
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15　　**T5MD:** Timer5 Module Disable bit
　　　　　1 = Timer5 module is disabled
　　　　　0 = Timer5 module is enabled

bit 14　　**T4MD:** Timer4 Module Disable bit
　　　　　1 = Timer4 module is disabled
　　　　　0 = Timer4 module is enabled

bit 13　　**T3MD:** Timer3 Module Disable bit
　　　　　1 = Timer3 module is disabled
　　　　　0 = Timer3 module is enabled

bit 12　　**T2MD:** Timer2 Module Disable bit
　　　　　1 = Timer2 module is disabled
　　　　　0 = Timer2 module is enabled

bit 11　　**T1MD:** Timer1 Module Disable bit
　　　　　1 = Timer1 module is disabled
　　　　　0 = Timer1 module is enabled

bit 10　　**QEI1MD:** QEI1 Module Disable bit
　　　　　1 = QEI1 module is disabled
　　　　　0 = QEI1 module is enabled

bit 9　　**PWMMD:** PWM Module Disable bit
　　　　　1 = PWM module is disabled
　　　　　0 = PWM module is enabled

bit 8　　**DCIMD:** DCI Module Disable bit
　　　　　1 = DCI module is disabled
　　　　　0 = DCI module is enabled

bit 7　　**I2C1MD:** I2C1 Module Disable bit
　　　　　1 = I2C1 module is disabled
　　　　　0 = I2C1 module is enabled

bit 6　　**U2MD:** UART2 Module Disable bit
　　　　　1 = UART2 module is disabled
　　　　　0 = UART2 module is enabled

bit 5　　**U1MD:** UART1 Module Disable bit
　　　　　1 = UART1 module is disabled
　　　　　0 = UART1 module is enabled

Note 1: These bits are available on dsPIC33EPXXXGM6XX/7XX devices only.

REGISTER 11-25: RPINR37: PERIPHERAL PIN SELECT INPUT REGISTER 37

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	SYNCI1R<6:0>						
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **SYNCI1R<6:0>:** Assign PWM Synchronization Input 1 to the Corresponding RPn Pin bits
(see Table 11-2 for input pin selection numbers)
1111100 = Input tied to RPI124
•
•
•
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

bit 7-0 **Unimplemented:** Read as '0'

REGISTER 11-28: RPINR40: PERIPHERAL PIN SELECT INPUT REGISTER 40

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—				DTCMP5R<6:0>			
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—				DTCMP4R<6:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15   **Unimplemented:** Read as '0'

bit 14-8   **DTCMP5R<6:0>:** Assign PWM Dead-Time Compensation Input 5 to the Corresponding RPn Pin bits
             (see Table 11-2 for input pin selection numbers)
             1111100 = Input tied to RPI124
             •
             •
             •
             0000001 = Input tied to CMP1
             0000000 = Input tied to Vss

bit 7   **Unimplemented:** Read as '0'

bit 6-0   **DTCMP4R<6:0>:** Assign PWM Dead-Time Compensation Input 4 to the Corresponding RPn Pin bits
             (see Table 11-2 for input pin selection numbers)
             1111100 = Input tied to RPI124
             •
             •
             •
             0000001 = Input tied to CMP1
             0000000 = Input tied to Vss

REGISTER 15-2: OCxCON2: OUTPUT COMPARE x CONTROL REGISTER 2

R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0
FLTMD	FLTOUT	FLTTRIEN	OCINV	—	—	—	OC32
bit 15							bit 8

R/W-0	R/W-0, HS	R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0
OCTRIG	TRIGSTAT	OCTRIS	SYNCSEL4	SYNCSEL3	SYNCSEL2	SYNCSEL1	SYNCSEL0
bit 7							bit 0

Legend:		HS = Hardware Settable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **FLTMD:** Fault Mode Select bit

1 = Fault mode is maintained until the Fault source is removed; the corresponding OCFLTx bit is cleared in software and a new PWM period starts
0 = Fault mode is maintained until the Fault source is removed and a new PWM period starts

bit 14 **FLTOUT:** Fault Out bit

1 = PWM output is driven high on a Fault
0 = PWM output is driven low on a Fault

bit 13 **FLTTRIEN:** Fault Output State Select bit

1 = OCx pin is tri-stated on a Fault condition
0 = OCx pin I/O state is defined by the FLTOUT bit on a Fault condition

bit 12 **OCINV:** OCx Invert bit

1 = OCx output is inverted
0 = OCx output is not inverted

bit 11-9 **Unimplemented:** Read as '0'

bit 8 **OC32:** Cascade Two OCx Modules Enable bit (32-bit operation)

1 = Cascade module operation is enabled
0 = Cascade module operation is disabled

bit 7 **OCTRIG:** OCx Trigger/Sync Select bit

1 = Triggers OCx from source designated by the SYNCSELx bits
0 = Synchronizes OCx with source designated by the SYNCSELx bits

bit 6 **TRIGSTAT:** Timer Trigger Status bit

1 = Timer source has been triggered and is running
0 = Timer source has not been triggered and is being held clear

bit 5 **OCTRIS:** OCx Output Pin Direction Select bit

1 = Output Compare x is tri-stated
0 = Output Compare x module drives the OCx pin

Note 1: Do not use the OCx module as its own synchronization or trigger source.

2: When the OCy module is turned off, it sends a trigger out signal. If the OCx module uses the OCy module as a trigger source, the OCy module must be unselected as a trigger source prior to disabling it.

3: Each Output Compare x module (OCx) has one PTG Trigger/Sync source. See **Section 25.0 "Peripheral Trigger Generator (PTG) Module"** for more information.
PTGO4 = OC1, OC5
PTGO5 = OC2, OC6
PTGO6 = OC3, OC7
PTGO7 = OC4, OC8

REGISTER 17-2:   QEIxIOC: QEIx I/O CONTROL REGISTER (CONTINUED)

bit 2   **INDEX:** Status of INDXx Input Pin After Polarity Control bit

1 = Pin is at logic '1'
0 = Pin is at logic '0'

bit 1   **QEB:** Status of QEBx Input Pin After Polarity Control and SWPAB Pin Swapping bit

1 = Pin is at logic '1'
0 = Pin is at logic '0'

bit 0   **QEA:** Status of QEAx Input Pin After Polarity Control and SWPAB Pin Swapping bit

1 = Pin is at logic '1'
0 = Pin is at logic '0'

REGISTER 17-6: POSxHLD: POSITION COUNTER x HOLD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
POSHLD<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
POSHLD<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **POSHLD<15:0>:** Holding Register for Reading and Writing POSxCNT bits

REGISTER 17-7: VELxCNT: VELOCITY COUNTER x REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
VELCNT<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
VELCNT<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **VELCNT<15:0>:** Velocity Counter x bits

REGISTER 21-13: CxBUFPNT2: CANx FILTERS 4-7 BUFFER POINTER REGISTER 2

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F7BP3	F7BP2	F7BP1	F7BP0	F6BP3	F6BP2	F6BP1	F6BP0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F5BP3	F5BP2	F5BP1	F5BP0	F4BP3	F4BP2	F4BP1	F4BP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-12 **F7BP<3:0>:** RX Buffer Mask for Filter 7 bits
`1111` = Filter hits received in RX FIFO buffer
`1110` = Filter hits received in RX Buffer 14
•
•
•
`0001` = Filter hits received in RX Buffer 1
`0000` = Filter hits received in RX Buffer 0

bit 11-8 **F6BP<3:0>:** RX Buffer Mask for Filter 6 bits (same values as bits 15-12)

bit 7-4 **F5BP<3:0>:** RX Buffer Mask for Filter 5 bits (same values as bits 15-12)

bit 3-0 **F4BP<3:0>:** RX Buffer Mask for Filter 4 bits (same values as bits 15-12)

REGISTER 21-14: CxBUFPNT3: CANx FILTERS 8-11 BUFFER POINTER REGISTER 3

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F11BP3	F11BP2	F11BP1	F11BP0	F10BP3	F10BP2	F10BP1	F10BP0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F9BP3	F9BP2	F9BP1	F9BP0	F8BP3	F8BP2	F8BP1	F8BP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-12 **F11BP<3:0>:** RX Buffer Mask for Filter 11 bits
`1111` = Filter hits received in RX FIFO buffer
`1110` = Filter hits received in RX Buffer 14
•
•
•
`0001` = Filter hits received in RX Buffer 1
`0000` = Filter hits received in RX Buffer 0

bit 11-8 **F10BP<3:0>:** RX Buffer Mask for Filter 10 bits (same values as bits 15-12)

bit 7-4 **F9BP<3:0>:** RX Buffer Mask for Filter 9 bits (same values as bits 15-12)

bit 3-0 **F8BP<3:0>:** RX Buffer Mask for Filter 8 bits (same values as bits 15-12)

REGISTER 21-20: CxRXMnSID: CANx ACCEPTANCE FILTER MASK n STANDARD IDENTIFIER REGISTER (n = 0-2)

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3
bit 15							bit 8

R/W-x	R/W-x	R/W-x	U-0	R/W-x	U-0	R/W-x	R/W-x
SID2	SID1	SID0	—	MIDE	—	EID17	EID16
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-5   **SID<10:0>:** Standard Identifier bits
      1 = Includes bit, SIDx, in filter comparison
      0 = Bit, SIDx, is a don't care in filter comparison

bit 4   **Unimplemented:** Read as '0'

bit 3   **MIDE:** Identifier Receive Mode bit
      1 = Matches only message types (standard or extended address) that correspond to the EXIDE bit in the filter
      0 = Matches either standard or extended address message if filters match
         (i.e., if (Filter SIDx) = (Message SIDx) or if (Filter SIDx/EIDx) = (Message SIDx/EIDx))

bit 2   **Unimplemented:** Read as '0'

bit 1-0   **EID<17:16>:** Extended Identifier bits
      1 = Includes bit, EIDx, in filter comparison
      0 = Bit, EIDx, is a don't care in filter comparison

REGISTER 21-21: CxRXMnEID: CANx ACCEPTANCE FILTER MASK n EXTENDED IDENTIFIER REGISTER (n = 0-2)

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
			EID<15:8>				
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
			EID<7:0>				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0   **EID<15:0>:** Extended Identifier bits
      1 = Includes bit, EIDx, in filter comparison
      0 = Bit, EIDx, is a don't care in filter comparison

25.3   Step Commands and Format

TABLE 25-1:   PTG STEP COMMAND FORMAT

Step Command Byte:			
STEPx<7:0>			
CMD<3:0>		OPTION<3:0>	
bit 7	bit 4	bit 3	bit 0

bit 7-4	CMD<3:0>	Step Command	Command Description
	0000	PTGCTRL	Execute control command as described by OPTION<3:0>
	0001	PTGADD	Add contents of PTGADJ register to target register as described by OPTION<3:0>
		PTGCOPY	Copy contents of PTGHOLD register to target register as described by OPTION<3:0>
	001x	PTGSTRB	Copy the value contained in CMD0:OPTION<3:0> to the CH0SA<4:0> bits (AD1CHS0<4:0>)
	0100	PTGWHI	Wait for a low-to-high edge input from selected PTG trigger input as described by OPTION<3:0>
	0101	PTGWLO	Wait for a high-to-low edge input from selected PTG trigger input as described by OPTION<3:0>
	0110	Reserved	Reserved
	0111	PTGIRQ	Generate individual interrupt request as described by OPTION<3:0>
	100x	PTGTRIG	Generate individual trigger output as described by <<CMD0:OPTION<3:0>>
	101x	PTGJMP	Copy the value indicated in <<CMD0:OPTION<3:0>> to the Queue Pointer (PTGQPTR) and jump to that step queue
	110x	PTGJMPC0	PTGC0 = PTGC0LIM: Increment the Queue Pointer (PTGQPTR)
			PTGC0 ≠ PTGC0LIM: Increment Counter 0 (PTGC0) and copy the value indicated in <<CMD0:OPTION<3:0>> to the Queue Pointer (PTGQPTR) and jump to that step queue
	111x	PTGJMPC1	PTGC1 = PTGC1LIM: Increment the Queue Pointer (PTGQPTR)
			PTGC1 ≠ PTGC1LIM: Increment Counter 1 (PTGC1) and copy the value indicated in <<CMD0:OPTION<3:0>> to the Queue Pointer (PTGQPTR) and jump to that step queue

Note 1:   All reserved commands or options will execute but have no effect (i.e., execute as a NOP instruction).

2:   Refer to Table 25-2 for the trigger output descriptions.

29.2 Programmable CRC Control Registers

REGISTER 29-1: CRCCON1: CRC CONTROL REGISTER 1

R/W-0	U-0	R/W-0	R-0	R-0	R-0	R-0	R-0
CRCEN	—	CSIDL	VWORD4	VWORD3	VWORD2	VWORD1	VWORD0
bit 15							bit 8

R-0	R-1	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
CRCFUL	CRCMPT	CRCISEL	CRCGO	LENDIAN	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **CRCEN:** CRC Enable bit

1 = CRC module is enabled
0 = CRC module is disabled; all state machines, pointers and CRCWDAT/CRCDAT are reset, other SFRs are not reset

bit 14 **Unimplemented:** Read as '0'

bit 13 **CSIDL:** CRC Stop in Idle Mode bit

1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12-8 **VWORD<4:0>:** Valid Word Pointer Value bits

Indicates the number of valid words in the FIFO; has a maximum value of 8 when PLEN<4:0> > 7 or 16 when PLEN<4:0> ≤ 7

bit 7 **CRCFUL**: CRC FIFO Full bit

1 = FIFO is full
0 = FIFO is not full

bit 6 **CRCMPT:** CRC FIFO Empty Bit

1 = FIFO is empty
0 = FIFO is not empty

bit 5 **CRCISEL:** CRC Interrupt Selection bit

1 = Interrupt on FIFO empty; final word of data is still shifting through CRC
0 = Interrupt on shift complete and CRCWDAT results are ready

bit 4 **CRCGO:** CRC Start bit

1 = Start CRC serial shifter
0 = CRC serial shifter is turned off

bit 3 **LENDIAN:** Data Word Little-Endian Configuration bit

1 = Data word is shifted into the CRC starting with the LSb (little endian)
0 = Data word is shifted into the CRC starting with the MSb (big endian)

bit 2-0 **Unimplemented:** Read as '0'

TABLE 33-39: SPI2 AND SPI3 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0) TIMING REQUIREMENTS

	AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	Symbol	Characteristic[1]	Min.	Typ.[2]	Max.	Units	Conditions
SP70	FscP	Maximum SCKx Input Frequency	—	—	11	MHz	(Note 3)
SP72	TscF	SCKx Input Fall Time	—	—	—	ns	See Parameter DO32 (Note 4)
SP73	TscR	SCKx Input Rise Time	—	—	—	ns	See Parameter DO31 (Note 4)
SP30	TdoF	SDOx Data Output Fall Time	—	—	—	ns	See Parameter DO32 (Note 4)
SP31	TdoR	SDOx Data Output Rise Time	—	—	—	ns	See Parameter DO31 (Note 4)
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid after SCKx Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	30	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{SSx}$ ↓ to SCKx ↑ or SCKx ↓ Input	120	—	—	ns	
SP51	TssH2doZ	$\overline{SSx}$ ↑ to SDOx Output High-Impedance	10	—	50	ns	(Note 4)
SP52	TscH2ssH TscL2ssH	$\overline{SSx}$ ↑ after SCKx Edge	1.5 TCY + 40	—	—	ns	(Note 4)

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCKx is 91 ns. Therefore, the SCKx clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPIx pins.

TABLE 33-47: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	Symbol	Characteristic[1]	Min.	Typ.[2]	Max.	Units	Conditions
SP70	FscP	Maximum SCK1 Input Frequency	—	—	25	MHz	(Note 3)
SP72	TscF	SCK1 Input Fall Time	—	—	—	ns	See Parameter DO32 (Note 4)
SP73	TscR	SCK1 Input Rise Time	—	—	—	ns	See Parameter DO31 (Note 4)
SP30	TdoF	SDO1 Data Output Fall Time	—	—	—	ns	See Parameter DO32 (Note 4)
SP31	TdoR	SDO1 Data Output Rise Time	—	—	—	ns	See Parameter DO31 (Note 4)
SP35	TscH2doV, TscL2doV	SDO1 Data Output Valid after SCK1 Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO1 Data Output Setup to First SCK1 Edge	20	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI1 Data Input to SCK1 Edge	20	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDI1 Data Input to SCK1 Edge	15	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{SS1}$ ↓ to SCK1 ↑ or SCK1 ↓ Input	120	—	—	ns	
SP51	TssH2doZ	$\overline{SS1}$ ↑ to SDO1 Output High-Impedance	10	—	50	ns	(Note 4)
SP52	TscH2ssH, TscL2ssH	$\overline{SS1}$ ↑ after SCK1 Edge	1.5 TCY + 40	—	—	ns	(Note 4)

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCK1 is 91 ns. Therefore, the SCK1 clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPI1 pins.

35.2 Package Details

44-Lead Plastic Thin Quad Flatpack (PT) – 10x10x1 mm Body, 2.00 mm [TQFP]

> **Note:** For the most current package drawings, please see the Microchip Packaging Specification located at
> http://www.microchip.com/packaging
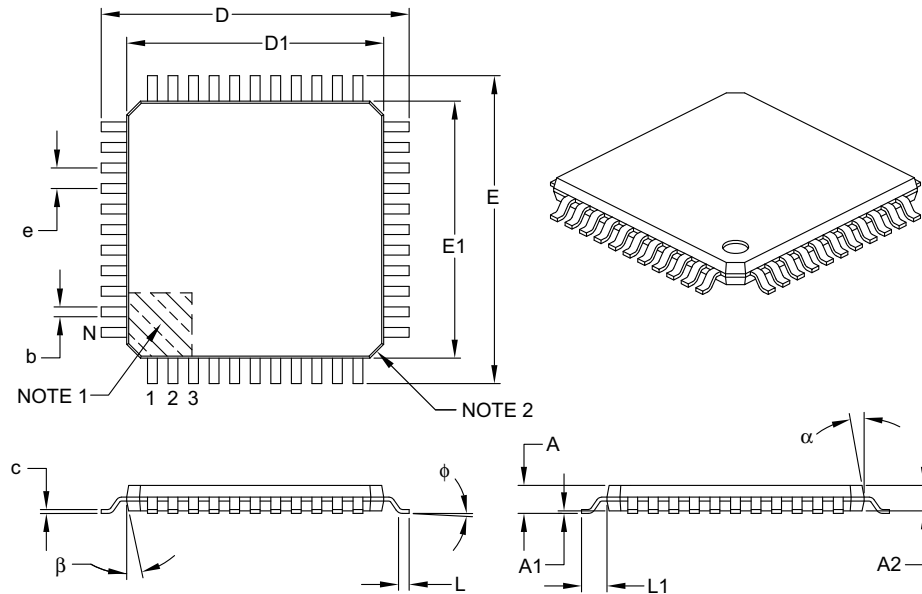
	Units		MILLIMETERS	
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		44	
Lead Pitch	e		0.80 BSC	
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	–	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	φ	0°	3.5°	7°
Overall Width	E		12.00 BSC	
Overall Length	D		12.00 BSC	
Molded Package Width	E1		10.00 BSC	
Molded Package Length	D1		10.00 BSC	
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.30	0.37	0.45
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

    BSC: Basic Dimension. Theoretically exact value shown without tolerances.
    REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-076B