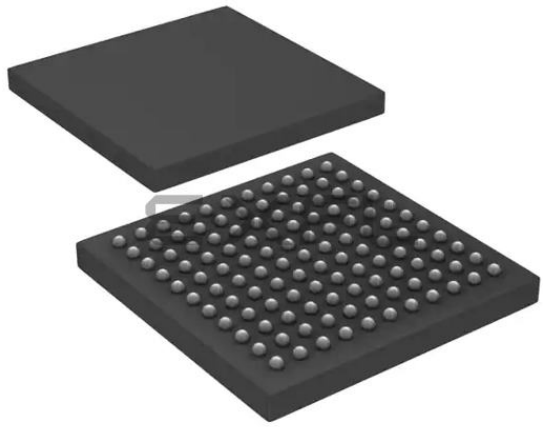

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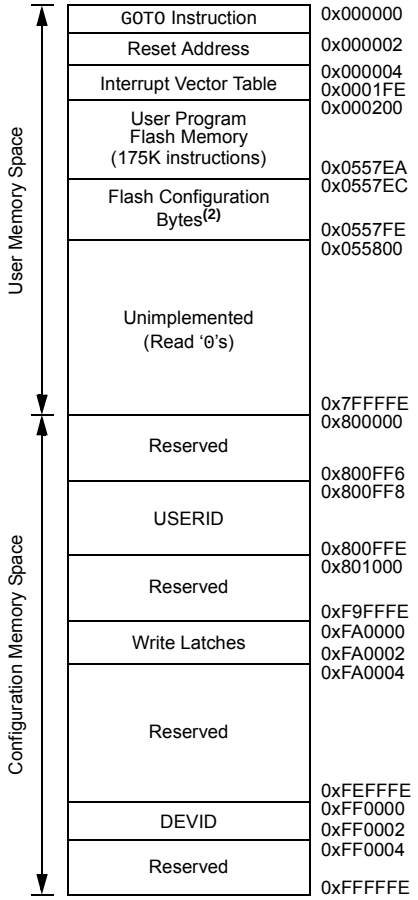
Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPs
Connectivity	CANbus, I²C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, Motor Control PWM, POR, PWM, WDT
Number of I/O	85
Program Memory Size	256KB (85.5K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 49x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	121-TFBGA
Supplier Device Package	121-TFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep256gm710-e-bg

FIGURE 4-3: PROGRAM MEMORY MAP FOR dsPIC33EP512GM3XX/6XX/7XX DEVICES(1)



Note 1: Memory areas are not shown to scale.

2: On Reset, these bits are automatically copied into the device Configuration Shadow registers.

TABLE 4-3: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EPXXXGM3XX DEVICES (CONTINUED)

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
IPC11	0856	—	T6IP2	T6IP1	T6IP0	—	—	—	—	—	PMPIP2(1)	PMPIP1(1)	PMPIP0(1)	—	OC8IP2	OC8IP1	OC8IP0	4444
IPC12	0858	—	T8IP2	T8IP1	T8IP0	—	MI2C2IP2	MI2C2IP1	MI2C2IP0	—	SI2C2IP2	SI2C2IP1	SI2C2IP0	—	T7IP2	T7IP1	T7IP0	4444
IPC13	085A	—	—	—	—	—	INT4IP2	INT4IP1	INT4IP0	—	INT3IP2	INT3IP1	INT3IP0	—	T9IP2	T9IP1	T9IP0	4444
IPC14	085C	—	DCIEIP2	DCIEIP1	DCIEIP0	—	QEI1IP2	QEI1IP2	QEI1IP0	—	PCEPIP2	PCEPIP1	PCEPIP0	—	—	—	—	4444
IPC15	085E	—	FLT1IP2	FLT1IP1	FLT1IP0	—	RTCCIP2(2)	RTCCIP1(2)	RTCCIP0(2)	—	—	—	—	—	DCIIP2	DCIIP1	DCIIP0	0404
IPC16	0860	—	CRCIP2	CRCIP1	CRCIP0	—	U2EIP2	U2EIP1	U2EIP0	—	U1EIP2	U1EIP1	U1EIP0	—	FLT2IP2	FLT2IP1	FLT2IP0	4440
IPC18	0864	—	C2TXIP2	C2TXIP1	C2TXIP0	—	FLT3IP2	FLT3IP1	FLT3IP0	—	PCESIP2	PCESIP1	PCESIP0	—	—	—	—	4040
IPC19	0866	—	—	—	—	—	—	—	—	—	CTMUIP2	CTMUIP1	CTMUIP0	—	FLT4IP2	FLT4IP1	FLT4IP0	0004
IPC20	0868	—	U3TXIP2	U3TXIP1	U3TXIP0	—	U3RXIP2	U3RXIP1	U3RXIP0	—	U3EIP2	U3EIP1	U3EIP0	—	—	—	—	0000
IPC21	086A	—	U4EIP2	U4EIP1	U4EIP0	—	—	—	—	—	—	—	—	—	—	—	—	0000
IPC22	086C	—	SPI3IP2	SPI3IP1	SPI3IP0	—	SPI3EIP2	SPI3EIP1	SPI3EIP0	—	U4TXIP2	U4TXIP1	U4TXIP0	—	U4RXIP2	U4RXIP1	U4RXIP0	0000
IPC23	086E	—	PGC2IP2	PGC2IP1	PGC2IP0	—	PWM1IP2	PWM1IP1	PWM1IP0	—	—	—	—	—	—	—	—	4400
IPC24	0870	—	PWM6IP2	PWM6IP1	PWM6IP0	—	PWM5IP2	PWM5IP1	PWM5IP0	—	PWM4IP2	PWM4IP1	PWM4IP0	—	PWM3IP2	PWM3IP1	PWM3IP0	4444
IPC35	0886	—	JTAGIP2	JTAGIP1	JTAGIP0	—	ICDIP2	ICDIP1	ICDIP0	—	—	—	—	—	—	—	—	4400
IPC36	0888	—	PTG0IP2	PTG0IP1	PTG0IP0	—	PTGWDTIP2	PTGWDTIP1	PTGWDTIP0	—	PTGSTEPIP2	PTGSTEPIP1	PTGSTEPIP0	—	—	—	—	4440
IPC37	088A	—	—	—	—	—	PTG3IP2	PTG3IP1	PTG3IP0	—	PTG2IP2	PTG2IP1	PTG2IP0	—	PTG1IP2	PTG1IP1	PTG1IP0	0444
INTTREG	08C8	—	—	—	—	ILR3	ILR2	ILR1	ILR0	VECNUM7	VECNUM6	VECNUM5	VECNUM4	VECNUM3	VECNUM2	VECNUM1	VECNUM0	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: The PMPIF/PMPIE/PMPIPx flags are not available on 44-pin devices.

2: The RTCCIF/RTCCIE/RTCCIPx flags are not available on 44-pin devices.

TABLE 4-27: CAN2 REGISTER MAP WHEN WIN (C1CTRL<0>) = 0 FOR dsPIC33EPXXXGM60X/7XX DEVICES(1)

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
	0500-051E	See definition when WIN = x																
C2RXFUL1	0520	RXFUL<15:0>																0000
C2RXFUL2	0522	RXFUL<31:16>																0000
C2RXOVF1	0528	RXOVF<15:0>																0000
C2RXOVF2	052A	RXOVF<31:16>																0000
C2TR01CON	0530	TXEN1	TXABT1	TXLARB1	TXERR1	TXREQ1	RTREN1	TX1PRI1	TX1PRI0	TXEN0	TXABAT0	TXLARB0	TXERR0	TXREQ0	RTREN0	TX0PRI1	TX0PRI0	0000
C2TR23CON	0532	TXEN3	TXABT3	TXLARB3	TXERR3	TXREQ3	RTREN3	TX3PRI1	TX3PRI0	TXEN2	TXABAT2	TXLARB2	TXERR2	TXREQ2	RTREN2	TX2PRI1	TX2PRI0	0000
C2TR45CON	0534	TXEN5	TXABT5	TXLARB5	TXERR5	TXREQ5	RTREN5	TX5PRI1	TX5PRI0	TXEN4	TXABAT4	TXLARB4	TXERR4	TXREQ4	RTREN4	TX4PRI1	TX4PRI0	0000
C2TR67CON	0536	TXEN7	TXABT7	TXLARB7	TXERR7	TXREQ7	RTREN7	TX7PRI1	TX7PRI0	TXEN6	TXABAT6	TXLARB6	TXERR6	TXREQ6	RTREN6	TX6PRI1	TX6PRI0	xxxx
C2RXD	0540	CAN2 Receive Data Word Register																xxxx
C2TXD	0542	CAN2 Transmit Data Word Register																xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: These registers are not present on dsPIC33EPXXXGM3XX devices.

4.3.4 SOFTWARE STACK

The W15 register serves as a dedicated Software Stack Pointer (SSP) and is automatically modified by exception processing, subroutine calls and returns; however, W15 can be referenced by any instruction in the same manner as all other W registers. This simplifies reading, writing and manipulating of the Stack Pointer (for example, creating stack frames).

Note:	To protect against misaligned stack accesses, W15<0> is fixed to '0' by the hardware.

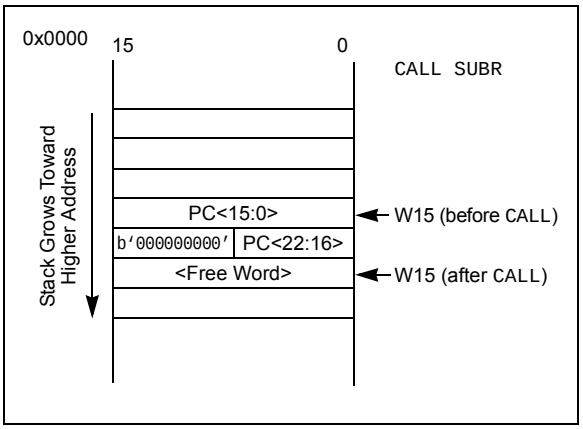
W15 is initialized to 0x1000 during all Resets. This address ensures that the SSP points to valid RAM in all dsPIC33EPXXXGM3XX/6XX/7XX devices and permits stack availability for non-maskable trap exceptions. These can occur before the SSP is initialized by the user software. You can reprogram the SSP during initialization to any location within Data Space.

The Software Stack Pointer always points to the first available free word and fills the software stack, working from lower toward higher addresses. Figure 4-13 illustrates how it pre-decrements for a stack pop (read) and post-increments for a stack push (writes).

When the PC is pushed onto the stack, PC<15:0> are pushed onto the first available stack word, then PC<22:16> are pushed into the second available stack location. For a PC push during any CALL instruction, the MSB of the PC is zero-extended before the push, as shown in Figure 4-13. During exception processing, the MSB of the PC is concatenated with the lower 8 bits of the CPU STATUS Register, SR. This allows the contents of SRL to be preserved automatically during interrupt processing.

Note 1:	To maintain the Software Stack Pointer (W15) coherency, W15 is never subject to (EDS) paging, and is therefore, restricted to an address range of 0x0000 to 0xFFFF. The same applies to the W14 when used as a Stack Frame Pointer (SFA = 1).
2:	As the stack can be placed in, and can access X and Y spaces, care must be taken regarding its use, particularly with regard to local automatic variables in a 'C' development environment

FIGURE 4-13: CALL STACK FRAME



4.4 Instruction Addressing Modes

The addressing modes shown in Table 4-66 form the basis of the addressing modes optimized to support the specific features of the individual instructions. The addressing modes provided in the MAC class of instructions differ from those in the other instruction types.

4.4.1 FILE REGISTER INSTRUCTIONS

Most file register instructions use a 13-bit address field (f) to directly address data present in the first 8192 bytes of data memory (Near Data Space). Most file register instructions employ a Working register, W0, which is denoted as WREG in these instructions. The destination is typically either the same file register or WREG (with the exception of the MUL instruction), which writes the result to a register or register pair. The MOV instruction allows additional flexibility and can access the entire Data Space.

4.4.2 MCU INSTRUCTIONS

The three-operand MCU instructions are of the form:

Operand 3 = Operand 1 <function> Operand 2

where Operand 1 is always a Working register (that is, the addressing mode can only be Register Direct), which is referred to as Wb. Operand 2 can be a W register fetched from data memory or a 5-bit literal. The result location can be either a W register or a data memory location. The following addressing modes are supported by MCU instructions:

- Register Direct
- Register Indirect
- Register Indirect Post-Modified
- Register Indirect Pre-Modified
- 5-Bit or 10-Bit Literal

Note:	Not all instructions support all of the addressing modes given above. Individual instructions can support different subsets of these addressing modes.

REGISTER 11-16: RPINR22: PERIPHERAL PIN SELECT INPUT REGISTER 22

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	SCK2R<6:0>						
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	SDI2R<6:0>						
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-8 **SCK2R<6:0>:** Assign SPI2 Clock Input (SCK2) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

1111100 = Input tied to RPI124
•
•
•
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as ‘0’

bit 6-0 **SDI2R<6:0>:** Assign SPI2 Data Input (SDI2) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

1111100 = Input tied to RPI124
•
•
•
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

REGISTER 11-38: RPOR8: PERIPHERAL PIN SELECT OUTPUT REGISTER 8(1)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP70R<5:0>					
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP69R<5:0>					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP70R<5:0>:** Peripheral Output Function is Assigned to RP70 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP69R<5:0>:** Peripheral Output Function is Assigned to RP69 Output Pin bits (see Table 11-3 for peripheral function numbers)

Note 1: This register is not available on dsPIC33EPXXXGM304/604 devices.

REGISTER 11-39: RPOR9: PERIPHERAL PIN SELECT OUTPUT REGISTER 9(1)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP97R<5:0>					
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP81R<5:0>(2)					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP97R<5:0>:** Peripheral Output Function is Assigned to RP97 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP81R<5:0>:** Peripheral Output Function is Assigned to RP81 Output Pin bits(2) (see Table 11-3 for peripheral function numbers)

Note 1: This register is not available on dsPIC33EPXXXGM304/604 devices.

2: These bits are not available on dsPIC33EPXXXGM306/706 devices.

REGISTER 16-6: STCON2: PWMx SECONDARY MASTER CLOCK DIVIDER SELECT REGISTER 2

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	—	—	—	—	PCLKDIV<2:0>(1)		
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-3 **Unimplemented:** Read as ‘0’

bit 2-0 **PCLKDIV<2:0>:** PWMx Input Clock Prescaler (Divider) Select bits(1)

111 = Reserved
110 = Divide-by-64
101 = Divide-by-32
100 = Divide-by-16
011 = Divide-by-8
010 = Divide-by-4
001 = Divide-by-2
000 = Divide-by-1, maximum PWMx timing resolution (power-on default)

Note 1: These bits should be changed only when PTEN = 0. Changing the clock selection during operation will yield unpredictable results.

20.0 UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UART)

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGM3XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"Universal Asynchronous Receiver Transmitter (UART)"** (DS70000582), which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGM3XX/6XX/7XX family of devices contains four UART modules.

The Universal Asynchronous Receiver Transmitter (UART) module is one of the serial I/O modules available in the dsPIC33EPXXXGM3XX/6XX/7XX device family. The UART is a full-duplex, asynchronous system that can communicate with peripheral devices, such as personal computers, LIN/J2602, RS-232 and RS-485 interfaces. The module also supports a hardware flow control option with the $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ pins, and also includes an IrDA® encoder and decoder.

Note: Hardware flow control using $\overline{\text{UxRTS}}$ and $\overline{\text{UxCTS}}$ is not available on all pin count devices. See the **"Pin Diagrams"** section for availability.

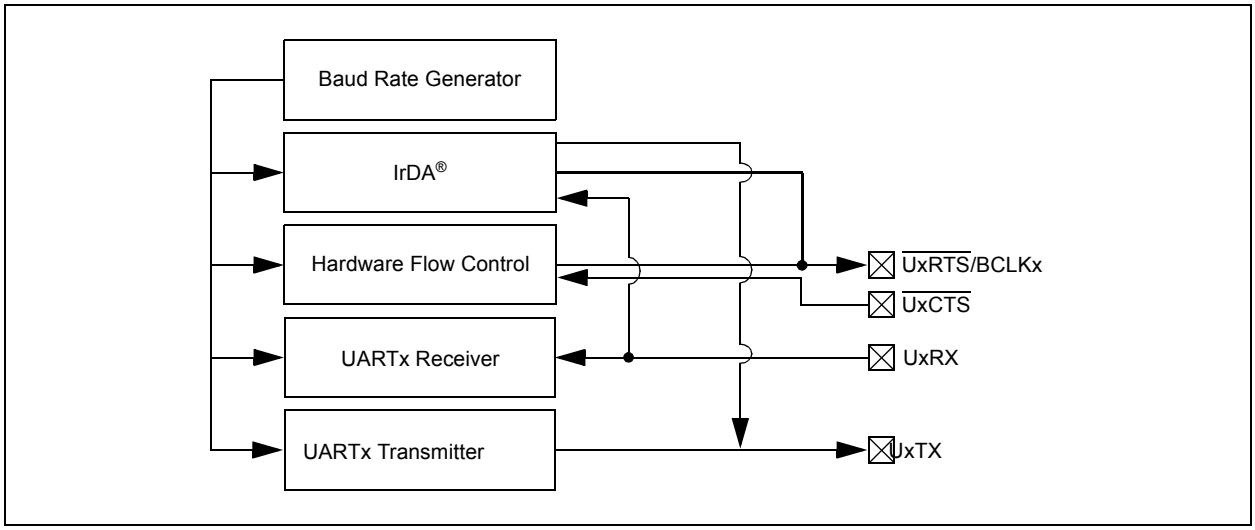
The primary features of the UART module are:

- Full-Duplex, 8 or 9-Bit Data Transmission through the UxTX and UxRX Pins
- Even, Odd or No Parity Options (for 8-bit data)
- One or Two Stop Bits
- Hardware Flow Control Option with $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ Pins
- Fully Integrated Baud Rate Generator with 16-Bit Prescaler
- Baud Rates Ranging from 4.375 Mbps to 67 bps at 16x mode at 70 MIPS
- Baud Rates Ranging from 17.5 Mbps to 267 bps at 4x mode at 70 MIPS
- 4-Deep First-In First-Out (FIFO) Transmit Data Buffer
- 4-Deep FIFO Receive Data Buffer
- Parity, Framing and Buffer Overrun Error Detection
- Support for 9-Bit mode with Address Detect (9th bit = 1)
- Transmit and Receive Interrupts
- A Separate Interrupt for All UART Error Conditions
- Loopback mode for Diagnostic Support
- Support for Sync and Break Characters
- Support for Automatic Baud Rate Detection
- IrDA® Encoder and Decoder Logic
- 16x Baud Clock Output for IrDA® Support

A simplified block diagram of the UART module is shown in Figure 20-1. The UART module consists of these key hardware elements:

- Baud Rate Generator
- Asynchronous Transmitter
- Asynchronous Receiver

FIGURE 20-1: UARTx SIMPLIFIED BLOCK DIAGRAM



REGISTER 21-15: CxBUFPNT4: CANx FILTERS 12-15 BUFFER POINTER REGISTER 4

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F15BP3	F15BP2	F15BP1	F15BP0	F14BP3	F14BP2	F14BP1	F14BP0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F13BP3	F13BP2	F13BP1	F13BP0	F12BP3	F12BP2	F12BP1	F12BP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-12 **F15BP<3:0>:** RX Buffer Mask for Filter 15 bits
1111 = Filter hits received in RX FIFO buffer
1110 = Filter hits received in RX Buffer 14
•
•
•
0001 = Filter hits received in RX Buffer 1
0000 = Filter hits received in RX Buffer 0

bit 11-8 **F14BP<3:0>:** RX Buffer Mask for Filter 14 bits (same values as bits 15-12)

bit 7-4 **F13BP<3:0>:** RX Buffer Mask for Filter 13 bits (same values as bits 15-12)

bit 3-0 **F12BP<3:0>:** RX Buffer Mask for Filter 12 bits (same values as bits 15-12)

REGISTER 26-7: CVR1CON: COMPARATOR VOLTAGE REFERENCE CONTROL REGISTER 1

U-0	U-0	U-0	U-0	R/W-0	R/W-0	U-0	U-0
—	—	—	—	CVRR1	VREFSEL	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CVREN	CVROE	CVRR0	CVRSS	CVR3	CVR2	CVR1	CVR0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-12 **Unimplemented:** Read as '0'

bit 11 **CVRR1:** Comparator Voltage Reference Range Selection bit
See bit 5.

bit 10 **VREFSEL:** Voltage Reference Select bit
1 = $CV_{REFIN} = V_{REF+}$
0 = CV_{REFIN} is generated by the resistor network

bit 9-8 **Unimplemented:** Read as '0'

bit 7 **CVREN:** Comparator Voltage Reference Enable bit
1 = Comparator voltage reference circuit is powered on
0 = Comparator voltage reference circuit is powered down

bit 6 **CVROE:** Comparator Voltage Reference Output Enable on CV_{REF1O} Pin bit
1 = Voltage level is output on the CV_{REF1O} pin
0 = Voltage level is disconnected from the CV_{REF1O} pin

bit 11, 5 **CVRR<1:0>:** Comparator Voltage Reference Range Selection bits
11 = 0.00 CV_{RSRC} to 0.94, with CV_{RSRC}/16 step-size
10 = 0.33 CV_{RSRC} to 0.96, with CV_{RSRC}/24 step-size
01 = 0.00 CV_{RSRC} to 0.67, with CV_{RSRC}/24 step-size
00 = 0.25 CV_{RSRC} to 0.75, with CV_{RSRC}/32 step-size

bit 4 **CVRSS:** Comparator Voltage Reference Source Selection bit
1 = Comparator voltage reference source, $CV_{RSRC} = CV_{REF+} – AV_{SS}$
0 = Comparator voltage reference source, $CV_{RSRC} = AV_{DD} – AV_{SS}$

bit 3-0 **CVR<3:0>** Comparator Voltage Reference Value Selection $0 \le CVR<3:0> \le 15$ bits
When CVRR<1:0> = 11:
$CV_{REF} = (CVR<3:0>/16) \bullet (CV_{RSRC})$
When CVRR<1:0> = 10:
$CV_{REF} = (1/3) \bullet (CV_{RSRC}) + (CVR<3:0>/24) \bullet (CV_{RSRC})$
When CVRR<1:0> = 01:
$CV_{REF} = (CVR<3:0>/24) \bullet (CV_{RSRC})$
When CVRR<1:0> = 00:
$CV_{REF} = (1/4) \bullet (CV_{RSRC}) + (CVR<3:0>/32) \bullet (CV_{RSRC})$

REGISTER 27-8: ALRMVAL (WHEN ALRMPTR<1:0> = 10): ALARM MONTH AND DAY VALUE REGISTER(1)

U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	—	MTHTEN0	MTHONE3	MTHONE2	MTHONE1	MTHONE0
bit 15							bit 8

U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	DAYTEN1	DAYTEN0	DAYONE3	DAYONE2	DAYONE1	DAYONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-13 **Unimplemented:** Read as '0'

bit 12 **MTHTEN0:** Binary Coded Decimal Value of Month's Tens Digit bit
Contains a value of 0 or 1.

bit 11-8 **MTHONE<3:0>:** Binary Coded Decimal Value of Month's Ones Digit bits
Contains a value from 0 to 9.

bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 **DAYTEN<1:0>:** Binary Coded Decimal Value of Day's Tens Digit bits
Contains a value from 0 to 3.

bit 3-0 **DAYONE<3:0>:** Binary Coded Decimal Value of Day's Ones Digit bits
Contains a value from 0 to 9.

Note 1: A write to this register is only allowed when RTCWREN = 1.

REGISTER 28-3: PMADDR: PARALLEL MASTER PORT ADDRESS REGISTER (MASTER MODES ONLY)(1,2)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CS2	CS1	ADDR13	ADDR12	ADDR11	ADDR10	ADDR9	ADDR8
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADDR7	ADDR6	ADDR5	ADDR4	ADDR3	ADDR2	ADDR1	ADDR0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at Reset	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **CS2:** Chip Select 2 bit
If PMCON<7:6> = 10 or 01:
1 = Chip Select 2 is active
0 = Chip Select 2 is inactive
If PMCON<7:6> = 11 or 00:
Bit functions as ADDR15.

bit 14 **CS1:** Chip Select 1 bit
If PMCON<7:6> = 10:
1 = Chip Select 1 is active
0 = Chip Select 1 is inactive
If PMCON<7:6> = 11 or 0x:
Bit functions as ADDR14.

bit 13-0 **ADDR<13:0>:** Destination Address bits

Note 1: In Enhanced Slave mode, PMADDR functions as PMDOUT1, one of the two Data Buffer registers.
2: This register is not available on 44-pin devices.

29.2 Programmable CRC Control Registers

REGISTER 29-1: CRCCON1: CRC CONTROL REGISTER 1

R/W-0	U-0	R/W-0	R-0	R-0	R-0	R-0	R-0
CRCEN	—	CSIDL	VWORD4	VWORD3	VWORD2	VWORD1	VWORD0
bit 15							bit 8

R-0	R-1	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0
CRCFUL	CRCMPT	CRCISEL	CRCGO	LENDIAN	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **CRCEN:** CRC Enable bit
1 = CRC module is enabled
0 = CRC module is disabled; all state machines, pointers and CRCWDAT/CRCDAT are reset, other SFRs are not reset

bit 14 **Unimplemented:** Read as '0'

bit 13 **CSIDL:** CRC Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12-8 **VWORD<4:0>:** Valid Word Pointer Value bits
Indicates the number of valid words in the FIFO; has a maximum value of 8 when PLEN<4:0> > 7 or 16 when PLEN<4:0> ≤ 7

bit 7 **CRCFUL**: CRC FIFO Full bit
1 = FIFO is full
0 = FIFO is not full

bit 6 **CRCMPT:** CRC FIFO Empty Bit
1 = FIFO is empty
0 = FIFO is not empty

bit 5 **CRCISEL:** CRC Interrupt Selection bit
1 = Interrupt on FIFO empty; final word of data is still shifting through CRC
0 = Interrupt on shift complete and CRCWDAT results are ready

bit 4 **CRCGO:** CRC Start bit
1 = Start CRC serial shifter
0 = CRC serial shifter is turned off

bit 3 **LENDIAN:** Data Word Little-Endian Configuration bit
1 = Data word is shifted into the CRC starting with the LSb (little endian)
0 = Data word is shifted into the CRC starting with the MSb (big endian)

bit 2-0 **Unimplemented:** Read as '0'

30.0 SPECIAL FEATURES

Note: This data sheet summarizes the features of the dsPIC33EPXXXGM3XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the related section of the "*dsPIC33/PIC24 Family Reference Manual*", which is available from the Microchip web site (www.microchip.com).

dsPIC33EPXXXGM3XX/6XX/7XX devices include several features intended to maximize application flexibility and reliability, and minimize cost through elimination of external components. These are:

- Flexible Configuration
- Watchdog Timer (WDT)
- Code Protection and CodeGuard™ Security
- JTAG Boundary Scan Interface
- In-Circuit Serial Programming™ (ICSP™)
- In-Circuit Emulation

30.1 Configuration Bits

In dsPIC33EPXXXGM3XX/6XX/7XX devices, the Configuration bytes are implemented as volatile memory. This means that configuration data must be programmed each time the device is powered up. Configuration data is stored at the top of the on-chip program memory space, known as the Flash Configuration bytes. Their specific locations are shown in Table 30-1. The configuration data is automatically loaded from the Flash Configuration bytes to the proper Configuration Shadow registers during device Resets.

Note: Configuration data is reloaded on all types of device Resets.

When creating applications for these devices, users should always specifically allocate the location of the Flash Configuration bytes for configuration data in their code for the compiler. This is to make certain that program code is not stored in this address when the code is compiled.

The upper 2 bytes of all Flash Configuration Words in program memory should always be '1111 1111 1111 1111'. This makes them appear to be NOP instructions in the remote event that their locations are ever executed by accident. Since Configuration bits are not implemented in the corresponding locations, writing '1's to these locations has no effect on device operation.

Note: Performing a page erase operation on the last page of program memory clears the Flash Configuration bytes, enabling code protection as a result. Therefore, users should avoid performing page erase operations on the last page of program memory.

The Configuration Flash bytes map is shown in Table 30-1.

FIGURE 33-28: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 1, SMP = 0) TIMING CHARACTERISTICS

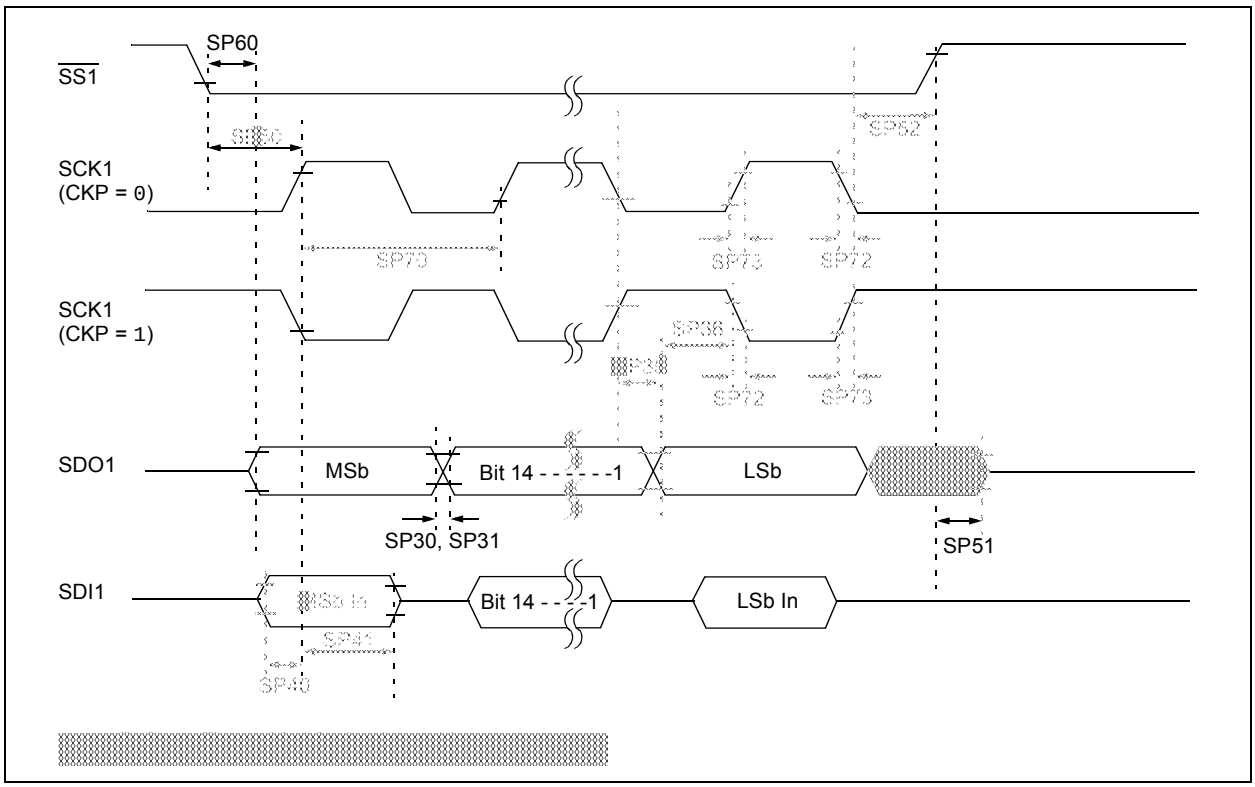


TABLE 33-45: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 1, SMP = 0) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
SP70	FscP	Maximum SCK1 Input Frequency	—	—	25	MHz	**(Note 3)**
SP72	TscF	SCK1 Input Fall Time	—	—	—	ns	See Parameter DO32 **(Note 4)**
SP73	TscR	SCK1 Input Rise Time	—	—	—	ns	See Parameter DO31 **(Note 4)**
SP30	TdoF	SDO1 Data Output Fall Time	—	—	—	ns	See Parameter DO32 **(Note 4)**
SP31	TdoR	SDO1 Data Output Rise Time	—	—	—	ns	See Parameter DO31 **(Note 4)**
SP35	TscH2doV, TscL2doV	SDO1 Data Output Valid after SCK1 Edge	—	6	20	ns	
SP36	TdoV2scH, TdoV2scL	SDO1 Data Output Setup to First SCK1 Edge	20	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDI1 Data Input to SCK1 Edge	20	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDI1 Data Input to SCK1 Edge	15	—	—	ns	
SP50	TssL2scH, TssL2scL	$\overline{SS1}$ ↓ to SCK1 ↑ or SCK1 ↓ Input	120	—	—	ns	
SP51	TssH2doZ	$\overline{SS1}$ ↑ to SDO1 Output High-Impedance	10	—	50	ns	**(Note 4)**
SP52	TscH2ssH, TscL2ssH	$\overline{SS1}$ ↑ after SCK1 Edge	1.5 TCY + 40	—	—	ns	**(Note 4)**
SP60	TssL2doV	SDO1 Data Output Valid after $\overline{SS1}$ Edge	—	—	50	ns	

Note 1: These parameters are characterized, but are not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCK1 is 91 ns. Therefore, the SCK1 clock generated by the master must not violate this specification.

4: Assumes 50 pF load on all SPI1 pins.

FIGURE 33-33: I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (SLAVE MODE)

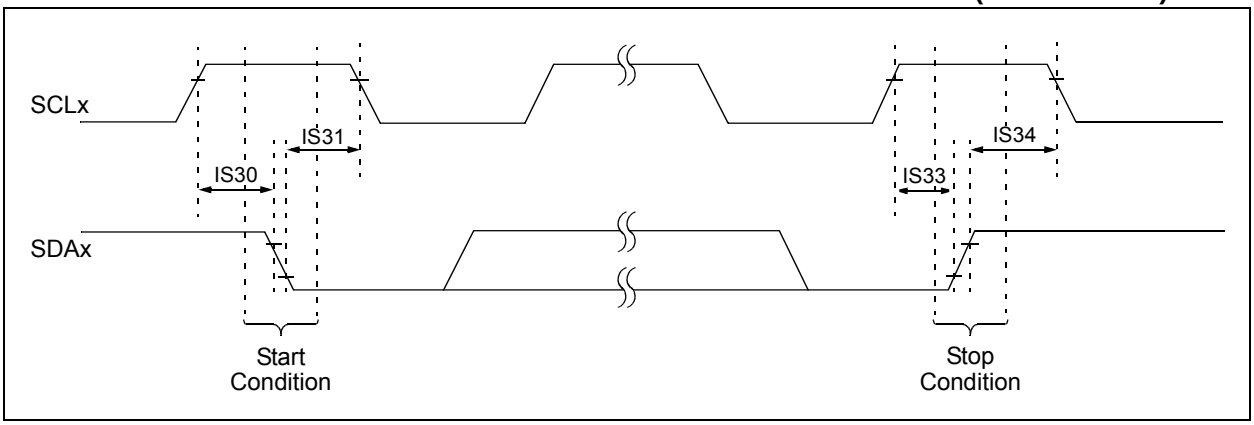
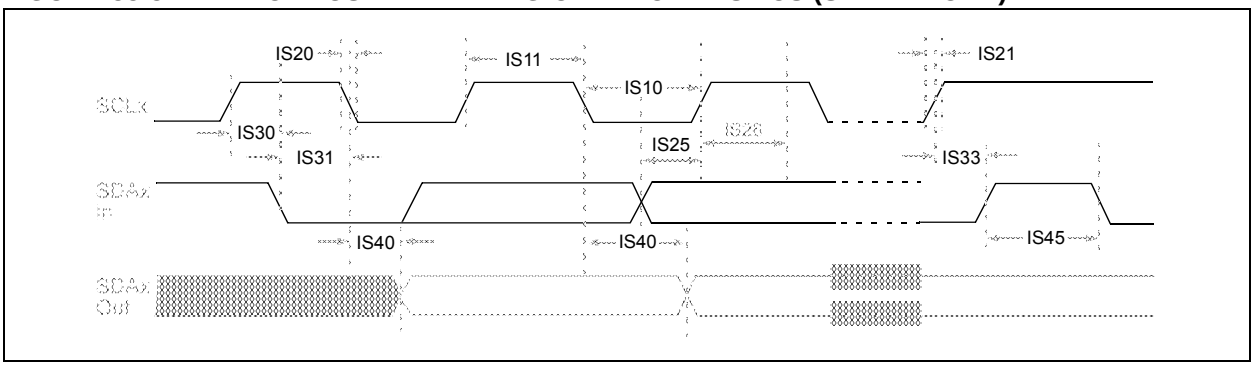
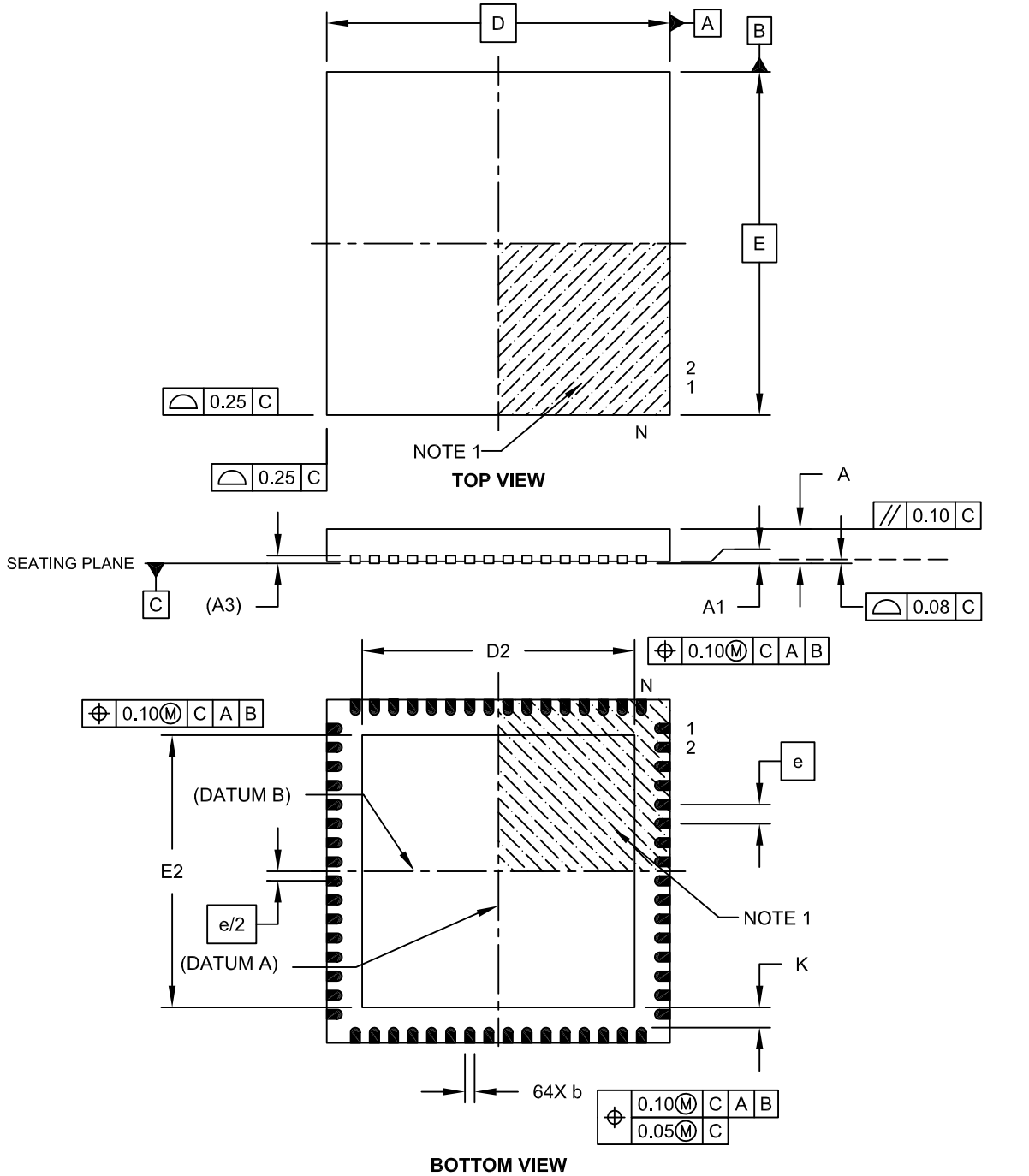


FIGURE 33-34: I2Cx BUS DATA TIMING CHARACTERISTICS (SLAVE MODE)



64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN]
With 7.15 x 7.15 Exposed Pad

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



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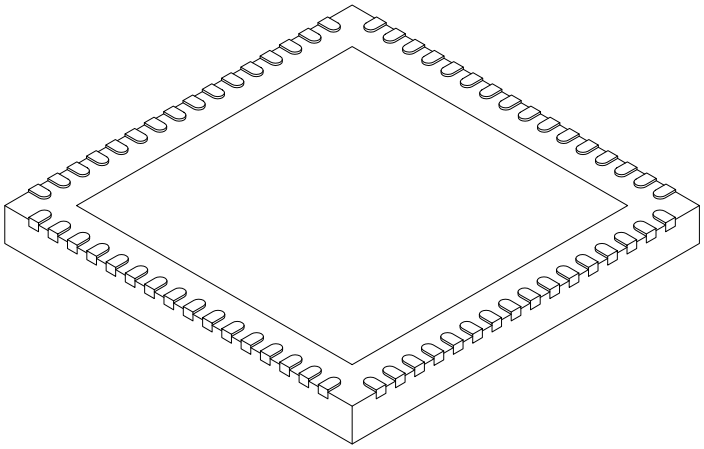
64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN]
With 7.15 x 7.15 Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		64	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		9.00 BSC	
Exposed Pad Width	E2	7.05	7.15	7.50
Overall Length	D		9.00 BSC	
Exposed Pad Length	D2	7.05	7.15	7.50
Contact Width	b	0.18	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

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