

Welcome to [E-XFL.COM](#)

What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPS
Connectivity	CANbus, I ² C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, Motor Control PWM, POR, PWM, WDT
Number of I/O	85
Program Memory Size	256KB (85.5K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 49x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	121-TFBGA
Supplier Device Package	121-TFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep256gm710-i-bg

dsPIC33EPXXXGM3XX/6XX/7XX

Pin Diagrams (Continued)

121-Pin TFBGA⁽¹⁾

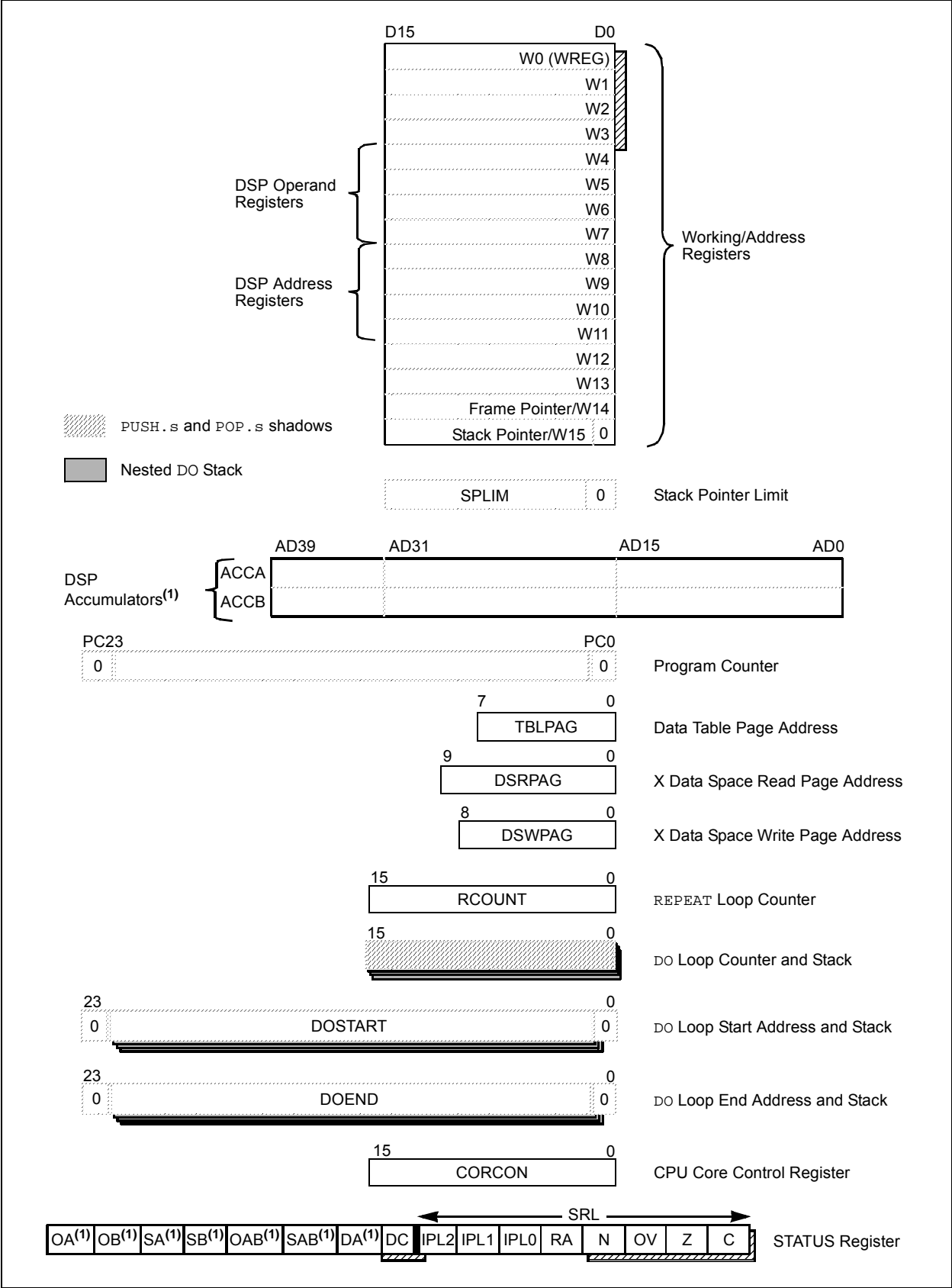
● = Pins are up to 5V tolerant

dsPIC33EP128GM310/710
dsPIC33EP256GM310/710
dsPIC33EP512GM310/710

	1	2	3	4	5	6	7	8	9	10	11
A	● RA10	● RB13	● RG13	● RB10	● RG0	● RF1	○ VDD	○ NC	● RD12	● RC6	○ RB9
B	○ NC	○ RG15	● RB12	● RB11	● RF7	● RF0	○ VCAP	● RD5	● RC7	○ VSS	○ RB8
C	● RB14	○ VDD	● RG12	● RG14	● RF6	○ NC	● RC9	● RC8	○ NC	○ RC13	○ RC10
D	● RD1	● RB15	● RA7	○ NC	○ NC	○ NC	● RD6	● RD13	○ RB7	○ NC	● RB6
E	● RD4	● RD3	○ RG6	● RD2	○ NC	● RG1	○ NC	○ RA15	● RD8	● RB5	○ RA14
F	● MCLR	○ RG8	○ RG9	○ RG7	○ VSS	○ NC	○ NC	○ VDD	○ RC12	○ VSS	○ RC15
G	○ RE8	○ RE9	○ RG10	○ NC	○ VDD	○ VSS	○ VSS	○ NC	○ RF5	○ RG3	○ RF4
H	○ RA12	○ RA11	○ NC	○ NC	○ NC	○ VDD	○ NC	○ RA9	○ RC3	○ RC5	○ RG2
J	○ RA0	○ RA1	○ RB3	○ AVDD	○ RC11	○ RG11	○ RE12	○ NC	○ NC	○ RE1	○ RC4
K	○ RB0	○ RB1	○ RF10	○ RC0	○ NC	○ RF12	○ RE14	○ VDD	○ RD15	○ RA4	○ RE0
L	○ RB2	○ RF9	○ AVSS	○ RC1	○ RC2	○ RF13	○ RE13	○ RE15	○ RD14	● RA8	● RB4

Note 1: Refer to Table 2 for full pin names.

FIGURE 3-2: PROGRAMMER'S MODEL



4.5 Modulo Addressing

Modulo Addressing mode is a method of providing an automated means to support circular data buffers using hardware. The objective is to remove the need for software to perform data address boundary checks when executing tightly looped code, as is typical in many DSP algorithms.

Modulo Addressing can operate in either Data or Program Space (since the Data Pointer mechanism is essentially the same for both). One circular buffer can be supported in each of the X (which also provides the pointers into Program Space) and Y Data Spaces. Modulo Addressing can operate on any W Register Pointer. However, it is not advisable to use W14 or W15 for Modulo Addressing since these two registers are used as the Stack Frame Pointer and Stack Pointer, respectively.

In general, any particular circular buffer can be configured to operate in only one direction, as there are certain restrictions on the buffer start address (for incrementing buffers) or end address (for decrementing buffers), based upon the direction of the buffer.

The only exception to the usage restrictions is for buffers that have a power-of-two length. As these buffers satisfy the start and end address criteria, they can operate in a Bidirectional mode (that is, address boundary checks are performed on both the lower and upper address boundaries).

4.5.1 START AND END ADDRESS

The Modulo Addressing scheme requires that a starting and ending address be specified and loaded into the 16-bit Modulo Buffer Address registers: XMODSRT, XMODEND, YMODSRT and YMODEND (see Table 4-1).

Note: Y space Modulo Addressing EA calculations assume word-sized data (LSb of every EA is always clear).

The length of a circular buffer is not directly specified. It is determined by the difference between the corresponding start and end addresses. The maximum possible length of the circular buffer is 32K words (64 Kbytes).

4.5.2 W ADDRESS REGISTER SELECTION

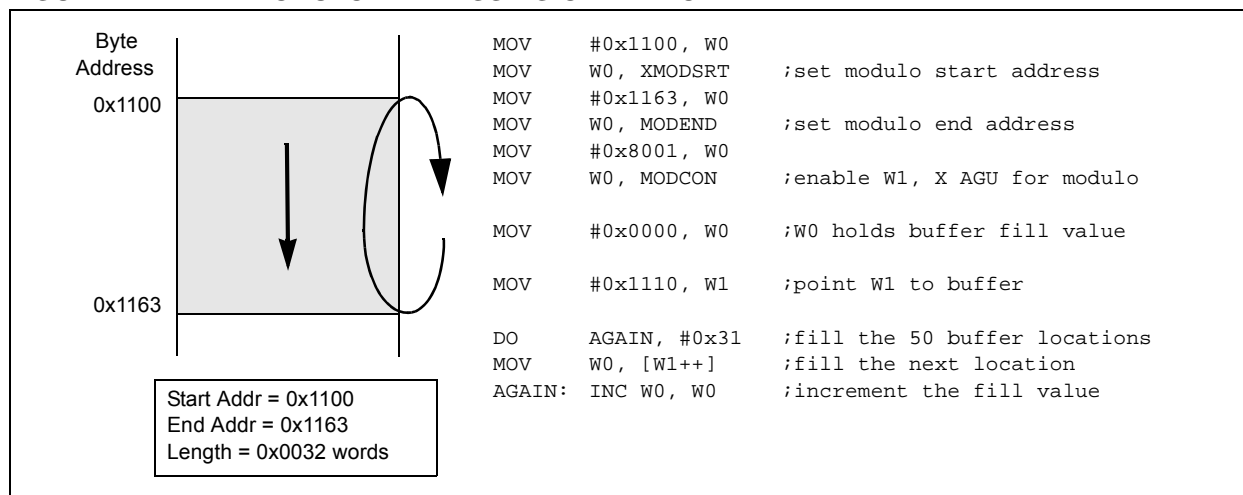
The Modulo and Bit-Reversed Addressing Control register bits, MODCON<15:0>, contain enable flags as well as a W register field to specify the W Address registers. The XWM and YWM fields select the registers that operate with Modulo Addressing:

- If XWM = 1111, X RAGU and X WAGU Modulo Addressing is disabled
- If YWM = 1111, Y AGU Modulo Addressing is disabled

The X Address Space Pointer W register (XWM) to which Modulo Addressing is to be applied is stored in MODCON<3:0> (see Table 4-1). Modulo Addressing is enabled for X Data Space when XWM is set to any value other than '1111' and the XMODEN bit is set (MODCON<15>).

The Y Address Space Pointer W register (YWM) to which Modulo Addressing is to be applied is stored in MODCON<7:4>. Modulo Addressing is enabled for Y Data Space when YWM is set to any value other than '1111' and the YMODEN bit is set (MODCON<14>).

FIGURE 4-14: MODULO ADDRESSING OPERATION EXAMPLE



5.0 FLASH PROGRAM MEMORY

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGM3XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the “dsPIC33/PIC24 Family Reference Manual”, “Flash Programming” (DS70609), which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGM3XX/6XX/7XX devices contain internal Flash program memory for storing and executing application code. The memory is readable, writable and erasable during normal operation, over the entire VDD range.

Flash memory can be programmed in two ways:

- In-Circuit Serial Programming™ (ICSP™)
- Run-Time Self-Programming (RTSP)

ICSP allows for a dsPIC33EPXXXGM3XX/6XX/7XX device to be serially programmed while in the end application circuit. This is done with two lines for programming clock and programming data (one of the alternate programming pin pairs: PGECx/PGEDx), and three other lines for power (VDD), ground (VSS) and

Master Clear ($\overline{\text{MCLR}}$). This allows customers to manufacture boards with unprogrammed devices and then program the device just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

RTSP is accomplished using TBLRD (Table Read) and TBLWT (Table Write) instructions. With RTSP, the user application can write program memory data as a double program memory word, a row of 64 instructions (192 bytes), and erase program memory in blocks of 512 instruction words (1536 bytes) at a time.

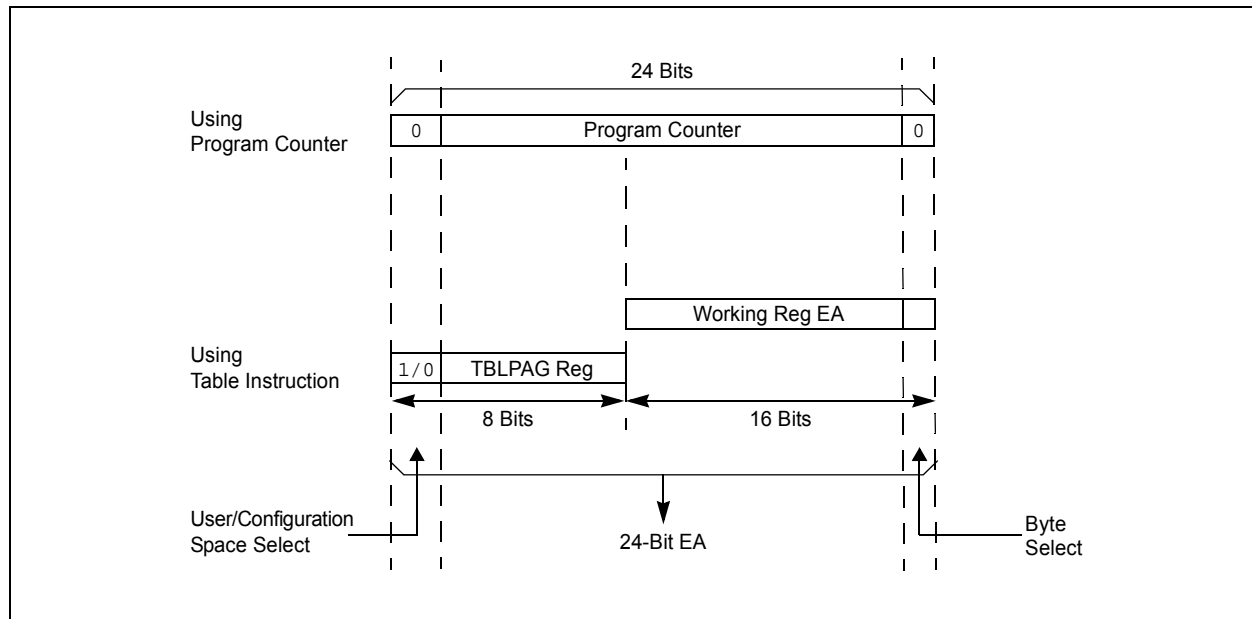
5.1 Table Instructions and Flash Programming

The Flash memory read and the double-word programming operations make use of the TBLRD and TBLWT instructions, respectively. These allow direct read and write access to the program memory space from the data memory while the device is in normal operating mode. The 24-bit target address in the program memory is formed using the TBLPAG<7:0> bits and the Effective Address (EA) from a W register, specified in the table instruction, as shown in Figure 5-1.

The TBLRDL and the TBLWTL instructions are used to read or write to bits<15:0> of program memory. TBLRDL and TBLWTL can access program memory in both Word and Byte modes.

The TBLRDH and TBLWTH instructions are used to read or write to bits<23:16> of program memory. TBLRDH and TBLWTH can also access program memory in Word or Byte mode.

FIGURE 5-1: ADDRESSING FOR TABLE REGISTERS



6.0 RESETS

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGM3XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the “dsPIC33/PIC24 Family Reference Manual”, “Reset” (DS70602), which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The Reset module combines all Reset sources and controls the device Master Reset Signal, $\overline{\text{SYSRST}}$. The following is a list of device Reset sources:

- POR: Power-on Reset
- BOR: Brown-out Reset
- MCLR: Master Clear Pin Reset
- SWR: RESET Instruction
- WDTO: Watchdog Timer Time-out Reset
- CM: Configuration Mismatch Reset
- TRAPR: Trap Conflict Reset
- IOPUWR: Illegal Condition Device Reset
 - Illegal Opcode Reset
 - Illegal Address Mode Reset
 - Uninitialized W Register Reset
 - Security Reset

A simplified block diagram of the Reset module is shown in Figure 6-1.

Any active source of Reset will make the $\overline{\text{SYSRST}}$ signal active. On system Reset, some of the registers associated with the CPU and peripherals are forced to a known Reset state and some are unaffected.

Note: Refer to the specific peripheral section or **Section 4.0 “Memory Organization”** of this manual for register Reset states.

All types of device Reset set a corresponding status bit in the RCON register to indicate the type of Reset (see Register 6-1).

A POR clears all the bits, except for the POR and BOR bits (RCON<1:0>) that are set. The user application can set or clear any bit at any time during code execution. The RCON bits only serve as status bits. Setting a particular Reset status bit in software does not cause a device Reset to occur.

The RCON register also has other bits associated with the Watchdog Timer and device power-saving states. The function of these bits is discussed in other sections of this manual.

Note: The status bits in the RCON register should be cleared after they are read so that the next RCON register value after a device Reset is meaningful.

Note: In all types of Resets, to select the device clock source, the contents of OSCCON are initialized from the FNOSC_x Configuration bits in the FOSCSEL Configuration register.

FIGURE 6-1: RESET SYSTEM BLOCK DIAGRAM

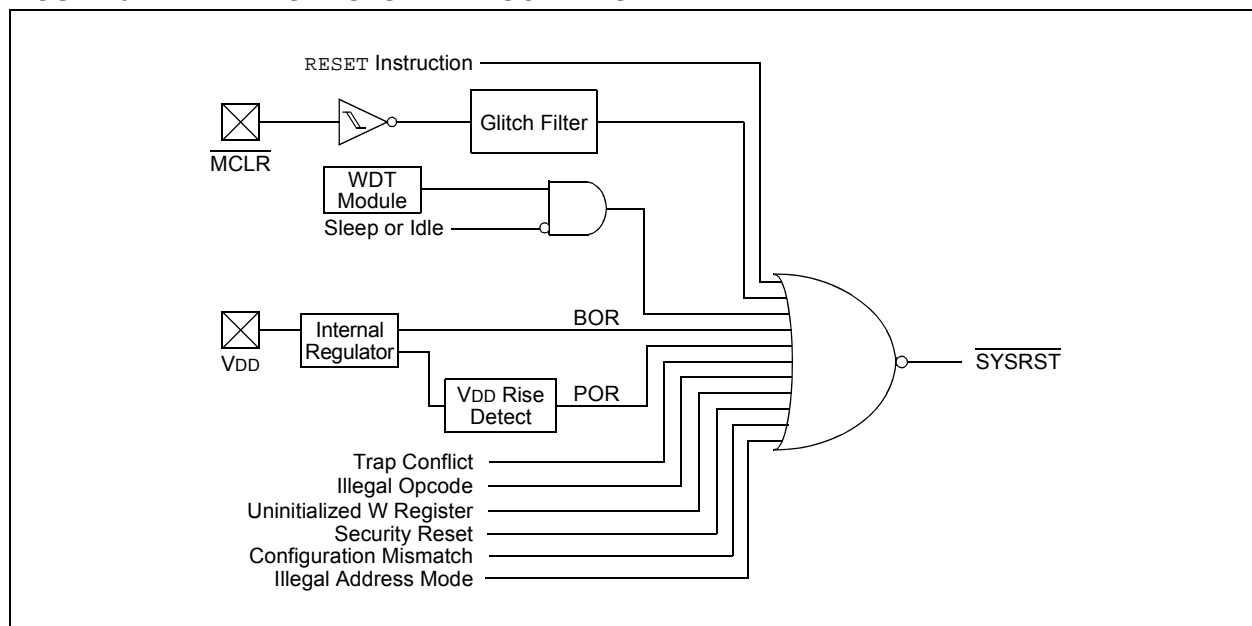


TABLE 7-1: INTERRUPT VECTOR DETAILS

Interrupt Source	Vector #	IRQ #	IVT Address	Interrupt Bit Location		
				Flag	Enable	Priority
Highest Natural Order Priority						
INT0 – External Interrupt 0	8	0	0x000014	IFS0<0>	IEC0<0>	IPC0<2:0>
IC1 – Input Capture 1	9	1	0x000016	IFS0<1>	IEC0<1>	IPC0<6:4>
OC1 – Output Compare 1	10	2	0x000018	IFS0<2>	IEC0<2>	IPC0<10:8>
T1 – Timer1	11	3	0x00001A	IFS0<3>	IEC0<3>	IPC0<14:12>
DMA0 – DMA Channel 0	12	4	0x00001C	IFS0<4>	IEC0<4>	IPC1<2:0>
IC2 – Input Capture 2	13	5	0x00001E	IFS0<5>	IEC0<5>	IPC1<6:4>
OC2 – Output Compare 2	14	6	0x000020	IFS0<6>	IEC0<6>	IPC1<10:8>
T2 – Timer2	15	7	0x000022	IFS0<7>	IEC0<7>	IPC1<14:12>
T3 – Timer3	16	8	0x000024	IFS0<8>	IEC0<8>	IPC2<2:0>
SPI1E – SPI1 Error	17	9	0x000026	IFS0<9>	IEC0<9>	IPC2<6:4>
SPI1 – SPI1 Transfer Done	18	10	0x000028	IFS0<10>	IEC0<10>	IPC2<10:8>
U1RX – UART1 Receiver	19	11	0x00002A	IFS0<11>	IEC0<11>	IPC2<14:12>
U1TX – UART1 Transmitter	20	12	0x00002C	IFS0<12>	IEC0<12>	IPC3<2:0>
AD1 – ADC1 Convert Done	21	13	0x00002E	IFS0<13>	IEC0<13>	IPC3<6:4>
DMA1 – DMA Channel 1	22	14	0x000030	IFS0<14>	IEC0<14>	IPC3<10:8>
Reserved	23	15	0x000032	—	—	—
SI2C1 – I2C1 Slave Event	24	16	0x000034	IFS1<0>	IEC1<0>	IPC4<2:0>
MI2C1 – I2C1 Master Event	25	17	0x000036	IFS1<1>	IEC1<1>	IPC4<6:4>
CMP1 – Comparator Combined Event	26	18	0x000038	IFS1<2>	IEC1<2>	IPC4<10:8>
CN – Input Change Interrupt	27	19	0x00003A	IFS1<3>	IEC1<3>	IPC4<14:12>
INT1 – External Interrupt 1	28	20	0x00003C	IFS1<4>	IEC1<4>	IPC5<2:0>
AD2 – ADC2 Convert Done	29	21	0x00003E	IFS1<5>	IEC1<5>	IPC5<6:4>
IC7 – Input Capture 7	30	22	0x000040	IFS1<6>	IEC1<6>	IPC5<10:8>
IC8 – Input Capture 8	31	23	0x000042	IFS1<7>	IEC1<7>	IPC5<14:12>
DMA2 – DMA Channel 2	32	24	0x000044	IFS1<8>	IEC1<8>	IPC6<2:0>
OC3 – Output Compare 3	33	25	0x000046	IFS1<9>	IEC1<9>	IPC6<6:4>
OC4 – Output Compare 4	34	26	0x000048	IFS1<10>	IEC1<10>	IPC6<10:8>
T4 – Timer4	35	27	0x00004A	IFS1<11>	IEC1<11>	IPC6<14:12>
T5 – Timer5	36	28	0x00004C	IFS1<12>	IEC1<12>	IPC7<2:0>
INT2 – External Interrupt 2	37	29	0x00004E	IFS1<13>	IEC1<13>	IPC7<6:4>
U2RX – UART2 Receiver	38	30	0x000050	IFS1<14>	IEC1<14>	IPC7<10:8>
U2TX – UART2 Transmitter	39	31	0x000052	IFS1<15>	IEC1<15>	IPC7<14:12>
SPI2E – SPI2 Error	40	32	0x000054	IFS2<0>	IEC2<0>	IPC8<2:0>
SPI2 – SPI2 Transfer Done	41	33	0x000056	IFS2<1>	IEC2<1>	IPC8<6:4>
C1RX – CAN1 RX Data Ready ⁽¹⁾	42	34	0x000058	IFS2<2>	IEC2<2>	IPC8<10:8>
C1 – CAN1 Event ⁽¹⁾	43	35	0x00005A	IFS2<3>	IEC2<3>	IPC8<14:12>
DMA3 – DMA Channel 3	44	36	0x00005C	IFS2<4>	IEC2<4>	IPC9<2:0>
IC3 – Input Capture 3	45	37	0x00005E	IFS2<5>	IEC2<5>	IPC9<6:4>
IC4 – Input Capture 4	46	38	0x000060	IFS2<6>	IEC2<6>	IPC9<10:8>
IC5 – Input Capture 5	47	39	0x000062	IFS2<7>	IEC2<7>	IPC9<14:12>
IC6 – Input Capture 6	48	40	0x000064	IFS2<8>	IEC2<8>	IPC10<2:0>

Note 1: This interrupt source is available on dsPIC33EPXXXGM6XX/7XX devices only.

2: This interrupt source is not available on 44-pin devices.

REGISTER 8-5: DMAxSTBH: DMA CHANNEL x START ADDRESS REGISTER B (HIGH)

U-0	U-0	U-0	U-0	R/W-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15				bit 8			
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STB<23:16>							
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **STB<23:16>:** DMA Secondary Start Address bits (source or destination)

REGISTER 8-6: DMAxSTBL: DMA CHANNEL x START ADDRESS REGISTER B (LOW)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STB<15:8>							
bit 15				bit 8			
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STB<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **STB<15:0>:** DMA Secondary Start Address bits (source or destination)

NOTES:

TABLE 9-1: CONFIGURATION BIT VALUES FOR CLOCK SELECTION

Oscillator Mode	Oscillator Source	POSCMD<1:0>	FNOSC<2:0>	See Notes
Fast RC Oscillator with Divide-by-N (FRCDIVN)	Internal	xx	111	1, 2
Fast RC Oscillator with Divide-by-16 (FRCDIV16)	Internal	xx	110	1
Low-Power RC Oscillator (LPRC)	Internal	xx	101	1
Secondary (Timer1) Oscillator (SOSC)	Secondary	xx	100	1
Primary Oscillator (HS) with PLL (HSPLL)	Primary	10	011	
Primary Oscillator (XT) with PLL (XTPLL)	Primary	01	011	
Primary Oscillator (EC) with PLL (ECPLL)	Primary	00	011	1
Primary Oscillator (HS)	Primary	10	010	
Primary Oscillator (XT)	Primary	01	010	
Primary Oscillator (EC)	Primary	00	010	1
Fast RC Oscillator (FRC) with Divide-by-N and PLL (FRCPLL)	Internal	xx	001	1
Fast RC Oscillator (FRC)	Internal	xx	000	1

Note 1: OSC2 pin function is determined by the OSCIOFNC Configuration bit.

2: This is the default oscillator mode for an unprogrammed (erased) device.

REGISTER 11-3: RPINR3: PERIPHERAL PIN SELECT INPUT REGISTER 3

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	T2CKR<6:0>						
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-7

Unimplemented: Read as '0'

bit 6-0

T2CKR<6:0>: Assign Timer2 External Clock (T2CK) to the Corresponding RPn pin bits (see Table 11-2 for input pin selection numbers)

1111100 = Input tied to RPI124

-
-
-

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

REGISTER 11-24: RPINR30: PERIPHERAL PIN SELECT INPUT REGISTER 30

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	SS3R<6:0>						
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-7

Unimplemented: Read as '0'

bit 6-0

SS3R<6:0>: Assign SPI3 Slave Select Input ($\overline{SS3}$) to the Corresponding RPN/RPIN Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP124

•

•

•

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

dsPIC33EPXXXGM3XX/6XX/7XX

REGISTER 16-11: PWMCONx: PWMx CONTROL REGISTER

HS/HC-0	HS/HC-0	HS/HC-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
FLTSTAT ⁽¹⁾	CLSTAT ⁽¹⁾	TRGSTAT	FLTIE	CLIE	TRGIE	ITB ⁽²⁾	MDCS ⁽²⁾
bit 15							bit 8

R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
DTC1	DTC0	DTCP ⁽³⁾	—	MTBS	CAM ^(2,4)	XPRES ⁽⁵⁾	IUE ⁽²⁾
bit 7							bit 0

Legend:	HC = Hardware Clearable bit	HS = Hardware Settable bit
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

- bit 15 **FLTSTAT:** Fault Interrupt Status bit⁽¹⁾
 1 = Fault interrupt is pending
 0 = No Fault interrupt is pending
 This bit is cleared by setting: FLTIE = 0.
- bit 14 **CLSTAT:** Current-Limit Interrupt Status bit⁽¹⁾
 1 = Current-limit interrupt is pending
 0 = No current-limit interrupt is pending
 This bit is cleared by setting: CLIE = 0.
- bit 13 **TRGSTAT:** Trigger Interrupt Status bit
 1 = Trigger interrupt is pending
 0 = No trigger interrupt is pending
 This bit is cleared by setting: TRGIE = 0.
- bit 12 **FLTIE:** Fault Interrupt Enable bit
 1 = Fault interrupt is enabled
 0 = Fault interrupt is disabled and the FLTSTAT bit is cleared
- bit 11 **CLIE:** Current-Limit Interrupt Enable bit
 1 = Current-limit interrupt is enabled
 0 = Current-limit interrupt is disabled and the CLSTAT bit is cleared
- bit 10 **TRGIE:** Trigger Interrupt Enable bit
 1 = A trigger event generates an interrupt request
 0 = Trigger event interrupts are disabled and the TRGSTAT bit is cleared
- bit 9 **ITB:** Independent Time Base Mode bit⁽²⁾
 1 = PHASEx register provides the time base period for this PWMx generator
 0 = PTPER register provides timing for this PWMx generator
- bit 8 **MDCS:** Master Duty Cycle Register Select bit⁽²⁾
 1 = MDC register provides duty cycle information for this PWMx generator
 0 = PDCx register provides duty cycle information for this PWMx generator

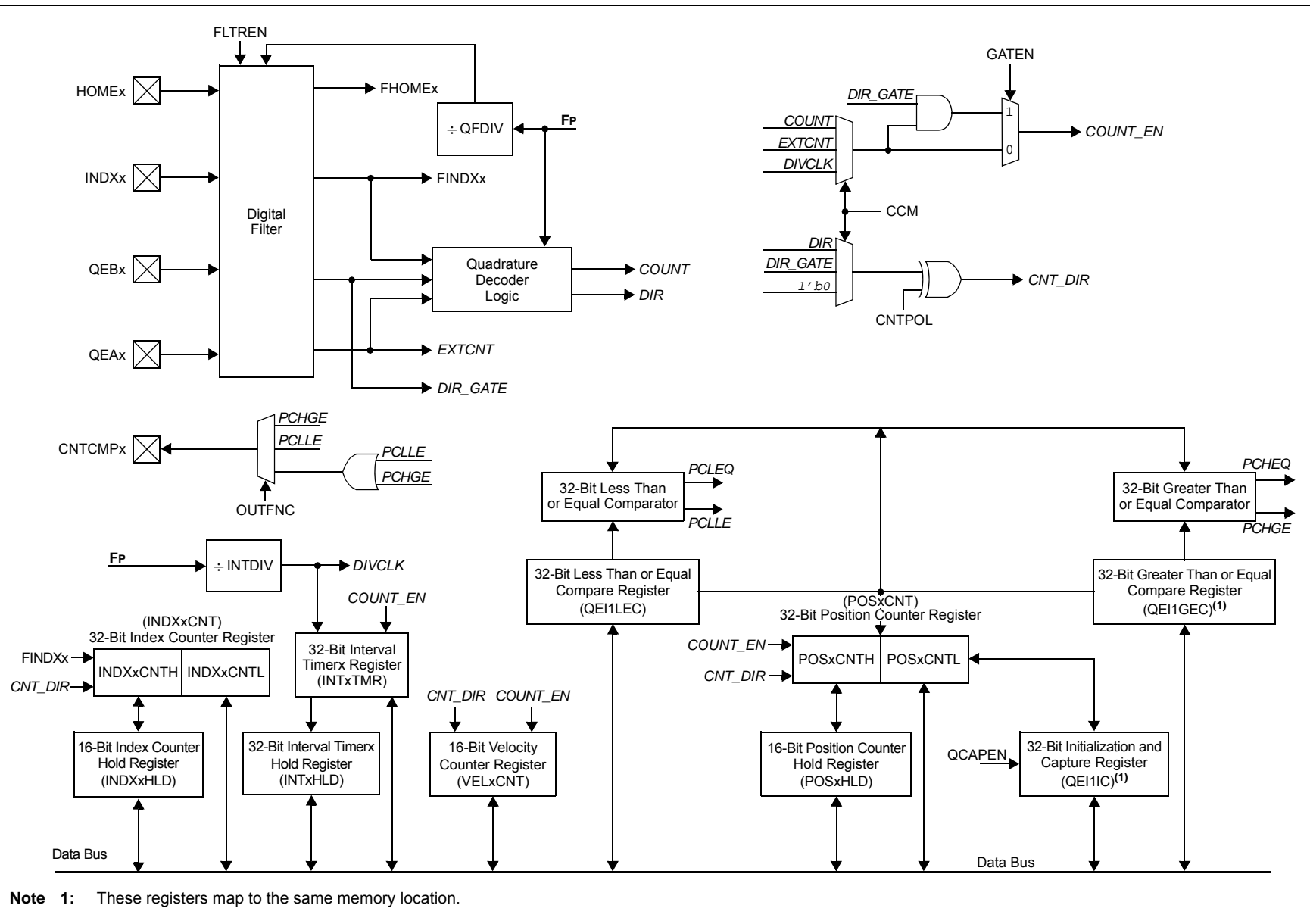
- Note 1:** Software must clear the interrupt status here and in the corresponding IFSx bit in the interrupt controller.
- Note 2:** These bits should not be changed after the PWMx is enabled (PTEN = 1).
- Note 3:** DTC<1:0> = 11 for DTCP to be effective; otherwise, DTCP is ignored.
- Note 4:** The Independent Time Base (ITB = 1) mode must be enabled to use Center-Aligned mode. If ITB = 0, the CAM bit is ignored.
- Note 5:** To operate in External Period Reset mode, the ITB bit must be '1' and the CLMOD bit in the FCLCONx register must be '0'.

REGISTER 16-21: FCLCONx: PWMx FAULT CURRENT-LIMIT CONTROL REGISTER (CONTINUED)

bit 7-3	FLTSRC<4:0>: Fault Control Signal Source Select for PWMx Generator # bits 11111 = Fault 32 (default) 11110 = Reserved • • • 01100 = Op Amp/Comparator 5 01011 = Comparator 4 01010 = Op Amp/Comparator 3 01001 = Op Amp/Comparator 2 01000 = Op Amp/Comparator 1 00111 = Fault 8 00110 = Fault 7 00101 = Fault 6 00100 = Fault 5 00011 = Fault 4 00010 = Fault 3 00001 = Fault 2 00000 = Fault 1
bit 2	FLTPOL: Fault Polarity for PWMx Generator # bit ⁽¹⁾ 1 = The selected Fault source is active-low 0 = The selected Fault source is active-high
bit 1-0	FLTMOD<1:0>: Fault Mode for PWMx Generator # bits 11 = Fault input is disabled 10 = Reserved 01 = The selected Fault source forces the PWMxH, PWMxL pins to FLTDATx values (cycle) 00 = The selected Fault source forces the PWMxH, PWMxL pins to FLTDATx values (latched condition)

Note 1: These bits should be changed only when PTEN = 0. Changing the clock selection during operation will yield unpredictable results.

dsPIC33EPXXGM3XX/6XX/7XX



BUFFER 21-3: CANx MESSAGE BUFFER WORD 2

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
EID5	EID4	EID3	EID2	EID1	EID0	RTR	RB1
bit 15							bit 8

U-x	U-x	U-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	—	RB0	DLC3	DLC2	DLC1	DLC0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15-10 **EID<5:0>**: Extended Identifier bits
- bit 9 **RTR**: Remote Transmission Request bit
When IDE = 1:
 1 = Message will request remote transmission
 0 = Normal message
When IDE = 0:
 The RTR bit is ignored.
- bit 8 **RB1**: Reserved Bit 1
 User must set this bit to '0' per CAN protocol.
- bit 7-5 **Unimplemented**: Read as '0'
- bit 4 **RB0**: Reserved Bit 0
 User must set this bit to '0' per CAN protocol.
- bit 3-0 **DLC<3:0>**: Data Length Code bits

BUFFER 21-4: CANx MESSAGE BUFFER WORD 3

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Byte 1<15:8>							
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Byte 0<7:0>							
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15-8 **Byte 1<15:8>**: CANx Message Byte 1
- bit 7-0 **Byte 0<7:0>**: CANx Message Byte 0

23.2 ADCx Helpful Tips

1. The SMP1x control bits in the ADxCON2 registers:
 - a) Determine when the ADCx interrupt flag is set and an interrupt is generated, if enabled.
 - b) When the CSCNA bit in the ADxCON2 register is set to '1', this determines when the ADCx analog scan channel list, defined in the AD1CSSL/AD1CSSH registers, starts over from the beginning.
 - c) When the DMA peripheral is not used (ADDMAEN = 0), this determines when the ADCx Result Buffer Pointer to ADC1BUF0-ADC1BUFF gets reset back to the beginning at ADC1BUF0.
 - d) When the DMA peripheral is used (ADDMAEN = 1), this determines when the DMA Address Pointer is incremented after a sample/conversion operation. ADC1BUF0 is the only ADCx buffer used in this mode. The ADCx Result Buffer Pointer to ADC1BUF0-ADC1BUFF gets reset back to the beginning at ADC1BUF0. The DMA address is incremented after completion of every 32nd sample/conversion operation. Conversion results are stored in the ADC1BUF0 register for transfer to RAM using the DMA peripheral.
2. When the DMA module is disabled (ADDMAEN = 0), the ADCx has 16 result buffers. ADCx conversion results are stored sequentially in ADC1BUF0-ADC1BUFF, regardless of which analog inputs are being used subject to the SMP1x bits and the condition described in 1.c) above. There is no relationship between the ANx input being measured and which ADCx buffer (ADC1BUF0-ADC1BUFF) that the conversion results will be placed in.
3. When the DMA module is enabled (ADDMAEN = 1), the ADCx module has only 1 ADCx result buffer (i.e., ADC1BUF0) per ADCx peripheral and the ADCx conversion result must be read, either by the CPU or DMA Controller, before the next ADCx conversion is complete to avoid overwriting the previous value.
4. The DONE bit (ADxCON1<0>) is only cleared at the start of each conversion and is set at the completion of the conversion, but remains set indefinitely, even through the next sample phase until the next conversion begins. If application code is monitoring the DONE bit in any kind of software loop, the user must consider this behavior because the CPU code execution is faster than the ADCx. As a result, in Manual Sample mode, particularly where the user's code is setting the SAMP bit (ADxCON1<1>), the DONE bit should also be cleared by the user application just before setting the SAMP bit.
5. Enabling op amps, comparator inputs and external voltage references can limit the availability of analog inputs (ANx pins). For example, when Op Amp 2 is enabled, the pins for AN0, AN1 and AN2 are used by the op amp's inputs and output. This negates the usefulness of Alternate Input mode since the MUXA selections use AN0-AN2. Carefully study the ADCx block diagram to determine the configuration that will best suit your application. Configuration examples are available in the *"dsPIC33/PIC24 Family Reference Manual"*, **"Analog-to-Digital Converter (ADC)"** (DS70621)

25.2 PTG Control Registers

REGISTER 25-1: PTGCST: PTG CONTROL/STATUS REGISTER

R/W-0	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
PTGEN	—	PTGSIDL	PTGTOGL	—	PTGSWT ⁽²⁾	PTGSSEN	PTGIVIS
bit 15							bit 8

R/W-0	HS-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
PTGSTRT	PTGWDTO	—	—	—	—	PTGITM1 ⁽¹⁾	PTGITM0 ⁽¹⁾
bit 7							bit 0

Legend:	HS = Hardware Settable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 15 **PTGEN:** PTG Module Enable bit
 1 = PTG module is enabled
 0 = PTG module is disabled
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **PTGSIDL:** PTG Stop in Idle Mode bit
 1 = Discontinues module operation when device enters Idle mode
 0 = Continues module operation in Idle mode
- bit 12 **PTGTOGL:** PTG TRIG Output Toggle Mode bit
 1 = Toggles the state of the PTGOx for each execution of the PTGTRIG command
 0 = Each execution of the PTGTRIG command will generate a single PTGOx pulse determined by the value in the PTGPWDx bits
- bit 11 **Unimplemented:** Read as '0'
- bit 10 **PTGSWT:** PTG Software Trigger bit⁽²⁾
 1 = Triggers the PTG module
 0 = No action (clearing this bit will have no effect)
- bit 9 **PTGSSEN:** PTG Enable Single-Step bit
 1 = Enables Single-Step mode
 0 = Disables Single-Step mode
- bit 8 **PTGIVIS:** PTG Counter/Timer Visibility Control bit
 1 = Reads of the PTGSDLIM, PTGCxLIM or PTGTxLIM registers return the current values of their corresponding Counter/Timer registers (PTGSD, PTGCx, PTGTx)
 0 = Reads of the PTGSDLIM, PTGCxLIM or PTGTxLIM registers return the value previously written to those PTG Limit registers
- bit 7 **PTGSTRT:** Start PTG Sequencer bit
 1 = Starts to sequentially execute commands (Continuous mode)
 0 = Stops executing commands
- bit 6 **PTGWDTO:** PTG Watchdog Timer Time-out Status bit
 1 = PTG Watchdog Timer has timed out
 0 = PTG Watchdog Timer has not timed out.
- bit 5-2 **Unimplemented:** Read as '0'

- Note 1:** These bits apply to the PTGWHI and PTGWLO commands only.
Note 2: This bit is only used with the PTGCTRL Step command software trigger option.

TABLE 31-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Base Instr #	Assembly Mnemonic	Assembly Syntax	Description	# of Words	# of Cycles	Status Flags Affected
72	SL	SL f	f = Left Shift f	1	1	C,N,OV,Z
		SL f, WREG	WREG = Left Shift f	1	1	C,N,OV,Z
		SL Ws, Wd	Wd = Left Shift Ws	1	1	C,N,OV,Z
		SL Wb, Wns, Wnd	Wnd = Left Shift Wb by Wns	1	1	N,Z
		SL Wb, #lit5, Wnd	Wnd = Left Shift Wb by lit5	1	1	N,Z
73	SUB	SUB Acc	Subtract Accumulators	1	1	OA,OB,OAB,SA,SB,SAB
		SUB f	f = f – WREG	1	1	C,DC,N,OV,Z
		SUB f, WREG	WREG = f – WREG	1	1	C,DC,N,OV,Z
		SUB #lit10, Wn	Wn = Wn – lit10	1	1	C,DC,N,OV,Z
		SUB Wb, Ws, Wd	Wd = Wb – Ws	1	1	C,DC,N,OV,Z
		SUB Wb, #lit5, Wd	Wd = Wb – lit5	1	1	C,DC,N,OV,Z
74	SUBB	SUBB f	f = f – WREG – (\overline{C})	1	1	C,DC,N,OV,Z
		SUBB f, WREG	WREG = f – WREG – (\overline{C})	1	1	C,DC,N,OV,Z
		SUBB #lit10, Wn	Wn = Wn – lit10 – (\overline{C})	1	1	C,DC,N,OV,Z
		SUBB Wb, Ws, Wd	Wd = Wb – Ws – (\overline{C})	1	1	C,DC,N,OV,Z
		SUBB Wb, #lit5, Wd	Wd = Wb – lit5 – (\overline{C})	1	1	C,DC,N,OV,Z
75	SUBR	SUBR f	f = WREG – f	1	1	C,DC,N,OV,Z
		SUBR f, WREG	WREG = WREG – f	1	1	C,DC,N,OV,Z
		SUBR Wb, Ws, Wd	Wd = Ws – Wb	1	1	C,DC,N,OV,Z
		SUBR Wb, #lit5, Wd	Wd = lit5 – Wb	1	1	C,DC,N,OV,Z
76	SUBBR	SUBBR f	f = WREG – f – (\overline{C})	1	1	C,DC,N,OV,Z
		SUBBR f, WREG	WREG = WREG – f – (\overline{C})	1	1	C,DC,N,OV,Z
		SUBBR Wb, Ws, Wd	Wd = Ws – Wb – (\overline{C})	1	1	C,DC,N,OV,Z
		SUBBR Wb, #lit5, Wd	Wd = lit5 – Wb – (\overline{C})	1	1	C,DC,N,OV,Z
77	SWAP	SWAP.b Wn	Wn = nibble swap Wn	1	1	None
		SWAP Wn	Wn = byte swap Wn	1	1	None
78	TBLRDH	TBLRDH Ws, Wd	Read Prog<23:16> to Wd<7:0>	1	5	None
79	TBLRDL	TBLRDL Ws, Wd	Read Prog<15:0> to Wd	1	5	None
80	TBLWTH	TBLWTH Ws, Wd	Write Ws<7:0> to Prog<23:16>	1	2	None
81	TBLWTL	TBLWTL Ws, Wd	Write Ws to Prog<15:0>	1	2	None
82	ULNK	ULNK	Unlink Frame Pointer	1	1	SFA
83	XOR	XOR f	f = f .XOR. WREG	1	1	N,Z
		XOR f, WREG	WREG = f .XOR. WREG	1	1	N,Z
		XOR #lit10, Wn	Wd = lit10 .XOR. Wd	1	1	N,Z
		XOR Wb, Ws, Wd	Wd = Wb .XOR. Ws	1	1	N,Z
		XOR Wb, #lit5, Wd	Wd = Wb .XOR. lit5	1	1	N,Z
84	ZE	ZE Ws, Wnd	Wnd = Zero-extend Ws	1	1	C,Z,N

Note: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

FIGURE 33-3: I/O TIMING CHARACTERISTICS

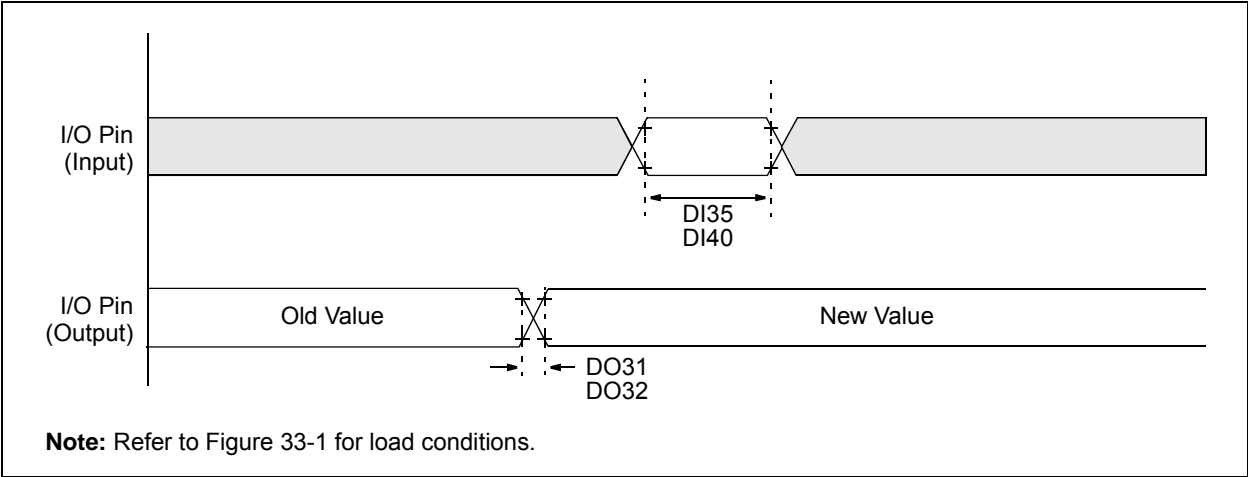
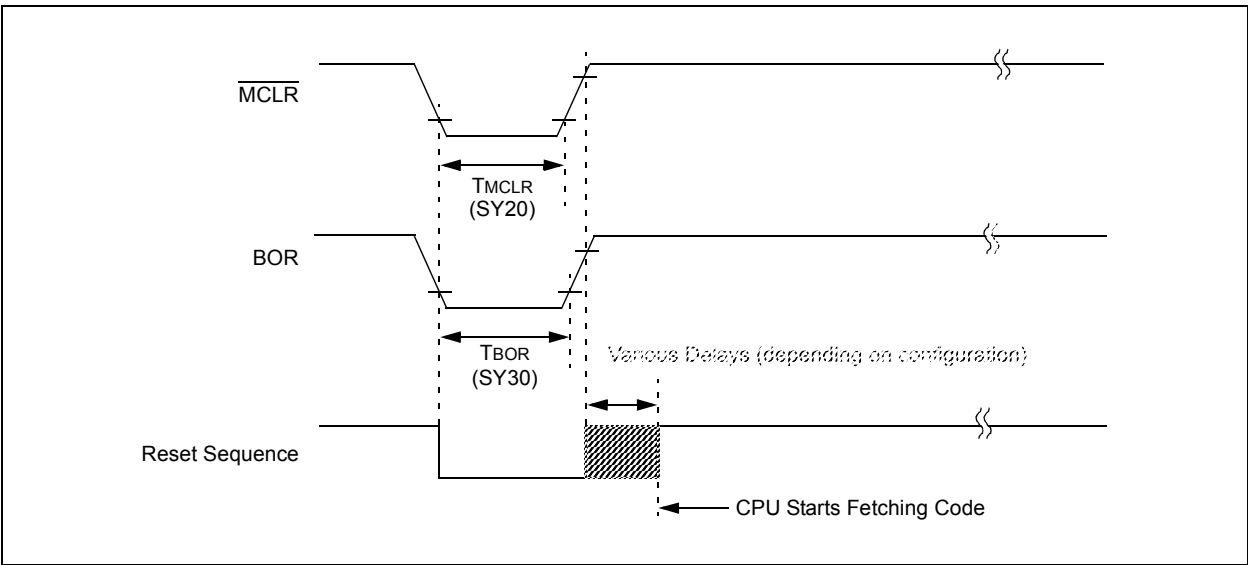


TABLE 33-20: I/O TIMING REQUIREMENTS

AC CHARACTERISTICS				Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Param No.	Symbol	Characteristic	Min.	Typ. ⁽¹⁾	Max.	Units	Conditions
DO31	TioR	Port Output Rise Time	—	5	10	ns	
DO32	TioF	Port Output Fall Time	—	5	10	ns	
DI35	TINP	INTx Pin High or Low Time (input)	20	—	—	ns	
DI40	TRBP	CNx High or Low Time (input)	2	—	—	Tcy	

Note 1: Data in “Typical” column is at 3.3V, +25°C unless otherwise stated.

FIGURE 33-4: BOR AND MASTER CLEAR RESET TIMING CHARACTERISTICS



dsPIC33EPXXXGM3XX/6XX/7XX

NOTES: