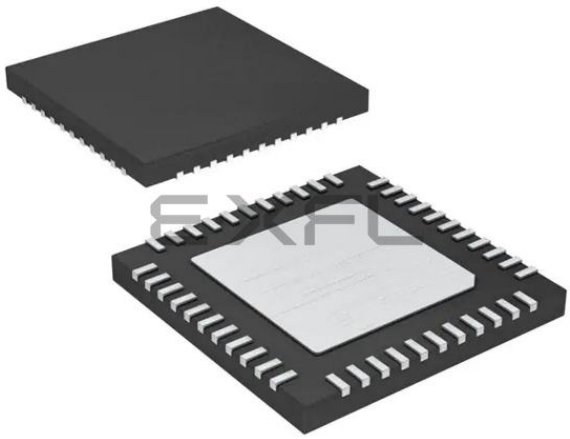

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | dsPIC |
| Core Size | 16-Bit |
| Speed | 60 MIPs |
| Connectivity | I²C, IrDA, LINbus, QEI, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, Motor Control PWM, POR, PWM, WDT |
| Number of I/O | 35 |
| Program Memory Size | 512KB (170K x 24) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 48K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 3.6V |
| Data Converters | A/D 18x10b/12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 44-VQFN Exposed Pad |
| Supplier Device Package | 44-QFN (8x8) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep512gm304-e-ml |

## Pin Diagrams (Continued)

**121-Pin TFBGA(1)**

● = Pins are up to 5V tolerant

**dsPIC33EP128GM310/710**
**dsPIC33EP256GM310/710**
**dsPIC33EP512GM310/710**

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| A | RA10 | RB13 | RG13 | RB10 | RG0 | RF1 | VDD | NC | RD12 | RC6 | RB9 |
| B | NC | RG15 | RB12 | RB11 | RF7 | RF0 | VCAP | RD5 | RC7 | VSS | RB8 |
| C | RB14 | VDD | RG12 | RG14 | RF6 | NC | RC9 | RC8 | NC | RC13 | RC10 |
| D | RD1 | RB15 | RA7 | NC | NC | NC | RD6 | RD13 | RB7 | NC | RB6 |
| E | RD4 | RD3 | RG6 | RD2 | NC | RG1 | NC | RA15 | RD8 | RB5 | RA14 |
| F | $\overline{\text{MCLR}}$ | RG8 | RG9 | RG7 | VSS | NC | NC | VDD | RC12 | VSS | RC15 |
| G | RE8 | RE9 | RG10 | NC | VDD | VSS | VSS | NC | RF5 | RG3 | RF4 |
| H | RA12 | RA11 | NC | NC | NC | VDD | NC | RA9 | RC3 | RC5 | RG2 |
| J | RA0 | RA1 | RB3 | AVDD | RC11 | RG11 | RE12 | NC | NC | RE1 | RC4 |
| K | RB0 | RB1 | RF10 | RC0 | NC | RF12 | RE14 | VDD | RD15 | RA4 | RE0 |
| L | RB2 | RF9 | AVSS | RC1 | RC2 | RF13 | RE13 | RE15 | RD14 | RA8 | RB4 |

**Note 1:** Refer to Table 2 for full pin names.

**TABLE 4-22: ADC1 AND ADC2 REGISTER MAP (CONTINUED)**

| SFR Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ADC2BUF9 | 0352 | ADC2 Data Buffer 9 | | | | | | | | | | | | | | | | xxxx |
| ADC2BUFA | 0354 | ADC2 Data Buffer 10 | | | | | | | | | | | | | | | | xxxx |
| ADC2BUFB | 0356 | ADC2 Data Buffer 11 | | | | | | | | | | | | | | | | xxxx |
| ADC2BUFC | 0358 | ADC2 Data Buffer 12 | | | | | | | | | | | | | | | | xxxx |
| ADC2BUFD | 035A | ADC2 Data Buffer 13 | | | | | | | | | | | | | | | | xxxx |
| ADC2BUFE | 035C | ADC2 Data Buffer 14 | | | | | | | | | | | | | | | | xxxx |
| ADC2BUFF | 035E | ADC2 Data Buffer 15 | | | | | | | | | | | | | | | | xxxx |
| AD2CON1 | 0360 | ADON | — | ADSIDL | ADDMABM | — | AD12B | FORM1 | FORM0 | SSRC2 | SSRC1 | SSRC0 | SSRCG | SIMSAM | ASAM | SAMP | DONE | 0000 |
| AD2CON2 | 0362 | VCFG2 | VCFG1 | VCFG0 | OFFCAL | — | CSCNA | CHPS1 | CHPS0 | BUFS | SMPI4 | SMPI3 | SMPI2 | SMPI1 | SMPI0 | BUFM | ALTS | 0000 |
| AD2CON3 | 0364 | ADRC | — | — | SAMC4 | SAMC3 | SAMC2 | SAMC1 | SAMC0 | ADCS7 | ADCS6 | ADCS5 | ADCS4 | ADCS3 | ADCS2 | ADCS1 | ADCS0 | 0000 |
| AD2CHS123 | 0366 | — | — | — | CH123SB2 | CH123SB1 | CH123NB1 | CH123NB0 | CH123SB0 | — | — | — | CH123SA2 | CH123SA1 | CH123NA1 | CH123NA0 | CH123SA0 | 0000 |
| AD2CHS0 | 0368 | CH0NB | — | CH0SB5(1) | CH0SB4 | CH0SB3 | CH0SB2 | CH0SB1 | CH0SB0 | CH0NA | — | CH0SA5(1) | CH0SA4 | CH0SA3 | CH0SA2 | CH0SA1 | CH0SA0 | 0000 |
| AD2CSSH | 036E | CSS<31:16> | | | | | | | | | | | | | | | | 0000 |
| AD2CSSL | 0370 | CSS<15:0> | | | | | | | | | | | | | | | | 0000 |
| AD2CON4 | 0372 | — | — | — | — | — | — | — | ADDMAEN | — | — | — | — | — | DMABL2 | DMABL1 | DMABL0 | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** Bits 13 and bit 5 are reserved in the AD2CHS0 register, unlike the AD1CHS0 register.

**TABLE 4-25: CAN1 REGISTER MAP WHEN WIN (C1CTRL<0>) = 1 FOR dsPIC33EPXXXGM60X/7XX DEVICES(1)**

| SFR Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0400-041E | See definition when WIN = x | | | | | | | | | | | | | | | | |
| C1BUFPNT1 | 0420 | F3BP3 | F3BP2 | F3BP1 | F3BP0 | F2BP3 | F2BP2 | F2BP1 | F2BP0 | F1BP3 | F1BP2 | F1BP1 | F1BP0 | F0BP3 | F0BP2 | F0BP1 | F0BP0 | 0000 |
| C1BUFPNT2 | 0422 | F7BP3 | F7BP2 | F7BP1 | F7BP0 | F6BP3 | F6BP2 | F6BP1 | F6BP0 | F5BP3 | F5BP2 | F5BP1 | F5BP0 | F4BP3 | F4BP2 | F4BP1 | F4BP0 | 0000 |
| C1BUFPNT3 | 0424 | F11BP3 | F11BP2 | F11BP1 | F11BP0 | F10BP3 | F10BP2 | F10BP1 | F10BP0 | F9BP3 | F9BP2 | F9BP1 | F9BP0 | F8BP3 | F8BP2 | F8BP1 | F8BP0 | 0000 |
| C1BUFPNT4 | 0426 | F15BP3 | F15BP2 | F15BP1 | F15BP0 | F14BP3 | F14BP2 | F14BP1 | F14BP0 | F13BP3 | F13BP2 | F13BP1 | F13BP0 | F12BP3 | F12BP2 | F12BP1 | F12BP0 | 0000 |
| C1RXM0SID | 0430 | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | — | MIDE | — | EID17 | EID16 | xxxx |
| C1RXM0EID | 0432 | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| C1RXM1SID | 0434 | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | — | MIDE | — | EID17 | EID16 | xxxx |
| C1RXM1EID | 0436 | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| C1RXM2SID | 0438 | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | — | MIDE | — | EID17 | EID16 | xxxx |
| C1RXM2EID | 043A | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| C1RXF0SID | 0440 | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | — | EXIDE | — | EID17 | EID16 | xxxx |
| C1RXF0EID | 0442 | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| C1RXF1SID | 0444 | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | — | EXIDE | — | EID17 | EID16 | xxxx |
| C1RXF1EID | 0446 | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| C1RXF2SID | 0448 | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | — | EXIDE | — | EID17 | EID16 | xxxx |
| C1RXF2EID | 044A | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| C1RXF3SID | 044C | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | — | EXIDE | — | EID17 | EID16 | xxxx |
| C1RXF3EID | 044E | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| C1RXF4SID | 0450 | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | — | EXIDE | — | EID17 | EID16 | xxxx |
| C1RXF4EID | 0452 | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| C1RXF5SID | 0454 | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | — | EXIDE | — | EID17 | EID16 | xxxx |
| C1RXF5EID | 0456 | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| C1RXF6SID | 0458 | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | — | EXIDE | — | EID17 | EID16 | xxxx |
| C1RXF6EID | 045A | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| C1RXF7SID | 045C | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | — | EXIDE | — | EID17 | EID16 | xxxx |
| C1RXF7EID | 045E | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| C1RXF8SID | 0460 | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | — | EXIDE | — | EID17 | EID16 | xxxx |
| C1RXF8EID | 0462 | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| C1RXF9SID | 0464 | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | — | EXIDE | — | EID17 | EID16 | xxxx |
| C1RXF9EID | 0466 | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| C1RXF10SID | 0468 | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | — | EXIDE | — | EID17 | EID16 | xxxx |
| C1RXF10EID | 046A | EID<15:0> | | | | | | | | | | | | | | | | xxxx |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** These registers are not present on dsPIC33EPXXXGM3XX devices.

**TABLE 4-28: CAN2 REGISTER MAP WHEN WIN (C1CTRL<0>) = 1 FOR dsPIC33EPXXXGM60X/7XX DEVICES(1)**

| SFR Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0500-051E | See definition when WIN = x | | | | | | | | | | | | | | | | |
| C2BUFPNT1 | 0520 | F3BP3 | F3BP2 | F3BP1 | F3BP0 | F2BP3 | F2BP2 | F2BP1 | F2BP0 | F1BP3 | F1BP2 | F1BP1 | F1BP0 | F0BP3 | F0BP2 | F0BP1 | F0BP0 | 0000 |
| C2BUFPNT2 | 0522 | F7BP3 | F7BP2 | F7BP1 | F7BP0 | F6BP3 | F6BP2 | F6BP1 | F6BP0 | F5BP3 | F5BP2 | F5BP1 | F5BP0 | F4BP3 | F4BP2 | F4BP1 | F4BP0 | 0000 |
| C2BUFPNT3 | 0524 | F11BP3 | F11BP2 | F11BP1 | F11BP0 | F10BP3 | F10BP2 | F10BP1 | F10BP0 | F9BP3 | F9BP2 | F9BP1 | F9BP0 | F8BP3 | F8BP2 | F8BP1 | F8BP0 | 0000 |
| C2BUFPNT4 | 0526 | F15BP3 | F15BP2 | F15BP1 | F15BP0 | F14BP3 | F14BP2 | F14BP1 | F14BP0 | F13BP3 | F13BP2 | F13BP1 | F13BP0 | F12BP3 | F12BP2 | F12BP1 | F12BP0 | 0000 |
| C2RXM0SID | 0530 | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | — | MIDE | — | EID17 | EID16 | xxxx |
| C2RXM0EID | 0532 | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| C2RXM1SID | 0534 | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | — | MIDE | — | EID17 | EID16 | xxxx |
| C2RXM1EID | 0536 | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| C2RXM2SID | 0538 | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | — | MIDE | — | EID17 | EID16 | xxxx |
| C2RXM2EID | 053A | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| C2RXF0SID | 0540 | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | — | MIDE | — | EID17 | EID16 | xxxx |
| C2RXF0EID | 0542 | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| C2RXF1SID | 0544 | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | — | MIDE | — | EID17 | EID16 | xxxx |
| C2RXF1EID | 0546 | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| C2RXF2SID | 0548 | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | — | MIDE | — | EID17 | EID16 | xxxx |
| C2RXF2EID | 054A | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| C2RXF3SID | 054C | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | — | MIDE | — | EID17 | EID16 | xxxx |
| C2RXF3EID | 054E | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| C2RXF4SID | 0550 | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | — | MIDE | — | EID17 | EID16 | xxxx |
| C2RXF4EID | 0552 | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| C2RXF5SID | 0554 | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | — | MIDE | — | EID17 | EID16 | xxxx |
| C2RXF5EID | 0556 | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| C2RXF6SID | 0558 | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | — | MIDE | — | EID17 | EID16 | xxxx |
| C2RXF6EID | 055A | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| C2RXF7SID | 055C | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | — | MIDE | — | EID17 | EID16 | xxxx |
| C2RXF7EID | 055E | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| C2RXF8SID | 0560 | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | — | MIDE | — | EID17 | EID16 | xxxx |
| C2RXF8EID | 0562 | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| C2RXF9SID | 0564 | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | — | MIDE | — | EID17 | EID16 | xxxx |
| C2RXF9EID | 0566 | EID<15:0> | | | | | | | | | | | | | | | | xxxx |
| C2RXF10SID | 0568 | SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 | SID2 | SID1 | SID0 | — | MIDE | — | EID17 | EID16 | xxxx |
| C2RXF10EID | 056A | EID<15:0> | | | | | | | | | | | | | | | | xxxx |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**Note 1:** These registers are not present on dsPIC33EPXXXGM3XX devices.

**TABLE 4-49: PORTB REGISTER MAP FOR dsPIC33EPXXXGM310/710 DEVICES**

| SFR Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRISB | 0E10 | TRISB<15:0> | | | | | | | | | | | | | | | | DF9F |
| PORTB | 0E12 | RB<15:0> | | | | | | | | | | | | | | | | xxxx |
| LATB | 0E14 | LATB<15:0> | | | | | | | | | | | | | | | | xxxx |
| ODCB | 0E16 | ODCB<15:0> | | | | | | | | | | | | | | | | 0000 |
| CNENB | 0E18 | CNIEB<15:0> | | | | | | | | | | | | | | | | 0000 |
| CNPUB | 0E1A | CNPUB<15:0> | | | | | | | | | | | | | | | | 0000 |
| CNPDB | 0E1C | CNPDB<15:0> | | | | | | | | | | | | | | | | 0000 |
| ANSELB | 0E1E | — | — | — | — | — | — | ANSB<9:7> | | | — | — | — | ANSB<3:0> | | | | 010F |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-50: PORTB REGISTER MAP FOR dsPIC33EPXXXGM306/706 DEVICES**

| SFR Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRISB | 0E10 | TRISB<15:0> | | | | | | | | | | | | | | | | DF9F |
| PORTB | 0E12 | RB<15:0> | | | | | | | | | | | | | | | | xxxx |
| LATB | 0E14 | LATB<15:0> | | | | | | | | | | | | | | | | xxxx |
| ODCB | 0E16 | ODCB<15:0> | | | | | | | | | | | | | | | | 0000 |
| CNENB | 0E18 | CNIEB<15:0> | | | | | | | | | | | | | | | | 0000 |
| CNPUB | 0E1A | CNPUB<15:0> | | | | | | | | | | | | | | | | 0000 |
| CNPDB | 0E1C | CNPDB<15:0> | | | | | | | | | | | | | | | | 0000 |
| ANSELB | 0E1E | — | — | — | — | — | — | ANSB<9:7> | | | — | — | — | ANSB<3:0> | | | | 010F |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-51: PORTB REGISTER MAP FOR dsPIC33EPXXXGM304/604 DEVICES**

| SFR Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRISB | 0E10 | TRISB<15:0> | | | | | | | | | | | | | | | | FFFF |
| PORTB | 0E12 | RB<15:0> | | | | | | | | | | | | | | | | xxxx |
| LATB | 0E14 | LATB<15:0> | | | | | | | | | | | | | | | | xxxx |
| ODCB | 0E16 | ODCB<15:0> | | | | | | | | | | | | | | | | 0000 |
| CNENB | 0E18 | CNIEB<15:0> | | | | | | | | | | | | | | | | 0000 |
| CNPUB | 0E1A | CNPUB<15:0> | | | | | | | | | | | | | | | | 0000 |
| CNPDB | 0E1C | CNPDB<15:0> | | | | | | | | | | | | | | | | 0000 |
| ANSELB | 0E1E | — | — | — | — | — | — | ANSB<9:7> | | | — | — | — | ANSB<3:0> | | | | 010F |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-61: PORTG REGISTER MAP FOR dsPIC33EPXXXGM310/710 DEVICES**

| SFR Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRISG | 0E60 | TRISG<15:6> | | | | | | | | | | — | — | TRISG<3:0> | | | | 03C0 |
| PORTG | 0E62 | RG<15:6> | | | | | | | | | | — | — | RG<3:0> | | | | xxxx |
| LATG | 0E64 | LATG<15:6> | | | | | | | | | | — | — | LATG<3:0> | | | | xxxx |
| ODCG | 0E66 | ODCG<15:6> | | | | | | | | | | — | — | ODCG<3:0> | | | | 0000 |
| CNENG | 0E68 | CNIEG<15:6> | | | | | | | | | | — | — | CNIEG<3:0> | | | | 0000 |
| CNPUG | 0E6A | CNPUG<15:6> | | | | | | | | | | — | — | CNPUG<3:0> | | | | 0000 |
| CNPDG | 0E6C | CNPDG<15:6> | | | | | | | | | | — | — | CNPDG<3:0> | | | | 0000 |
| ANSELG | 0E6E | ANSG15 | — | — | — | ANSG<11:6> | | | | | | — | — | ANSG<3:2> | | — | — | 0000 |

**Legend:** x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-62: PORTG REGISTER MAP FOR dsPIC33EPXXXGM306/706 DEVICES**

| SFR Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TRISG | 0E60 | — | — | — | — | — | — | TRISG<9:6> | | | | — | — | — | — | — | — | 03C0 |
| PORTG | 0E62 | — | — | — | — | — | — | RG<9:6> | | | | — | — | — | — | — | — | xxxx |
| LATG | 0E64 | — | — | — | — | — | — | LATG<9:6> | | | | — | — | — | — | — | — | xxxx |
| ODCG | 0E66 | — | — | — | — | — | — | ODCG<9:6> | | | | — | — | — | — | — | — | 0000 |
| CNENG | 0E68 | — | — | — | — | — | — | CNIEG<9:6> | | | | — | — | — | — | — | — | 0000 |
| CNPUG | 0E6A | — | — | — | — | — | — | CNPUG<9:6> | | | | — | — | — | — | — | — | 0000 |
| CNPDG | 0E6C | — | — | — | — | — | — | CNPDG<9:6> | | | | — | — | — | — | — | — | 0000 |
| ANSELG | 0E6E | — | — | — | — | — | — | ANSG<9:6> | | | | — | — | — | — | — | — | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-63: PAD CONFIGURATION REGISTER MAP**

| File Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| PADCFG1 | 0EFE | — | — | — | — | — | — | — | — | — | — | — | — | — | — | RTSECSEL | PMPTTL | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 7-1: INTERRUPT VECTOR DETAILS (CONTINUED)**

| Interrupt Source | Vector # | IRQ # | IVT Address | Interrupt Bit Location | | |
|---|---|---|---|---|---|---|
| | | | | Flag | Enable | Priority |
| SPI3E – SPI3 Error | 98 | 90 | 0x0000C8 | IFS5<10> | IEC5<10> | IPC22<10:8> |
| SPI3 – SPI3 Transfer Done | 99 | 91 | 0x0000CA | IFS5<11> | IEC5<11> | IPC22<14:12> |
| Reserved | 100-101 | 92-93 | 0x0000CC-0x0000CE | — | — | — |
| PWM1 – PWM Generator 1 | 102 | 94 | 0x0000D0 | IFS5<14> | IEC5<14> | IPC23<10:8> |
| PWM2 – PWM Generator 2 | 103 | 95 | 0x0000D2 | IFS5<15> | IEC5<15> | IPC23<14:12> |
| PWM3 – PWM Generator 3 | 104 | 96 | 0x0000D4 | IFS6<0> | IEC6<0> | IPC24<2:0> |
| PWM4 – PWM Generator 4 | 105 | 97 | 0x0000D6 | IFS6<1> | IEC6<1> | IPC24<6:4> |
| PWM5 – PWM Generator 5 | 106 | 98 | 0x0000D8 | IFS6<2> | IEC6<2> | IPC24<10:8> |
| PWM6 – PWM Generator 6 | 107 | 99 | 0x0000DA | IFS6<3> | IEC6<3> | IPC24<14:12> |
| Reserved | 108-149 | 100-141 | 0x0000DC-0x00012E | — | — | — |
| ICD – ICD Application | 150 | 142 | 0x000142 | IFS8<14> | IEC8<14> | IPC35<10:8> |
| JTAG – JTAG Programming | 151 | 143 | 0x000130 | IFS8<15> | IEC8<15> | IPC35<14:12> |
| Reserved | 152 | 144 | 0x000134 | — | — | — |
| PTGSTEP – PTG Step | 153 | 145 | 0x000136 | IFS9<1> | IEC9<1> | IPC36<6:4> |
| PTGWDT – PTG Watchdog Time-out | 154 | 146 | 0x000138 | IFS9<2> | IEC9<2> | IPC36<10:8> |
| PTG0 – PTG Interrupt 0 | 155 | 147 | 0x00013A | IFS9<3> | IEC9<3> | IPC36<14:12> |
| PTG1 – PTG Interrupt 1 | 156 | 148 | 0x00013C | IFS9<4> | IEC9<4> | IPC37<2:0> |
| PTG2 – PTG Interrupt 2 | 157 | 149 | 0x00013E | IFS9<5> | IEC9<5> | IPC37<6:4> |
| PTG3 – PTG Interrupt 3 | 158 | 150 | 0x000140 | IFS9<6> | IEC9<6> | IPC37<10:8> |
| Reserved | 159-245 | 151-245 | 0x000142-0x0001FE | — | — | — |
| Lowest Natural Order Priority | | | | | | |

**Note 1:** This interrupt source is available on dsPIC33EPXXXGM6XX/7XX devices only.

**2:** This interrupt source is not available on 44-pin devices.

**REGISTER 8-9: DSADRH: DMA MOST RECENT RAM HIGH ADDRESS REGISTER**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| DSADR<23:16> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7-0 **DSADR<23:16>:** Most Recent DMA Address Accessed by DMA bits

**REGISTER 8-10: DSADRL: DMA MOST RECENT RAM LOW ADDRESS REGISTER**

| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| DSADR<15:8> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| DSADR<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-0 **DSADR<15:0>:** Most Recent DMA Address Accessed by DMA bits

**REGISTER 9-2: CLKDIV: CLOCK DIVISOR REGISTER(2) (CONTINUED)**

bit 4-0 **PLLPRE<4:0>:** PLL Phase Detector Input Divider Select bits (also denoted as 'N1', PLL prescaler)
11111 = Input divided by 33
•
•
•
00001 = Input divided by 3
00000 = Input divided by 2 (default)

**Note 1:** This bit is cleared when the ROI bit is set and an interrupt occurs.

**2:** This register resets only on a Power-on Reset (POR).

**3:** The DOZE<2:0> bits can only be written to when the DOZEN bit is clear. If DOZEN = 1, any writes to DOZE<2:0> are ignored.

**4:** The DOZEN bit cannot be set if DOZE<2:0> = 000. If DOZE<2:0> = 000, any attempt by user software to set the DOZEN bit is ignored.

**REGISTER 11-18: RPINR24: PERIPHERAL PIN SELECT INPUT REGISTER 24**

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | CSCK2R<6:0> | | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | CSDIR<6:0> | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as ‘0’

bit 14-8 **CSCK2R<6:0>:** Assign DCI Clock Input (CSCK) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

1111100 = Input tied to RPI124
•
•
•
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as ‘0’

bit 6-0 **CSDIR<6:0>:** Assign DCI Data Input (CSDI) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

1111100 = Input tied to RPI124
•
•
•
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

## 20.0 UNIVERSAL ASYNCHRONOUS RECEIVER TRANSMITTER (UART)

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGM3XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"Universal Asynchronous Receiver Transmitter (UART)"** (DS70000582), which is available from the Microchip web site (www.microchip.com).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGM3XX/6XX/7XX family of devices contains four UART modules.

The Universal Asynchronous Receiver Transmitter (UART) module is one of the serial I/O modules available in the dsPIC33EPXXXGM3XX/6XX/7XX device family. The UART is a full-duplex, asynchronous system that can communicate with peripheral devices, such as personal computers, LIN/J2602, RS-232 and RS-485 interfaces. The module also supports a hardware flow control option with the $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ pins, and also includes an IrDA® encoder and decoder.

**Note:** Hardware flow control using $\overline{\text{UxRTS}}$ and $\overline{\text{UxCTS}}$ is not available on all pin count devices. See the **"Pin Diagrams"** section for availability.

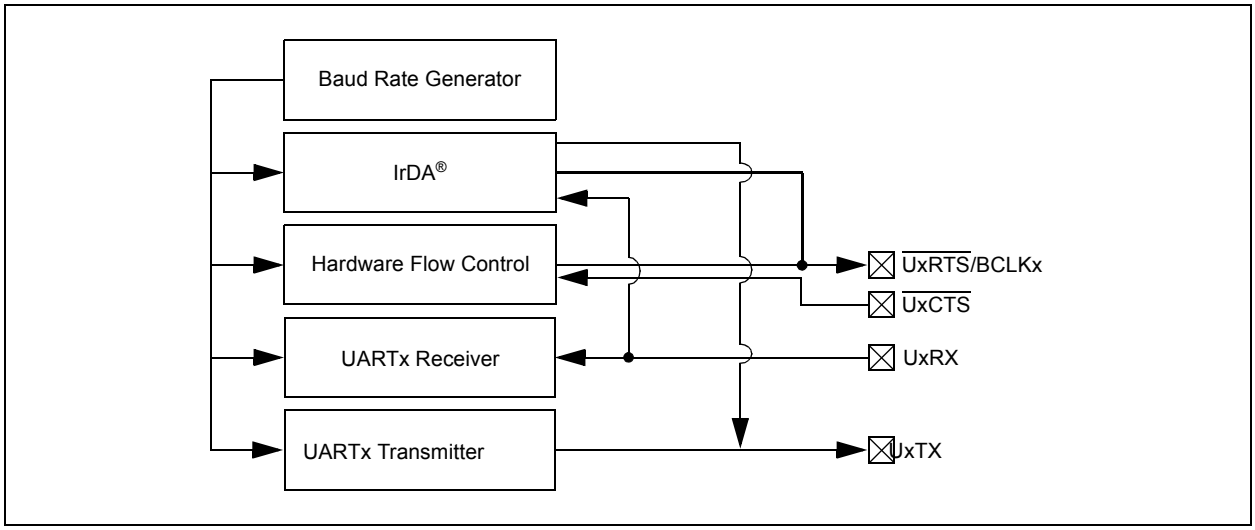
The primary features of the UART module are:

- Full-Duplex, 8 or 9-Bit Data Transmission through the UxTX and UxRX Pins
- Even, Odd or No Parity Options (for 8-bit data)
- One or Two Stop Bits
- Hardware Flow Control Option with $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ Pins
- Fully Integrated Baud Rate Generator with 16-Bit Prescaler
- Baud Rates Ranging from 4.375 Mbps to 67 bps at 16x mode at 70 MIPS
- Baud Rates Ranging from 17.5 Mbps to 267 bps at 4x mode at 70 MIPS
- 4-Deep First-In First-Out (FIFO) Transmit Data Buffer
- 4-Deep FIFO Receive Data Buffer
- Parity, Framing and Buffer Overrun Error Detection
- Support for 9-Bit mode with Address Detect (9th bit = 1)
- Transmit and Receive Interrupts
- A Separate Interrupt for All UART Error Conditions
- Loopback mode for Diagnostic Support
- Support for Sync and Break Characters
- Support for Automatic Baud Rate Detection
- IrDA® Encoder and Decoder Logic
- 16x Baud Clock Output for IrDA® Support

A simplified block diagram of the UART module is shown in Figure 20-1. The UART module consists of these key hardware elements:

- Baud Rate Generator
- Asynchronous Transmitter
- Asynchronous Receiver

**FIGURE 20-1: UARTx SIMPLIFIED BLOCK DIAGRAM**



**REGISTER 20-1: UxMODE: UARTx MODE REGISTER (CONTINUED)**

bit 5 **ABAUD:** Auto-Baud Enable bit
1 = Enables baud rate measurement on the next character – requires reception of a Sync field (55h) before other data; cleared in hardware upon completion
0 = Baud rate measurement is disabled or has completed

bit 4 **URXINV:** UARTx Receive Polarity Inversion bit
1 = UxRX Idle state is '0'
0 = UxRX Idle state is '1'

bit 3 **BRGH:** High Baud Rate Enable bit
1 = BRG generates 4 clocks per bit period (4x baud clock, High-Speed mode)
0 = BRG generates 16 clocks per bit period (16x baud clock, Standard mode)

bit 2-1 **PDSEL<1:0>:** Parity and Data Selection bits
11 = 9-bit data, no parity
10 = 8-bit data, odd parity
01 = 8-bit data, even parity
00 = 8-bit data, no parity

bit 0 **STSEL:** Stop Bit Selection bit
1 = Two Stop bits
0 = One Stop bit

**Note 1:** Refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"Universal Asynchronous Receiver Transmitter (UART)"** (DS70000582) for information on enabling the UART module for receive or transmit operation.
**2:** This feature is only available for the 16x BRG mode (BRGH = 0).
**3:** This feature is only available on 44-pin and 64-pin devices.
**4:** This feature is only available on 64-pin devices.

**REGISTER 25-1: PTGCST: PTG CONTROL/STATUS REGISTER (CONTINUED)**

bit 1-0 **PTGITM<1:0>:** PTG Input Trigger Command Operating Mode bits(1)

11 = Single level detect with step delay is not executed on exit of command (regardless of PTGCTRL command)
10 = Single level detect with step delay is executed on exit of command
01 = Continuous edge detect with step delay is not executed on exit of command (regardless of PTGCTRL command)
00 = Continuous edge detect with step delay is executed on exit of command

**Note 1:** These bits apply to the PTGWHI and PTGWLO commands only.

**2:** This bit is only used with the PTGCTRL Step command software trigger option.

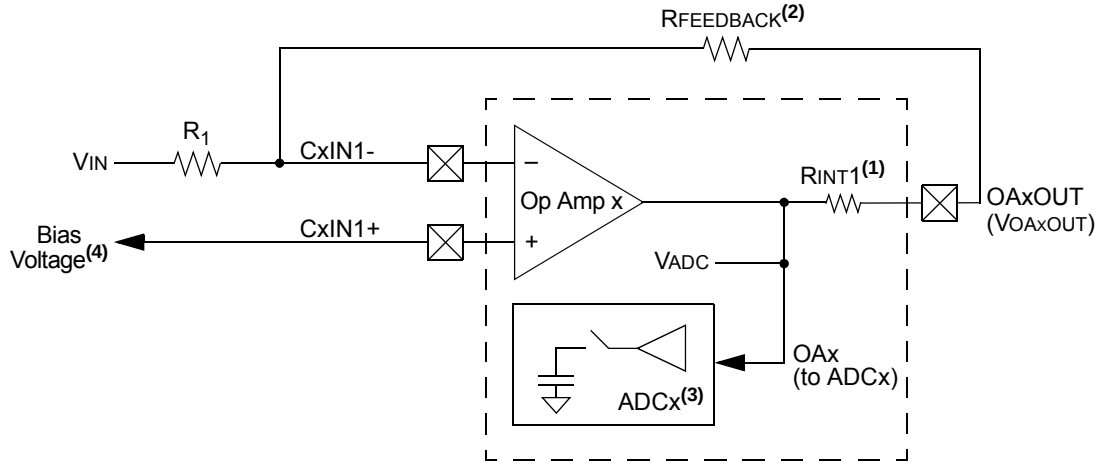
## 26.1 Op Amp Application Considerations

There are two configurations to take into consideration when designing with the op amp modules that are available in the dsPIC33EPXXXGM3XX/6XX/7XX devices. Configuration A (see Figure 26-5) takes advantage of the internal connection to the ADCx module to route the output of the op amp directly to the ADCx for measurement. Configuration B (see Figure 26-6) requires that the designer externally route the output of the op amp (OAxOUT) to a separate analog input pin (ANy) on the device. Table 33-53 in **Section 33.0 "Electrical Characteristics"** describes the performance characteristics for the op amps, distinguishing between the two configuration types where applicable.

### 26.1.1 OP AMP CONFIGURATION A

Figure 26-5 shows a typical inverting amplifier circuit taking advantage of the internal connections from the op amp output to the input of the ADCx. The advantage of this configuration is that the user does not need to consume another analog input (ANy) on the device, and allows the user to simultaneously sample all three op amps with the ADCx module, if needed. However, the presence of the internal resistance, RINT1, adds an error in the feedback path. Since RINT1 is an internal resistance, in relation to the op amp output (VOAXOUT) and ADCx internal connection (VADC), RINT1 must be included in the numerator term of the transfer function. See Table 33-52 in **Section 33.0 "Electrical Characteristics"** for the typical value of RINT1. Table 33-57 and Table 33-58 in **Section 33.0 "Electrical Characteristics"** describe the minimum sample time (TSAMP) requirements for the ADCx module in this configuration. Figure 26-5 also defines the equations that should be used when calculating the expected voltages at points, VADC and VOAXOUT.

**FIGURE 26-5: OP AMP CONFIGURATION A**




$$V_{ADC} = \left(\frac{R_{FEEDBACK} + R_{INT1}}{R_1}\right)( \ Bias\ Voltage - V_{IN} \ )$$

$$V_{OAxOUT} = \left(\frac{R_{FEEDBACK}}{R_1}\right)( \ Bias\ Voltage - V_{IN} \ )$$

**Note 1:** See Table 33-56 for the Typical value.
**2:** See Table 33-52 for the Minimum value for the feedback resistor.
**3:** See Table 33-59 and Table 33-60 for the Minimum Sample Time (TSAMP).
**4:** CVREF1O or CVREF2O are two options that are available for supplying bias voltage to the op amps.

**REGISTER 26-2: CMxCON: OP AMP/COMPARATOR x CONTROL REGISTER (x = 1, 2, 3 OR 5)**

| R/W-0 | R/W-0 | R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| CON | COE | CPOL | — | — | OPMODE(2) | CEVT(3) | COUT |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | U-0 | R/W-0 | U-0 | U-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| EVPOL1(3) | EVPOL0(3) | — | CREF(1) | — | — | CCH1(1) | CCH0(1) |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **CON:** Op Amp/Comparator Enable bit
1 = Comparator is enabled
0 = Comparator is disabled

bit 14 **COE:** Comparator Output Enable bit
1 = Comparator output is present on the CxOUT pin
0 = Comparator output is internal only

bit 13 **CPOL:** Comparator Output Polarity Select bit
1 = Comparator output is inverted
0 = Comparator output is not inverted

bit 12-11 **Unimplemented:** Read as '0'

bit 10 **OPMODE:** Op Amp Select bit(2)
1 = Op amp is enabled
0 = Op amp is disabled

bit 9 **CEVT:** Comparator Event bit(3)
1 = Comparator event, according to the EVPOL<1:0> settings, occurred; disables future triggers and interrupts until the bit is cleared
0 = Comparator event did not occur

bit 8 **COUT:** Comparator Output bit
When CPOL = 0 (non-inverted polarity):
1 = $V_{IN+} > V_{IN-}$
0 = $V_{IN+} < V_{IN-}$
When CPOL = 1 (inverted polarity):
1 = $V_{IN+} < V_{IN-}$
0 = $V_{IN+} > V_{IN-}$

**Note 1:** Inputs that are selected and not available will be tied to $V_{SS}$. See the **"Pin Diagrams"** section for available inputs for each package.

**2:** The op amp and the comparator can be used simultaneously in these devices. The OPMODE bit only enables the op amp while the comparator is still functional.

**3:** After configuring the comparator, either for a high-to-low or low-to-high COUT transition (EVPOL<1:0> (CMxCON<7:6>) = 10 or 01), the Comparator Event bit, CEVT (CMxCON<9>), and the Comparator Combined Interrupt Flag, CMPIF (IFS1<2>), **must be cleared** before enabling the Comparator Interrupt Enable bit, CMPIE (IEC1<2>).

**REGISTER 26-4: CMxMSKSRC: COMPARATOR x MASK SOURCE SELECT CONTROL REGISTER**

| U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | RW-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | SELSRCC3 | SELSRCC2 | SELSRCC1 | SELSRCC0 |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| SELSRCB3 | SELSRCB2 | SELSRCB1 | SELSRCB0 | SELSRCA3 | SELSRCA2 | SELSRCA1 | SELSRCA0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-12 **Unimplemented:** Read as ‘0’

bit 11-8 **SELSRCC<3:0>:** Mask C Input Select bits

1111 = FLT4
1110 = FLT2
1101 = PTGO19
1100 = PTGO18
1011 = PWM6H
1010 = PWM6L
1001 = PWM5H
1000 = PWM5L
0111 = PWM4H
0110 = PWM4L
0101 = PWM3H
0100 = PWM3L
0011 = PWM2H
0010 = PWM2L
0001 = PWM1H
0000 = PWM1L

bit 7-4 **SELSRCB<3:0>:** Mask B Input Select bits

1111 = FLT4
1110 = FLT2
1101 = PTGO19
1100 = PTGO18
1011 = PWM6H
1010 = PWM6L
1001 = PWM5H
1000 = PWM5L
0111 = PWM4H
0110 = PWM4L
0101 = PWM3H
0100 = PWM3L
0011 = PWM2H
0010 = PWM2L
0001 = PWM1H
0000 = PWM1L

**REGISTER 28-5: PMSTAT: PARALLEL MASTER PORT STATUS REGISTER (SLAVE MODE ONLY)(1)**

| R-0 | R/W-0, HS | U-0 | U-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| IBF | IBOV | — | — | IB3F | IB2F | IB1F | IB0F |
| bit 15 | | | | | | | bit 8 |

| R-1 | R/W-0, HS | U-0 | U-0 | R-1 | R-1 | R-1 | R-1 |
|---|---|---|---|---|---|---|---|
| OBE | OBUF | — | — | OB3E | OB2E | OB1E | OB0E |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | HS = Hardware Settable bit | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at Reset | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **IBF:** Input Buffer Full Status bit
1 = All writable Input Buffer registers are full
0 = Some or all of the writable Input Buffer registers are empty

bit 14 **IBOV:** Input Buffer Overflow Status bit
1 = A write attempt to a full Input Byte register occurred (must be cleared in software)
0 = No overflow occurred

bit 13-12 **Unimplemented:** Read as '0'

bit 11-8 **IB3F:IB0F:** Input Buffer x Status Full bit
1 = Input Buffer x contains data that has not been read (reading buffer will clear this bit)
0 = Input Buffer x does not contain any unread data

bit 7 **OBE:** Output Buffer Empty Status bit
1 = All readable Output Buffer registers are empty
0 = Some or all of the readable Output Buffer registers are full

bit 6 **OBUF:** Output Buffer Underflow Status bit
1 = A read occurred from an empty Output Byte register (must be cleared in software)
0 = No underflow occurred

bit 5-4 **Unimplemented:** Read as '0'

bit 3-0 **OB3E:OB0E:** Output Buffer x Status Empty bit
1 = Output Buffer x is empty (writing data to the buffer will clear this bit)
0 = Output Buffer x contains data that has not been transmitted

**Note 1:** This register is not available on 44-pin devices.

## 29.0 PROGRAMMABLE CYCLIC REDUNDANCY CHECK (CRC) GENERATOR

**Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGM3XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the "*dsPIC33/PIC24 Family Reference Manual*", **"32-Bit Programmable Cyclic Redundancy Check (CRC)"** (DS70346), which is available from the Microchip web site (www.microchip.com).

**2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The programmable CRC generator offers the following features:

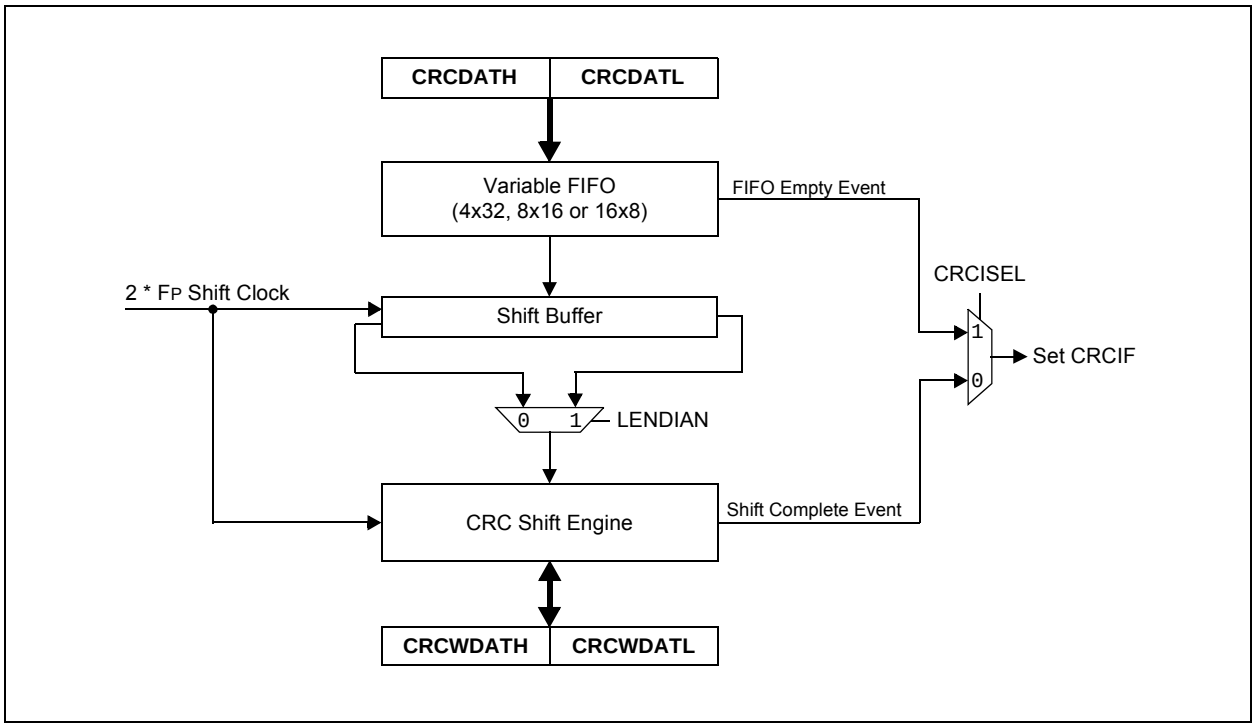
- User-Programmable (up to 32nd order) polynomial CRC equation
- Interrupt Output
- Data FIFO

The programmable CRC generator provides a hardware-implemented method of quickly generating checksums for various networking and security applications. It offers the following features:

- User-programmable CRC polynomial equation, up to 32 bits
- Programmable shift direction (little or big-endian)
- Independent data and polynomial lengths
- Configurable interrupt output
- Data FIFO

A simplified block diagram of the CRC generator is shown in Figure 29-1. A simple version of the CRC shift engine is shown in Figure 29-2.

**FIGURE 29-1: CRC BLOCK DIAGRAM**



# APPENDIX A: REVISION HISTORY

## Revision A (February 2013)

This is the initial released version of this document.

## Revision B (June 2013)

Changes to **Section 5.0 "Flash Program Memory"**, Register 5-1. Changes to **Section 6.0 "Resets"**, Figure 6-1. Changes to **Section 26.0 "Op Amp/Comparator Module"**, Register 26-2. Updates to most of the tables in **Section 33.0 "Electrical Characteristics"**. Minor text edits throughout the document.

## Revision C (September 2013)

Changes to Figure 23-1. Changes to Figure 26-2. Changes to Table 30-2. Changes to **Section 33.0 "Electrical Characteristics"**. Added **Section 34.0 "High-Temperature Electrical Characteristics"** to the data sheet. Minor typographical edits throughout the document.

## Revision D (August 2014)

This revision incorporates the following updates:

- Sections:
  - Updated **Section 2.0 "Guidelines for Getting Started with 16-Bit Digital Signal Controllers"**, **Section 8.0 "Direct Memory Access (DMA)"**, **Section 10.3 "Doze Mode"**, **Section 21.0 "Controller Area Network (CAN) Module (dsPIC33EPXXXGM6XX/7XX Devices Only)"**, **Section 23.0 "10-Bit/12-Bit Analog-to-Digital Converter (ADC)"**, **Section 23.1.2 "12-Bit ADCx Configuration"**, **Section 21.4 "CAN Message Buffers"**, **Section 35.0 "Packaging Information"**
- Figures:
  - Updated **"Pin Diagrams"**, Figure 1-1, Figure 9-1
- Registers:
  - Updated Register 5-1, Register 8-2, Register 21-1, Register 23-2
- Tables:
  - Updated Table 1-1, Table 7-1, Table 8-1, Table 34-9, Table 1, Table 4-2, Table 4-3, Table 4-25, Table 4-33, Table 4-34, Table 4-39, Table 4-30, Table 4-46, Table 4-47, Table 33-16,Table 34-8

Resets ..... 111
Brown-out Reset (BOR) ..... 111
Configuration Mismatch Reset (CM) ..... 111
Illegal Condition Reset (IOPUWR) ..... 111
Illegal Address Mode ..... 111
Illegal Opcode ..... 111
Security ..... 111
Uninitialized W Register ..... 111
Master Clear Pin Reset (MCLR) ..... 111
Master Reset Signal (SYSRST) ..... 111
Power-on Reset (POR) ..... 111
RESET Instruction (SWR) ..... 111
Trap Conflict Reset (TRAPR) ..... 111
Watchdog Timer Time-out Reset (WDTO) ..... 111
Revision History ..... 527
RTCC
Control Registers ..... 386
Resources ..... 385
Writing to the Timer ..... 385

## S

Serial Peripheral Interface (SPI) ..... 273
Special Features of the CPU ..... 411
SPI
Control Registers ..... 276
Helpful Tips ..... 275
Symbols Used in Opcode Descriptions ..... 420

## T

Temperature and Voltage Specifications
AC ..... 503
Timer
Control Registers ..... 216
Timer1 ..... 211
Control Register ..... 212
Timer2/3, Timer4/5, Timer6/7 and Timer8/9 ..... 213
Timing Diagrams
10-Bit ADC1 Conversion (CHPS<1:0> = 01, SIMSAM = 0, ASAM = 0, SSRC<2:0> = 000, SSRCG = 0) ..... 496
10-Bit ADC1 Conversion (CHPS<1:0> = 01, SIMSAM = 0, ASAM = 1, SSRC<2:0> = 111, SSRCG = 0, SAMC<4:0> = 00010) ..... 496
12-Bit ADC1 Conversion (ASAM = 0, SSRC<2:0> = 000, SSRCG = 0) ..... 494
BOR and Master Clear Reset ..... 448
CANx I/O ..... 487
External Clock ..... 446
High-Speed PWMx ..... 455
High-Speed PWMx Fault ..... 455
I/O Characteristics ..... 448
I2Cx Bus Data (Master Mode) ..... 483
I2Cx Bus Data (Slave Mode) ..... 485
I2Cx Bus Start/Stop Bits (Master Mode) ..... 483
I2Cx Bus Start/Stop Bits (Slave Mode) ..... 485
Input Capture x (ICx) ..... 453
Load Conditions ..... 490
OCx/PWMx ..... 454
Output Compare x (OCx) ..... 454
Power-on Reset Characteristics ..... 449
QEAx/QEBx Input ..... 457
QEIx Index Pulse ..... 458
SPI1 Master Mode (Full-Duplex, CKE = 0, CKP = x, SMP = 1) ..... 474
SPI1 Master Mode (Full-Duplex, CKE = 1, CKP = x, SMP = 1) ..... 473
SPI1 Master Mode (Half-Duplex, Transmit Only, CKE = 0) ..... 471
SPI1 Master Mode (Half-Duplex, Transmit Only, CKE = 1) ..... 472
SPI1 Slave Mode (Full-Duplex, CKE = 0, CKP = 0, SMP = 0) ..... 481
SPI1 Slave Mode (Full-Duplex, CKE = 0, CKP = 1, SMP = 0) ..... 479
SPI1 Slave Mode (Full-Duplex, CKE = 1, CKP = 0, SMP = 0) ..... 475
SPI1 Slave Mode (Full-Duplex, CKE = 1, CKP = 1, SMP = 0) ..... 477
SPI2, SPI3 Master Mode (Full-Duplex, CKE = 0, CKP = x, SMP = 1) ..... 462
SPI2, SPI3 Master Mode (Full-Duplex, CKE = 1, CKP = x, SMP = 1) ..... 461
SPI2, SPI3 Master Mode (Half-Duplex, Transmit Only, CKE = 0) ..... 459
SPI2, SPI3 Master Mode (Half-Duplex, Transmit Only, CKE = 1) ..... 460
SPI2, SPI3 Slave Mode (Full-Duplex, CKE = 0, CKP = 0, SMP = 0) ..... 469
SPI2, SPI3 Slave Mode (Full-Duplex, CKE = 0, CKP = 1, SMP = 0) ..... 467
SPI2, SPI3 Slave Mode (Full-Duplex, CKE = 1, CKP = 0, SMP = 0) ..... 463
SPI2, SPI3 Slave Mode (Full-Duplex, CKE = 1, CKP = 1, SMP = 0) ..... 465
Timer1-Timer5 External Clock ..... 451
TimerQ (QEIx Module) External Clock ..... 456
UARTx I/O ..... 487
Timing Specifications
I2Cx Bus Data Requirements (Master Mode) ..... 484
I2Cx Bus Data Requirements (Slave Mode) ..... 486

## U

UART
Control Registers ..... 291
Helpful Tips ..... 290
Universal Asynchronous Receiver Transmitter (UART) ..... 289
User ID Words ..... 416

## V

Voltage Regulator (On-Chip) ..... 416

## W

Watchdog Timer (WDT) ..... 411, 417
Programming Considerations ..... 417
WWW Address ..... 536
WWW, On-Line Support ..... 12