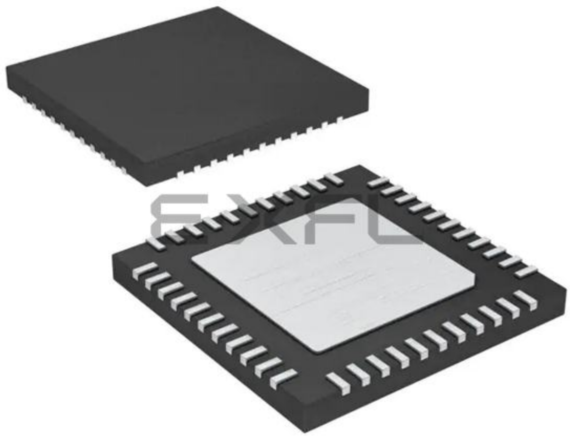

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | dsPIC |
| Core Size | 16-Bit |
| Speed | 70 MIPs |
| Connectivity | I²C, IrDA, LINbus, QEI, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, Motor Control PWM, POR, PWM, WDT |
| Number of I/O | 35 |
| Program Memory Size | 512KB (170K x 24) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 48K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 3.6V |
| Data Converters | A/D 18x10b/12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 44-VQFN Exposed Pad |
| Supplier Device Package | 44-QFN (8x8) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep512gm304-i-ml |

**TABLE 2: PIN NAMES: dsPIC33EP128/256/512GM310/710 DEVICES(1,2,3) (CONTINUED)**

| Pin # | Full Pin Name | Pin # | Full Pin Name |
|---|---|---|---|
| E1 | PWM6H/T8CK/RD4 | J8 | No Connect |
| E2 | PWM6L/T9CK/RD3 | J9 | No Connect |
| E3 | AN19/RP118/PMA5/RG6 | J10 | AN41/RP81/RE1 |
| E4 | PWM5H/RD2 | J11 | AN30/SDA1/RPI52/RC4 |
| E5 | No Connect | K1 | PGED3/OA2IN-/AN2/C2IN1-/$\overline{\text{SS1}}$/RPI32/CTED2/RB0 |
| E6 | RP113/RG1 | K2 | PGEC3/CVREF+/OA1OUT/AN3/C1IN4-/C4IN2-/RPI33/CTED1/RB1 |
| E7 | No Connect | K3 | VREF+/AN34/PMA7/RF10 |
| K4 | OA3OUT/AN6/C3IN4-/C4IN4-/C4IN1+/RP48/OCFB/RC0 | L3 | AVSS |
| K5 | No Connect | L4 | OA3IN-/AN7/C3IN1-/C4IN1-/RP49/RC1 |
| K6 | AN37/RF12 | L5 | OA3IN+/AN8/C3IN3-/C3IN1+/RPI50/$\overline{\text{U1RTS}}$/BCLK1/FLT3/PMA13/RC2 |
| K7 | AN14/RPI94/FLT7/PMA1/RE14 | L6 | AN36/RF13 |
| K8 | VDD | L7 | AN13/C3IN2-/$\overline{\text{U2CTS}}$/FLT6/PMA10/RE13 |
| K9 | AN39/RD15 | L8 | AN15/RPI95/FLT8/PMA0/RE15 |
| K10 | OA5IN+/AN24/C5IN3-/C5IN1+/SDO1/RP20/T1CK/RA4 | L9 | AN38/RD14 |
| K11 | AN40/RPI80/RE0 | L10 | SDA2/RPI24/PMA9/RA8 |
| L1 | PGEC1/OA1IN+/AN4/C1IN3-/C1IN1+/C2IN3-/RPI34/RB2 | L11 | FLT32/SCL2/RP36/PMA8/RB4 |
| L2 | VREF-/AN33/PMA6/RF9 | | |

**Note 1:** The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select (PPS)"** for available peripherals and for information on limitations.

**2:** Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

**3:** The availability of $I^2C$™ interfaces varies by device. Selection (SDAx/SCLx or ASDAx/ASCLx) is made using the device Configuration bits, ALTI2C1 and ALTI2C2 (FPOR<5:4>). See **Section 30.0 "Special Features"** for more information.

**TABLE 4-4: TIMERS REGISTER MAP**

| SFR Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TMR1 | 0100 | Timer1 Register | | | | | | | | | | | | | | | | 0000 |
| PR1 | 0102 | Period Register 1 | | | | | | | | | | | | | | | | FFFF |
| T1CON | 0104 | TON | — | TSIDL | — | — | — | — | — | — | TGATE | TCKPS1 | TCKPS0 | — | TSYNC | TCS | — | 0000 |
| TMR2 | 0106 | Timer2 Register | | | | | | | | | | | | | | | | 0000 |
| TMR3HLD | 0108 | Timer3 Holding Register (For 32-bit timer operations only) | | | | | | | | | | | | | | | | xxxx |
| TMR3 | 010A | Timer3 Register | | | | | | | | | | | | | | | | 0000 |
| PR2 | 010C | Period Register 2 | | | | | | | | | | | | | | | | FFFF |
| PR3 | 010E | Period Register 3 | | | | | | | | | | | | | | | | FFFF |
| T2CON | 0110 | TON | — | TSIDL | — | — | — | — | — | — | TGATE | TCKPS1 | TCKPS0 | T32 | — | TCS | — | 0000 |
| T3CON | 0112 | TON | — | TSIDL | — | — | — | — | — | — | TGATE | TCKPS1 | TCKPS0 | — | — | TCS | — | 0000 |
| TMR4 | 0114 | Timer4 Register | | | | | | | | | | | | | | | | 0000 |
| TMR5HLD | 0116 | Timer5 Holding Register (For 32-bit timer operations only) | | | | | | | | | | | | | | | | xxxx |
| TMR5 | 0118 | Timer5 Register | | | | | | | | | | | | | | | | 0000 |
| PR4 | 011A | Period Register 4 | | | | | | | | | | | | | | | | FFFF |
| PR5 | 011C | Period Register 5 | | | | | | | | | | | | | | | | FFFF |
| T4CON | 011E | TON | — | TSIDL | — | — | — | — | — | — | TGATE | TCKPS1 | TCKPS0 | T32 | — | TCS | — | 0000 |
| T5CON | 0120 | TON | — | TSIDL | — | — | — | — | — | — | TGATE | TCKPS1 | TCKPS0 | — | — | TCS | — | 0000 |
| TMR6 | 0122 | Timer6 Register | | | | | | | | | | | | | | | | 0000 |
| TMR7HLD | 0124 | Timer7 Holding Register (For 32-bit timer operations only) | | | | | | | | | | | | | | | | xxxx |
| TMR7 | 0126 | Timer7 Register | | | | | | | | | | | | | | | | 0000 |
| PR6 | 0128 | Period Register 6 | | | | | | | | | | | | | | | | FFFF |
| PR7 | 012A | Period Register 7 | | | | | | | | | | | | | | | | FFFF |
| T6CON | 012C | TON | — | TSIDL | — | — | — | — | — | — | TGATE | TCKPS1 | TCKPS0 | T32 | — | TCS | — | 0000 |
| T7CON | 012E | TON | — | TSIDL | — | — | — | — | — | — | TGATE | TCKPS1 | TCKPS0 | — | — | TCS | — | 0000 |
| TMR8 | 0130 | Timer8 Register | | | | | | | | | | | | | | | | 0000 |
| TMR9HLD | 0132 | Timer9 Holding Register (For 32-bit timer operations only) | | | | | | | | | | | | | | | | xxxx |
| TMR9 | 0134 | Timer9 Register | | | | | | | | | | | | | | | | 0000 |
| PR8 | 0136 | Period Register 8 | | | | | | | | | | | | | | | | FFFF |
| PR9 | 0138 | Period Register 9 | | | | | | | | | | | | | | | | FFFF |
| T8CON | 013A | TON | — | TSIDL | — | — | — | — | — | — | TGATE | TCKPS1 | TCKPS0 | T32 | — | TCS | — | 0000 |
| T9CON | 013C | TON | — | TSIDL | — | — | — | — | — | — | TGATE | TCKPS1 | TCKPS0 | — | — | TCS | — | 0000 |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

## 5.2 RTSP Operation

RTSP allows the user application to erase a single page of memory, program a row and to program two instruction words at a time. See Table 1 in the **"dsPIC33EPXXXGM3XX/6XX/7XX Product Family"** section for the page sizes of each device.

The Flash program memory array is organized into rows of 64 instructions or 192 bytes. RTSP allows the user application to erase a page of program memory, which consists of eight rows (512 instructions) at a time, and to program one row or two adjacent words at a time. The 8-row erase pages and single row write rows are edge-aligned, from the beginning of program memory, on boundaries of 1536 bytes and 192 bytes, respectively.

For more information on erasing and programming Flash memory, refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"Flash Programming"** (DS70609).

## 5.3 Programming Operations

A complete programming sequence is necessary for programming or erasing the internal Flash in RTSP mode. The processor stalls (waits) until the programming operation is finished.

For erase and program times, refer to Parameters D137a and D137b (Page Erase Time), and D138a and D138b (Word Write Cycle Time), in Table 33-13.

Setting the WR bit (NVMCON<15>) starts the operation and the WR bit is automatically cleared when the operation is finished.

### 5.3.1 PROGRAMMING ALGORITHM FOR FLASH PROGRAM MEMORY

Programmers can program two adjacent words (24 bits x 2) of program Flash memory at a time on every other word address boundary (0x000002, 0x000006, 0x00000A, etc.). To do this, it is necessary to erase the page that contains the desired address of the location the user wants to change. Programmers can also program a row of data (64 instruction words/ 192 bytes) at a time using the row programming feature present in these devices. For row programming, the source data is fetched directly from the data memory (RAM) on these devices. Two new registers have been provided to point to the RAM location where the source data resides. The page that has the row to be programmed must first be erased before the programming operation.

For protection against accidental operations, the write initiate sequence for NVMKEY must be used to allow any erase or program operation to proceed. After the programming command has been executed, the user application must wait for the programming time until programming is complete. The two instructions following the start of the programming sequence should be `NOP`s.

Refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"Flash Programming"** (DS70609) for details and code examples on programming using RTSP.

## 5.4 Control Registers

Six SFRs are used to read and write the program Flash memory: NVMCON, NVMKEY, NVMADR, NVMADRU, NVMSRCADRL and NVMSRCADRH.

The NVMCON register (Register 5-1) controls which blocks are to be erased, which memory type is to be programmed and the start of the programming cycle.

NVMKEY (Register 5-4) is a write-only register that is used for write protection. To start a programming or erase sequence, the user application must consecutively write 0x55 and 0xAA to the NVMKEY register.

There are two NVM Address registers: NVMADRU and NVMADR. These two registers, when concatenated, form the 24-bit Effective Address (EA) of the selected word for programming operations, or the selected page for erase operations.

The NVMADRU register is used to hold the upper 8 bits of the EA, while the NVMADR register is used to hold the lower 16 bits of the EA.

The NVMSRCADRH and NVMSRCADRL registers are used to hold the source address of the data in the data memory that needs to be written to Flash memory.

### REGISTER 6-1: RCON: RESET CONTROL REGISTER[1]

| R/W-0 | R/W-0 | U-0 | U-0 | R/W-0 | U-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| TRAPR | IOPUWR | — | — | VREGSF | — | CM | VREGS |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-1 | R/W-1 |
|---|---|---|---|---|---|---|---|
| EXTR | SWR | SWDTEN[2] | WDTO | SLEEP | IDLE | BOR | POR |
| bit 7 | | | | | | | bit 0 |

| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **TRAPR:** Trap Reset Flag bit
1 = A Trap Conflict Reset has occurred
0 = A Trap Conflict Reset has not occurred

bit 14 **IOPUWR:** Illegal Opcode or Uninitialized W Access Reset Flag bit
1 = An illegal opcode detection, an illegal address mode or Uninitialized W register used as an Address Pointer caused a Reset
0 = An illegal opcode or Uninitialized W Register Reset has not occurred

bit 13-12 **Unimplemented:** Read as '0'

bit 11 **VREGSF:** Flash Voltage Regulator Standby During Sleep bit
1 = Flash Voltage regulator is active during Sleep
0 = Flash Voltage regulator goes into Standby mode during Sleep

bit 10 **Unimplemented:** Read as '0'

bit 9 **CM:** Configuration Mismatch Flag bit
1 = A Configuration Mismatch Reset has occurred.
0 = A Configuration Mismatch Reset has NOT occurred

bit 8 **VREGS:** Voltage Regulator Standby During Sleep bit
1 = Voltage regulator is active during Sleep
0 = Voltage regulator goes into Standby mode during Sleep

bit 7 **EXTR:** External Reset ($\overline{\text{MCLR}}$) Pin bit
1 = A Master Clear (pin) Reset has occurred
0 = A Master Clear (pin) Reset has not occurred

bit 6 **SWR:** Software RESET (Instruction) Flag bit
1 = A RESET instruction has been executed
0 = A RESET instruction has not been executed

bit 5 **SWDTEN:** Software Enable/Disable of WDT bit[2]
1 = WDT is enabled
0 = WDT is disabled

bit 4 **WDTO:** Watchdog Timer Time-out Flag bit
1 = WDT time-out has occurred
0 = WDT time-out has not occurred

**Note 1:** All of the Reset status bits can be set or cleared in software. Setting one of these bits in software does not cause a device Reset.

**2:** If the FWDTEN Configuration bit is '1' (unprogrammed), the WDT is always enabled, regardless of the SWDTEN bit setting.

**NOTES:**

## 9.1 CPU Clocking System

The dsPIC33EPXXXGM3XX/6XX/7XX family of devices provides seven system clock options:

- Fast RC (FRC) Oscillator
- FRC Oscillator with Phase-Locked Loop (PLL)
- FRC Oscillator with Postscaler
- Primary (XT, HS or EC) Oscillator
- Primary Oscillator with PLL
- Low-Power RC (LPRC) Oscillator
- Secondary (LP) Oscillator

Instruction execution speed or device operating frequency, FCY, is given by Equation 9-1.

**EQUATION 9-1: DEVICE OPERATING FREQUENCY**

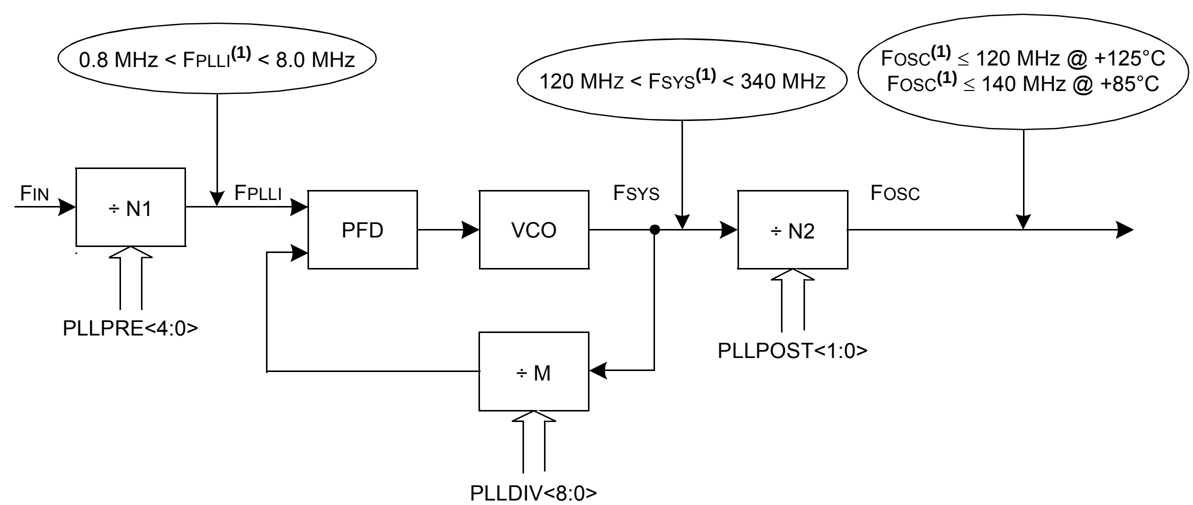
$$F_{CY} = F_{OSC}/2$$

Figure 9-2 is a block diagram of the PLL module.

Equation 9-2 provides the relationship between input frequency (FIN) and output frequency (FOSC).

Equation 9-3 provides the relationship between input frequency (FIN) and VCO frequency (FSYS).

**FIGURE 9-2: PLL BLOCK DIAGRAM**




**Note 1:** This frequency range must be met at all times.

**EQUATION 9-2: FOSC CALCULATION**

$$F_{OSC} = F_{IN} \times \left(\frac{M}{N1 \times N2}\right) = F_{IN} \times \left(\frac{(PLLDIV<8:0> + 2)}{(PLLPRE<4:0> + 2) \times 2(PLLPOST<1:0> + 1)}\right)$$

Where:

$N1 = PLLPRE<4:0> + 2$

$N2 = 2 \times (PLLPOST<1:0> + 1)$

$M = PLLDIV<8:0> + 2$

**EQUATION 9-3: FVCO CALCULATION**

$$F_{SYS} = F_{IN} \times \left(\frac{M}{N1}\right) = F_{IN} \times \left(\frac{(PLLDIV<8:0> + 2)}{(PLLPRE<4:0> + 2)}\right)$$

### REGISTER 9-4: OSCTUN: FRC OSCILLATOR TUNING REGISTER(1)

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | TUN<5:0> | | | | | |
| bit 7 | | | | | | | bit 0 |

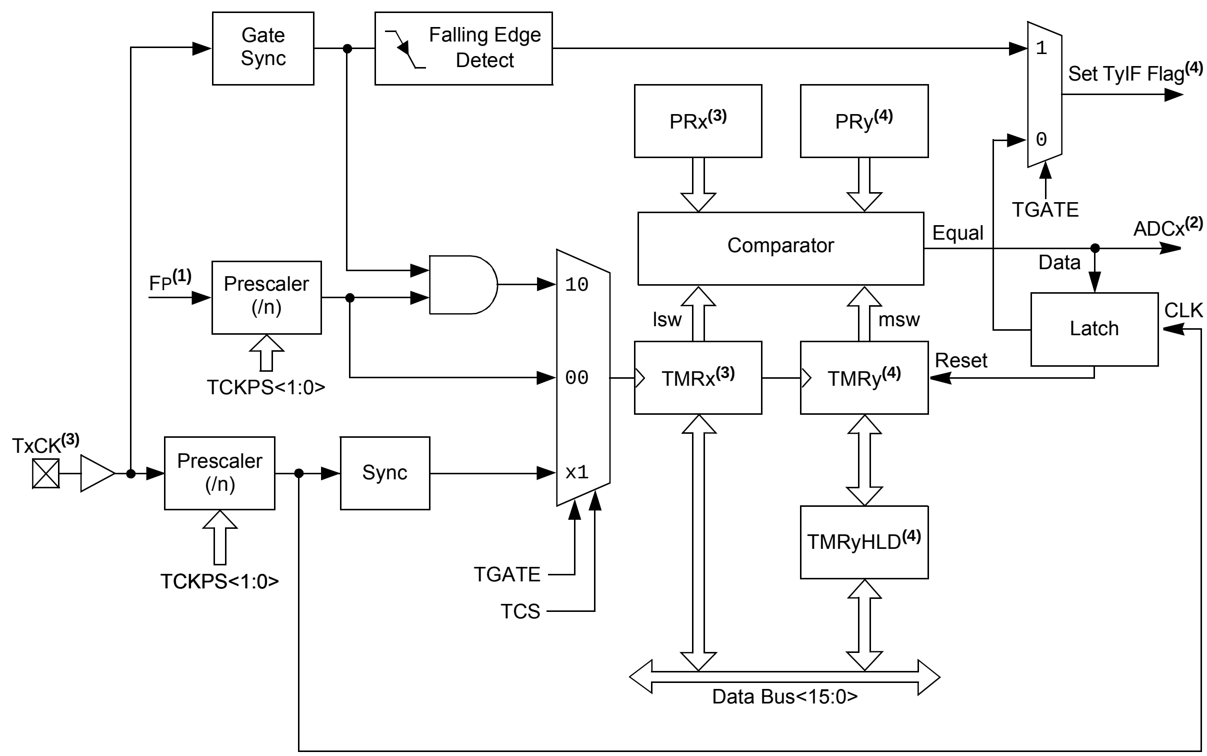
| Legend: | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-6 **Unimplemented:** Read as ‘0’

bit 5-0 **TUN<5:0>:** FRC Oscillator Tuning bits
111111 = Center frequency – 0.047%
•
•
•
100001 = Center frequency – 1.453%
100000 = Center frequency – 1.5% (7.355 MHz)
011111 = Center frequency + 1.5% (7.385 MHz)
011110 = Center frequency + 1.453%
•
•
•
000001 = Center frequency + 0.047%
000000 = Center frequency (7.3728 MHz nominal)

**Note 1:** This register resets only on a Power-on Reset (POR).

**FIGURE 13-3: TYPE B/TYPE C TIMER PAIR BLOCK DIAGRAM (32-BIT TIMER)**




**Note 1:** FP is the peripheral clock.
**2:** The ADCx trigger is available only on the TMR3:TMR2 andTMR5:TMR4 32-bit timer pairs.
**3:** Timerx is a Type B timer (x = 2 and 4).
**4:** Timery is a Type C timer (x = 3 and 5).

**REGISTER 16-1: PTCON: PWMx TIME BASE CONTROL REGISTER (CONTINUED)**

bit 6-4 **SYNCSRC<2:0>:** Synchronous Source Selection bits[1]

111 = Reserved
•
•
•
100 = Reserved
011 = PTGO17[2]
010 = PTGO16[2]
001 = Reserved
000 = SYNCI1

bit 3-0 **SEVTPS<3:0>:** PWMx Special Event Trigger Output Postscaler Select bits[1]

1111 = 1:16 Postscaler generates Special Event Trigger on every sixteenth compare match event
•
•
•
0001 = 1:2 Postscaler generates Special Event Trigger on every second compare match event
0000 = 1:1 Postscaler generates Special Event Trigger on every compare match event

**Note 1:** These bits should be changed only when PTEN = 0. In addition, when using the SYNCI1 feature, the user application must program the Period register with a value that is slightly larger than the expected period of the external synchronization input signal.

**2:** See **Section 25.0 “Peripheral Trigger Generator (PTG) Module”** for information on this selection.

**REGISTER 16-23: LEBDLYx: LEADING-EDGE BLANKING DELAY REGISTER x**

| U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | LEB<11:8> | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| LEB<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-12 **Unimplemented:** Read as ‘0’

bit 11-0 **LEB<11:0>:** Leading-Edge Blanking Delay for Current-Limit and Fault Inputs bits

**REGISTER 21-16: CxRXFnSID: CANx ACCEPTANCE FILTER n STANDARD IDENTIFIER REGISTER (n = 0-15)**

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| SID10 | SID9 | SID8 | SID7 | SID6 | SID5 | SID4 | SID3 |
| bit 15 | | | | | | | bit 8 |

| R/W-x | R/W-x | R/W-x | U-0 | R/W-x | U-0 | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| SID2 | SID1 | SID0 | — | EXIDE | — | EID17 | EID16 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-5 **SID<10:0>:** Standard Identifier bits
1 = Message address bit, SIDx, must be ‘1’ to match filter
0 = Message address bit, SIDx, must be ‘0’ to match filter

bit 4 **Unimplemented:** Read as ‘0’

bit 3 **EXIDE:** Extended Identifier Enable bit
If MIDE = 1:
1 = Matches only messages with Extended Identifier addresses
0 = Matches only messages with Standard Identifier addresses
If MIDE = 0:
Ignores EXIDE bit.

bit 2 **Unimplemented:** Read as ‘0’

bit 1-0 **EID<17:16>:** Extended Identifier bits
1 = Message address bit, EIDx, must be ‘1’ to match filter
0 = Message address bit, EIDx, must be ‘0’ to match filter

**REGISTER 21-17: CxRXFnEID: CANx ACCEPTANCE FILTER n EXTENDED IDENTIFIER REGISTER (n = 0-15)**

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| EID<15:8> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
|---|---|---|---|---|---|---|---|
| EID<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-0 **EID<15:0>:** Extended Identifier bits
1 = Message address bit, EIDx, must be ‘1’ to match filter
0 = Message address bit, EIDx, must be ‘0’ to match filter

**TABLE 25-1: PTG STEP COMMAND FORMAT (CONTINUED)**

| bit 3-0 | Step Command | OPTION<3:0> | Option Description |
|---|---|---|---|
| | PTGCTRL(1) | 0000 | Reserved |
| | | 0001 | Reserved |
| | | 0010 | Disable Step Delay Timer (PTGSD) |
| | | 0011 | Reserved |
| | | 0100 | Reserved |
| | | 0101 | Reserved |
| | | 0110 | Enable Step Delay Timer (PTGSD) |
| | | 0111 | Reserved |
| | | 1000 | Start and wait for the PTG Timer0 to match Timer0 Limit register |
| | | 1001 | Start and wait for the PTG Timer1 to match Timer1 Limit register |
| | | 1010 | Reserved |
| | | 1011 | Wait for software trigger bit transition from low-to-high before continuing (PTGSWT = 0 to 1) |
| | | 1100 | Copy contents of the Counter 0 register to the AD1CHS0 register |
| | | 1101 | Copy contents of the Counter 1 register to the AD1CHS0 register |
| | | 1110 | Copy contents of the Literal 0 register to the AD1CHS0 register |
| | | 1111 | Generate the triggers indicated in the PTG Broadcast Trigger Enable register (PTGBTE) |
| | PTGADD(1) | 0000 | Add contents of PTGADJ register to the Counter 0 Limit register (PTGC0LIM) |
| | | 0001 | Add contents of PTGADJ register to the Counter 1 Limit register (PTGC1LIM) |
| | | 0010 | Add contents of PTGADJ register to the Timer0 Limit register (PTGT0LIM) |
| | | 0011 | Add contents of PTGADJ register to the Timer1 Limit register (PTGT1LIM) |
| | | 0100 | Add contents of PTGADJ register to the Step Delay Limit register (PTGSDLIM) |
| | | 0101 | Add contents of PTGADJ register to the Literal 0 register (PTGL0) |
| | | 0110 | Reserved |
| | | 0111 | Reserved |
| | PTGCOPY(1) | 1000 | Copy contents of PTGHOLD register to the Counter 0 Limit register (PTGC0LIM) |
| | | 1001 | Copy contents of PTGHOLD register to the Counter 1 Limit register (PTGC1LIM) |
| | | 1010 | Copy contents of PTGHOLD register to the Timer0 Limit register (PTGT0LIM) |
| | | 1011 | Copy contents of PTGHOLD register to the Timer1 Limit register (PTGT1LIM) |
| | | 1100 | Copy contents of PTGHOLD register to the Step Delay Limit register (PTGSDLIM) |
| | | 1101 | Copy contents of PTGHOLD register to the Literal 0 register (PTGL0) |
| | | 1110 | Reserved |
| | | 1111 | Reserved |

**Note 1:** All reserved commands or options will execute but have no effect (i.e., execute as a NOP instruction).
**2:** Refer to Table 25-2 for the trigger output descriptions.

**REGISTER 28-5: PMSTAT: PARALLEL MASTER PORT STATUS REGISTER (SLAVE MODE ONLY)(1)**

| R-0 | R/W-0, HS | U-0 | U-0 | R-0 | R-0 | R-0 | R-0 |
|---|---|---|---|---|---|---|---|
| IBF | IBOV | — | — | IB3F | IB2F | IB1F | IB0F |
| bit 15 | | | | | | | bit 8 |

| R-1 | R/W-0, HS | U-0 | U-0 | R-1 | R-1 | R-1 | R-1 |
|---|---|---|---|---|---|---|---|
| OBE | OBUF | — | — | OB3E | OB2E | OB1E | OB0E |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | HS = Hardware Settable bit | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at Reset | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 15 **IBF:** Input Buffer Full Status bit
1 = All writable Input Buffer registers are full
0 = Some or all of the writable Input Buffer registers are empty

bit 14 **IBOV:** Input Buffer Overflow Status bit
1 = A write attempt to a full Input Byte register occurred (must be cleared in software)
0 = No overflow occurred

bit 13-12 **Unimplemented:** Read as '0'

bit 11-8 **IB3F:IB0F:** Input Buffer x Status Full bit
1 = Input Buffer x contains data that has not been read (reading buffer will clear this bit)
0 = Input Buffer x does not contain any unread data

bit 7 **OBE:** Output Buffer Empty Status bit
1 = All readable Output Buffer registers are empty
0 = Some or all of the readable Output Buffer registers are full

bit 6 **OBUF:** Output Buffer Underflow Status bit
1 = A read occurred from an empty Output Byte register (must be cleared in software)
0 = No underflow occurred

bit 5-4 **Unimplemented:** Read as '0'

bit 3-0 **OB3E:OB0E:** Output Buffer x Status Empty bit
1 = Output Buffer x is empty (writing data to the buffer will clear this bit)
0 = Output Buffer x contains data that has not been transmitted

**Note 1:** This register is not available on 44-pin devices.

**TABLE 33-17: PLL CLOCK TIMING SPECIFICATIONS**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min.** | **Typ.(1)** | **Max.** | **Units** | **Conditions** |
| OS50 | FPLLI | PLL Voltage Controlled Oscillator (VCO) Input Frequency Range | 0.8 | — | 8.0 | MHz | ECPLL, XTPLL modes |
| OS51 | FSYS | On-Chip VCO System Frequency | 120 | — | 340 | MHz | |
| OS52 | TLOCK | PLL Start-up Time (Lock Time) | 0.9 | 1.5 | 3.1 | ms | |
| OS53 | DCLK | CLKO Stability (Jitter)(2) | -3 | 0.5 | 3 | % | |

**Note 1:** Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

**2:** This jitter specification is based on clock cycle-by-clock cycle measurements. To get the effective jitter for individual time bases or communication clocks used by the application, use the following formula:

$$Effective\ Jitter = \frac{D_{CLK}}{\sqrt{\frac{F_{OSC}}{Time\ Base\ or\ Communication\ Clock}}}$$

For example, if FOSC = 120 MHz and the SPI bit rate = 10 MHz, the effective jitter is as follows:

$$Effective\ Jitter = \frac{D_{CLK}}{\sqrt{\frac{120}{10}}} = \frac{D_{CLK}}{\sqrt{12}} = \frac{D_{CLK}}{3.464}$$

**TABLE 33-18: INTERNAL FRC ACCURACY**

| AC CHARACTERISTICS | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Characteristic** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** | |
| **Internal FRC Accuracy @ FRC Frequency = 7.3728 MHz(1)** | | | | | | | |
| F20a | FRC | -1.5 | 0.5 | +1.5 | % | -40°C ≤ TA ≤ +85°C | VDD = 3.0-3.6V |
| F20b | FRC | -2 | 1.5 | +2 | % | -40°C ≤ TA ≤ +125°C | VDD = 3.0-3.6V |

**Note 1:** Frequency calibrated at +25°C and 3.3V. TUNx bits can be used to compensate for temperature drift.

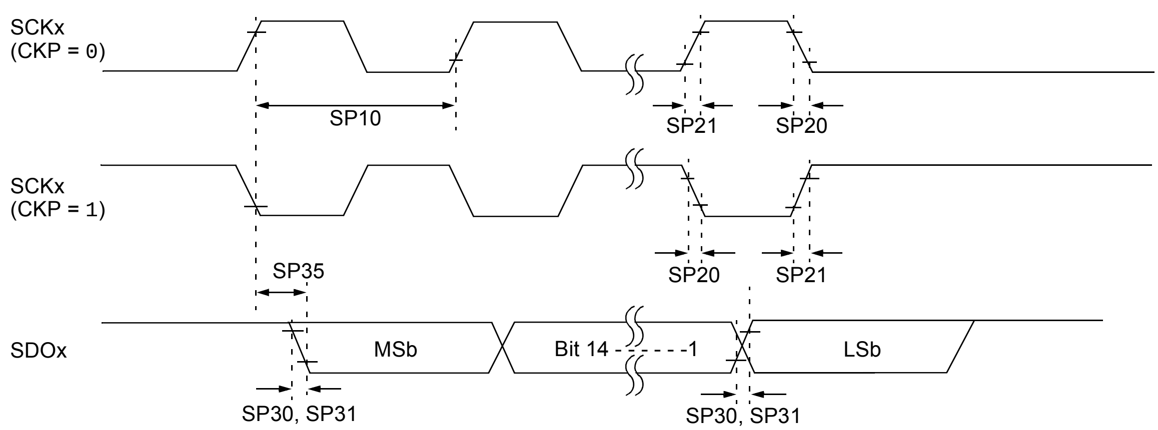
**TABLE 33-19: INTERNAL LPRC ACCURACY**

| AC CHARACTERISTICS | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Characteristic** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** | |
| **LPRC @ 32.768 kHz** | | | | | | | |
| F21a | LPRC | -15 | 5 | +15 | % | -40°C ≤ TA ≤ +85°C | VDD = 3.0-3.6V |
| F21b | LPRC | -30 | 10 | +30 | % | -40°C ≤ TA ≤ +125°C | VDD = 3.0-3.6V |

**TABLE 33-32: SPI2 AND SPI3 MAXIMUM DATA/CLOCK RATE SUMMARY**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | |
|---|---|---|---|---|---|---|
| **Maximum Data Rate** | **Master Transmit Only (Half-Duplex)** | **Master Transmit/Receive (Full-Duplex)** | **Slave Transmit/Receive (Full-Duplex)** | **CKE** | **CKP** | **SMP** |
| 15 MHz | Table 33-33 | — | — | 0,1 | 0,1 | 0,1 |
| 9 MHz | — | Table 33-34 | — | 1 | 0,1 | 1 |
| 9 MHz | — | Table 33-35 | — | 0 | 0,1 | 1 |
| 15 MHz | — | — | Table 33-36 | 1 | 0 | 0 |
| 11 MHz | — | — | Table 33-37 | 1 | 1 | 0 |
| 15 MHz | — | — | Table 33-38 | 0 | 1 | 0 |
| 11 MHz | — | — | Table 33-39 | 0 | 0 | 0 |

**FIGURE 33-15: SPI2 AND SPI3 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY, CKE = 0) TIMING CHARACTERISTICS**




**Note:** Refer to Figure 33-1 for load conditions.

**FIGURE 33-20: SPI2 AND SPI3 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 1, SMP = 0) TIMING CHARACTERISTICS**

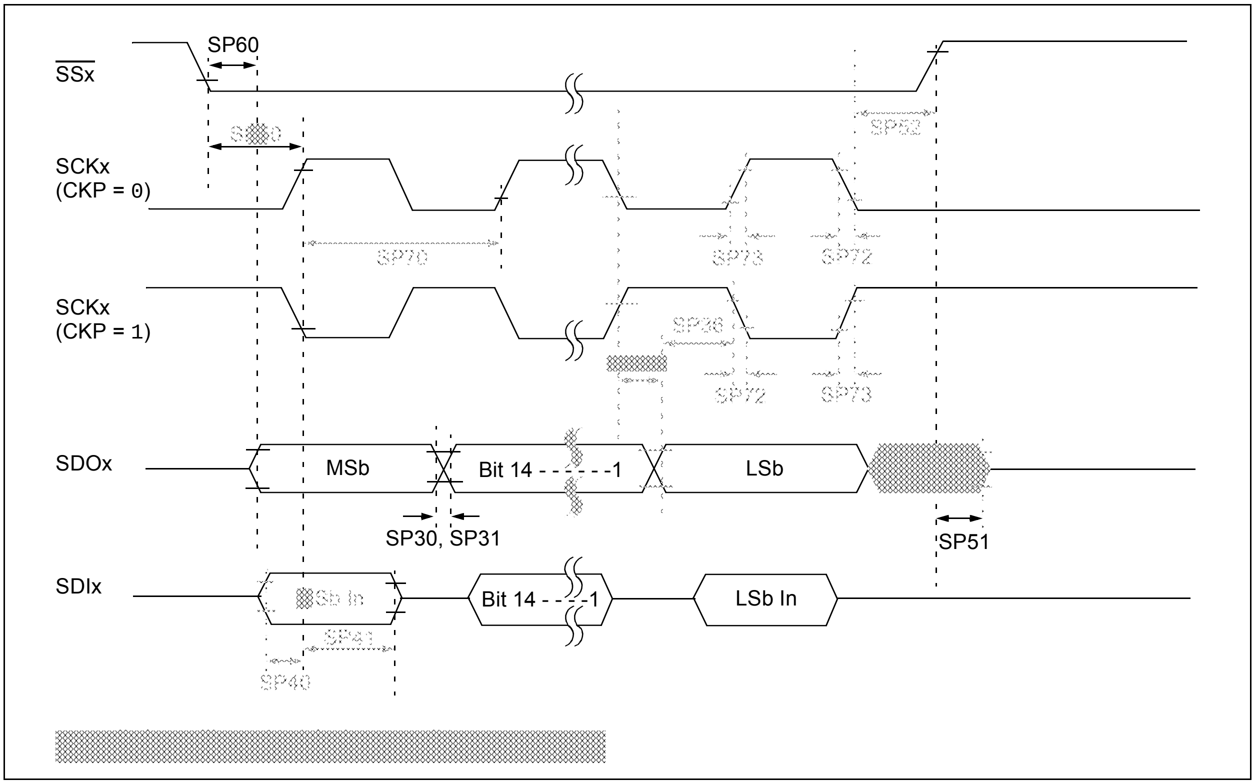


**FIGURE 33-27: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 0, SMP = 0) TIMING CHARACTERISTICS**

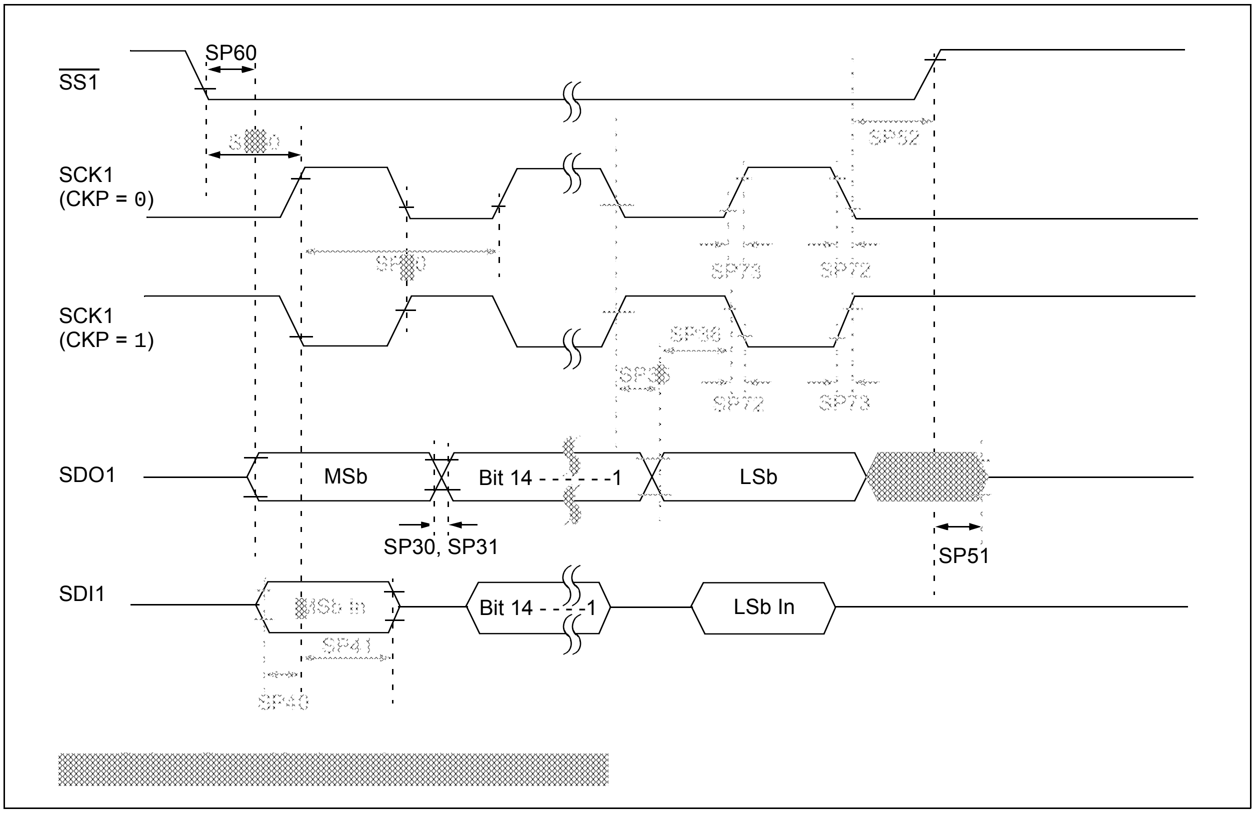


**TABLE 33-52: OP AMP/COMPARATOR SPECIFICATIONS**

| **DC CHARACTERISTICS** | | | **Standard Operating Conditions (see Note 3): 3.0V to 3.6V (unless otherwise stated)**<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min.** | **Typ.[(1)]** | **Max.** | **Units** | **Conditions** |
| **Comparator AC Characteristics** | | | | | | | |
| CM10 | TRESP | Response Time | — | 19 | — | ns | V+ input step of 100 mV, V- input held at VDD/2 |
| CM11 | TMC2OV | Comparator Mode Change to Output Valid | — | — | 10 | µs | |
| **Comparator DC Characteristics** | | | | | | | |
| CM30 | VOFFSET | Comparator Offset Voltage | — | ±20 | ±75 | mV | |
| CM31 | VHYST | Input Hysteresis Voltage | — | 30 | — | mV | |
| CM32 | TRISE/ TFALL | Comparator Output Rise/Fall Time | — | 20 | — | ns | 1 pF load capacitance on input |
| CM33 | VGAIN | Open-Loop Voltage Gain | — | 90 | — | db | |
| CM34 | VICM | Input Common-Mode Voltage | AVSS | — | AVDD | V | |
| **Op Amp AC Characteristics** | | | | | | | |
| CM20 | SR | Slew Rate | — | 9 | — | V/µs | 10 pF load |
| CM21a | PM | Phase Margin | — | 68 | — | Degree | G = 100V/V; 10 pF load |
| CM22 | GM | Gain Margin | — | 20 | — | db | G = 100V/V; 10 pF load |
| CM23a | GBW | Gain Bandwidth | — | 10 | — | MHz | 10 pF load |
| **Op Amp DC Characteristics** | | | | | | | |
| CM40 | VCMR | Common-Mode Input Voltage Range | AVSS | — | AVDD | V | |
| CM41 | CMRR | Common-Mode Rejection Ratio | — | 40 | — | db | VCM = AVDD/2 |
| CM42 | VOFFSET | Op Amp Offset Voltage | — | ±20 | ±70 | mV | |
| CM43 | VGAIN | Open-Loop Voltage Gain | — | 90 | — | db | |
| CM44 | IOS | Input Offset Current | — | — | — | — | See pad leakage currents in Table 33-10 |
| CM45 | IB | Input Bias Current | — | — | — | — | See pad leakage currents in Table 33-10 |
| CM46 | IOUT | Output Current | — | — | 420 | µA | With minimum value of RFEEDBACK (CM48) |
| CM48 | RFEEDBACK | Feedback Resistance Value | 8 | — | — | kΩ | **(Note 2)** |
| CM49a | VOUT | Output Voltage | AVSS + 0.075 | — | AVDD – 0.075 | V | IOUT = 420 µA |

**Note 1:** Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.

**2:** Resistances can vary by ±10% between op amps.

**3:** Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules: ADC, op amp/comparator and comparator voltage reference, will have degraded performance. Refer to Parameter BO10 in Table 33-12 for the minimum and maximum BOR values.

**TABLE 33-57: ADCx MODULE SPECIFICATIONS (12-BIT MODE)**

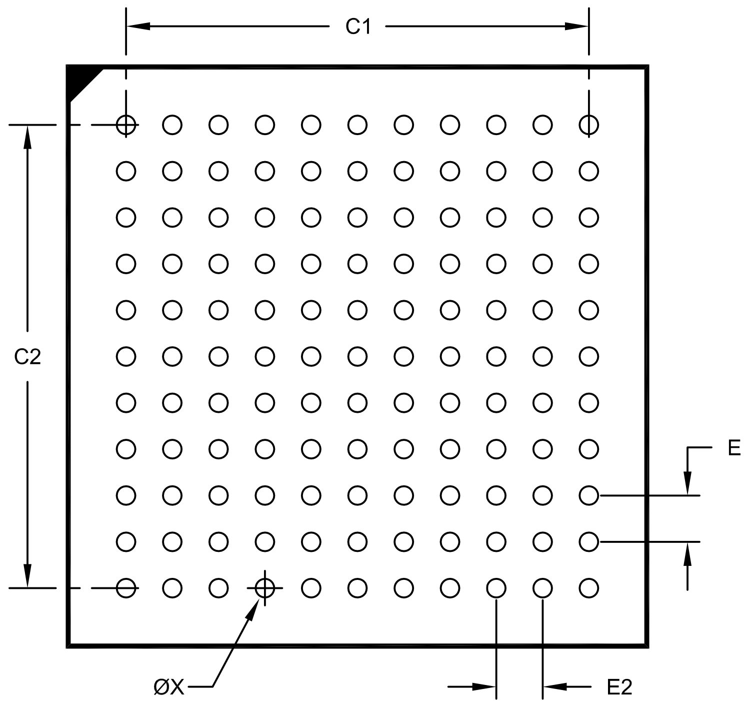
| AC CHARACTERISTICS | | | Standard Operating Conditions (see Note 1): 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| **ADC Accuracy (12-Bit Mode) – VREF-** | | | | | | | |
| AD20a | Nr | Resolution | 12 data bits | | | bits | |
| AD21a | INL | Integral Nonlinearity | -3 | — | +3 | LSb | VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V **(Note 2)** |
| AD22a | DNL | Differential Nonlinearity | ≥ 1 | — | < 1 | LSb | VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V **(Note 2)** |
| AD23a | GERR | Gain Error | -10 | — | 10 | LSb | VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V **(Note 2)** |
| AD24a | EOFF | Offset Error | -5 | — | 5 | LSb | VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V **(Note 2)** |
| AD25a | — | Monotonicity | — | — | — | — | Guaranteed |
| **Dynamic Performance (12-Bit Mode)** | | | | | | | |
| AD30a | THD | Total Harmonic Distortion | — | — | -75 | dB | |
| AD31a | SINAD | Signal to Noise and Distortion | 68.5 | 69.5 | — | dB | |
| AD32a | SFDR | Spurious Free Dynamic Range | 80 | — | — | dB | |
| AD33a | FNYQ | Input Signal Bandwidth | — | — | 250 | kHz | |
| AD34a | ENOB | Effective Number of Bits | 11.09 | 11.3 | — | bits | |

**Note 1:** Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules: ADC, op amp/comparator and comparator voltage reference, will have degraded performance. Refer to Parameter BO10 in Table 33-12 for the minimum and maximum BOR values.

**2:** For all accuracy specifications, VINL = AVSS = VREFL = 0V and AVDD = VREFH = 3.6V.

### 121-Lead Plastic Thin Profile Ball Grid Array (BG) - 10x10x1.10 mm Body [TFBGA--Formerly XBGA]

| | |
|---|---|
| **Note:** | For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging |




RECOMMENDED LAND PATTERN

| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | E1 | 0.80 BSC | | |
| Contact Pitch | E2 | 0.80 BSC | | |
| Contact Pad Spacing | C1 | | 8.00 | |
| Contact Pad Spacing | C2 | | 8.00 | |
| Contact Pad Diameter (X121) | X | | | 0.32 |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2148 Rev D