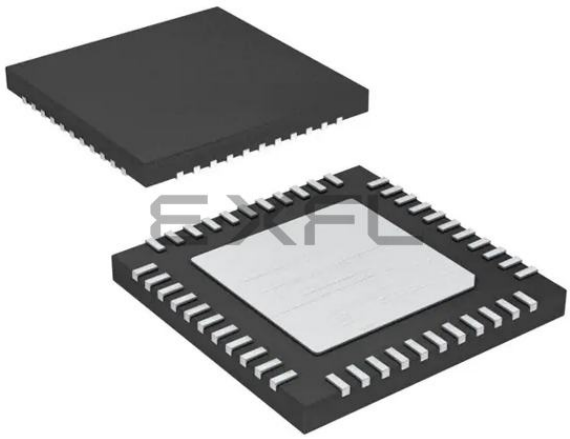
Microchip Technology - DSPIC33EP512GM304T-I/ML Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	I²C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, Motor Control PWM, POR, PWM, WDT
Number of I/O	35
Program Memory Size	512KB (170K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	-
Data Converters	A/D 18x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep512gm304t-i-ml

3.0 CPU

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGM3XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the "*dsPIC33/PIC24 Family Reference Manual*", **"CPU"** (DS70359), which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The CPU has a 16-bit (data) modified Harvard architecture with an enhanced instruction set, including significant support for digital signal processing. The CPU has a 24-bit instruction word, with a variable length opcode field. The Program Counter (PC) is 23 bits wide and addresses up to 4M x 24 bits of user program memory space.

An instruction prefetch mechanism helps maintain throughput and provides predictable execution. Most instructions execute in a single-cycle, effective execution rate, with the exception of instructions that change the program flow, the double-word move (`MOV.D`) instruction, PSV accesses and the table instructions. Overhead-free program loop constructs are supported using the `DO` and `REPEAT` instructions, both of which are interruptible at any point.

3.1 Registers

The dsPIC33EPXXXGM3XX/6XX/7XX devices have sixteen 16-bit Working registers in the programmer's model. Each of the Working registers can act as a data, address or address offset register. The 16th Working register (W15) operates as a Software Stack Pointer for interrupts and calls.

3.2 Instruction Set

The device instruction set has two classes of instructions: the MCU class of instructions and the DSP class of instructions. These two instruction classes are seamlessly integrated into the architecture and execute from a single execution unit. The instruction set includes many addressing modes and was designed for optimum C compiler efficiency.

3.3 Data Space Addressing

The Base Data Space can be addressed as 4K words or 8 Kbytes and is split into two blocks, referred to as X and Y data memory. Each memory block has its own independent Address Generation Unit (AGU). The MCU class of instructions operate solely through the X memory AGU, which accesses the entire memory map as one linear Data Space. On dsPIC33EP devices, certain DSP instructions operate through the X and Y AGUs to support dual operand reads, which splits the data address space into two parts. The X and Y Data Space boundary is device-specific.

The upper 32 Kbytes of the Data Space memory map can optionally be mapped into Program Space at any 16K program word boundary. The program-to-Data Space mapping feature, known as Program Space Visibility (PSV), lets any instruction access Program Space as if it were Data Space. Moreover, the Base Data Space address is used in conjunction with a Data Space Read or Write Page register (DSRPAG or DSWPAG) to form an Extended Data Space (EDS) address. The EDS can be addressed as 8M words or 16 Mbytes. Refer to **"Data Memory"** (DS70595) and **"Program Memory"** (DS70613) in the *"dsPIC33/PIC24 Family Reference Manual"* for more details on EDS, PSV and table accesses.

On dsPIC33EP devices, overhead-free circular buffers (Modulo Addressing) are supported in both X and Y address spaces. The Modulo Addressing removes the software boundary checking overhead for DSP algorithms. The X AGU circular addressing can be used with any of the MCU class of instructions. The X AGU also supports Bit-Reversed Addressing to greatly simplify input or output data reordering for radix-2 FFT algorithms.

3.4 Addressing Modes

The CPU supports these addressing modes:

- Inherent (no operand)
- Relative
- Literal
- Memory Direct
- Register Direct
- Register Indirect

Each instruction is associated with a predefined addressing mode group, depending upon its functional requirements. As many as six addressing modes are supported for each instruction.

TABLE 4-3: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EPXXXGM3XX DEVICES (CONTINUED)

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
IPC11	0856	—	T6IP2	T6IP1	T6IP0	—	—	—	—	—	PMPIP2(1)	PMPIP1(1)	PMPIP0(1)	—	OC8IP2	OC8IP1	OC8IP0	4444
IPC12	0858	—	T8IP2	T8IP1	T8IP0	—	MI2C2IP2	MI2C2IP1	MI2C2IP0	—	SI2C2IP2	SI2C2IP1	SI2C2IP0	—	T7IP2	T7IP1	T7IP0	4444
IPC13	085A	—	—	—	—	—	INT4IP2	INT4IP1	INT4IP0	—	INT3IP2	INT3IP1	INT3IP0	—	T9IP2	T9IP1	T9IP0	4444
IPC14	085C	—	DCIEIP2	DCIEIP1	DCIEIP0	—	QEI1IP2	QEI1IP2	QEI1IP0	—	PCEPIP2	PCEPIP1	PCEPIP0	—	—	—	—	4444
IPC15	085E	—	FLT1IP2	FLT1IP1	FLT1IP0	—	RTCCIP2(2)	RTCCIP1(2)	RTCCIP0(2)	—	—	—	—	—	DCIIP2	DCIIP1	DCIIP0	0404
IPC16	0860	—	CRCIP2	CRCIP1	CRCIP0	—	U2EIP2	U2EIP1	U2EIP0	—	U1EIP2	U1EIP1	U1EIP0	—	FLT2IP2	FLT2IP1	FLT2IP0	4440
IPC18	0864	—	C2TXIP2	C2TXIP1	C2TXIP0	—	FLT3IP2	FLT3IP1	FLT3IP0	—	PCESIP2	PCESIP1	PCESIP0	—	—	—	—	4040
IPC19	0866	—	—	—	—	—	—	—	—	—	CTMUIP2	CTMUIP1	CTMUIP0	—	FLT4IP2	FLT4IP1	FLT4IP0	0004
IPC20	0868	—	U3TXIP2	U3TXIP1	U3TXIP0	—	U3RXIP2	U3RXIP1	U3RXIP0	—	U3EIP2	U3EIP1	U3EIP0	—	—	—	—	0000
IPC21	086A	—	U4EIP2	U4EIP1	U4EIP0	—	—	—	—	—	—	—	—	—	—	—	—	0000
IPC22	086C	—	SPI3IP2	SPI3IP1	SPI3IP0	—	SPI3EIP2	SPI3EIP1	SPI3EIP0	—	U4TXIP2	U4TXIP1	U4TXIP0	—	U4RXIP2	U4RXIP1	U4RXIP0	0000
IPC23	086E	—	PGC2IP2	PGC2IP1	PGC2IP0	—	PWM1IP2	PWM1IP1	PWM1IP0	—	—	—	—	—	—	—	—	4400
IPC24	0870	—	PWM6IP2	PWM6IP1	PWM6IP0	—	PWM5IP2	PWM5IP1	PWM5IP0	—	PWM4IP2	PWM4IP1	PWM4IP0	—	PWM3IP2	PWM3IP1	PWM3IP0	4444
IPC35	0886	—	JTAGIP2	JTAGIP1	JTAGIP0	—	ICDIP2	ICDIP1	ICDIP0	—	—	—	—	—	—	—	—	4400
IPC36	0888	—	PTG0IP2	PTG0IP1	PTG0IP0	—	PTGWDTIP2	PTGWDTIP1	PTGWDTIP0	—	PTGSTEPIP2	PTGSTEPIP1	PTGSTEPIP0	—	—	—	—	4440
IPC37	088A	—	—	—	—	—	PTG3IP2	PTG3IP1	PTG3IP0	—	PTG2IP2	PTG2IP1	PTG2IP0	—	PTG1IP2	PTG1IP1	PTG1IP0	0444
INTTREG	08C8	—	—	—	—	ILR3	ILR2	ILR1	ILR0	VECNUM7	VECNUM6	VECNUM5	VECNUM4	VECNUM3	VECNUM2	VECNUM1	VECNUM0	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: The PMPIF/PMPIE/PMPIPx flags are not available on 44-pin devices.

2: The RTCCIF/RTCCIE/RTCCIPx flags are not available on 44-pin devices.

NOTES:

REGISTER 10-3: PMD3: PERIPHERAL MODULE DISABLE CONTROL REGISTER 3

R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
T9MD	T8MD	T7MD	T6MD	—	CMPMD	RTCCMD(1)	PMPMD
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CRCMD	DACMD	QEI2MD	PWM2MD	U3MD	I2C3MD	I2C2MD	ADC2MD
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **T9MD:** Timer9 Module Disable bit
1 = Timer9 module is disabled
0 = Timer9 module is enabled

bit 13 **T8MD:** Timer8 Module Disable bit
1 = Timer8 module is disabled
0 = Timer8 module is enabled

bit 14 **T7MD:** Timer7 Module Disable bit
1 = Timer7 module is disabled
0 = Timer7 module is enabled

bit 12 **T6MD:** Timer6 Module Disable bit
1 = Timer6 module is disabled
0 = Timer6 module is enabled

bit 11 **Unimplemented:** Read as ‘0’

bit 10 **CMPMD:** Comparator Module Disable bit
1 = Comparator module is disabled
0 = Comparator module is enabled

bit 9 **RTCCMD:** RTCC Module Disable bit(1)
1 = RTCC module is disabled
0 = RTCC module is enabled

bit 8 **PMPMD:** PMP Module Disable bit
1 = PMP module is disabled
0 = PMP module is enabled

bit 7 **CRCMD:** CRC Module Disable bit
1 = CRC module is disabled
0 = CRC module is enabled

bit 6 **DACMD:** DAC Module Disable bit
1 = DAC module is disabled
0 = DAC module is enabled

bit 5 **QEI2MD:** QEI2 Module Disable bit
1 = QEI2 module is disabled
0 = QEI2 module is enabled

bit 4 **PWM2MD:** PWM2 Module Disable bit
1 = PWM2 module is disabled
0 = PWM2 module is enabled

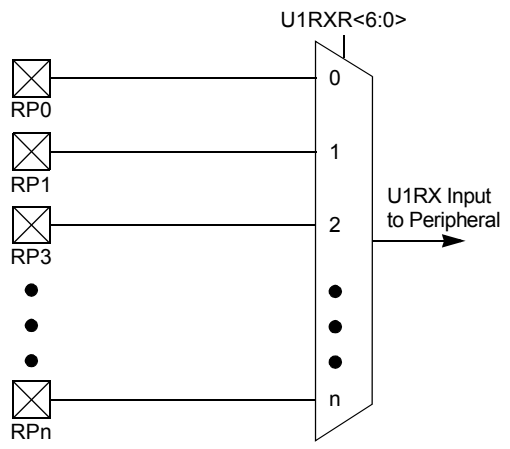
Note 1: The RTCCMD bit is not available on 44-pin devices.

11.4.4 INPUT MAPPING

The inputs of the Peripheral Pin Select options are mapped on the basis of the peripheral. That is, a control register associated with a peripheral dictates the pin it will be mapped to. The RPINRx registers are used to configure peripheral input mapping (see Register 11-1 through Register 11-29). Each register contains sets of 7-bit fields, with each set associated with one of the remappable peripherals. Programming a given peripheral's bit field with an appropriate 7-bit value maps the RPn pin with the corresponding value to that peripheral. For any given device, the valid range of values for any bit field corresponds to the maximum number of Peripheral Pin Selections supported by the device.

For example, Figure 11-2 illustrates remappable pin selection for the U1RX input.

FIGURE 11-2: REMAPPABLE INPUT FOR U1RX



Note: For input only, Peripheral Pin Select functionality does not have priority over TRISx settings. Therefore, when configuring an RPn pin for input, the corresponding bit in the TRISx register must also be configured for input (set to '1').

11.4.4.1 Virtual Connections

dsPIC33EPXXXGM3XX/6XX/7XX devices support virtual (internal) connections to the output of the op amp/comparator module (see Figure 26-1 in **Section 26.0 "Op Amp/Comparator Module"**) and the PTG module (see **Section 25.0 "Peripheral Trigger Generator (PTG) Module"**).

In addition, dsPIC33EPXXXGM3XX/6XX/7XX devices support virtual connections to the filtered QEIx module inputs: FINDX1, FHOME1, FINDX2 and FHOME2 (see Figure 17-1 in **Section 17.0 "Quadrature Encoder Interface (QEI) Module"**).

Virtual connections provide a simple way of inter-peripheral connection without utilizing a physical pin. For example, by setting the FLT1R<6:0> bits of the RPINR12 register to the value of 'b0000001, the output of the analog comparator, C1OUT, will be connected to the PWM Fault 1 input, which allows the analog comparator to trigger PWM Faults without the use of an actual physical pin on the device.

Virtual connection to the QEIx module allows peripherals to be connected to the QEIx digital filter input. To utilize this filter, the QEIx module must be enabled and its inputs must be connected to a physical RPn pin. Example 11-2 illustrates how the input capture module can be connected to the QEIx digital filter.

EXAMPLE 11-2: CONNECTING IC1 TO THE HOME1 QEI1 DIGITAL FILTER INPUT ON PIN 43

```
RPINR15 = 0x2500;      /* Connect the QEI1 HOME1 input to RP37 (pin 43) */
RPINR7 = 0x009;        /* Connect the IC1 input to the digital filter on the FHOME1 input */

QEI1IOC = 0x4000;      /* Enable the QEI digital filter */
QEI1CON = 0x8000;      /* Enable the QEI module */
```

TABLE 11-2: INPUT PIN SELECTION FOR SELECTABLE INPUT SOURCES

Peripheral Pin Select Input Register Value	Input/ Output	Pin Assignment	Peripheral Pin Select Input Register Value	Input/ Output	Pin Assignment
000 0000	I	Vss	010 1100	I	RPI44
000 0001	I	CMP1(1)	010 1101	I	RPI45
000 0010	I	CMP2(1)	010 1110	I	RPI46
000 0011	I	CMP3(1)	010 1111	I	RPI47
000 0100	I	CMP4(1)	011 0000	I/O	RP48
000 0101	—	—	011 0001	I/O	RP49
000 0110	I	PTGO30(1)	011 0010	I	RPI50
000 0111	I	PTGO31(1)	011 0011	I	RPI51
000 1000	I	INDX1(1)	011 0100	I	RPI52
000 1001	I	HOME1(1)	011 0101	I	RPI53
000 1010	I	INDX2(1)	011 0110	I/O	RP54
000 1011	I	HOME2(1)	011 0111	I/O	RP55
000 1100	I	CMP5(1)	011 1000	I/O	RP56
000 1101	—	—	011 1001	I/O	RP57
000 1110	—	—	011 1010	I	RPI58
000 1111	—	—	011 1011	—	—
001 0000	I	RPI16	011 1100	I	RPI60
001 0001	I	RPI17	011 1101	I	RPI61
001 0010	I	RPI18	011 1110	—	—
001 0011	I	RPI19	011 1111	I	RPI 63
001 0100	I/O	RP20	100 0000	—	—
001 0101	—	—	100 0001	—	—
001 0110	—	—	100 0010	—	—
001 0111	—	—	100 0011	—	—
001 1000	I	RPI24	100 0100	—	—
001 1001	I	RPI25	100 0101	I/O	RP69
001 1010	—	—	100 0110	I/O	RP70
001 1011	I	RPI27	100 0111	—	—
001 1100	I	RPI28	100 1000	I	RPI72
001 1101	—	—	100 1001	—	—
001 1110	—	—	100 1010	—	—
001 1111	—	—	100 1011	—	—
010 0000	I	RPI32	100 1100	I	RPI76
010 0001	I	RPI33	100 1101	I	RPI77
010 0010	I	RPI34	100 1110	—	—
010 0011	I/O	RP35	100 1111	—	—
010 0100	I/O	RP36	101 0000	I	RPI80
010 0101	I/O	RP37	101 0001	I/O	RP81
010 0110	I/O	RP38	101 0010	—	—
010 0111	I/O	RP39	101 0011	—	—
010 1000	I/O	RP40	101 0100	—	—

Legend: Shaded rows indicate PPS Input register values that are unimplemented.

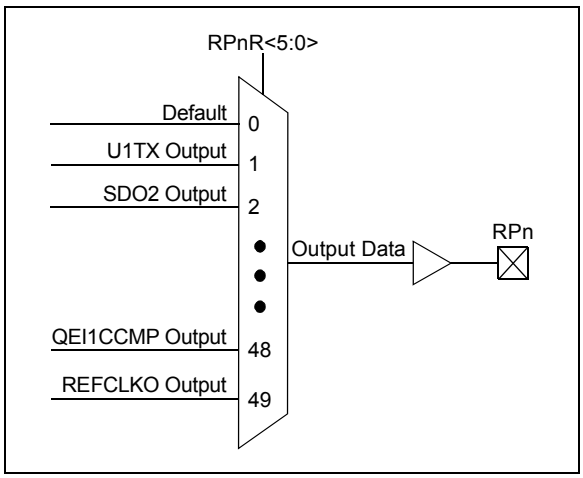
Note 1: See **Section 11.4.4.1 “Virtual Connections”** for more information on selecting this pin assignment.

11.4.5 OUTPUT MAPPING

In contrast to inputs, the outputs of the Peripheral Pin Select options are mapped on the basis of the pin. In this case, a control register associated with a particular pin dictates the peripheral output to be mapped. The RPORx registers are used to control output mapping. Like the RPINRx registers, each register contains sets of 6-bit fields, with each set associated with one RPn pin (see Register 11-30 through Register 11-42). The value of the bit field corresponds to one of the peripherals and that peripheral's output is mapped to the pin (see Table 11-3 and Figure 11-3).

A null output is associated with the output register Reset value of '0'. This is done to ensure that remappable outputs remain disconnected from all output pins by default.

FIGURE 11-3: MULTIPLEXING REMAPPABLE OUTPUT FOR RPn



11.4.5.1 Mapping Limitations

The control schema of the peripheral select pins is not limited to a small range of fixed peripheral configurations. There are no mutual or hardware-enforced lockouts between any of the peripheral mapping SFRs. Literally any combination of peripheral mappings across any or all of the RPn pins is possible. This includes both many-to-one and one-to-many mappings of peripheral inputs and outputs to pins. While such mappings may be technically possible from a configuration point of view, they may not be supportable from an electrical point of view.

REGISTER 14-2: ICxCON2: INPUT CAPTURE x CONTROL REGISTER 2

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	IC32(1)
bit 15							bit 8

R/W-0	R/W/HS-0	U-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-1
ICTRIG(2)	TRIGSTAT(3)	—	SYNCSEL4(4)	SYNCSEL3(4)	SYNCSEL2(4)	SYNCSEL1(4)	SYNCSEL0(4)
bit 7							bit 0

Legend:	HS = Hardware Settable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-9 **Unimplemented:** Read as '0'

bit 8 **IC32:** Input Capture x 32-Bit Timer Mode Select bit (Cascade mode)(1)
- 1 = Odd ICx and Even ICx form a single 32-bit input capture module
- 0 = Cascade module operation is disabled

bit 7 **ICTRIG:** Input Capture x Trigger Operation Select bit(2)
- 1 = Input source is used to trigger the input capture timer (Trigger mode)
- 0 = Input source is used to synchronize the input capture timer to the timer of another module (Synchronization mode)

bit 6 **TRIGSTAT:** Timer Trigger Status bit(3)
- 1 = ICxTMR has been triggered and is running
- 0 = ICxTMR has not been triggered and is being held clear

bit 5 **Unimplemented:** Read as '0'

Note 1: The IC32 bit in both the Odd and Even ICx must be set to enable Cascade mode.

2: The input source is selected by the SYNCSEL<4:0> bits of the ICxCON2 register.

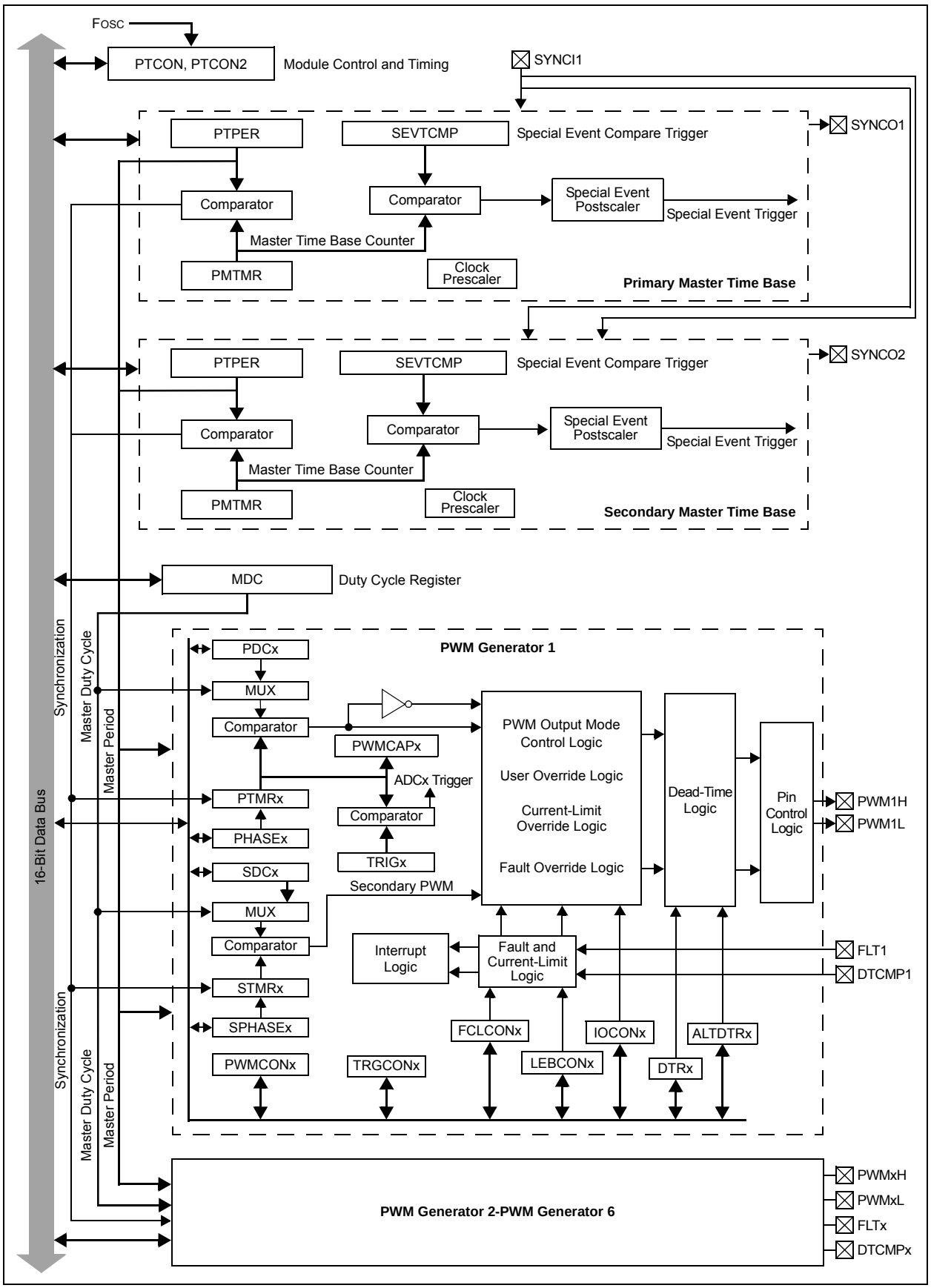
3: This bit is set by the selected input source (selected by SYNCSEL<4:0> bits); it can be read, set and cleared in software.

4: Do not use the ICx module as its own Sync or Trigger source.

5: This option should only be selected as a trigger source and not as a synchronization source.

6: Each Input Capture x module (ICx) has one PTG input source. See **Section 25.0 "Peripheral Trigger Generator (PTG) Module"** for more information.
PTGO8 = IC1, IC5
PTGO9 = IC2, IC6
PTGO10 = IC3, IC7
PTGO11 = IC4, IC8

FIGURE 16-2: HIGH-SPEED PWMx MODULE REGISTER INTERCONNECTION DIAGRAM



REGISTER 17-2: QEIxIOC: QEIx I/O CONTROL REGISTER (CONTINUED)

bit 2 **INDEX:** Status of INDXx Input Pin After Polarity Control bit
1 = Pin is at logic '1'
0 = Pin is at logic '0'

bit 1 **QEB:** Status of QEBx Input Pin After Polarity Control and SWPAB Pin Swapping bit
1 = Pin is at logic '1'
0 = Pin is at logic '0'

bit 0 **QEA:** Status of QEAx Input Pin After Polarity Control and SWPAB Pin Swapping bit
1 = Pin is at logic '1'
0 = Pin is at logic '0'

REGISTER 21-5: CxFIFO: CANx FIFO STATUS REGISTER

U-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0
—	—	FBP5	FBP4	FBP3	FBP2	FBP1	FBP0
bit 15							bit 8

U-0	U-0	R-0	R-0	R-0	R-0	R-0	R-0
—	—	FNRB5	FNRB4	FNRB3	FNRB2	FNRB1	FNRB0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-8 **FBP<5:0>:** FIFO Buffer Pointer bits

011111 = RB31 buffer
011110 = RB30 buffer
•
•
•
000001 = TRB1 buffer
000000 = TRB0 buffer

bit 7-6 **Unimplemented:** Read as ‘0’

bit 5-0 **FNRB<5:0>:** FIFO Next Read Buffer Pointer bits

011111 = RB31 buffer
011110 = RB30 buffer
•
•
•
000001 = TRB1 buffer
000000 = TRB0 buffer

REGISTER 21-20: CxRXMnSID: CANx ACCEPTANCE FILTER MASK n STANDARD IDENTIFIER REGISTER (n = 0-2)

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3
bit 15							bit 8

R/W-x	R/W-x	R/W-x	U-0	R/W-x	U-0	R/W-x	R/W-x
SID2	SID1	SID0	—	MIDE	—	EID17	EID16
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-5 **SID<10:0>:** Standard Identifier bits
1 = Includes bit, SIDx, in filter comparison
0 = Bit, SIDx, is a don't care in filter comparison

bit 4 **Unimplemented:** Read as '0'

bit 3 **MIDE:** Identifier Receive Mode bit
1 = Matches only message types (standard or extended address) that correspond to the EXIDE bit in the filter
0 = Matches either standard or extended address message if filters match (i.e., if (Filter SIDx) = (Message SIDx) or if (Filter SIDx/EIDx) = (Message SIDx/EIDx))

bit 2 **Unimplemented:** Read as '0'

bit 1-0 **EID<17:16>:** Extended Identifier bits
1 = Includes bit, EIDx, in filter comparison
0 = Bit, EIDx, is a don't care in filter comparison

REGISTER 21-21: CxRXMnEID: CANx ACCEPTANCE FILTER MASK n EXTENDED IDENTIFIER REGISTER (n = 0-2)

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
EID<15:8>							
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
EID<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **EID<15:0>:** Extended Identifier bits
1 = Includes bit, EIDx, in filter comparison
0 = Bit, EIDx, is a don't care in filter comparison

REGISTER 27-9: ALRMVAL (WHEN ALRMPTR<1:0> = 01): ALARM WEEKDAY AND HOURS VALUE REGISTER(1)

U-0	U-0	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x
—	—	—	—	—	WDAY2	WDAY1	WDAY0
bit 15							bit 8

U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	HRTEN1	HRTEN0	HRONE3	HRONE2	HRONE1	HRONE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-11 **Unimplemented:** Read as '0'

bit 10-8 **WDAY<2:0>:** Binary Coded Decimal Value of Weekday Digit bits
Contains a value from 0 to 6.

bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 **HRTEN<1:0>:** Binary Coded Decimal Value of Hour's Tens Digit bits
Contains a value from 0 to 2.

bit 3-0 **HRONE<3:0>:** Binary Coded Decimal Value of Hour's Ones Digit bits
Contains a value from 0 to 9.

Note 1: A write to this register is only allowed when RTCWREN = 1.

TABLE 31-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Base Instr #	Assembly Mnemonic	Assembly Syntax		Description	# of Words	# of Cycles	Status Flags Affected
72	SL	SL	f	f = Left Shift f	1	1	C,N,OV,Z
		SL	f,WREG	WREG = Left Shift f	1	1	C,N,OV,Z
		SL	Ws,Wd	Wd = Left Shift Ws	1	1	C,N,OV,Z
		SL	Wb,Wns,Wnd	Wnd = Left Shift Wb by Wns	1	1	N,Z
		SL	Wb,#lit5,Wnd	Wnd = Left Shift Wb by lit5	1	1	N,Z
73	SUB	SUB	Acc	Subtract Accumulators	1	1	OA,OB,OAB, SA,SB,SAB
		SUB	f	f = f – WREG	1	1	C,DC,N,OV,Z
		SUB	f,WREG	WREG = f – WREG	1	1	C,DC,N,OV,Z
		SUB	#lit10,Wn	Wn = Wn – lit10	1	1	C,DC,N,OV,Z
		SUB	Wb,Ws,Wd	Wd = Wb – Ws	1	1	C,DC,N,OV,Z
		SUB	Wb,#lit5,Wd	Wd = Wb – lit5	1	1	C,DC,N,OV,Z
74	SUBB	SUBB	f	f = f – WREG – ($\overline{C}$)	1	1	C,DC,N,OV,Z
		SUBB	f,WREG	WREG = f – WREG – ($\overline{C}$)	1	1	C,DC,N,OV,Z
		SUBB	#lit10,Wn	Wn = Wn – lit10 – ($\overline{C}$)	1	1	C,DC,N,OV,Z
		SUBB	Wb,Ws,Wd	Wd = Wb – Ws – ($\overline{C}$)	1	1	C,DC,N,OV,Z
		SUBB	Wb,#lit5,Wd	Wd = Wb – lit5 – ($\overline{C}$)	1	1	C,DC,N,OV,Z
75	SUBR	SUBR	f	f = WREG – f	1	1	C,DC,N,OV,Z
		SUBR	f,WREG	WREG = WREG – f	1	1	C,DC,N,OV,Z
		SUBR	Wb,Ws,Wd	Wd = Ws – Wb	1	1	C,DC,N,OV,Z
		SUBR	Wb,#lit5,Wd	Wd = lit5 – Wb	1	1	C,DC,N,OV,Z
76	SUBBR	SUBBR	f	f = WREG – f – ($\overline{C}$)	1	1	C,DC,N,OV,Z
		SUBBR	f,WREG	WREG = WREG – f – ($\overline{C}$)	1	1	C,DC,N,OV,Z
		SUBBR	Wb,Ws,Wd	Wd = Ws – Wb – ($\overline{C}$)	1	1	C,DC,N,OV,Z
		SUBBR	Wb,#lit5,Wd	Wd = lit5 – Wb – ($\overline{C}$)	1	1	C,DC,N,OV,Z
77	SWAP	SWAP.b	Wn	Wn = nibble swap Wn	1	1	None
		SWAP	Wn	Wn = byte swap Wn	1	1	None
78	TBLRDH	TBLRDH	Ws,Wd	Read Prog<23:16> to Wd<7:0>	1	5	None
79	TBLRDL	TBLRDL	Ws,Wd	Read Prog<15:0> to Wd	1	5	None
80	TBLWTH	TBLWTH	Ws,Wd	Write Ws<7:0> to Prog<23:16>	1	2	None
81	TBLWTL	TBLWTL	Ws,Wd	Write Ws to Prog<15:0>	1	2	None
82	ULNK	ULNK		Unlink Frame Pointer	1	1	SFA
83	XOR	XOR	f	f = f .XOR. WREG	1	1	N,Z
		XOR	f,WREG	WREG = f .XOR. WREG	1	1	N,Z
		XOR	#lit10,Wn	Wd = lit10 .XOR. Wd	1	1	N,Z
		XOR	Wb,Ws,Wd	Wd = Wb .XOR. Ws	1	1	N,Z
		XOR	Wb,#lit5,Wd	Wd = Wb .XOR. lit5	1	1	N,Z
84	ZE	ZE	Ws,Wnd	Wnd = Zero-extend Ws	1	1	C,Z,N

Note: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

33.1 DC Characteristics

TABLE 33-1: OPERATING MIPS vs. VOLTAGE

Characteristic	VDD Range (in Volts)	Temperature Range (in °C)	Maximum MIPS
			dsPIC33EPXXXGM3XX/6XX/7XX
I-Temp	3.0V to 3.6V(1)	-40°C to +85°C	70
E-Temp	3.0V to 3.6V(1)	-40°C to +125°C	60

Note 1: Device is functional at VBORMIN < VDD < VDDMIN. Analog modules: ADC, op amp/comparator and comparator voltage reference will have degraded performance. Device functionality is tested but not characterized. Refer to Parameter BO10 in Table 33-12 for the minimum and maximum BOR values.

TABLE 33-2: THERMAL OPERATING CONDITIONS

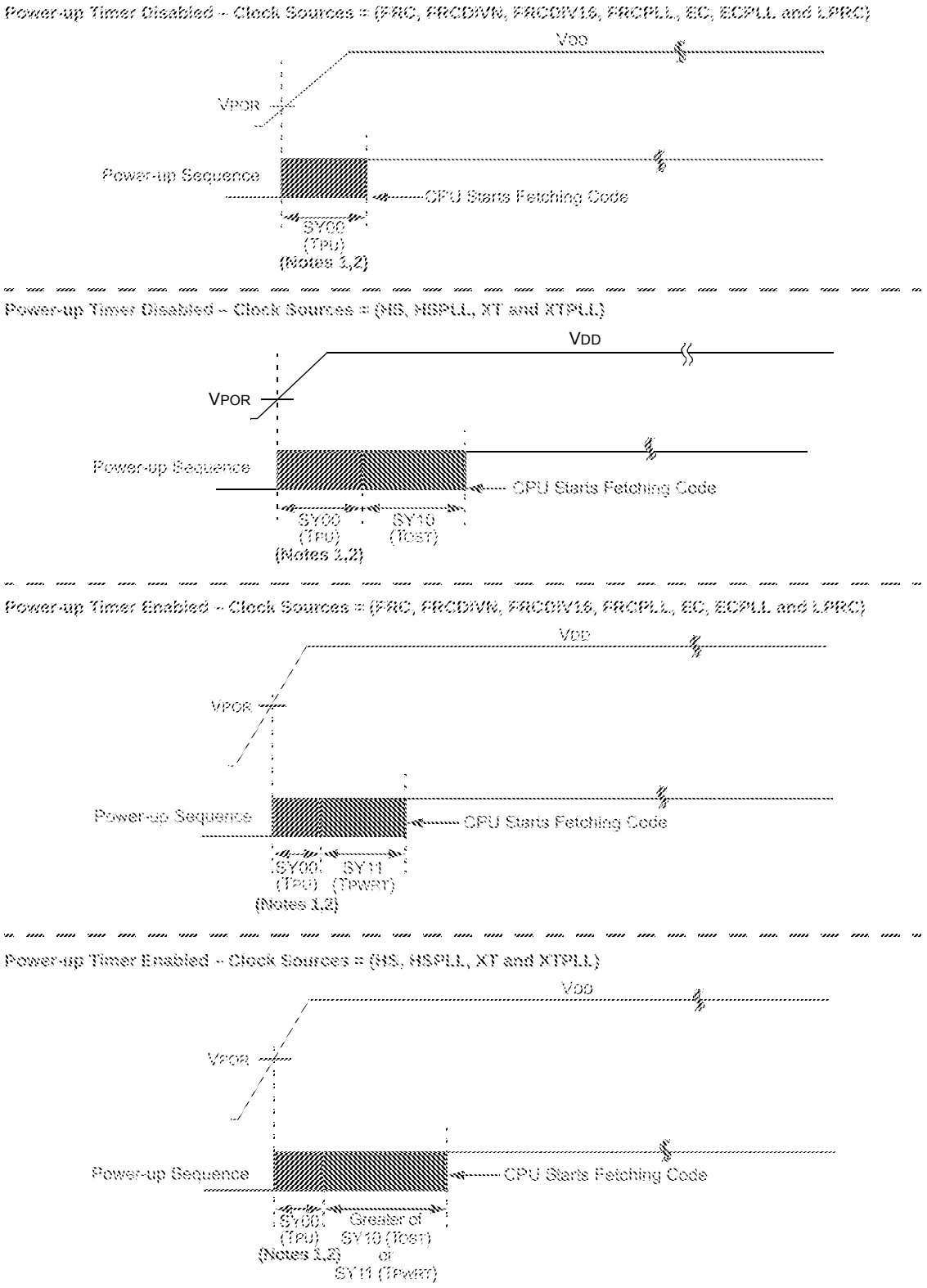
Rating	Symbol	Min.	Typ.	Max.	Unit
Industrial Temperature Devices:					
Operating Junction Temperature Range	TJ	-40	—	+125	°C
Operating Ambient Temperature Range	TA	-40	—	+85	°C
Extended Temperature Devices:					
Operating Junction Temperature Range	TJ	-40	—	+140	°C
Operating Ambient Temperature Range	TA	-40	—	+125	°C
Power Dissipation: Internal Chip Power Dissipation: PINT = VDD x (IDD – Σ IOH) I/O Pin Power Dissipation: I/O = Σ ({VDD – VOH} x IOH) + Σ (VOL x IOL)	PD	PINT + PI/O			W
Maximum Allowed Power Dissipation	PDMAX	(TJ – TA)/θJA			W

TABLE 33-3: THERMAL PACKAGING CHARACTERISTICS

Characteristic	Symbol	Typ.	Max.	Unit	Notes
Package Thermal Resistance, 121-Pin BGA	θJA	40	—	°C/W	1
Package Thermal Resistance, 100-Pin TQFP 12x12 mm	θJA	43	—	°C/W	1
Package Thermal Resistance, 100-Pin TQFP 14x14 mm	θJA		—	°C/W	1
Package Thermal Resistance, 64-Pin QFN	θJA	28.0	—	°C/W	1
Package Thermal Resistance, 64-Pin TQFP 10x10 mm	θJA	48.3	—	°C/W	1
Package Thermal Resistance, 44-Pin QFN	θJA	29.0	—	°C/W	1
Package Thermal Resistance, 44-Pin TQFP 10x10 mm	θJA	49.8	—	°C/W	1
Package Thermal Resistance, 44-Pin VTLA 6x6 mm	θJA	25.2	—	°C/W	1
Package Thermal Resistance, 36-Pin VTLA 5x5 mm	θJA	28.5	—	°C/W	1
Package Thermal Resistance, 28-Pin QFN-S	θJA	30.0	—	°C/W	1
Package Thermal Resistance, 28-Pin SSOP	θJA	71.0	—	°C/W	1
Package Thermal Resistance, 28-Pin SOIC	θJA	69.7	—	°C/W	1
Package Thermal Resistance, 28-Pin SPDIP	θJA	60.0	—	°C/W	1

Note 1: Junction to ambient thermal resistance, Theta-JA (θJA) numbers are achieved by package simulations.

FIGURE 33-5: POWER-ON RESET TIMING CHARACTERISTICS



Note 1: The power-up period will be extended if the power-up sequence completes before the device exits from BOR ($V_{DD} < V_{BOR}$).

2: The power-up period includes internal voltage regulator stabilization delay.

TABLE 33-59: ADCx CONVERSION (12-BIT MODE) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions (see Note 2): 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ.(4)**	**Max.**	**Units**	**Conditions**
Clock Parameters							
AD50	TAD	ADCx Clock Period	117.6	—	—	ns	
AD51	tRC	ADCx Internal RC Oscillator Period	—	250	—	ns	
Conversion Rate							
AD55	tCONV	Conversion Time	—	14 TAD		ns	
AD56	FCNV	Throughput Rate	—	—	500	ksps	
AD57a	TSAMP	Sample Time When Sampling Any ANx Input	3 TAD	—	—	—	
AD57b	TSAMP	Sample Time When Sampling the Op Amp Outputs	3 TAD	—	—	—	
Timing Parameters							
AD60	tPCS	Conversion Start from Sample Trigger(1)	2 TAD	—	3 TAD	—	Auto-convert trigger is not selected
AD61	tPSS	Sample Start from Setting Sample (SAMP) bit(1)	2 TAD	—	3 TAD	—	
AD62	tCSS	Conversion Completion to Sample Start (ASAM = 1)(1)	—	0.5 TAD	—	—	
AD63	tDPU	Time to Stabilize Analog Stage from ADCx Off to ADCx On(1)	—	—	20	μs	**(Note 3)**

Note 1: Because the sample caps will eventually lose charge, clock rates below 10 kHz may affect linearity performance, especially at elevated temperatures.

2: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules: ADC, op amp/comparator and comparator voltage reference, will have degraded performance. Refer to Parameter BO10 in Table 33-12 for the minimum and maximum BOR values.

3: The parameter, tDPU, is the time required for the ADCx module to stabilize at the appropriate level when the module is turned on (ADON (AD1CON1<15>) = 1). During this time, the ADCx result is indeterminate.

4: These parameters are characterized, but not tested in manufacturing.

TABLE 33-61: DMA MODULE TIMING REQUIREMENTS

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Characteristic**	**Min.**	**Typ.(1)**	**Max.**	**Units**	**Conditions**
DM1	DMA Byte/Word Transfer Latency	1 TCY(2)	—	—	ns	

Note 1: These parameters are characterized, but not tested in manufacturing.

2: Because DMA transfers use the CPU data bus, this time is dependent on other functions on the bus.

TABLE 34-8: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +150°C				
Param.	**Symbol**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
HDO10	VOL	**Output Low Voltage** 4x Sink Driver Pins(2)	—	—	0.4	V	IOL ≤ 5 mA, VDD = 3.3V **(Note 1)**
		Output Low Voltage 8x Sink Driver Pins(3)	—	—	0.4	V	IOL ≤ 8 mA, VDD = 3.3V **(Note 1)**
HDO20	VOH	**Output High Voltage** 4x Source Driver Pins(2)	2.4	—	—	V	IOH ≥ -10 mA, VDD = 3.3V **(Note 1)**
		Output High Voltage 8x Source Driver Pins(3)	2.4	—	—	V	IOH ≥ 15 mA, VDD = 3.3V **(Note 1)**
HDO20A	VOH1	**Output High Voltage** 4x Source Driver Pins(2)	1.5	—	—	V	IOH ≥ -3.9 mA, VDD = 3.3V **(Note 1)**
			2.0	—	—		IOH ≥ -3.7 mA, VDD = 3.3V **(Note 1)**
			3.0	—	—		IOH ≥ -2 mA, VDD = 3.3V **(Note 1)**
		Output High Voltage 8x Source Driver Pins(3)	1.5	—	—	V	IOH ≥ -7.5 mA, VDD = 3.3V **(Note 1)**
			2.0	—	—		IOH ≥ -6.8 mA, VDD = 3.3V **(Note 1)**
			3.0	—	—		IOH ≥ -3 mA, VDD = 3.3V **(Note 1)**

Note 1: Parameters are characterized, but not tested.

2: Includes all I/O pins that are not 8x Sink Driver pins (see below).

3: Includes the following pins:
For 44-pin devices: RA3, RA4, RA7, RA9, RA10, RB7, RB<15:9>, RC1 and RC<9:3>
For 64-pin devices: RA4, RA7, RA<10:9>, RB7, RB<15:9>, RC1, RC<9:3>, RC15 and RG<8:7>
For 100-pin devices: RA4, RA7, RA9, RA10, RB7, RB<15:9>, RC1, RC<9:3>, RC15, RD<3:1> and RG<8:6>

TABLE 34-9: DC CHARACTERISTICS: PROGRAM MEMORY

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +150°C				
Param.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
		Program Flash Memory					
HD130	EP	Cell Endurance	10,000	—	—	E/W	-40°C to +150°C(2)
HD134	TRETD	Characteristic Retention	20	—	—	Year	1000 E/W cycles or less and no other specifications are violated

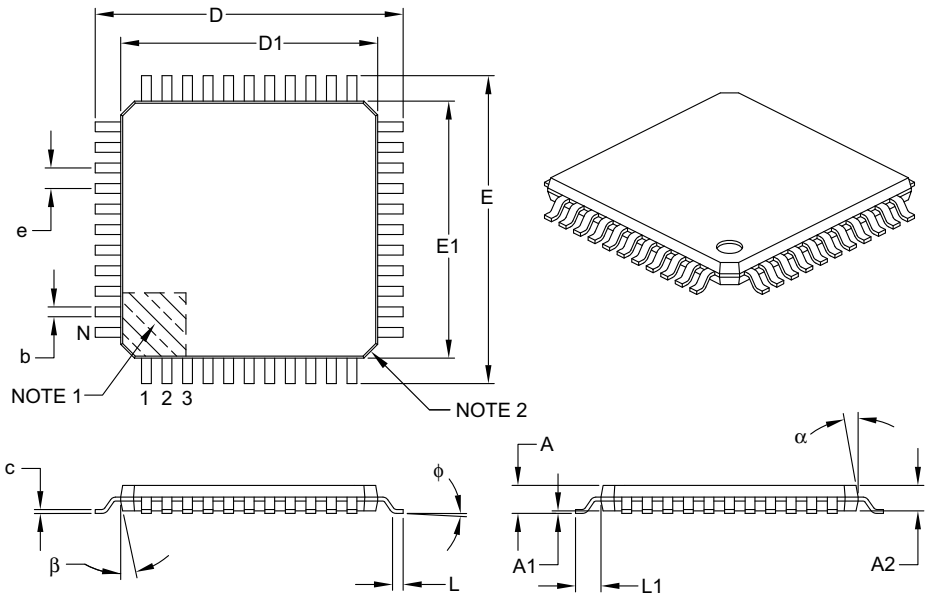
Note 1: These parameters are assured by design, but are not characterized or tested in manufacturing.

2: Programming of the Flash memory is allowed up to +150°C.

35.2 Package Details

44-Lead Plastic Thin Quad Flatpack (PT) – 10x10x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		44	
Lead Pitch	e		0.80 BSC	
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	–	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	φ	0°	3.5°	7°
Overall Width	E		12.00 BSC	
Overall Length	D		12.00 BSC	
Molded Package Width	E1		10.00 BSC	
Molded Package Length	D1		10.00 BSC	
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.30	0.37	0.45
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-076B