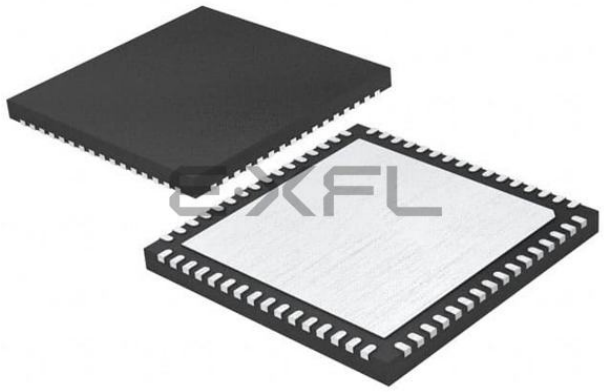

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	I²C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, Motor Control PWM, POR, PWM, WDT
Number of I/O	53
Program Memory Size	512KB (170K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	-
Data Converters	A/D 30x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-VQFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep512gm306t-i-mr

4.2 Data Address Space

The dsPIC33EPXXXGM3XX/6XX/7XX CPU has a separate 16-bit wide data memory space. The Data Space is accessed using separate Address Generation Units (AGUs) for read and write operations. The data memory maps, which are presented by device family and memory size, are shown in Figure 4-5 through Figure 4-7.

All Effective Addresses (EAs) in the data memory space are 16 bits wide and point to bytes within the Data Space. This arrangement gives a Base Data Space address range of 64 Kbytes or 32K words.

The Base Data Space address is used in conjunction with a Data Space Read or Write Page register (DSRPAG or DSWPAG) to form an Extended Data Space, which has a total address range of 16 Mbytes.

dsPIC33EPXXXGM3XX/6XX/7XX devices implement up to 52 Kbytes of data memory (4 Kbytes of data memory for Special Function Registers and up to 48 Kbytes of data memory for RAM). If an EA points to a location outside of this area, an all zero word or byte is returned.

4.2.1 DATA SPACE WIDTH

The data memory space is organized in byte-addressable, 16-bit wide blocks. Data is aligned in data memory and registers as 16-bit words, but all Data Space EAs resolve to bytes. The Least Significant Bytes (LSBs) of each word have even addresses, while the Most Significant Bytes (MSBs) have odd addresses.

4.2.2 DATA MEMORY ORGANIZATION AND ALIGNMENT

To maintain backward compatibility with PIC® MCU devices and improve Data Space memory usage efficiency, the dsPIC33EPXXXGM3XX/6XX/7XX instruction set supports both word and byte operations. As a consequence of byte accessibility, all Effective Address calculations are internally scaled to step through word-aligned memory. For example, the core recognizes that Post-Modified Register Indirect Addressing mode [Ws++] results in a value of Ws + 1 for byte operations and Ws + 2 for word operations.

A data byte read, reads the complete word that contains the byte, using the LSb of any EA to determine which byte to select. The selected byte is placed onto the LSB of the data path. That is, data memory and registers are organized as two parallel, byte-wide entities with shared (word) address decode but separate write lines. Data byte writes only write to the corresponding side of the array or register that matches the byte address.

All word accesses must be aligned to an even address. Misaligned word data fetches are not supported, so care must be taken when mixing byte and word operations, or translating from 8-bit MCU code. If a misaligned read or write is attempted, an address error trap is generated. If the error occurred on a read, the instruction underway is completed. If the error occurred on a write, the instruction is executed but the write does not occur. In either case, a trap is then executed, allowing the system and/or user application to examine the machine state prior to execution of the address Fault.

All byte loads into any W register are loaded into the LSB; the MSB is not modified.

A Sign-Extend (SE) instruction is provided to allow user applications to translate 8-bit signed data to 16-bit signed values. Alternatively, for 16-bit unsigned data, user applications can clear the MSB of any W register by executing a Zero-Extend (ZE) instruction on the appropriate address.

4.2.3 SFR SPACE

The first 4 Kbytes of the Near Data Space, from 0x0000 to 0x0FFF, is primarily occupied by Special Function Registers (SFRs). These are used by the dsPIC33EPXXXGM3XX/6XX/7XX core and peripheral modules for controlling the operation of the device.

SFRs are distributed among the modules that they control and are generally grouped together by module. Much of the SFR space contains unused addresses; these are read as '0'.

Note:	The actual set of peripheral features and interrupts varies by the device. Refer to the corresponding device tables and pinout diagrams for device-specific information.

4.2.4 NEAR DATA SPACE

The 8-Kbyte area, between 0x0000 and 0x1FFF, is referred to as the Near Data Space. Locations in this space are directly addressable through a 13-bit absolute address field within all memory direct instructions. Additionally, the whole Data Space is addressable using MOV instructions, which support Memory Direct Addressing mode with a 16-bit address field, or by using Indirect Addressing mode using a Working register as an Address Pointer.

4.2.5 X AND Y DATA SPACES

The dsPIC33EP core has two Data Spaces: X and Y. These Data Spaces can be considered either separate (for some DSP instructions) or as one unified linear address range (for MCU instructions). The Data Spaces are accessed using two Address Generation Units (AGUs) and separate data paths. This feature allows certain instructions to concurrently fetch two words from RAM, thereby enabling efficient execution of DSP algorithms, such as Finite Impulse Response (FIR) filtering and Fast Fourier Transform (FFT).

The X Data Space is used by all instructions and supports all addressing modes. The X Data Space has separate read and write data buses. The X read data bus is the read data path for all instructions that view Data Space as combined X and Y address space. It is also the X data prefetch path for the dual operand DSP instructions (MAC class).

The Y Data Space is used in concert with the X Data Space by the MAC class of instructions (CLR, ED, EDAC, MAC, MOVSAC, MPY, MPY.N and MSC) to provide two concurrent data read paths.

Both the X and Y Data Spaces support Modulo Addressing mode for all instructions, subject to addressing mode restrictions. Bit-Reversed Addressing mode is only supported for writes to X Data Space.

All data memory writes, including in DSP instructions, view Data Space as combined X and Y address space. The boundary between the X and Y Data Spaces is device-dependent and is not user-programmable.

TABLE 4-8: PWM REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PTCON	0C00	PTEN	—	PTSIDL	SESTAT	SEIEN	EIPU	SYNCPOL	SYNCOEN	SYNCEN	SYNCSRC2	SYNCSRC1	SYNCSRC0	SEVTPS3	SEVTPS2	SEVTPS1	SEVTPS0	0000
PTCON2	0C02	—	—	—	—	—	—	—	—	—	—	—	—	—	PCLKDIV<2:0>			0000
PTPER	0C04	PTPER<15:0>																00F8
SEVTCMP	0C06	SEVTCMP<15:0>																0000
MDC	0C0A	MDC<15:0>																0000
STCON	0C0E	—	—	—	SESTAT	SEIEN	EIPU	SYNCPOL	SYNCOEN	SYNCEN	SYNCSRC2	SYNCSRC1	SYNCSRC0	SEVTPS3	SEVTPS2	SEVTPS1	SEVTPS0	0000
STCON2	0C10	—	—	—	—	—	—	—	—	—	—	—	—	—	PCLKDIV<2:0>			0000
STPER	0C12	STPER<15:0>																0000
SSEVTCMP	0C14	SSEVTCMP<15:0>																0000
CHOP	0C1A	CHPCLKEN	—	—	—	—	—	CHOPCLK9	CHOPCLK8	CHOPCLK7	CHOPCLK6	CHOPCLK5	CHOPCLK4	CHOPCLK3	CHOPCLK2	CHOPCLK1	CHOPCLK0	0000
PWMKEY	0C1E	PWMKEY<15:0>																0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-9: PWM GENERATOR 1 REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PWMCON1	0C20	FLTSTAT	CLSTAT	TRGSTAT	FLTIEN	CLIEN	TRGIEN	ITB	MDCS	DTC1	DTC0	DTCP	—	MTBS	CAM	XPRES	IUE	0000
IOCON1	0C22	PENH	PENL	POLH	POLL	PMOD1	PMOD0	OVRENH	OVRENL	OVRDAT1	OVRDAT0	FLTDAT1	FLTDAT0	CLDAT1	CLDAT0	SWAP	OSYNC	C000
FCLCON1	0C24	IFLTMOD	CLSRC4	CLSRC3	CLSRC2	CLSRC1	CLSRC0	CLPOL	CLMOD	FLTSRC4	FLTSRC3	FLTSRC2	FLTSRC1	FLTSRC0	FLTPOL	FLTMOD1	FLTMOD0	0000
PDC1	0C26	PDC1<15:0>																FFF8
PHASE1	0C28	PHASE1<15:0>																0000
DTR1	0C2A	—	—	DTR1<13:0>														0000
ALTDTR1	0C2C	—	—	ALTDTR1<13:0>														0000
SDC1	0C2E	SDC1<15:0>																0000
SPHASE1	0C30	SPHASE1<15:0>																0000
TRIG1	0C32	TRGCMP<15:0>																0000
TRGCON1	0C34	TRGDIV3	TRGDIV2	TRGDIV1	TRGDIV0	—	—	—	—	—	—	TRGSTRT5	TRGSTRT4	TRGSTRT3	TRGSTRT2	TRGSTRT1	TRGSTRT0	0000
PWMCAP1	0C38	PWMCAP1<15:0>																0000
LEBCON1	0C3A	PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	—	—	—	—	BCH	BCL	BPHH	BPHL	BPLH	BPLL	0000
LEBDLY1	0C3C	—	—	—	—	LEB<11:0>												0000
AUXCON1	0C3E	—	—	—	—	BLANKSEL3	BLANKSEL2	BLANKSEL1	BLANKSEL0	—	—	CHOPSEL3	CHOPSEL2	CHOPSEL1	CHOPSEL0	CHOPHEN	CHOPLEN	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-23: CAN1 REGISTER MAP WHEN WIN (C1CTRL<0>) = 0 OR 1 FOR dsPIC33EPXXXGM60X/7XX DEVICES(1)

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
C1CTRL1	0400	—	—	CSIDL	ABAT	CANCKS	REQOP2	REQOP1	REQOP0	OPMODE2	OPMODE1	OPMODE0	—	CANCAP	—	—	WIN	0480
C1CTRL2	0402	—	—	—	—	—	—	—	—	—	—	—	DNCNT<4:0>					0000
C1VEC	0404	—	—	—	FILHIT4	FILHIT3	FILHIT2	FILHIT1	FILHIT0	—	ICODE6	ICODE5	ICODE4	ICODE3	ICODE2	ICODE1	ICODE0	0040
C1FCTRL	0406	DMABS2	DMABS1	DMABS0	—	—	—	—	—	—	—	—	FSA4	FSA3	FSA2	FSA1	FSA0	0000
C1FIFO	0408	—	—	FBP5	FBP4	FBP3	FBP2	FBP1	FBP0	—	—	FNRB5	FNRB4	FNRB3	FNRB2	FNRB1	FNRB0	0000
C1INTF	040A	—	—	TXBO	TXBP	RXBP	TXWAR	RXWAR	EWARN	IVRIF	WAKIF	ERRIF	—	FIFOIF	RBOVIF	RBIF	TBIF	0000
C1INTE	040C	—	—	—	—	—	—	—	—	IVRIE	WAKIE	ERRIE	—	FIFOIE	RBOVIE	RBIE	TBIE	0000
C1EC	040E	TERRCNT7	TERRCNT6	TERRCNT5	TERRCNT4	TERRCNT3	TERRCNT2	TERRCNT1	TERRCNT0	RERRCNT7	RERRCNT6	RERRCNT5	RERRCNT4	RERRCNT3	RERRCNT2	RERRCNT1	RERRCNT0	0000
C1CFG1	0410	—	—	—	—	—	—	—	—	SJW1	SJW0	BRP5	BRP4	BRP3	BRP2	BRP1	BRP0	0000
C1CFG2	0412	—	WAKFIL	—	—	—	SEG2PH2	SEG2PH1	SEG2PH0	SEG2PHTS	SAM	SEG1PH2	SEG1PH1	SEG1PH0	PRSEG2	PRSEG1	PRSEG0	0000
C1FEN1	0414	FLTEN<15:0>																FFFF
C1FMSKSEL1	0418	F7MSK1	F7MSK0	F6MSK1	F6MSK0	F5MSK1	F5MSK0	F4MSK1	F4MSK0	F3MSK1	F3MSK0	F2MSK1	F2MSK0	F1MSK1	F1MSK0	F0MSK1	F0MSK0	0000
C1FMSKSEL2	041A	F15MSK1	F15MSK0	F14MSK1	F14MSK0	F13MSK1	F13MSK0	F12MSK1	F12MSK0	F11MSK1	F11MSK0	F10MSK1	F10MSK0	F9MSK1	F9MSK0	F8MSK1	F8MSK0	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
Note 1: These registers are not present on dsPIC33EPXXXGM3XX devices.

TABLE 4-24: CAN1 REGISTER MAP WHEN WIN (C1CTRL<0>) = 0 FOR dsPIC33EPXXXGM60X/7XX DEVICES(1)

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
	0400-041E	See definition when WIN = x																
C1RXFUL1	0420	RXFUL<15:0>																0000
C1RXFUL2	0422	RXFUL<31:16>																0000
C1RXOVF1	0428	RXOVF<15:0>																0000
C1RXOVF2	042A	RXOVF<31:16>																0000
C1TR01CON	0430	TXEN1	TXABT1	TXLARB1	TXERR1	TXREQ1	RTREN1	TX1PRI1	TX1PRI0	TXEN0	TXABAT0	TXLARB0	TXERR0	TXREQ0	RTREN0	TX0PRI1	TX0PRI0	0000
C1TR23CON	0432	TXEN3	TXABT3	TXLARB3	TXERR3	TXREQ3	RTREN3	TX3PRI1	TX3PRI0	TXEN2	TXABAT2	TXLARB2	TXERR2	TXREQ2	RTREN2	TX2PRI1	TX2PRI0	0000
C1TR45CON	0434	TXEN5	TXABT5	TXLARB5	TXERR5	TXREQ5	RTREN5	TX5PRI1	TX5PRI0	TXEN4	TXABAT4	TXLARB4	TXERR4	TXREQ4	RTREN4	TX4PRI1	TX4PRI0	0000
C1TR67CON	0436	TXEN7	TXABT7	TXLARB7	TXERR7	TXREQ7	RTREN7	TX7PRI1	TX7PRI0	TXEN6	TXABAT6	TXLARB6	TXERR6	TXREQ6	RTREN6	TX6PRI1	TX6PRI0	xxxx
C1RXD	0440	CAN1 Receive Data Word																xxxx
C1TXD	0442	CAN1 Transmit Data Word																xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.
Note 1: These registers are not present on dsPIC33EPXXXGM3XX devices.

TABLE 4-61: PORTG REGISTER MAP FOR dsPIC33EPXXXGM310/710 DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISG	0E60	TRISG<15:6>										—	—	TRISG<3:0>				03C0
PORTG	0E62	RG<15:6>										—	—	RG<3:0>				xxxx
LATG	0E64	LATG<15:6>										—	—	LATG<3:0>				xxxx
ODCG	0E66	ODCG<15:6>										—	—	ODCG<3:0>				0000
CNENG	0E68	CNIEG<15:6>										—	—	CNIEG<3:0>				0000
CNPUG	0E6A	CNPUG<15:6>										—	—	CNPUG<3:0>				0000
CNPDG	0E6C	CNPDG<15:6>										—	—	CNPDG<3:0>				0000
ANSELG	0E6E	ANSG15	—	—	—	ANSG<11:6>						—	—	ANSG<3:2>		—	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-62: PORTG REGISTER MAP FOR dsPIC33EPXXXGM306/706 DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISG	0E60	—	—	—	—	—	—	TRISG<9:6>				—	—	—	—	—	—	03C0
PORTG	0E62	—	—	—	—	—	—	RG<9:6>				—	—	—	—	—	—	xxxx
LATG	0E64	—	—	—	—	—	—	LATG<9:6>				—	—	—	—	—	—	xxxx
ODCG	0E66	—	—	—	—	—	—	ODCG<9:6>				—	—	—	—	—	—	0000
CNENG	0E68	—	—	—	—	—	—	CNIEG<9:6>				—	—	—	—	—	—	0000
CNPUG	0E6A	—	—	—	—	—	—	CNPUG<9:6>				—	—	—	—	—	—	0000
CNPDG	0E6C	—	—	—	—	—	—	CNPDG<9:6>				—	—	—	—	—	—	0000
ANSELG	0E6E	—	—	—	—	—	—	ANSG<9:6>				—	—	—	—	—	—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-63: PAD CONFIGURATION REGISTER MAP

File Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PADCFG1	0EFE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RTSECSEL	PMPTTL	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

4.5.3 MODULO ADDRESSING APPLICABILITY

Modulo Addressing can be applied to the Effective Address (EA) calculation associated with any W register. Address boundaries check for addresses equal to:

- The upper boundary addresses for incrementing buffers
- The lower boundary addresses for decrementing buffers

It is important to realize that the address boundaries check for addresses less than or greater than the upper (for incrementing buffers) and lower (for decrementing buffers) boundary addresses (not just equal to). Address changes can, therefore, jump beyond boundaries and still be adjusted correctly.

Note:	The modulo corrected Effective Address is written back to the register only when Pre-Modify or Post-Modify Addressing mode is used to compute the Effective Address. When an address offset (such as [W7 + W2]) is used, Modulo Addressing correction is performed, but the contents of the register remain unchanged.

4.6 Bit-Reversed Addressing

Bit-Reversed Addressing mode is intended to simplify data reordering for radix-2 FFT algorithms; it is supported by the X AGU for data writes only.

The modifier, which can be a constant value or register contents, is regarded as having its bit order reversed. The address source and destination are kept in normal order. Thus, the only operand requiring reversal is the modifier.

4.6.1 BIT-REVERSED ADDRESSING IMPLEMENTATION

Bit-Reversed Addressing mode is enabled when all of these conditions are met:

- BWM bits (W register selection) in the MODCON register are any value other than '1111' (the stack cannot be accessed using Bit-Reversed Addressing)
- The BREN bit is set in the XBREV register
- The addressing mode used is Register Indirect with Pre-Increment or Post-Increment

If the length of a bit-reversed buffer is $M = 2^N$ bytes, the last 'N' bits of the data buffer start address must be zeros.

XB<14:0> is the Bit-Reversed Addressing modifier, or 'pivot point', which is typically a constant. In the case of an FFT computation, its value is equal to half of the FFT data buffer size.

Note:	All bit-reversed EA calculations assume word-sized data (LSb of every EA is always clear). The XB value is scaled accordingly to generate compatible (byte) addresses.

When enabled, Bit-Reversed Addressing is executed only for Register Indirect with Pre-Increment or Post-Increment Addressing and word-sized data writes. It does not function for any other addressing mode or for byte-sized data and normal addresses are generated instead. When Bit-Reversed Addressing is active, the W Address Pointer is always added to the address modifier (XB) and the offset associated with the Register Indirect Addressing mode is ignored. In addition, as word-sized data is a requirement, the LSb of the EA is ignored (and always clear).

Note:	Modulo Addressing and Bit-Reversed Addressing can be enabled simultaneously using the same W register, but Bit-Reversed Addressing operation will always take precedence for data writes when enabled.

If Bit-Reversed Addressing has already been enabled by setting the BREN (XBREV<15>) bit, a write to the XBREV register should not be immediately followed by an indirect read operation using the W register that has been designated as the Bit-Reversed Pointer.

REGISTER 6-1: RCON: RESET CONTROL REGISTER(1) (CONTINUED)

bit 3 **SLEEP:** Wake-up from Sleep Flag bit
1 = Device was in Sleep mode
0 = Device was not in Sleep mode

bit 2 **IDLE:** Wake-up from Idle Flag bit
1 = Device was in Idle mode
0 = Device was not in Idle mode

bit 1 **BOR:** Brown-out Reset Flag bit
1 = A Brown-out Reset has occurred
0 = A Brown-out Reset has not occurred

bit 0 **POR:** Power-on Reset Flag bit
1 = A Power-on Reset has occurred
0 = A Power-on Reset has not occurred

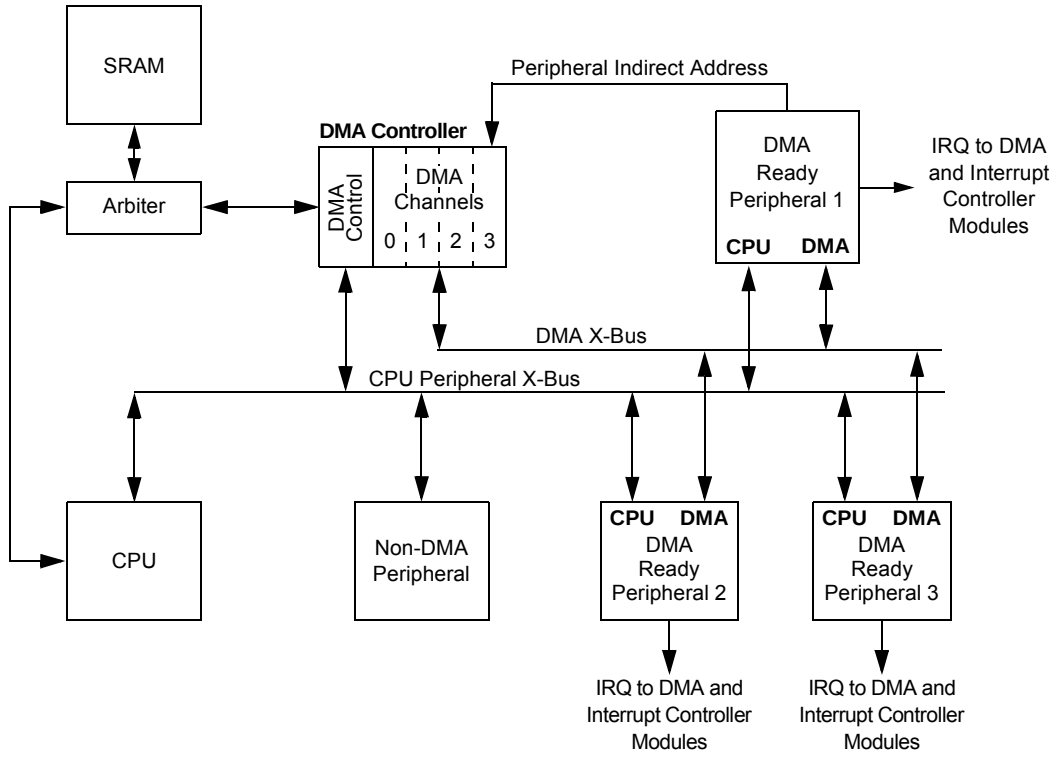
Note 1: All of the Reset status bits can be set or cleared in software. Setting one of these bits in software does not cause a device Reset.

2: If the FWDTEN Configuration bit is '1' (unprogrammed), the WDT is always enabled, regardless of the SWDTEN bit setting.

TABLE 8-1: DMA CHANNEL TO PERIPHERAL ASSOCIATIONS (CONTINUED)

Peripheral to DMA Association	DMAxREQ Register IRQSEL<7:0> Bits	DMAxPAD Register (Values to Read from Peripheral)	DMAxPAD Register (Values to Write to Peripheral)
CAN1 – RX Data Ready	00100010	0x0440 (C1RXD)	—
CAN1 – TX Data Request	01000110	—	0x0442 (C1TXD)
CAN2 – RX Data Ready	00110111	0X0540(C2RXD)	—
CAN2 – TX Data Request	01000111	—	0X0542(C2TXD)
DCI – Codec Transfer Done	00111100	0X0290(RXBUF0)	0X0298(TXBUF0)
ADC1 – ADC1 Convert Done	00001101	0x0300 (ADC1BUF0)	—
ADC2 – ADC2 Convert Done	00010101	0X0340(ADC2BUF0)	—
PMP – PMP Data Move	00101101	0X0608(PMPDAT1)	0X0608(PMPDAT1)

FIGURE 8-2: DMA CONTROLLER BLOCK DIAGRAM



Note: CPU and DMA address buses are not shown for clarity.

REGISTER 9-2: CLKDIV: CLOCK DIVISOR REGISTER(2) (CONTINUED)

bit 4-0 **PLLPRE<4:0>:** PLL Phase Detector Input Divider Select bits (also denoted as 'N1', PLL prescaler)
11111 = Input divided by 33
•
•
•
00001 = Input divided by 3
00000 = Input divided by 2 (default)

Note 1: This bit is cleared when the ROI bit is set and an interrupt occurs.

2: This register resets only on a Power-on Reset (POR).

3: The DOZE<2:0> bits can only be written to when the DOZEN bit is clear. If DOZEN = 1, any writes to DOZE<2:0> are ignored.

4: The DOZEN bit cannot be set if DOZE<2:0> = 000. If DOZE<2:0> = 000, any attempt by user software to set the DOZEN bit is ignored.

REGISTER 10-3: PMD3: PERIPHERAL MODULE DISABLE CONTROL REGISTER 3

R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
T9MD	T8MD	T7MD	T6MD	—	CMPMD	RTCCMD(1)	PMPMD
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CRCMD	DACMD	QEI2MD	PWM2MD	U3MD	I2C3MD	I2C2MD	ADC2MD
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **T9MD:** Timer9 Module Disable bit
1 = Timer9 module is disabled
0 = Timer9 module is enabled

bit 13 **T8MD:** Timer8 Module Disable bit
1 = Timer8 module is disabled
0 = Timer8 module is enabled

bit 14 **T7MD:** Timer7 Module Disable bit
1 = Timer7 module is disabled
0 = Timer7 module is enabled

bit 12 **T6MD:** Timer6 Module Disable bit
1 = Timer6 module is disabled
0 = Timer6 module is enabled

bit 11 **Unimplemented:** Read as ‘0’

bit 10 **CMPMD:** Comparator Module Disable bit
1 = Comparator module is disabled
0 = Comparator module is enabled

bit 9 **RTCCMD:** RTCC Module Disable bit(1)
1 = RTCC module is disabled
0 = RTCC module is enabled

bit 8 **PMPMD:** PMP Module Disable bit
1 = PMP module is disabled
0 = PMP module is enabled

bit 7 **CRCMD:** CRC Module Disable bit
1 = CRC module is disabled
0 = CRC module is enabled

bit 6 **DACMD:** DAC Module Disable bit
1 = DAC module is disabled
0 = DAC module is enabled

bit 5 **QEI2MD:** QEI2 Module Disable bit
1 = QEI2 module is disabled
0 = QEI2 module is enabled

bit 4 **PWM2MD:** PWM2 Module Disable bit
1 = PWM2 module is disabled
0 = PWM2 module is enabled

Note 1: The RTCCMD bit is not available on 44-pin devices.

TABLE 11-3: OUTPUT SELECTION FOR REMAPPABLE PINS (RPn)

Function	RPnR<5:0>	Output Name
Default Port	000000	RPn tied to Default Pin
U1TX	000001	RPn tied to UART1 Transmit
U2TX	000011	RPn tied to UART2 Transmit
SDO2	001000	RPn tied to SPI2 Data Output
SCK2	001001	RPn tied to SPI2 Clock Output
$\overline{SS2}$	001010	RPn tied to SPI2 Slave Select
CSDO	001011	RPn tied to DCI Data Output
CSCK	001100	RPn tied to DCI Clock Output
COFS	001101	RPn tied to DCI Frame Sync
C1TX	001110	RPn tied to CAN1 Transmit
C2TX	001111	RPn tied to CAN2 Transmit
OC1	010000	RPn tied to Output Compare 1 Output
OC2	010001	RPn tied to Output Compare 2 Output
OC3	010010	RPn tied to Output Compare 3 Output
OC4	010011	RPn tied to Output Compare 4 Output
OC5	010100	RPn tied to Output Compare 5 Output
OC6	010101	RPn tied to Output Compare 6 Output
OC7	010110	RPn tied to Output Compare 7 Output
OC8	010111	RPn tied to Output Compare 8 Output
C1OUT	011000	RPn tied to Comparator Output 1
C2OUT	011001	RPn tied to Comparator Output 2
C3OUT	011010	RPn tied to Comparator Output 3
U3TX	011011	RPn tied to UART3 Transmit
$\overline{U3RTS}$	011100	RPn tied to UART3 Ready-to-Send
U4TX	011101	RPn tied to UART4 Transmit
$\overline{U4RTS}$	011110	RPn tied to UART4 Ready-to-Send
SDO3	011111	RPn tied to SPI3 Slave Output
SCK3	100000	RPn tied to SPI3 Clock Output
$\overline{SS3}$	100001	RPn tied to SPI3 Slave Select
SYNCO1	101101	RPn tied to PWM Primary Time Base Sync Output
SYNCO2	101110	RPn tied to PWM Secondary Time Base Sync Output
QEI1CCMP	101111	RPn tied to QEI1 Counter Comparator Output
QEI2CCMP	110000	RPn tied to QEI2 Counter Comparator Output
REFCLKO	110001	RPn tied to Reference Clock Output
C4OUT	110010	RPn tied to Comparator Output 4
C5OUT	110011	RPn tied to Comparator Output 5

REGISTER 11-3: RPINR3: PERIPHERAL PIN SELECT INPUT REGISTER 3

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	T2CKR<6:0>						
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-7 **Unimplemented:** Read as ‘0’

bit 6-0 **T2CKR<6:0>:** Assign Timer2 External Clock (T2CK) to the Corresponding RPn pin bits (see Table 11-2 for input pin selection numbers)

1111100 = Input tied to RPI124
•
•
•
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

REGISTER 11-40: RPOR10: PERIPHERAL PIN SELECT OUTPUT REGISTER 10(1)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP118R<5:0>					
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP113R<5:0>					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP118R<5:0>:** Peripheral Output Function is Assigned to RP118 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP113R<5:0>:** Peripheral Output Function is Assigned to RP113 Output Pin bits (see Table 11-3 for peripheral function numbers)

Note 1: This register is not available on dsPIC33EPXXXGM30X/604/706 devices.

REGISTER 11-41: RPOR11: PERIPHERAL PIN SELECT OUTPUT REGISTER 11(1)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP125R<5:0>					
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP120R<5:0>					
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **RP125R<5:0>:** Peripheral Output Function is Assigned to RP125 Output Pin bits (see Table 11-3 for peripheral function numbers)

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **RP120R<5:0>:** Peripheral Output Function is Assigned to RP120 Output Pin bits (see Table 11-3 for peripheral function numbers)

Note 1: This register is not available on dsPIC33EPXXXGM30X/604/706 devices.

21.3 CAN Control Registers

REGISTER 21-1: CxCTRL1: CANx CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-0
—	—	CSIDL	ABAT	CANCKS	REQOP2	REQOP1	REQOP0
bit 15							bit 8

R-1	R-0	R-0	U-0	R/W-0	U-0	U-0	R/W-0
OPMODE2	OPMODE1	OPMODE0	—	CANCAP	—	—	WIN
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13 **CSIDL:** CANx Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12 **ABAT:** Abort All Pending Transmissions bit
1 = Signals all transmit buffers to abort transmission
0 = Module will clear this bit when all transmissions are aborted

bit 11 **CANCKS:** CANx Module Clock (FCAN) Source Select bit
1 = FCAN is equal to 2 * FP
0 = FCAN is equal to FP

bit 10-8 **REQOP<2:0>:** Request Operation Mode bits
111 = Set Listen All Messages mode
110 = Reserved
101 = Reserved
100 = Set Configuration mode
011 = Set Listen Only mode
010 = Set Loopback mode
001 = Set Disable mode
000 = Set Normal Operation mode

bit 7-5 **OPMODE<2:0>**: Operation Mode bits
111 = Module is in Listen All Messages mode
110 = Reserved
101 = Reserved
100 = Module is in Configuration mode
011 = Module is in Listen Only mode
010 = Module is in Loopback mode
001 = Module is in Disable mode
000 = Module is in Normal Operation mode

bit 4 **Unimplemented:** Read as '0'

bit 3 **CANCAP:** CANx Message Receive Timer Capture Event Enable bit
1 = Enables input capture based on CAN message receive
0 = Disables CAN capture

bit 2-1 **Unimplemented:** Read as '0'

bit 0 **WIN:** SFR Map Window Select bit
1 = Uses filter window
0 = Uses buffer window

BUFFER 21-5: CANx MESSAGE BUFFER WORD 4

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Byte 3<15:8>							
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Byte 2<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Byte 3<15:8>:** CANx Message Byte 3

bit 7-0 **Byte 2<7:0>:** CANx Message Byte 2

BUFFER 21-6: CANx MESSAGE BUFFER WORD 5

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Byte 5<15:8>							
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
Byte 4<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **Byte 5<15:8>:** CANx Message Byte 5

bit 7-0 **Byte 4<7:0>:** CANx Message Byte 4

REGISTER 22-2: CTMUCON2: CTMU CONTROL REGISTER 2

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
EDG1MOD	EDG1POL	EDG1SEL3	EDG1SEL2	EDG1SEL1	EDG1SEL0	EDG2STAT	EDG1STAT
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
EDG2MOD	EDG2POL	EDG2SEL3	EDG2SEL2	EDG2SEL1	EDG2SEL0	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **EDG1MOD:** Edge 1 Edge Sampling Mode Selection bit
1 = Edge 1 is edge-sensitive
0 = Edge 1 is level-sensitive

bit 14 **EDG1POL:** Edge 1 Polarity Select bit
1 = Edge 1 is programmed for a positive edge response
0 = Edge 1 is programmed for a negative edge response

bit 13-10 **EDG1SEL<3:0>:** Edge 1 Source Select bits
1111 = FOSC
1110 = OSCI pin
1101 = FRC oscillator
1100 = Reserved
1011 = Internal LPRC oscillator
1010 = Reserved
100x = Reserved
01xx = Reserved
0011 = CTED1 pin
0010 = CTED2 pin
0001 = OC1 module
0000 = Timer1 module

bit 9 **EDG2STAT:** Edge 2 Status bit
Indicates the status of Edge 2 and can be written to control the edge source.
1 = Edge 2 has occurred
0 = Edge 2 has not occurred

bit 8 **EDG1STAT:** Edge 1 Status bit
Indicates the status of Edge 1 and can be written to control the edge source.
1 = Edge 1 has occurred
0 = Edge 1 has not occurred

bit 7 **EDG2MOD:** Edge 2 Edge Sampling Mode Selection bit
1 = Edge 2 is edge-sensitive
0 = Edge 2 is level-sensitive

bit 6 **EDG2POL:** Edge 2 Polarity Select bit
1 = Edge 2 is programmed for a positive edge response
0 = Edge 2 is programmed for a negative edge response

Note 1: If the TGEN bit is set to ‘1’, then the CMP1 module should be selected as the Edge 2 source in the EDG2SELx bits field; otherwise, the module will not function.

REGISTER 22-3: CTMUICON: CTMU CURRENT CONTROL REGISTER(3)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ITRIM5	ITRIM4	ITRIM3	ITRIM2	ITRIM1	ITRIM0	IRNG1	IRNG0
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-10 **ITRIM<5:0>:** Current Source Trim bits
011111 = Maximum positive change from nominal current + 62%
011110 = Maximum positive change from nominal current + 60%
•
•
•
000010 = Minimum positive change from nominal current + 4%
000001 = Minimum positive change from nominal current + 2%
000000 = Nominal current output specified by IRNG<1:0>
111111 = Minimum negative change from nominal current – 2%
111110 = Minimum negative change from nominal current – 4%
•
•
•
100010 = Maximum negative change from nominal current – 60%
100001 = Maximum negative change from nominal current – 62%

bit 9-8 **IRNG<1:0>:** Current Source Range Select bits
11 = 100 × Base Current(2)
10 = 10 × Base Current(2)
01 = Base Current Level(2)
00 = 1000 × Base Current(1,2)

bit 7-0 **Unimplemented:** Read as '0'

Note 1: This current range is not available for use with the internal temperature measurement diode.

2: Refer to the CTMU Current Source Specifications (Table 33-55) in **Section 33.0 "Electrical Characteristics"** for the current range selection values.

3: Current sources are not generated when 12-Bit ADC mode is chosen. Current sources are active only when 10-Bit ADC mode is chosen.

REGISTER 25-12: PTGQPTR: PTG STEP QUEUE POINTER REGISTER(1)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	PTGQPTR<4:0>				
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-5 **Unimplemented:** Read as '0'

bit 4-0 **PTGQPTR<4:0>:** PTG Step Queue Pointer Register bits
This register points to the currently active Step command in the step queue.

Note 1: This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

REGISTER 25-13: PTGQUEx: PTG STEP QUEUE REGISTER x (x = 0-15)(1,3)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STEP(2x + 1)<7:0>(2)							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STEP(2x)<7:0>(2)							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **STEP(2x + 1)<7:0>:** PTG Step Queue Pointer Register bits(2)
A queue location for storage of the STEP(2x +1) command byte.

bit 7-0 **STEP(2x)<7:0>:** PTG Step Queue Pointer Register bits(2)
A queue location for storage of the STEP(2x) command byte.

Note 1: This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

2: Refer to Table 25-1 for the Step command encoding.

3: The Step registers maintain their values on any type of Reset.

REGISTER 28-5: PMSTAT: PARALLEL MASTER PORT STATUS REGISTER (SLAVE MODE ONLY)(1)

R-0	R/W-0, HS	U-0	U-0	R-0	R-0	R-0	R-0
IBF	IBOV	—	—	IB3F	IB2F	IB1F	IB0F
bit 15							bit 8

R-1	R/W-0, HS	U-0	U-0	R-1	R-1	R-1	R-1
OBE	OBUF	—	—	OB3E	OB2E	OB1E	OB0E
bit 7							bit 0

Legend:	HS = Hardware Settable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at Reset	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **IBF:** Input Buffer Full Status bit
1 = All writable Input Buffer registers are full
0 = Some or all of the writable Input Buffer registers are empty

bit 14 **IBOV:** Input Buffer Overflow Status bit
1 = A write attempt to a full Input Byte register occurred (must be cleared in software)
0 = No overflow occurred

bit 13-12 **Unimplemented:** Read as '0'

bit 11-8 **IB3F:IB0F:** Input Buffer x Status Full bit
1 = Input Buffer x contains data that has not been read (reading buffer will clear this bit)
0 = Input Buffer x does not contain any unread data

bit 7 **OBE:** Output Buffer Empty Status bit
1 = All readable Output Buffer registers are empty
0 = Some or all of the readable Output Buffer registers are full

bit 6 **OBUF:** Output Buffer Underflow Status bit
1 = A read occurred from an empty Output Byte register (must be cleared in software)
0 = No underflow occurred

bit 5-4 **Unimplemented:** Read as '0'

bit 3-0 **OB3E:OB0E:** Output Buffer x Status Empty bit
1 = Output Buffer x is empty (writing data to the buffer will clear this bit)
0 = Output Buffer x contains data that has not been transmitted

Note 1: This register is not available on 44-pin devices.