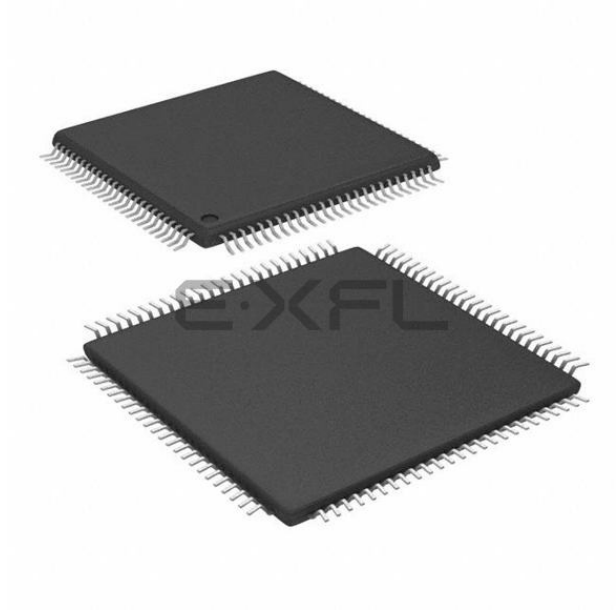
Microchip Technology - DSPIC33EP512GM310-H/PT Datasheet



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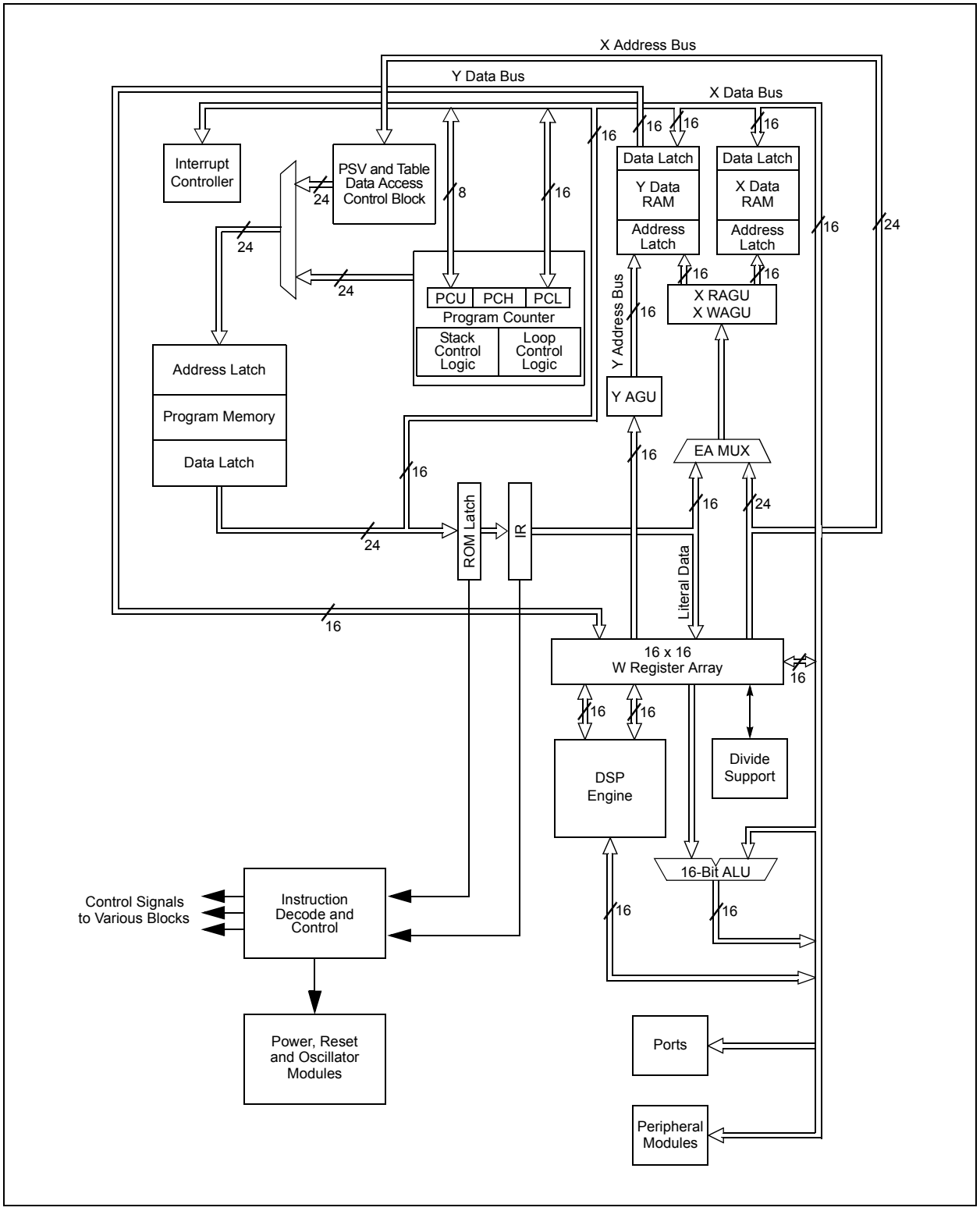
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	-
Connectivity	I²C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, Motor Control PWM, POR, PWM, WDT
Number of I/O	85
Program Memory Size	512KB (170K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	-
Data Converters	A/D 49x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep512gm310-h-pt

FIGURE 3-1: dsPIC33EPXXXGM3XX/6XX/7XX CPU BLOCK DIAGRAM



NOTES:

4.2.5 X AND Y DATA SPACES

The dsPIC33EP core has two Data Spaces: X and Y. These Data Spaces can be considered either separate (for some DSP instructions) or as one unified linear address range (for MCU instructions). The Data Spaces are accessed using two Address Generation Units (AGUs) and separate data paths. This feature allows certain instructions to concurrently fetch two words from RAM, thereby enabling efficient execution of DSP algorithms, such as Finite Impulse Response (FIR) filtering and Fast Fourier Transform (FFT).

The X Data Space is used by all instructions and supports all addressing modes. The X Data Space has separate read and write data buses. The X read data bus is the read data path for all instructions that view Data Space as combined X and Y address space. It is also the X data prefetch path for the dual operand DSP instructions (MAC class).

The Y Data Space is used in concert with the X Data Space by the MAC class of instructions (CLR, ED, EDAC, MAC, MOVSAC, MPY, MPY.N and MSC) to provide two concurrent data read paths.

Both the X and Y Data Spaces support Modulo Addressing mode for all instructions, subject to addressing mode restrictions. Bit-Reversed Addressing mode is only supported for writes to X Data Space.

All data memory writes, including in DSP instructions, view Data Space as combined X and Y address space. The boundary between the X and Y Data Spaces is device-dependent and is not user-programmable.

TABLE 4-27: CAN2 REGISTER MAP WHEN WIN (C1CTRL<0>) = 0 FOR dsPIC33EPXXXGM60X/7XX DEVICES(1)

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
	0500-051E	See definition when WIN = x																
C2RXFUL1	0520	RXFUL<15:0>																0000
C2RXFUL2	0522	RXFUL<31:16>																0000
C2RXOVF1	0528	RXOVF<15:0>																0000
C2RXOVF2	052A	RXOVF<31:16>																0000
C2TR01CON	0530	TXEN1	TXABT1	TXLARB1	TXERR1	TXREQ1	RTREN1	TX1PRI1	TX1PRI0	TXEN0	TXABAT0	TXLARB0	TXERR0	TXREQ0	RTREN0	TX0PRI1	TX0PRI0	0000
C2TR23CON	0532	TXEN3	TXABT3	TXLARB3	TXERR3	TXREQ3	RTREN3	TX3PRI1	TX3PRI0	TXEN2	TXABAT2	TXLARB2	TXERR2	TXREQ2	RTREN2	TX2PRI1	TX2PRI0	0000
C2TR45CON	0534	TXEN5	TXABT5	TXLARB5	TXERR5	TXREQ5	RTREN5	TX5PRI1	TX5PRI0	TXEN4	TXABAT4	TXLARB4	TXERR4	TXREQ4	RTREN4	TX4PRI1	TX4PRI0	0000
C2TR67CON	0536	TXEN7	TXABT7	TXLARB7	TXERR7	TXREQ7	RTREN7	TX7PRI1	TX7PRI0	TXEN6	TXABAT6	TXLARB6	TXERR6	TXREQ6	RTREN6	TX6PRI1	TX6PRI0	xxxx
C2RXD	0540	CAN2 Receive Data Word Register																xxxx
C2TXD	0542	CAN2 Transmit Data Word Register																xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: These registers are not present on dsPIC33EPXXXGM3XX devices.

TABLE 4-38: PARALLEL MASTER/SLAVE PORT REGISTER MAP(2)

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PMCON	0600	PMPEN	—	PSIDL	ADRMUX1	ADRMUX0	PTBEEN	PTWREN	PTRDEN	CSF1	CSF0	ALP	CS2P	CS1P	BEP	WRSP	RDSP	0000
PMMODE	0602	BUSY	IRQM1	IRQM0	INCM1	INCM0	MODE16	MODE1	MODE0	WAITB1	WAITB0	WAITM3	WAITM2	WAITM1	WAITM0	WAITE1	WAITE0	0000
PMADDR(1)	0604	CS2	CS1	Parallel Port Address Register (ADDR<13:0>)														0000
PMDOUT1(1)	0604	Parallel Port Data Out Register 1 (Buffer Levels 0 and 1)																0000
PMDOUT2	0606	Parallel Port Data Out Register 2 (Buffer Levels 2 and 3)																0000
PMDIN1	0608	Parallel Port Data In Register 1 (Buffer Levels 0 and 1)																0000
PMDIN2	060A	Parallel Port Data In Register 2 (Buffer Levels 2 and 3)																0000
PMAEN	060C	PTEN<15:0>																0000
PMSTAT	060E	IBF	IBOV	—	—	IB3F	IB2F	IB1F	IB0F	OBE	OBUF	—	—	OB3E	OB2E	OB1E	OB0E	008F

Legend: — = unimplemented, read as '0'. Shaded bits are not used in the operation of the PMP module.

Note 1: PMADDR and PMDOUT1 are the same physical register, but are defined differently depending on the module's operating mode.

2: PMP is not present on 44-pin devices.

TABLE 4-39: PMD REGISTER MAP FOR dsPIC33EPXXXGM6XX/7XX DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PMD1	0760	T5MD	T4MD	T3MD	T2MD	T1MD	QEIMD	PWMMD	DCIMD	I2C1MD	U2MD	U1MD	SPI2MD	SPI1MD	C2MD	C1MD	AD1MD	0000
PMD2	0762	IC8MD	IC7MD	IC6MD	IC5MD	IC4MD	IC3MD	IC2MD	IC1MD	OC8MD	OC7MD	OC6MD	OC5MD	OC4MD	OC3MD	OC2MD	OC1MD	0000
PMD3	0764	T9MD	T8MD	T7MD	T6MD	—	CMPMD	RTCCMD(1)	PMPMD	CRCMD	DACMD	QEI2MD	PWM2MD	U3MD	I2C3MD	I2C2MD	ADC2MD	0000
PMD4	0766	—	—	—	—	—	—	—	—	—	—	U4MD	—	REFOMD	CTMUMD	—	—	0000
PMD6	076A	—	—	PWM6MD	PWM5MD	PWM4MD	PWM3MD	PWM2MD	PWM1MD	—	—	—	—	—	—	—	SPI3MD	0000
PMD7	076C	—	—	—	—	—	—	—	—	—	—	—	DMA0MD DMA1MD DMA2MD DMA3MD	PTGMD	—	—	—	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: The RTCCMD bit is not available on 44-pin devices.

REGISTER 8-9: DSADRH: DMA MOST RECENT RAM HIGH ADDRESS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
DSADR<23:16>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-8 **Unimplemented:** Read as ‘0’

bit 7-0 **DSADR<23:16>:** Most Recent DMA Address Accessed by DMA bits

REGISTER 8-10: DSADRL: DMA MOST RECENT RAM LOW ADDRESS REGISTER

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
DSADR<15:8>							
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
DSADR<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **DSADR<15:0>:** Most Recent DMA Address Accessed by DMA bits

10.3 Doze Mode

The preferred strategies for reducing power consumption are changing clock speed and invoking one of the power-saving modes. In some circumstances, this cannot be practical. For example, it may be necessary for an application to maintain uninterrupted synchronous communication, even while it is doing nothing else. Reducing system clock speed can introduce communication errors, while using a power-saving mode can stop communications completely.

Doze mode is a simple and effective alternative method to reduce power consumption while the device is still executing code. In this mode, the system clock continues to operate from the same source and at the same speed. Peripheral modules continue to be clocked at the same speed, while the CPU clock speed is reduced. Synchronization between the two clock domains is maintained, allowing the peripherals to access the SFRs while the CPU executes code at a slower rate.

Doze mode is enabled by setting the DOZEN bit (CLKDIV<11>). The ratio between peripheral and core clock speed is determined by the DOZE<2:0> bits (CLKDIV<14:12>). There are eight possible configurations, from 1:1 to 1:128, with 1:1 being the default setting.

Programs can use Doze mode to selectively reduce power consumption in event-driven applications. This allows clock-sensitive functions, such as synchronous communications, to continue without interruption while the CPU Idles, waiting for something to invoke an interrupt routine. An automatic return to full-speed CPU operation on interrupts can be enabled by setting the ROI bit (CLKDIV<15>). By default, interrupt events have no effect on Doze mode operation.

For example, suppose the device is operating at 20 MIPS and the CAN module has been configured for 500 kbps based on this device operating speed. If the device is placed in Doze mode with a clock frequency ratio of 1:4, the CAN module continues to communicate at the required bit rate of 500 kbps, but the CPU now starts executing instructions at a frequency of 5 MIPS.

10.4 Peripheral Module Disable

The Peripheral Module Disable (PMD) registers provide a method to disable a peripheral module by stopping all clock sources supplied to that module. When a peripheral is disabled, using the appropriate PMD control bit, the peripheral is in a minimum power consumption state. The control and status registers associated with the peripheral are also disabled, so writes to those registers do not have effect and read values are invalid.

A peripheral module is enabled only if both the associated bit in the PMD register is cleared and the peripheral is supported by the specific dsPIC® DSC variant. If the peripheral is present in the device, it is enabled in the PMD register by default.

Note:	If a PMD bit is set, the corresponding module is disabled after a delay of one instruction cycle. Similarly, if a PMD bit is cleared, the corresponding module is enabled after a delay of one instruction cycle (assuming the module control registers are already configured to enable module operation).

REGISTER 15-1: OCxCON1: OUTPUT COMPARE x CONTROL REGISTER 1 (CONTINUED)

bit 3 **TRIGMODE:** Trigger Status Mode Select bit
1 = TRIGSTAT (OCxCON2<6>) is cleared when OCxRS = OCxTMR or in software
0 = TRIGSTAT is cleared only by software

bit 2-0 **OCM<2:0>:** Output Compare x Mode Select bits
111 = Center-Aligned PWM mode: Output sets high when OCxTMR = OCxR and sets low when OCxTMR = OCxRS(1)
110 = Edge-Aligned PWM mode: Output sets high when OCxTMR = 0 and sets low when OCxTMR = OCxR(1)
101 = Double Compare Continuous Pulse mode: Initializes OCx pin low, toggles OCx state continuously on alternate matches of OCxR and OCxRS
100 = Double Compare Single-Shot mode: Initializes OCx pin low, toggles OCx state on matches of OCxR and OCxRS for one cycle
011 = Single Compare mode: Compare event with OCxR, continuously toggles OCx pin
010 = Single Compare Single-Shot mode: Initializes OCx pin high, compare event with OCxR, forces OCx pin low
001 = Single Compare Single-Shot mode: Initializes OCx pin low, compare event with OCxR, forces OCx pin high
000 = Output compare channel is disabled

Note 1: OCxR and OCxRS are double-buffered in PWM mode only.

2: Each Output Compare x module (OCx) has one PTG clock source. See **Section 25.0 "Peripheral Trigger Generator (PTG) Module"** for more information.
PTGO4 = OC1, OC5
PTGO5 = OC2, OC6
PTGO6 = OC3, OC7
PTGO7 = OC4, OC8

REGISTER 16-14: PHASEx: PWMx PRIMARY PHASE-SHIFT REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PHASEx<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PHASEx<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **PHASEx<15:0>:** Phase-Shift Value or Independent Time Base Period for the PWMx Generator bits

Note 1: If ITB (PWMCONx<9>) = 0, the following applies based on the mode of operation:
Complementary, Redundant and Push-Pull Output mode (PMOD<1:0> (IOCONx<11:10>) = 00, 01 or 10), PHASEx<15:0> = Phase-shift value for PWMxH and PWMxL outputs.

2: If ITB (PWMCONx<9>) = 1, the following applies based on the mode of operation:
Complementary, Redundant and Push-Pull Output mode (PMOD<1:0> (IOCONx<11:10>) = 00, 01 or 10), PHASEx<15:0> = Independent Time Base Period Value for PWMxH and PWMxL.

REGISTER 16-15: SPHASEx: PWMx SECONDARY PHASE-SHIFT REGISTER(1,2)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SPHASEx<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SPHASEx<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **SPHASEx<15:0>:** Secondary Phase Offset for PWMxL Output Pin bits
(used in Independent PWM mode only)

Note 1: If ITB (PWMCONx<9>) = 0, the following applies based on the mode of operation:
- Complementary, Redundant and Push-Pull Output mode (PMOD<1:0> (IOCONx<11:10>) = 00, 01 or 10), SPHASEx<15:0> = Not used.
- True Independent Output mode (PMOD<1:0> (IOCONx<11:10>) = 11), SPHASEx<15:0> = Phase-Shift Value for PWMxL only.

2: If ITB (PWMCONx<9>) = 1, the following applies based on the mode of operation:
- Complementary, Redundant and Push-Pull Output mode (PMOD<1:0> (IOCONx<11:10>) = 00, 01 or 10), SPHASEx<15:0> = Not used.
- True Independent Output mode (PMOD<1:0> (IOCONx<11:10>) = 11), SPHASEx<15:0> = Independent Time Base Period Value for PWMxL only.

REGISTER 16-19: IOCONx: PWMx I/O CONTROL REGISTER(2) (CONTINUED)

bit 1 **SWAP:** SWAP PWMxH and PWMxL Pins bit
1 = PWMxH output signal is connected to the PWMxL pins; PWMxL output signal is connected to the PWMxH pins
0 = PWMxH and PWMxL pins are mapped to their respective pins

bit 0 **OSYNC:** Output Override Synchronization bit
1 = Output overrides via the OVRDAT<1:0> bits are synchronized to the PWM time base
0 = Output overrides via the OVDDAT<1:0> bits occur on the next CPU clock boundary

Note 1: These bits should not be changed after the PWMx module is enabled (PTEN = 1).
2: If the PWMLOCK Configuration bit (FOSCSEL<6>) is a '1', the IOCONx register can only be written after the unlock sequence has been executed.

REGISTER 16-20: TRIGx: PWMx PRIMARY TRIGGER COMPARE VALUE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TRGCMP<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TRGCMP<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **TRGCMP<15:0>:** Trigger Control Value bits
When the primary PWMx functions in the local time base, this register contains the compare values that can trigger the ADCx module.

22.0 CHARGE TIME MEASUREMENT UNIT (CTMU)

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGM3XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"Charge Time Measurement Unit (CTMU)"** (DS70661), which is available on the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The Charge Time Measurement Unit is a flexible analog module that provides accurate differential time measurement between pulse sources, as well as asynchronous pulse generation. Its key features include:

- Four edge input trigger sources
- Polarity control for each edge source
- Control of edge sequence
- Control of response to edges
- Precise time measurement resolution of 1 ns
- Accurate current source suitable for capacitive measurement
- On-chip temperature measurement using a built-in diode

Together with other on-chip analog modules, the CTMU can be used to precisely measure time, measure capacitance, measure relative changes in capacitance or generate output pulses that are independent of the system clock.

The CTMU module is ideal for interfacing with capacitive-based sensors. The CTMU is controlled through three registers: CTMUCON1, CTMUCON2 and CTMUICON. CTMUCON1 and CTMUCON2 enable the module and control edge source selection, edge source polarity selection and edge sequencing. The CTMUICON register controls the selection and trim of the current source.

REGISTER 23-1: ADxCON1: ADCx CONTROL REGISTER 1 (CONTINUED)

bit 7-5 **SSRC<2:0>:** Sample Clock Source Select bits

If SSRCG = 1:

111 = Reserved
110 = PTGO15 primary trigger compare ends sampling and starts conversion(1)
101 = PTGO14 primary trigger compare ends sampling and starts conversion(1)
100 = PTGO13 primary trigger compare ends sampling and starts conversion(1)
011 = PTGO12 primary trigger compare ends sampling and starts conversion(1)
010 = PWM Generator 3 primary trigger compare ends sampling and starts conversion
001 = PWM Generator 2 primary trigger compare ends sampling and starts conversion
000 = PWM Generator 1 primary trigger compare ends sampling and starts conversion

If SSRCG = 0:

111 = Internal counter ends sampling and starts conversion (auto-convert)
110 = CTMU ends sampling and starts conversion
101 = PWM secondary Special Event Trigger ends sampling and starts conversion
100 = Timer5 compare ends sampling and starts conversion
011 = PWM primary Special Event Trigger ends sampling and starts conversion
010 = Timer3 compare ends sampling and starts conversion
001 = Active transition on the INT0 pin ends sampling and starts conversion
000 = Clearing the Sample bit (SAMP) ends sampling and starts conversion (Manual mode)

bit 4 **SSRCG:** Sample Trigger Source Group bit

See SSRC<2:0> for details.

bit 3 **SIMSAM:** Simultaneous Sample Select bit (only applicable when CHPS<1:0> = 01 or 1x)

In 12-Bit Mode (AD12B = 1), SIMSAM is Unimplemented and is Read as '0':

1 = Samples CH0, CH1, CH2, CH3 simultaneously (when CHPS<1:0> = 1x), or samples CH0 and CH1 simultaneously (when CHPS<1:0> = 01)
0 = Samples multiple channels individually in sequence

bit 2 **ASAM:** ADCx Sample Auto-Start bit

1 = Sampling begins immediately after last conversion; SAMP bit is auto-set
0 = Sampling begins when SAMP bit is set

bit 1 **SAMP:** ADCx Sample Enable bit

1 = ADCx Sample-and-Hold amplifiers are sampling
0 = ADCx Sample-and-Hold amplifiers are holding

If ASAM = 0, software can write '1' to begin sampling. Automatically set by hardware if ASAM = 1. If SSRC<2:0> = 000, software can write '0' to end sampling and start conversion. If SSRC<2:0> ≠ 000, automatically cleared by hardware to end sampling and start conversion.

bit 0 **DONE:** ADCx Conversion Status bit(2)

1 = ADCx conversion cycle is completed.
0 = ADCx conversion has not started or is in progress

Automatically set by hardware when A/D conversion is complete. Software can write '0' to clear DONE status (software not allowed to write '1'). Clearing this bit does NOT affect any operation in progress. Automatically cleared by hardware at the start of a new conversion.

Note 1: See **Section 25.0 "Peripheral Trigger Generator (PTG) Module"** for information on this selection.
2: Do not clear the DONE bit in software if ADCx Sample Auto-Start bit is enabled (ASAM = 1).

REGISTER 23-7: ADxCSSH: ADCx INPUT SCAN SELECT REGISTER HIGH(2)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CSS31	CSS30	CSS29	CSS28	CSS27	CSS26(1)	CSS25(1)	CSS24(1)
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CSS23	CSS22	CSS21	CSS20	CSS19	CSS18	CSS17	CSS16
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **CSS31:** ADCx Input Scan Selection bit
1 = Selects ANx for input scan
0 = Skips ANx for input scan

bit 14 **CSS30:** ADCx Input Scan Selection bit
1 = Selects ANx for input scan
0 = Skips ANx for input scan

bit 13 **CSS29:** ADCx Input Scan Selection bits
1 = Selects ANx for input scan
0 = Skips ANx for input scan

bit 12 **CSS28:** ADCx Input Scan Selection bit
1 = Selects ANx for input scan
0 = Skips ANx for input scan

bit 11 **CSS27:** ADCx Input Scan Selection bit
1 = Selects ANx for input scan
0 = Skips ANx for input scan

bit 10 **CSS26:** ADCx Input Scan Selection bit(1)
1 = Selects OA3/AN6 for input scan
0 = Skips OA3/AN6 for input scan

bit 9 **CSS25:** ADCx Input Scan Selection bit(1)
1 = Selects OA2/AN0 for input scan
0 = Skips OA2/AN0 for input scan

bit 8 **CSS24:** ADCx Input Scan Selection bit(1)
1 = Selects OA1/AN3 for input scan
0 = Skips OA1/AN3 for input scan

bit 7 **CSS23:** ADCx Input Scan Selection bit
1 = Selects ANx for input scan
0 = Skips ANx for input scan

bit 6 **CSS22:** ADCx Input Scan Selection bits
1 = Selects ANx for input scan
0 = Skips ANx for input scan

bit 5 **CSS21:** ADCx Input Scan Selection bits
1 = Selects ANx for input scan
0 = Skips ANx for input scan

Note 1: If the op amp is selected (OPMODE bit (CMxCON<10>) = 1), the OAx input is used; otherwise, the ANx input is used.

2: All bits in this register can be selected by the user application. However, inputs selected for scan without a corresponding input on the device convert VREFL.

24.0 DATA CONVERTER INTERFACE (DCI) MODULE

Note 1: This data sheet is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"Data Converter Interface (DCI) Module"** (DS70356), which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

24.1 Module Introduction

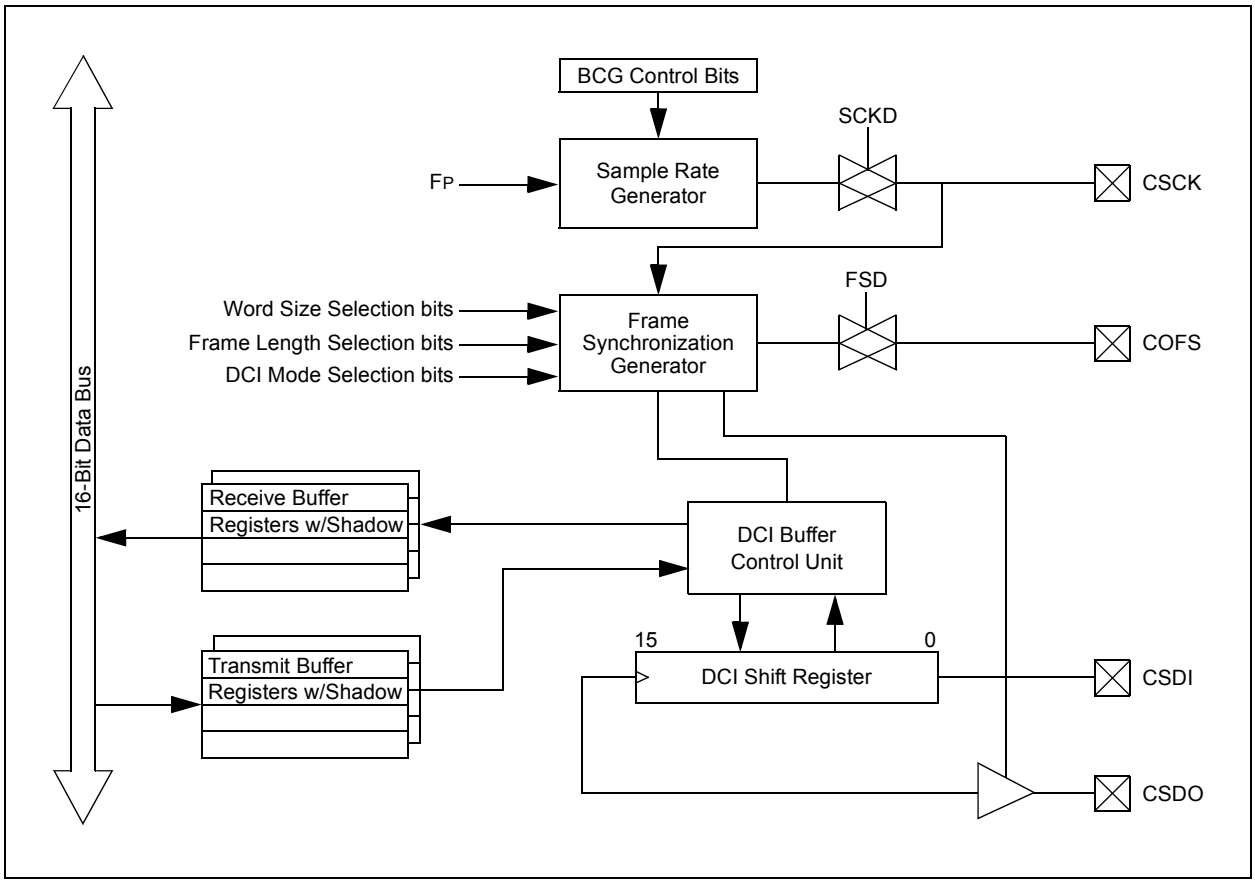
The Data Converter Interface (DCI) module allows simple interfacing of devices, such as audio coder/ decoders (Codecs), ADC and D/A Converters. The following interfaces are supported:

- Framed Synchronous Serial Transfer (Single or Multi-Channel)
- Inter-IC Sound (I^2S) Interface
- AC-Link Compliant mode

General features include:

- Programmable word size up to 16 bits
- Supports up to 16 time slots, for a maximum frame size of 256 bits
- Data buffering for up to 4 samples without CPU overhead

FIGURE 24-1: DCI MODULE BLOCK DIAGRAM



30.5 Watchdog Timer (WDT)

For dsPIC33EPXXXGM3XX/6XX/7XX devices, the WDT is driven by the LPRC oscillator. When the WDT is enabled, the clock source is also enabled.

30.5.1 PRESCALER/POSTSCALER

The nominal WDT clock source from LPRC is 32 kHz. This feeds a prescaler that can be configured for either 5-bit (divide-by-32) or 7-bit (divide-by-128) operation. The prescaler is set by the WDTPRE Configuration bit. With a 32 kHz input, the prescaler yields a WDT time-out period (T_{WDT}), as shown in Parameter SY12 in Table 33-21.

A variable postscaler divides down the WDT prescaler output and allows for a wide range of time-out periods. The postscaler is controlled by the WDTPOST<3:0> Configuration bits (FWDT<3:0>), which allow the selection of 16 settings, from 1:1 to 1:32,768. Using the prescaler and postscaler, time-out periods ranging from 1 ms to 131 seconds can be achieved.

The WDT, prescaler and postscaler are reset:

- On any device Reset
- On the completion of a clock switch, whether invoked by software (i.e., setting the OSWEN bit after changing the NOSCx bits) or by hardware (i.e., Fail-Safe Clock Monitor)
- When a PWRSAV instruction is executed (i.e., Sleep or Idle mode is entered)
- When the device exits Sleep or Idle mode to resume normal operation
- By a CLRWDT instruction during normal execution

Note: The CLRWDT and PWRSAV instructions clear the prescaler and postscaler counts when executed.

30.5.2 SLEEP AND IDLE MODES

If the WDT is enabled, it continues to run during Sleep or Idle modes. When the WDT time-out occurs, the device wakes the device and code execution continues from where the PWRSAV instruction was executed. The corresponding SLEEP or IDLE bit (RCON<3,2>) needs to be cleared in software after the device wakes up.

30.5.3 ENABLING WDT

The WDT is enabled or disabled by the FWDTEN Configuration bit in the FWDT Configuration register. When the FWDTEN Configuration bit is set, the WDT is always enabled.

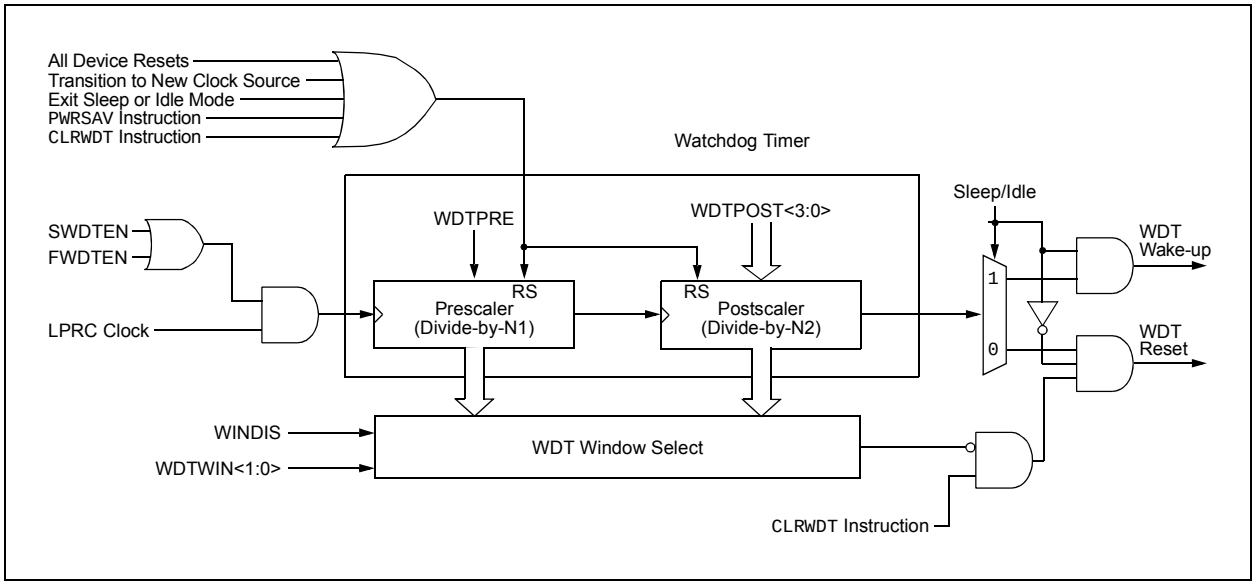
The WDT can be optionally controlled in software when the FWDTEN Configuration bit has been programmed to '0'. The WDT is enabled in software by setting the SWDTEN control bit (RCON<5>). The SWDTEN control bit is cleared on any device Reset. The software WDT option allows the user application to enable the WDT for critical code segments and disable the WDT during non-critical segments for maximum power savings.

The WDT flag bit, WDTO (RCON<4>), is not automatically cleared following a WDT time-out. To detect subsequent WDT events, the flag must be cleared in software.

30.5.4 WDT WINDOW

The Watchdog Timer has an optional Windowed mode enabled by programming the WINDIS bit in the WDT Configuration register (FWDT<6>). In the Windowed mode (WINDIS = 0), the WDT should be cleared based on the settings in the programmable Watchdog Timer Window select bits (WDTWIN<1:0>).

FIGURE 30-2: WDT BLOCK DIAGRAM



NOTES:

33.0 ELECTRICAL CHARACTERISTICS

This section provides an overview of dsPIC33EPXXXGM3XX/6XX/7XX electrical characteristics. Additional information will be provided in future revisions of this document as it becomes available.

Absolute maximum ratings for the dsPIC33EPXXXGM3XX/6XX/7XX family are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions above the parameters indicated in the operation listings of this specification is not implied.

Absolute Maximum Ratings

(See Note 1)

Ambient temperature under bias ..... -40°C to +125°C
Storage temperature ..... -65°C to +160°C
Voltage on V_{DD} with respect to V_{SS} ..... -0.3V to +4.0V
Voltage on any pin that is not 5V tolerant with respect to V_{SS} **(3)** ..... -0.3V to (V_{DD} + 0.3V)
Voltage on any 5V tolerant pin with respect to V_{SS} when $V_{DD} \geq 3.0V$ **(3)** ..... -0.3V to +5.5V
Voltage on any 5V tolerant pin with respect to Vss when $V_{DD} < 3.0V$ **(3)** ..... -0.3V to +3.6V
Voltage on V_{CAP} with respect to V_{SS} ..... 1.62V to 1.98V
Maximum current out of V_{SS} pin ..... 350 mA
Maximum current into V_{DD} pin **(2)** ..... 350 mA
Maximum current sunk by any I/O pin ..... 20 mA
Maximum current sourced by I/O pin ..... 18 mA
Maximum current sourced/sunk by all ports **(2,4)** ..... 200 mA

Note 1: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2: Maximum allowable current is a function of device maximum power dissipation (see Table 33-2).

3: See the **“Pin Diagrams”** section for the 5V tolerant pins.

4: Exceptions are: RA3, RA4, RA7, RA9, RA10, RB7-RB15, RC3, RC15, RD1-RD4, which are able to sink 30 mA and source 20 mA.

TABLE 33-4: DC TEMPERATURE AND VOLTAGE SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions (see Note 3): 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ.(1)**	**Max.**	**Units**	**Conditions**
Operating Voltage							
DC10	VDD	**Supply Voltage(3)**	3.0	—	3.6	V	
DC12	VDR	**RAM Data Retention Voltage(2)**	1.95	—	—	V	
DC16	VPOR	**VDD Start Voltage** to Ensure Internal Power-on Reset Signal	—	—	VSS	V	
DC17	SVDD	**VDD Rise Rate** to Ensure Internal Power-on Reset Signal	0.03	—	—	V/ms	0V-3.0V in 3 ms
DC18	VCORE	**VDD Core(3)** Internal Regulator Voltage	1.62	1.8	1.98	V	Voltage is dependent on load, temperature and VDD

Note 1: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated.

2: This is the limit to which VDD may be lowered without losing RAM data.

3: Device is functional at VBORMIN < VDD < VDDMIN. Analog modules: ADC, op amp/comparator and comparator voltage reference will have degraded performance. Device functionality is tested but not characterized. Refer to Parameter BO10 in Table 33-12 for the minimum and maximum BOR values.

TABLE 33-5: FILTER CAPACITOR (CEFC) SPECIFICATIONS

			Standard Operating Conditions (unless otherwise stated): Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Comments**
	CEFC	External Filter Capacitor Value(1)	4.7	10	—	μF	Capacitor must have a low series resistance (< 1 Ohm)

Note 1: Typical VCAP voltage = 1.8 volts when VDD ≥ VDDMIN.

TABLE 33-9: DC CHARACTERISTICS: DOZE CURRENT (IDOZE)

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Parameter No.	**Typ.(2)**	**Max.**	**Doze Ratio**	**Units**	**Conditions**		
Doze Current (IDOZE)(1)							
DC73a	20	53	1:2	mA	-40°C	3.3V	70 MIPS
DC73g	8	30	1:128	mA			
DC70a	19	53	1:2	mA	+25°C	3.3V	60 MIPS
DC70g	8	30	1:128	mA			
DC71a	20	53	1:2	mA	+85°C	3.3V	60 MIPS
DC71g	10	30	1:128	mA			
DC72a	25	42	1:2	mA	+125°C	3.3V	50 MIPS
DC72g	12	30	1:128	mA			

Note 1: IDOZE is primarily a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption. The test conditions for all IDOZE measurements are as follows:

- Oscillator is configured in EC mode and external clock is active, OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)
- CLKO is configured as an I/O input pin in the Configuration Word
- All I/O pins are configured as outputs and driving low
- $\overline{MCLR}$ = VDD, WDT and FSCM are disabled
- CPU, SRAM, program memory and data memory are operational
- No peripheral modules are operating or being clocked (defined PMDx bits are all ones)
- CPU executing

```
while(1)
{
NOP();
}
```

- JTAG is disabled

2: Data in the “Typical” column is at 3.3V, +25°C unless otherwise specified.

APPENDIX A: REVISION HISTORY

Revision A (February 2013)

This is the initial released version of this document.

Revision B (June 2013)

Changes to **Section 5.0 "Flash Program Memory"**, Register 5-1. Changes to **Section 6.0 "Resets"**, Figure 6-1. Changes to **Section 26.0 "Op Amp/Comparator Module"**, Register 26-2. Updates to most of the tables in **Section 33.0 "Electrical Characteristics"**. Minor text edits throughout the document.

Revision C (September 2013)

Changes to Figure 23-1. Changes to Figure 26-2. Changes to Table 30-2. Changes to **Section 33.0 "Electrical Characteristics"**. Added **Section 34.0 "High-Temperature Electrical Characteristics"** to the data sheet. Minor typographical edits throughout the document.

Revision D (August 2014)

This revision incorporates the following updates:

- Sections:
  - Updated **Section 2.0 "Guidelines for Getting Started with 16-Bit Digital Signal Controllers"**, **Section 8.0 "Direct Memory Access (DMA)"**, **Section 10.3 "Doze Mode"**, **Section 21.0 "Controller Area Network (CAN) Module (dsPIC33EPXXXGM6XX/7XX Devices Only)"**, **Section 23.0 "10-Bit/12-Bit Analog-to-Digital Converter (ADC)"**, **Section 23.1.2 "12-Bit ADCx Configuration"**, **Section 21.4 "CAN Message Buffers"**, **Section 35.0 "Packaging Information"**
- Figures:
  - Updated **"Pin Diagrams"**, Figure 1-1, Figure 9-1
- Registers:
  - Updated Register 5-1, Register 8-2, Register 21-1, Register 23-2
- Tables:
  - Updated Table 1-1, Table 7-1, Table 8-1, Table 34-9, Table 1, Table 4-2, Table 4-3, Table 4-25, Table 4-33, Table 4-34, Table 4-39, Table 4-30, Table 4-46, Table 4-47, Table 33-16,Table 34-8