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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

| | |
|----------------------------|---|
| Product Status | Active |
| Core Processor | dsPIC |
| Core Size | 16-Bit |
| Speed | 70 MIPS |
| Connectivity | I ² C, IrDA, LINbus, QEI, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, I ² S, Motor Control PWM, POR, PWM, WDT |
| Number of I/O | 85 |
| Program Memory Size | 512KB (170K x 24) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 48K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 3.6V |
| Data Converters | A/D 49x10b/12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-TQFP |
| Supplier Device Package | 100-TQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep512gm310-i-pf |

3.0 CPU

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGM3XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the “dsPIC33/PIC24 Family Reference Manual”, “CPU” (DS70359), which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The CPU has a 16-bit (data) modified Harvard architecture with an enhanced instruction set, including significant support for digital signal processing. The CPU has a 24-bit instruction word, with a variable length opcode field. The Program Counter (PC) is 23 bits wide and addresses up to 4M x 24 bits of user program memory space.

An instruction prefetch mechanism helps maintain throughput and provides predictable execution. Most instructions execute in a single-cycle, effective execution rate, with the exception of instructions that change the program flow, the double-word move (MOV.D) instruction, PSV accesses and the table instructions. Overhead-free program loop constructs are supported using the DO and REPEAT instructions, both of which are interruptible at any point.

3.1 Registers

The dsPIC33EPXXXGM3XX/6XX/7XX devices have sixteen 16-bit Working registers in the programmer's model. Each of the Working registers can act as a data, address or address offset register. The 16th Working register (W15) operates as a Software Stack Pointer for interrupts and calls.

3.2 Instruction Set

The device instruction set has two classes of instructions: the MCU class of instructions and the DSP class of instructions. These two instruction classes are seamlessly integrated into the architecture and execute from a single execution unit. The instruction set includes many addressing modes and was designed for optimum C compiler efficiency.

3.3 Data Space Addressing

The Base Data Space can be addressed as 4K words or 8 Kbytes and is split into two blocks, referred to as X and Y data memory. Each memory block has its own independent Address Generation Unit (AGU). The MCU class of instructions operate solely through the X memory AGU, which accesses the entire memory map as one linear Data Space. On dsPIC33EP devices, certain DSP instructions operate through the X and Y AGUs to support dual operand reads, which splits the data address space into two parts. The X and Y Data Space boundary is device-specific.

The upper 32 Kbytes of the Data Space memory map can optionally be mapped into Program Space at any 16K program word boundary. The program-to-Data Space mapping feature, known as Program Space Visibility (PSV), lets any instruction access Program Space as if it were Data Space. Moreover, the Base Data Space address is used in conjunction with a Data Space Read or Write Page register (DSRPAG or DSWPAG) to form an Extended Data Space (EDS) address. The EDS can be addressed as 8M words or 16 Mbytes. Refer to “Data Memory” (DS70595) and “Program Memory” (DS70613) in the “dsPIC33/PIC24 Family Reference Manual” for more details on EDS, PSV and table accesses.

On dsPIC33EP devices, overhead-free circular buffers (Modulo Addressing) are supported in both X and Y address spaces. The Modulo Addressing removes the software boundary checking overhead for DSP algorithms. The X AGU circular addressing can be used with any of the MCU class of instructions. The X AGU also supports Bit-Reversed Addressing to greatly simplify input or output data reordering for radix-2 FFT algorithms.

3.4 Addressing Modes

The CPU supports these addressing modes:

- Inherent (no operand)
- Relative
- Literal
- Memory Direct
- Register Direct
- Register Indirect

Each instruction is associated with a predefined addressing mode group, depending upon its functional requirements. As many as six addressing modes are supported for each instruction.

TABLE 4-10: PWM GENERATOR 2 REGISTER MAP

| SFR Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|----------|-------|---------------|---------|---------------|---------|-----------|-----------|-----------|-----------|---------|---------|----------|----------|----------|----------|---------|---------|------------|
| PWMCON2 | 0C40 | FLTSTAT | CLSTAT | TRGSTAT | FLTIE | CLIE | TRGIE | ITB | MDCS | DTC1 | DTC0 | DTCP | — | MTBS | CAM | XPRES | IUE | 0000 |
| IOCON2 | 0C42 | PENH | PENL | POLH | POLL | PMOD1 | PMOD0 | OVRENH | OVRENL | OVRDAT1 | OVRDAT0 | FLTDAT1 | FLTDAT0 | CLDAT1 | CLDAT0 | SWAP | OSYNC | C000 |
| FCLCON2 | 0C44 | IFLTMOD | CLSRC4 | CLSRC3 | CLSRC2 | CLSRC1 | CLSRC0 | CLPOL | CLMOD | FLTSRC4 | FLTSRC3 | FLTSRC2 | FLTSRC1 | FLTSRC0 | FLTPOL | FLTMOD1 | FLTMOD0 | 00F8 |
| PDC2 | 0C46 | PDC2<15:0> | | | | | | | | | | | | | | | | 0000 |
| PHASE2 | 0C48 | PHASE2<15:0> | | | | | | | | | | | | | | | | 0000 |
| DTR2 | 0C4A | — | — | DTR2<13:0> | | | | | | | | | | | | | | 0000 |
| ALTDTR2 | 0C4C | — | — | ALTDTR2<13:0> | | | | | | | | | | | | | | 0000 |
| SDC2 | 0C4E | SDC2<15:0> | | | | | | | | | | | | | | | | 0000 |
| SPHASE2 | 0C50 | SPHASE2<15:0> | | | | | | | | | | | | | | | | 0000 |
| TRIG2 | 0C52 | TRGCMPL<15:0> | | | | | | | | | | | | | | | | 0000 |
| TRGCON2 | 0C54 | TRGDIV3 | TRGDIV2 | TRGDIV1 | TRGDIV0 | — | — | — | — | — | — | TRGSTR5 | TRGSTR4 | TRGSTR3 | TRGSTR2 | TRGSTR1 | TRGSTR0 | 0000 |
| PWMCAP2 | 0C78 | PWMCAP2<15:0> | | | | | | | | | | | | | | | | 0000 |
| LEBCON2 | 0C5A | PHR | PHF | PLR | PLF | FLTBLEN | CLLBEN | — | — | — | — | BCH | BCL | BPHH | BPHL | BPLH | BPLL | 0000 |
| LEBDLY2 | 0C5C | — | — | — | — | LEB<11:0> | | | | | | | | | | | | 0000 |
| AUXCON2 | 0C5E | — | — | — | — | BLANKSEL3 | BLANKSEL2 | BLANKSEL1 | BLANKSEL0 | — | — | CHOPSEL3 | CHOPSEL2 | CHOPSEL1 | CHOPSEL0 | CHOPHEN | CHOPLEN | 0000 |

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-11: PWM GENERATOR 3 REGISTER MAP

| SFR Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|----------|-------|---------------|---------|---------------|---------|-----------|-----------|-----------|-----------|---------|---------|----------|----------|----------|----------|---------|---------|------------|
| PWMCON3 | 0C60 | FLTSTAT | CLSTAT | TRGSTAT | FLTIE | CLIE | TRGIE | ITB | MDCS | DTC1 | DTC0 | DTCP | — | MTBS | CAM | XPRES | IUE | 0000 |
| IOCON3 | 0C62 | PENH | PENL | POLH | POLL | PMOD1 | PMOD0 | OVRENH | OVREN | OVRDAT1 | OVRDAT0 | FLTDAT1 | FLTDAT0 | CLDAT1 | CLDAT0 | SWAP | OSYNC | C000 |
| FCLCON3 | 0C64 | IFLTMOD | CLSRC4 | CLSRC3 | CLSRC2 | CLSRC1 | CLSRC0 | CLPOL | CLMOD | FLTSRC4 | FLTSRC3 | FLTSRC2 | FLTSRC1 | FLTSRC0 | FLTPOL | FLTMOD1 | FLTMOD0 | 00F8 |
| PDC3 | 0C66 | PDC3<15:0> | | | | | | | | | | | | | | | | 0000 |
| PHASE3 | 0C68 | PHASE3<15:0> | | | | | | | | | | | | | | | | 0000 |
| DTR3 | 0C6A | — | — | DTR3<13:0> | | | | | | | | | | | | | | 0000 |
| ALTDTR3 | 0C6C | — | — | ALTDTR3<13:0> | | | | | | | | | | | | | | 0000 |
| SDC3 | 0C6E | SDC3<15:0> | | | | | | | | | | | | | | | | 0000 |
| SPHASE3 | 0C70 | SPHASE3<15:0> | | | | | | | | | | | | | | | | 0000 |
| TRIG3 | 0C72 | TRGCMPL<15:0> | | | | | | | | | | | | | | | | 0000 |
| TRGCON3 | 0C74 | TRGDIV3 | TRGDIV2 | TRGDIV1 | TRGDIV0 | — | — | — | — | — | — | TRGSTR5 | TRGSTR4 | TRGSTR3 | TRGSTR2 | TRGSTR1 | TRGSTR0 | 0000 |
| PWMCAP3 | 0C78 | PWMCAP3<15:0> | | | | | | | | | | | | | | | | 0000 |
| LEBCON3 | 0C7A | PHR | PHF | PLR | PLF | FLTBLEN | CLLBEN | — | — | — | — | BCH | BCL | BPHH | BPHL | BPLH | BPLL | 0000 |
| LEBDLY3 | 0C7C | — | — | — | — | LEB<11:0> | | | | | | | | | | | | 0000 |
| AUXCON3 | 0C7E | — | — | — | — | BLANKSEL3 | BLANKSEL2 | BLANKSEL1 | BLANKSEL0 | — | — | CHOPSEL3 | CHOPSEL2 | CHOPSEL1 | CHOPSEL0 | CHOPHEN | CHOPLEN | 0000 |

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-23: CAN1 REGISTER MAP WHEN WIN (C1CTRL<0>) = 0 OR 1 FOR dsPIC33EPXXXGM60X/7XX DEVICES⁽¹⁾

| SFR Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|------------|-------|-------------|----------|----------|----------|----------|----------|----------|----------|----------|----------|----------|------------|----------|----------|----------|----------|------------|
| C1CTRL1 | 0400 | — | — | CSIDL | ABAT | CANCKS | REQOP2 | REQOP1 | REQOP0 | OPMODE2 | OPMODE1 | OPMODE0 | — | CANCAP | — | — | WIN | 0480 |
| C1CTRL2 | 0402 | — | — | — | — | — | — | — | — | — | — | — | DNCNT<4:0> | | | | | 0000 |
| C1VEC | 0404 | — | — | — | FILHIT4 | FILHIT3 | FILHIT2 | FILHIT1 | FILHIT0 | — | ICODE6 | ICODE5 | ICODE4 | ICODE3 | ICODE2 | ICODE1 | ICODE0 | 0040 |
| C1FCTRL | 0406 | DMABS2 | DMABS1 | DMABS0 | — | — | — | — | — | — | — | — | FSA4 | FSA3 | FSA2 | FSA1 | FSA0 | 0000 |
| C1FIFO | 0408 | — | — | FBP5 | FBP4 | FBP3 | FBP2 | FBP1 | FBP0 | — | — | FNRB5 | FNRB4 | FNRB3 | FNRB2 | FNRB1 | FNRB0 | 0000 |
| C1INTF | 040A | — | — | TXBO | TXBP | RXPB | TXWAR | RXWAR | EWARN | IVRIF | WAKIF | ERRIF | — | FIFOIF | RBOVIF | RBIF | TBIF | 0000 |
| C1INTE | 040C | — | — | — | — | — | — | — | — | IVRIE | WAKIE | ERRIE | — | FIFOIE | RBOVIE | RBIE | TBIE | 0000 |
| C1EC | 040E | TERRCNT7 | TERRCNT6 | TERRCNT5 | TERRCNT4 | TERRCNT3 | TERRCNT2 | TERRCNT1 | TERRCNT0 | RERRCNT7 | RERRCNT6 | RERRCNT5 | RERRCNT4 | RERRCNT3 | RERRCNT2 | RERRCNT1 | RERRCNT0 | 0000 |
| C1CFG1 | 0410 | — | — | — | — | — | — | — | — | SJW1 | SJW0 | BRP5 | BRP4 | BRP3 | BRP2 | BRP1 | BRP0 | 0000 |
| C1CFG2 | 0412 | — | WAKFIL | — | — | — | SEG2PH2 | SEG2PH1 | SEG2PH0 | SEG2PHTS | SAM | SEG1PH2 | SEG1PH1 | SEG1PH0 | PRSEG2 | PRSEG1 | PRSEG0 | 0000 |
| C1FEN1 | 0414 | FLTEN<15:0> | | | | | | | | | | | | | | | | FFFF |
| C1FMSKSEL1 | 0418 | F7MSK1 | F7MSK0 | F6MSK1 | F6MSK0 | F5MSK1 | F5MSK0 | F4MSK1 | F4MSK0 | F3MSK1 | F3MSK0 | F2MSK1 | F2MSK0 | F1MSK1 | F1MSK0 | F0MSK1 | F0MSK0 | 0000 |
| C1FMSKSEL2 | 041A | F15MSK1 | F15MSK0 | F14MSK1 | F14MSK0 | F13MSK1 | F13MSK0 | F12MSK1 | F12MSK0 | F11MSK1 | F11MSK0 | F10MSK1 | F10MSK0 | F9MSK1 | F9MSK0 | F8MSK1 | F8MSK0 | 0000 |

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: These registers are not present on dsPIC33EPXXXGM3XX devices.

TABLE 4-24: CAN1 REGISTER MAP WHEN WIN (C1CTRL<0>) = 0 FOR dsPIC33EPXXXGM60X/7XX DEVICES⁽¹⁾

| SFR Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|-----------|-----------|-----------------------------|--------|---------|--------|--------|--------|---------|---------|-------|---------|---------|--------|--------|--------|---------|---------|------------|
| | 0400-041E | See definition when WIN = x | | | | | | | | | | | | | | | | |
| C1RXFUL1 | 0420 | RXFUL<15:0> | | | | | | | | | | | | | | | | 0000 |
| C1RXFUL2 | 0422 | RXFUL<31:16> | | | | | | | | | | | | | | | | 0000 |
| C1RXOVF1 | 0428 | RXOVF<15:0> | | | | | | | | | | | | | | | | 0000 |
| C1RXOVF2 | 042A | RXOVF<31:16> | | | | | | | | | | | | | | | | 0000 |
| C1TR01CON | 0430 | TXEN1 | TXABT1 | TXLARB1 | TXERR1 | TXREQ1 | RTREN1 | TX1PRI1 | TX1PRI0 | TXEN0 | TXABAT0 | TXLARB0 | TXERR0 | TXREQ0 | RTREN0 | TX0PRI1 | TX0PRI0 | 0000 |
| C1TR23CON | 0432 | TXEN3 | TXABT3 | TXLARB3 | TXERR3 | TXREQ3 | RTREN3 | TX3PRI1 | TX3PRI0 | TXEN2 | TXABAT2 | TXLARB2 | TXERR2 | TXREQ2 | RTREN2 | TX2PRI1 | TX2PRI0 | 0000 |
| C1TR45CON | 0434 | TXEN5 | TXABT5 | TXLARB5 | TXERR5 | TXREQ5 | RTREN5 | TX5PRI1 | TX5PRI0 | TXEN4 | TXABAT4 | TXLARB4 | TXERR4 | TXREQ4 | RTREN4 | TX4PRI1 | TX4PRI0 | 0000 |
| C1TR67CON | 0436 | TXEN7 | TXABT7 | TXLARB7 | TXERR7 | TXREQ7 | RTREN7 | TX7PRI1 | TX7PRI0 | TXEN6 | TXABAT6 | TXLARB6 | TXERR6 | TXREQ6 | RTREN6 | TX6PRI1 | TX6PRI0 | xxxx |
| C1RXD | 0440 | CAN1 Receive Data Word | | | | | | | | | | | | | | | | xxxx |
| C1TXD | 0442 | CAN1 Transmit Data Word | | | | | | | | | | | | | | | | xxxx |

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: These registers are not present on dsPIC33EPXXXGM3XX devices.

TABLE 4-34: PERIPHERAL PIN SELECT INPUT REGISTER MAP FOR dsPIC33EPXXXGM3XX DEVICES

| SFR Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets | | |
|----------|-------|--------|--------------|--------|--------|--------|--------|-------|-------|-------|--------------|--------------|-------|-------|-------|-------|-------|------------|------|------|
| RPINR0 | 06A0 | — | INT1R<6:0> | | | | | | | | — | — | — | — | — | — | — | — | 0000 | |
| RPINR1 | 06A2 | — | — | — | — | — | — | — | — | — | INT2R<6:0> | | | | | | | | 0000 | |
| RPINR3 | 06A6 | — | — | — | — | — | — | — | — | — | T2CKR<6:0> | | | | | | | | 0000 | |
| RPINR7 | 06AE | — | IC2R<6:0> | | | | | | | | — | IC1R<6:0> | | | | | | | | 0000 |
| RPINR8 | 06B0 | — | IC4R<6:0> | | | | | | | | — | IC3R<6:0> | | | | | | | | 0000 |
| RPINR9 | 06B2 | — | IC6R<6:0> | | | | | | | | — | IC5R<6:0> | | | | | | | | 0000 |
| RPINR10 | 06B4 | — | IC8R<6:0> | | | | | | | | — | IC7R<6:0> | | | | | | | | 0000 |
| RPINR11 | 06B6 | — | — | — | — | — | — | — | — | — | OCFAR<6:0> | | | | | | | | 0000 | |
| RPINR12 | 06B8 | — | FLT2R<6:0> | | | | | | | | — | FLT1R<6:0> | | | | | | | | 0000 |
| RPINR14 | 06BC | — | QEB1R<6:0> | | | | | | | | — | QEA1R<6:0> | | | | | | | | 0000 |
| RPINR15 | 06BE | — | HOME1R<6:0> | | | | | | | | — | INDX1R<6:0> | | | | | | | | 0000 |
| RPINR16 | 06C0 | — | QEB2R<6:0> | | | | | | | | — | QEA2R<6:0> | | | | | | | | 0000 |
| RPINR17 | 06C2 | — | HOME2R<6:0> | | | | | | | | — | INDX2R<6:0> | | | | | | | | 0000 |
| RPINR18 | 06C4 | — | — | — | — | — | — | — | — | — | U1RXR<6:0> | | | | | | | | 0000 | |
| RPINR19 | 06C6 | — | — | — | — | — | — | — | — | — | U2RXR<6:0> | | | | | | | | 0000 | |
| RPINR22 | 06CC | — | SCK2R<6:0> | | | | | | | | — | SDI2R<6:0> | | | | | | | | 0000 |
| RPINR23 | 06CE | — | — | — | — | — | — | — | — | — | SS2R<6:0> | | | | | | | | 0000 | |
| RPINR24 | 06D0 | — | CSCKR<6:0> | | | | | | | | — | CSDIR<6:0> | | | | | | | | 0000 |
| RPINR25 | 06D2 | — | — | — | — | — | — | — | — | — | COFSR<6:0> | | | | | | | | 0000 | |
| RPINR27 | 06D6 | — | U3CTSR<6:0> | | | | | | | | — | U3RXR<6:0> | | | | | | | | 0000 |
| RPINR28 | 06D8 | — | U4CTSR<6:0> | | | | | | | | — | U4RXR<6:0> | | | | | | | | 0000 |
| RPINR29 | 06DA | — | SCK3R<6:0> | | | | | | | | — | SDI3R<6:0> | | | | | | | | 0000 |
| RPINR30 | 06DC | — | — | — | — | — | — | — | — | — | SS3R<6:0> | | | | | | | | 0000 | |
| RPINR37 | 06EA | — | SYNCI1R<6:0> | | | | | | | | — | — | — | — | — | — | — | — | 0000 | |
| RPINR38 | 06EC | — | DTCMP1R<6:0> | | | | | | | | — | — | — | — | — | — | — | — | 0000 | |
| RPINR39 | 06EE | — | DTCMP3R<6:0> | | | | | | | | — | DTCMP2R<6:0> | | | | | | | | 0000 |
| RPINR40 | 06F0 | — | DTCMP5R<6:0> | | | | | | | | — | DTCMP4R<6:0> | | | | | | | | 0000 |
| RPINR41 | 06F2 | — | — | — | — | — | — | — | — | — | DTCMP6R<6:0> | | | | | | | | 0000 | |

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-52: PORTC REGISTER MAP FOR dsPIC33EPXXXGM310/710 DEVICES

| SFR Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|----------|-------|---------|--------|-------------|-------------|--------|--------|-------|-------|-------|-------|-----------|-------|-------|-------|-------|-------|------------|
| TRISC | 0E20 | TRISC15 | — | TRISC<13:0> | | | | | | | | | | | | | | BFFF |
| PORTC | 0E22 | RC15 | — | RC<13:0> | | | | | | | | | | | | | | xxxx |
| LATC | 0E24 | LATC15 | — | LATC<13:0> | | | | | | | | | | | | | | xxxx |
| ODCC | 0E26 | ODCC15 | — | ODCC<13:0> | | | | | | | | | | | | | | 0000 |
| CNENC | 0E28 | CNIEC15 | — | CNIEC<13:0> | | | | | | | | | | | | | | 0000 |
| CNPUC | 0E2A | CNPUC15 | — | CNPUC<13:0> | | | | | | | | | | | | | | 0000 |
| CNPDC | 0E2C | CNPDC15 | — | CNPDC<13:0> | | | | | | | | | | | | | | 0000 |
| ANSEL | 0E2E | — | — | — | ANSC<12:10> | | | — | — | — | — | ANSC<5:0> | | | | | | 0807 |

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-53: PORTC REGISTER MAP FOR dsPIC33EPXXXGM306/706 DEVICES

| SFR Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|----------|-------|---------|--------|-------------|--------|--------|--------|-------|-------|-------|-------|-----------|-------|-------|-------|-------|-------|------------|
| TRISC | 0E20 | TRISC15 | — | TRISC<13:0> | | | | | | | | | | | | | | BFFF |
| PORTC | 0E22 | RC15 | — | RC<13:0> | | | | | | | | | | | | | | xxxx |
| LATC | 0E24 | LATC15 | — | LATC<13:0> | | | | | | | | | | | | | | xxxx |
| ODCC | 0E26 | ODCC15 | — | ODCC<13:0> | | | | | | | | | | | | | | 0000 |
| CNENC | 0E28 | CNIEC15 | — | CNIEC<13:0> | | | | | | | | | | | | | | 0000 |
| CNPUC | 0E2A | CNPUC15 | — | CNPUC<13:0> | | | | | | | | | | | | | | 0000 |
| CNPDC | 0E2C | CNPDC15 | — | CNPDC<13:0> | | | | | | | | | | | | | | 0000 |
| ANSEL | 0E2E | — | — | — | | | | — | — | — | — | ANSC<5:0> | | | | | | 0807 |

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-54: PORTC REGISTER MAP FOR dsPIC33EPXXXGM304/604 DEVICES

| SFR Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|----------|-------|--------|--------|--------|--------|--------|--------|------------|-------|-------|-------|-----------|-------|-------|-------|-------|-------|------------|
| TRISC | 0E20 | — | — | — | — | — | — | TRISC<9:0> | | | | | | | | | | BFFF |
| PORTC | 0E22 | — | — | — | — | — | — | RC<9:0> | | | | | | | | | | xxxx |
| LATC | 0E24 | — | — | — | — | — | — | LATC<9:0> | | | | | | | | | | xxxx |
| ODCC | 0E26 | — | — | — | — | — | — | ODCC<9:0> | | | | | | | | | | 0000 |
| CNENC | 0E28 | — | — | — | — | — | — | CNIEC<9:0> | | | | | | | | | | 0000 |
| CNPUC | 0E2A | — | — | — | — | — | — | CNPUC<9:0> | | | | | | | | | | 0000 |
| CNPDC | 0E2C | — | — | — | — | — | — | CNPDC<9> | | | | | | | | | | 0000 |
| ANSEL | 0E2E | — | — | — | — | — | — | — | — | — | — | ANSC<5:0> | | | | | | 0807 |

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

REGISTER 5-2: NVMADRU: NONVOLATILE MEMORY UPPER ADDRESS REGISTER

| | | | | | | | |
|--------|-----|-----|-----|-----|-----|-----|-------|
| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|----------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| NVMADRU<23:16> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **NVMADRU<23:16>:** Nonvolatile Memory Upper Write Address bits

Selects the upper 8 bits of the location to program or erase in program Flash memory. This register may be read or written to by the user application.

REGISTER 5-3: NVMADR: NONVOLATILE MEMORY LOWER ADDRESS REGISTER

| | | | | | | | |
|--------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| NVMADR<15:8> | | | | | | | |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|-------------|-------|-------|-------|-------|-------|-------|-------|
| R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x | R/W-x |
| NVMADR<7:0> | | | | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **NVMADR<15:0>:** Nonvolatile Memory Lower Write Address bits

Selects the lower 16 bits of the location to program or erase in program Flash memory. This register may be read or written to by the user application.

7.0 INTERRUPT CONTROLLER

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGM3XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the “*dsPIC33/PIC24 Family Reference Manual*”, “**Interrupts**” (DS70000600), which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGM3XX/6XX/7XX interrupt controller reduces the numerous peripheral interrupt request signals to a single interrupt request signal to the dsPIC33EPXXXGM3XX/6XX/7XX CPU.

The interrupt controller has the following features:

- Up to eight processor exceptions and software traps
- Eight user-selectable priority levels
- Interrupt Vector Table (IVT) with a unique vector for each interrupt or exception source
- Fixed priority within a specified user priority level
- Fixed interrupt entry and return latencies

7.1 Interrupt Vector Table

The dsPIC33EPXXXGM3XX/6XX/7XX Interrupt Vector Table (IVT), shown in Figure 7-1, resides in program memory, starting at location, 000004h. The IVT contains seven non-maskable trap vectors and up to 151 sources of interrupt. In general, each interrupt source has its own vector. Each interrupt vector contains a 24-bit-wide address. The value programmed into each interrupt vector location is the starting address of the associated Interrupt Service Routine (ISR).

Interrupt vectors are prioritized in terms of their natural priority. This priority is linked to their position in the vector table. Lower addresses generally have a higher natural priority. For example, the interrupt associated with Vector 0 takes priority over interrupts at any other vector address.

7.2 Reset Sequence

A device Reset is not a true exception because the interrupt controller is not involved in the Reset process. The dsPIC33EPXXXGM3XX/6XX/7XX devices clear their registers in response to a Reset, which forces the PC to zero. The device then begins program execution at location, 0x000000. A GOTO instruction at the Reset address can redirect program execution to the appropriate start-up routine.

Note: Any unimplemented or unused vector locations in the IVT should be programmed with the address of a default interrupt handler routine that contains a RESET instruction.

REGISTER 9-1: OSCCON: OSCILLATOR CONTROL REGISTER^(1,3) (CONTINUED)

| | |
|-------|---|
| bit 5 | LOCK: PLL Lock Status bit (read-only) 1 = Indicates that PLL is in lock or PLL start-up timer is satisfied 0 = Indicates that PLL is out of lock, start-up timer is in progress or PLL is disabled |
| bit 4 | Unimplemented: Read as '0' |
| bit 3 | CF: Clock Fail Detect bit (read/clear by application) ⁽⁵⁾ 1 = FSCM has detected clock failure 0 = FSCM has not detected clock failure |
| bit 2 | Unimplemented: Read as '0' |
| bit 1 | LPOSCEN: Secondary (LP) Oscillator Enable bit 1 = Enables Secondary Oscillator (SOSC) 0 = Disables Secondary Oscillator |
| bit 0 | OSWEN: Oscillator Switch Enable bit 1 = Requests oscillator switch to selection specified by the NOSC<2:0> bits 0 = Oscillator switch is complete |

- Note 1:** Writes to this register require an unlock sequence. Refer to the “dsPIC33/PIC24 Family Reference Manual”, “**Oscillator**” (DS70580), available from the Microchip web site for details.
- 2:** Direct clock switches between any primary oscillator mode with PLL and FRCPLL mode are not permitted. This applies to clock switches in either direction. In these instances, the application must switch to FRC mode as a transitional clock source between the two PLL modes.
- 3:** This register resets only on a Power-on Reset (POR).
- 4:** Secondary Oscillator (SOSC) selection is valid on 64-pin and 100-pin devices, and defaults to FRC/N on 44-pin devices.
- 5:** Only '0' should be written to the CF bit in order to clear it. If a '1' is written to CF, it will have the same effect as a detected clock failure, including an oscillator fail trap.

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REGISTER 11-4: RPINR7: PERIPHERAL PIN SELECT INPUT REGISTER 7

| | | | | | | | |
|--------|-----------|-------|-------|-------|-------|-------|-------|
| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| — | IC2R<6:0> | | | | | | |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|-------|-----------|-------|-------|-------|-------|-------|-------|
| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| — | IC1R<6:0> | | | | | | |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **IC2R<6:0>:** Assign Input Capture 2 (IC2) to the Corresponding RPn Pin bits
(see Table 11-2 for input pin selection numbers)

1111100 = Input tied to RPI124

•
•
•

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **IC1R<6:0>:** Assign Input Capture 1 (IC1) to the Corresponding RPn Pin bits
(see Table 11-2 for input pin selection numbers)

1111100 = Input tied to RPI124

•
•
•

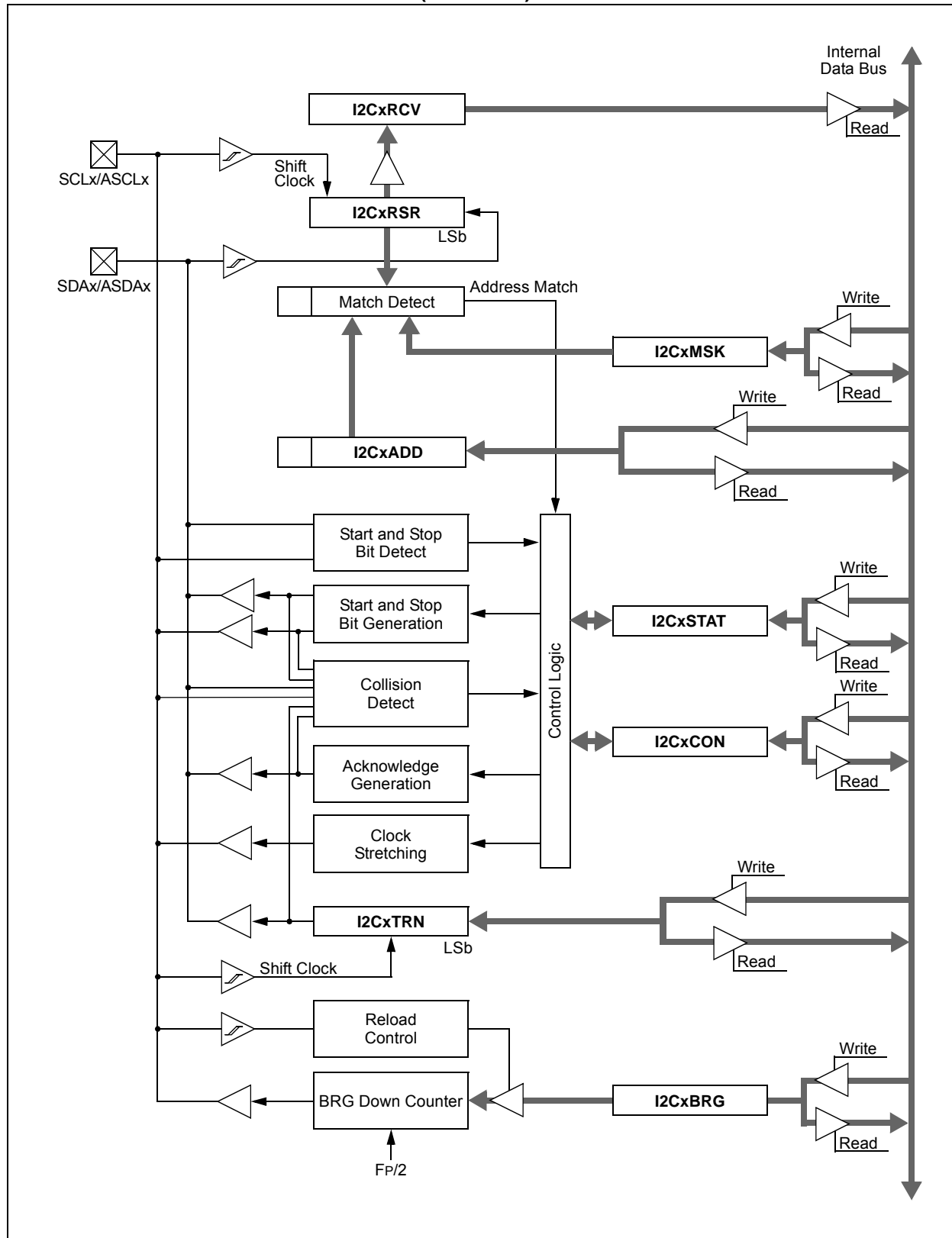
0000001 = Input tied to CMP1

0000000 = Input tied to Vss

REGISTER 17-2: QEIXIOC: QEIX I/O CONTROL REGISTER (CONTINUED)

| | |
|-------|--|
| bit 2 | INDEX: Status of INDXX Input Pin After Polarity Control bit 1 = Pin is at logic '1' 0 = Pin is at logic '0' |
| bit 1 | QEB: Status of QEBx Input Pin After Polarity Control and SWPAB Pin Swapping bit 1 = Pin is at logic '1' 0 = Pin is at logic '0' |
| bit 0 | QEA: Status of QEAx Input Pin After Polarity Control and SWPAB Pin Swapping bit 1 = Pin is at logic '1' 0 = Pin is at logic '0' |

FIGURE 19-1: I2Cx BLOCK DIAGRAM (x = 1 OR 2)



REGISTER 19-2: I2CxSTAT: I2Cx STATUS REGISTER

| | | | | | | | |
|----------|----------|-----|-----|-----|-----------|----------|----------|
| R-0, HSC | R-0, HSC | U-0 | U-0 | U-0 | R/C-0, HS | R-0, HSC | R-0, HSC |
| ACKSTAT | TRSTAT | — | — | — | BCL | GCSTAT | ADD10 |
| bit 15 | | | | | | bit 8 | |

| | | | | | | | |
|-----------|-----------|----------|------------|------------|----------|----------|----------|
| R/C-0, HS | R/C-0, HS | R-0, HSC | R/C-0, HSC | R/C-0, HSC | R-0, HSC | R-0, HSC | R-0, HSC |
| IWCOL | I2COV | D_A | P | S | R_W | RBF | TBF |
| bit 7 | | | | | | bit 0 | |

| | | |
|-------------------|-------------------|--|
| Legend: | C = Clearable bit | U = Unimplemented bit, read as '0' |
| R = Readable bit | W = Writable bit | HS = Hardware Settable bit HSC = Hardware Settable/Clearable bit |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared x = Bit is unknown |

- bit 15 **ACKSTAT:** Acknowledge Status bit
(when operating as I²C™ master, applicable to master transmit operation)
1 = NACK received from slave
0 = ACK received from slave
Hardware sets or clears at the end of a slave Acknowledge.
- bit 14 **TRSTAT:** Transmit Status bit (when operating as I²C master, applicable to master transmit operation)
1 = Master transmit is in progress (8 bits + ACK)
0 = Master transmit is not in progress
Hardware sets at the beginning of a master transmission. Hardware clears at the end of a slave Acknowledge.
- bit 13-11 **Unimplemented:** Read as '0'
- bit 10 **BCL:** Master Bus Collision Detect bit
1 = A bus collision has been detected during a master operation
0 = No collision
Hardware sets at detection of a bus collision.
- bit 9 **GCSTAT:** General Call Status bit
1 = General call address was received
0 = General call address was not received
Hardware sets when address matches the general call address. Hardware clears at Stop detection.
- bit 8 **ADD10:** 10-Bit Address Status bit
1 = 10-bit address was matched
0 = 10-bit address was not matched
Hardware sets at a match of the 2nd byte of a matched 10-bit address. Hardware clears at Stop detection.
- bit 7 **IWCOL:** I2Cx Write Collision Detect bit
1 = An attempt to write to the I2CxTRN register failed because the I²C module is busy
0 = No collision
Hardware sets at an occurrence of a write to I2CxTRN while busy (cleared by software).
- bit 6 **I2COV:** I2Cx Receive Overflow Flag bit
1 = A byte was received while the I2CxRCV register was still holding the previous byte
0 = No overflow
Hardware sets at an attempt to transfer I2CxRSR to I2CxRCV (cleared by software).
- bit 5 **D_A:** Data/Address bit (when operating as I²C slave)
1 = Indicates that the last byte received was data
0 = Indicates that the last byte received was a device address
Hardware clears at a device address match. Hardware sets by reception of a slave byte.
- bit 4 **P:** Stop bit
1 = Indicates that a Stop bit has been detected last
0 = Stop bit was not detected last
Hardware sets or clears when Start, Repeated Start or Stop is detected.

20.2 UART Control Registers

REGISTER 20-1: UxMODE: UARTx MODE REGISTER

| | | | | | | | |
|-----------------------|-----|-------|---------------------|-------|-----|-------|-------|
| R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | U-0 | R/W-0 | R/W-0 |
| UARTEN ⁽¹⁾ | — | USIDL | IREN ⁽²⁾ | RTSMD | — | UEN1 | UEN0 |
| bit 15 | | | | | | bit 8 | |

| | | | | | | | |
|-----------|--------|-----------|--------|-------|--------|--------|-------|
| R/W-0, HC | R/W-0 | R/W-0, HC | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| WAKE | LPBACK | ABAUD | URXINV | BRGH | PDSEL1 | PDSEL0 | STSEL |
| bit 7 | | | | | | bit 0 | |

| | | | |
|-------------------|-----------------------------|------------------------------------|--------------------|
| Legend: | HC = Hardware Clearable bit | | |
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

- bit 15 **UARTEN:** UARTx Enable bit⁽¹⁾
1 = UARTx is enabled; all UARTx pins are controlled by UARTx as defined by UEN<1:0>
0 = UARTx is disabled; all UARTx pins are controlled by PORT latches; UARTx power consumption is minimal
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **USIDL:** UARTx Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode
- bit 12 **IREN:** IrDA[®] Encoder and Decoder Enable bit⁽²⁾
1 = IrDA encoder and decoder are enabled
0 = IrDA encoder and decoder are disabled
- bit 11 **RTSMD:** Mode Selection for $\overline{\text{UxRTS}}$ Pin bit
1 = $\overline{\text{UxRTS}}$ pin is in Simplex mode
0 = $\overline{\text{UxRTS}}$ pin is in Flow Control mode
- bit 10 **Unimplemented:** Read as '0'
- bit 9-8 **UEN<1:0>:** UARTx Pin Enable bits
11 = UxTX, UxRX and BCLKx pins are enabled and used; $\overline{\text{UxCTS}}$ pin is controlled by PORT latches⁽³⁾
10 = UxTX, UxRX, $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ pins are enabled and used⁽⁴⁾
01 = UxTX, UxRX and $\overline{\text{UxRTS}}$ pins are enabled and used; $\overline{\text{UxCTS}}$ pin is controlled by PORT latches⁽⁴⁾
00 = UxTX and UxRX pins are enabled and used; $\overline{\text{UxCTS}}$ and $\overline{\text{UxRTS}}$ /BCLKx pins are controlled by PORT latches
- bit 7 **WAKE:** Wake-up on Start bit Detect During Sleep Mode Enable bit
1 = UARTx continues to sample the UxRX pin, interrupt is generated on the falling edge; bit is cleared in hardware on the following rising edge
0 = No wake-up is enabled
- bit 6 **LPBACK:** UARTx Loopback Mode Select bit
1 = Enables Loopback mode
0 = Loopback mode is disabled

- Note 1:** Refer to the “dsPIC33/PIC24 Family Reference Manual”, “Universal Asynchronous Receiver Transmitter (UART)” (DS70000582) for information on enabling the UART module for receive or transmit operation.
- 2:** This feature is only available for the 16x BRG mode (BRGH = 0).
- 3:** This feature is only available on 44-pin and 64-pin devices.
- 4:** This feature is only available on 64-pin devices.

REGISTER 20-2: UxSTA: UARTx STATUS AND CONTROL REGISTER (CONTINUED)

- bit 5 **ADDEN**: Address Character Detect bit (bit 8 of received data = 1)
1 = Address Detect mode is enabled; if 9-bit mode is not selected, this does not take effect
0 = Address Detect mode is disabled
- bit 4 **RIDLE**: Receiver Idle bit (read-only)
1 = Receiver is Idle
0 = Receiver is active
- bit 3 **PERR**: Parity Error Status bit (read-only)
1 = Parity error has been detected for the current character (character at the top of the receive FIFO)
0 = Parity error has not been detected
- bit 2 **FERR**: Framing Error Status bit (read-only)
1 = Framing error has been detected for the current character (character at the top of the receive FIFO)
0 = Framing error has not been detected
- bit 1 **OERR**: Receive Buffer Overrun Error Status bit (clear/read-only)
1 = Receive buffer has overflowed
0 = Receive buffer has not overflowed; clearing a previously set OERR bit (1 → 0 transition) resets the receive buffer and the UxRSR to the empty state
- bit 0 **URXDA**: UARTx Receive Buffer Data Available bit (read-only)
1 = Receive buffer has data, at least one more character can be read
0 = Receive buffer is empty

Note 1: Refer to the “dsPIC33/PIC24 Family Reference Manual”, “Universal Asynchronous Receiver Transmitter (UART)” (DS70000582) for information on enabling the UART module for transmit operation.

22.1 CTMU Control Registers

REGISTER 22-1: CTMUCON1: CTMU CONTROL REGISTER 1

| | | | | | | | |
|--------|-----|----------|-------|-------|----------|------------------------|--------|
| R/W-0 | U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| CTMUEN | — | CTMUSIDL | TGEN | EDGEN | EDGSEQEN | IDISSEN ⁽¹⁾ | CTTRIG |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|-------|-----|-----|-----|-----|-----|-----|-------|
| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| — | — | — | — | — | — | — | — |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15 **CTMUEN:** CTMU Enable bit
 1 = Module is enabled
 0 = Module is disabled
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **CTMUSIDL:** CTMU Stop in Idle Mode bit
 1 = Discontinues module operation when device enters Idle mode
 0 = Continues module operation in Idle mode
- bit 12 **TGEN:** Time Generation Enable bit
 1 = Enables edge delay generation
 0 = Disables edge delay generation
- bit 11 **EDGEN:** Edge Enable bit
 1 = Hardware modules are used to trigger edges (TMRx, CTEDx, etc.)
 0 = Software is used to trigger edges (manual set of EDGxSTAT)
- bit 10 **EDGSEQEN:** Edge Sequence Enable bit
 1 = Edge 1 event must occur before Edge 2 event can occur
 0 = No edge sequence is needed
- bit 9 **IDISSEN:** Analog Current Source Control bit⁽¹⁾
 1 = Analog current source output is grounded
 0 = Analog current source output is not grounded
- bit 8 **CTTRIG:** ADCx Trigger Control bit
 1 = CTMU triggers ADCx start of conversion
 0 = CTMU does not trigger ADCx start of conversion
- bit 7-0 **Unimplemented:** Read as '0'

Note 1: The ADCx module Sample-and-Hold (S&H) capacitor is not automatically discharged between sample/conversion cycles. Any software using the ADCx as part of a capacitance measurement must discharge the ADCx capacitor before conducting the measurement. The IDISSEN bit, when set to '1', performs this function. The ADCx must be sampling while the IDISSEN bit is active to connect the discharge sink to the capacitor array.

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REGISTER 23-8: ADxCSSL: ADCx INPUT SCAN SELECT REGISTER LOW^(1,2)

| | | | | | | | |
|-----------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| CSS<15:8> | | | | | | | |
| bit 15 | | | | bit 8 | | | |

| | | | | | | | |
|----------|-------|-------|-------|-------|-------|-------|-------|
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| CSS<7:0> | | | | | | | |
| bit 7 | | | | bit 0 | | | |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **CSS<15:0>**: ADCx Input Scan Selection bits

1 = Selects ANx for input scan

0 = Skips ANx for input scan

Note 1: On devices with less than 16 analog inputs, all bits in this register can be selected by the user application. However, inputs selected for scan without a corresponding input on the device convert VREFL.

2: CSSx = ANx, where 'x' = 0-15.

REGISTER 26-6: CMxFLTR: COMPARATOR x FILTER CONTROL REGISTER

| | | | | | | | |
|--------|-----|-----|-----|-----|-----|-----|-------|
| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| | | | | | | | |
|-------|--------|--------|--------|---------|--------|--------|--------|
| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| — | CFSEL2 | CFSEL1 | CFSEL0 | CFLTREN | CFDIV2 | CFDIV1 | CFDIV0 |
| bit 7 | | | | | | | bit 0 |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-7 **Unimplemented:** Read as '0'

bit 6-4 **CFSEL<2:0>:** Comparator Filter Input Clock Select bits

111 = T5CLK⁽¹⁾

110 = T4CLK⁽²⁾

101 = T3CLK⁽¹⁾

100 = T2CLK⁽²⁾

011 = SYNCO2

010 = SYNCO1⁽³⁾

001 = Fosc⁽⁴⁾

000 = Fp⁽⁴⁾

bit 3 **CFLTREN:** Comparator Filter Enable bit

1 = Digital filter is enabled

0 = Digital filter is disabled

bit 2-0 **CFDIV<2:0>:** Comparator Filter Clock Divide Select bits

111 = Clock Divide 1:128

110 = Clock Divide 1:64

101 = Clock Divide 1:32

100 = Clock Divide 1:16

011 = Clock Divide 1:8

010 = Clock Divide 1:4

001 = Clock Divide 1:2

000 = Clock Divide 1:1

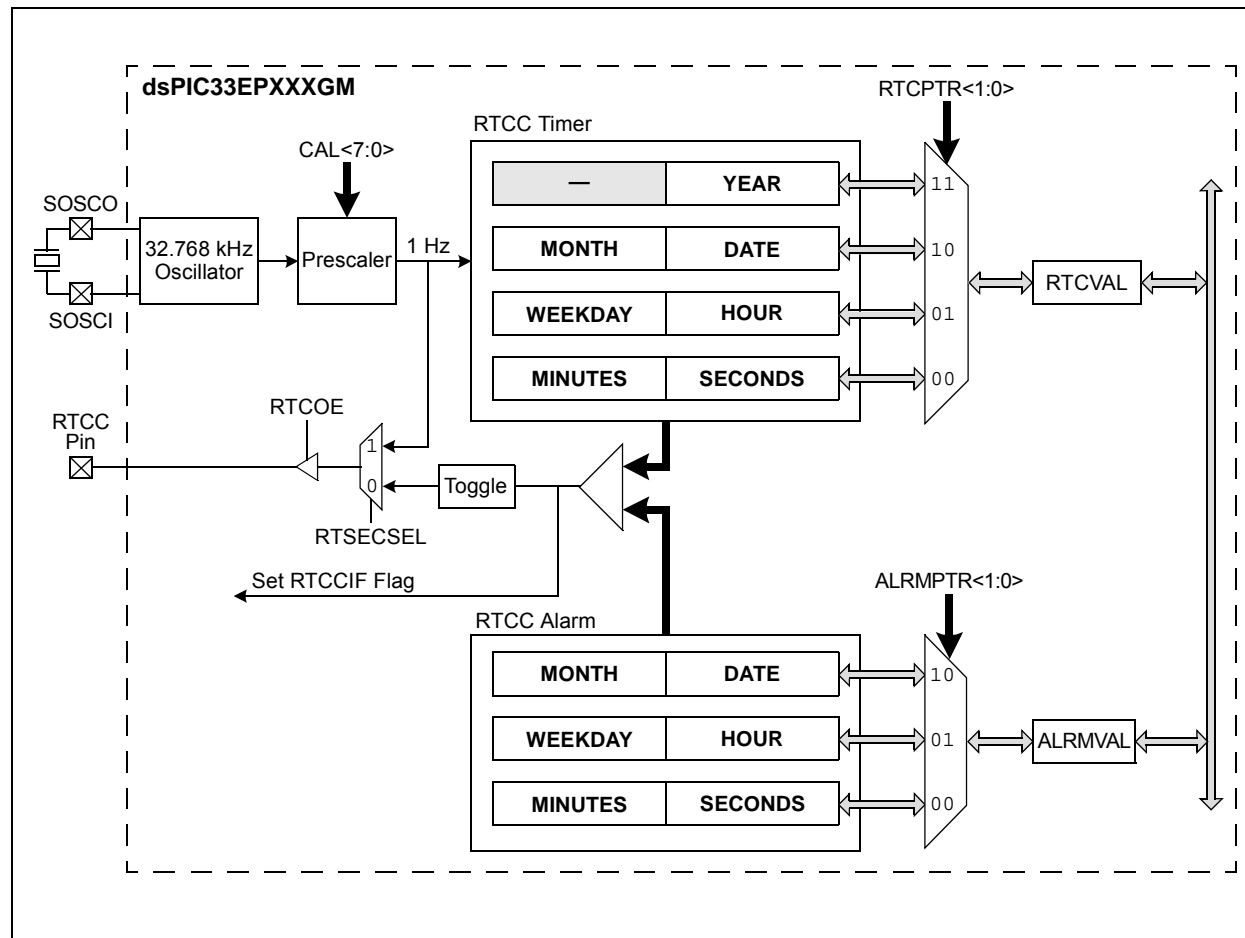
Note 1: See the Type C Timer Block Diagram (Figure 13-2).

2: See the Type B Timer Block Diagram (Figure 13-1).

3: See the PWMx Module Register Interconnect Diagram (Figure 16-2).

4: See the Oscillator System Diagram (Figure 9-1).

FIGURE 27-1: RTCC BLOCK DIAGRAM



Note: The RTCC is only operational on devices which include the SOSC; therefore, the RTCC module is not available on 44-pin devices.

REGISTER 28-2: PMMODE: PARALLEL MASTER PORT MODE REGISTER⁽⁴⁾ (CONTINUED)

bit 5-2 **WAITM<3:0>**: Read to Byte Enable Strobe Wait State Configuration bits

1111 = Wait of additional 15 TP

•
•
•

0001 = Wait of additional 1 TP

0000 = No additional Wait cycles (operation forced into one TP)

bit 1-0 **WAITE<1:0>**: Data Hold After Strobe Wait State Configuration bits^(1,2,3)

11 = Wait of 4 TP

10 = Wait of 3 TP

01 = Wait of 2 TP

00 = Wait of 1 TP

Note 1: The applied Wait state depends on whether data and address are multiplexed or demultiplexed. See **Section 4.1.8 “Wait States”** in the **“Parallel Master Port (PMP)”** (DS70576) in the *“dsPIC33/PIC24 Family Reference Manual”* for more information.

2: WAITB<1:0> and WAITE<1:0> bits are ignored whenever WAITM<3:0> = 0000.

3: TP = 1/Fp.

4: This register is not available on 44-pin devices.

FIGURE 33-27: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 0, SMP = 0)
TIMING CHARACTERISTICS

