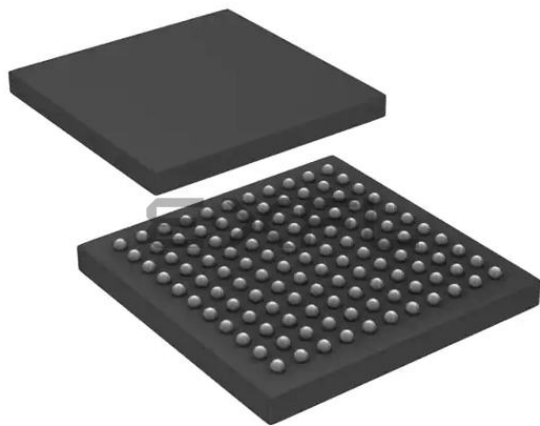




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Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPS
Connectivity	I ² C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, Motor Control PWM, POR, PWM, WDT
Number of I/O	85
Program Memory Size	512KB (170K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	-
Data Converters	A/D 49x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	121-TFBGA
Supplier Device Package	121-TFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep512gm310t-i-bg

FIGURE 4-3: PROGRAM MEMORY MAP FOR dsPIC33EP512GM3XX/6XX/7XX DEVICES⁽¹⁾

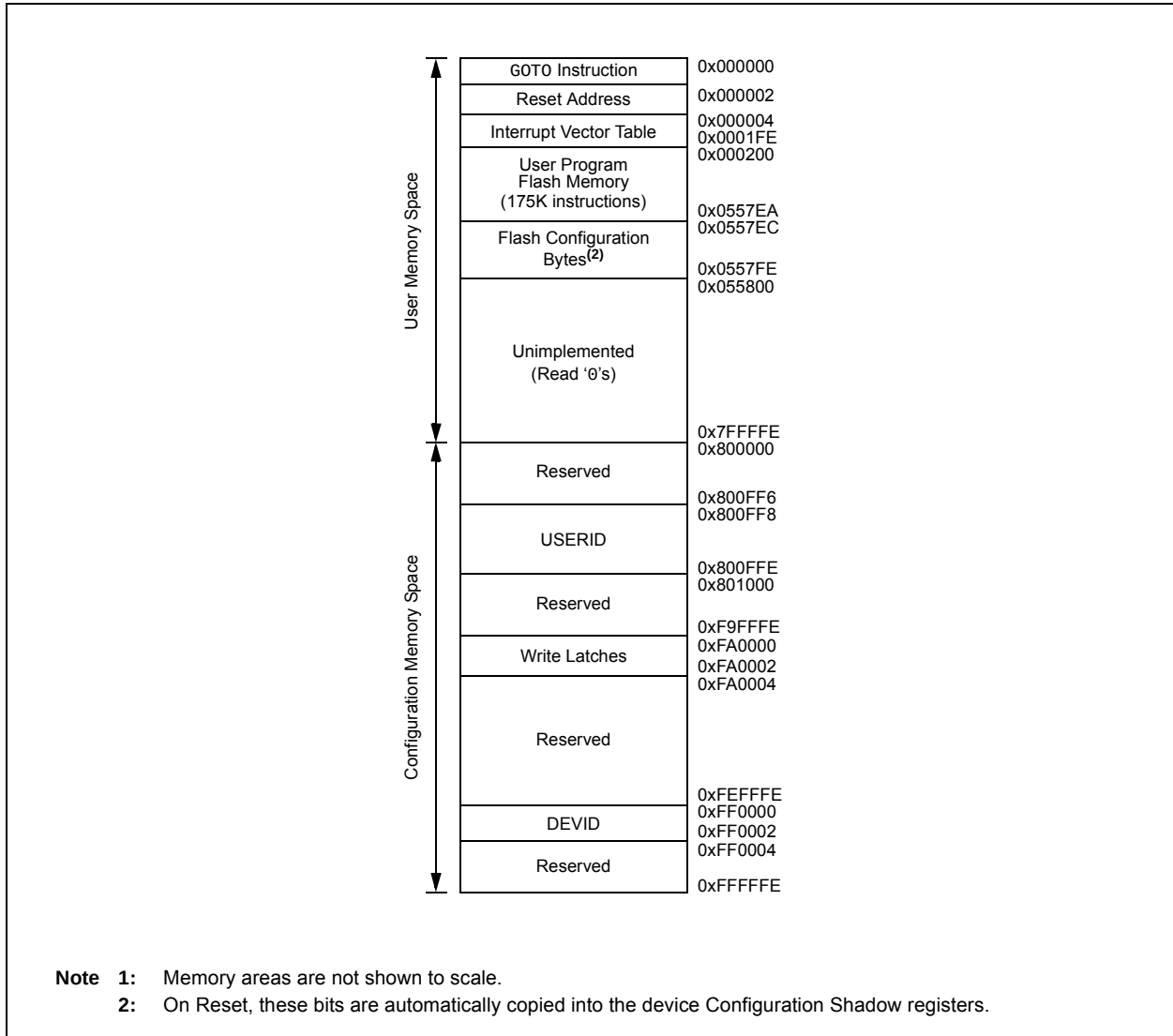


TABLE 4-2: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EPXXXGM6XX/7XX DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
INTCON1	08C0	NSTDIS	OVAERR	OVBERR	COVAERR	COVBERR	OVATE	OVATE	COVTE	SFTACERR	DIV0ERR	DMACERR	MATHERR	ADDRERR	STKERR	OSCFail	—	0000
INTCON2	08C2	GIE	DISI	SWTRAP	—	—	—	—	—	—	—	—	—	—	INT2EP	INT1EP	INT0EP	0000
INTCON3	08C4	—	—	—	—	—	—	—	—	—	—	DAE	DOOVR	—	—	—	—	0000
INTCON4	08C6	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SGHT	0000
IFS0	0800	—	DMA1IF	AD1IF	U1TXIF	U1RXIF	SPI1IF	SPI1EIF	T3IF	T2IF	OC2IF	IC2IF	DMA0IF	T1IF	OC1IF	IC1IF	INT0IF	0000
IFS1	0802	U2TXIF	U2RXIF	INT2IF	T5IF	T4IF	OC4IF	OC3IF	DMA2IF	IC8IF	IC7IF	AD2IF	INT1IF	CNIF	CMP1IF	MI2C1IF	SI2C1IF	0000
IFS2	0804	T6IF	—	PMPIF ⁽¹⁾	OC8IF	OC7IF	OC6IF	OC5IF	IC6IF	IC5IF	IC4IF	IC3IF	DMA3IF	C1IF	C1RXIF	SPI2IF	SPI2EIF	0000
IFS3	0806	FLT1IF	RTCCIF ⁽²⁾	—	DCIIF	DCIEIF	QE1IF	PSEMIIF	C2IF	C2RXIF	INT4IF	INT3IF	T9IF	T8IF	MI2C2IF	SI2C2IF	T7IF	0000
IFS4	0808	—	—	CTMUIF	FLT4IF	QE2IF	FLT3IF	PSESMIF	—	C2TXIF	C1TXIF	—	—	CRCIF	U2EIF	U1EIF	FLT2IF	0000
IFS5	080A	PWM2IF	PWM1IF	—	—	SPI3IF	SPI3EIF	U4TXIF	U4RXIF	U4EIF	—	—	—	U3TXIF	U3RXIF	U3EIF	—	0000
IFS6	080C	—	—	—	—	—	—	—	—	—	—	—	—	PWM6IF	PWM5IF	PWM4IF	PWM3IF	0000
IFS8	0810	JTAGIF	ICDIF	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IFS9	0812	—	—	—	—	—	—	—	—	—	PTG3IF	PTG2IF	PTG1IF	PTG0IF	PTGWDTIF	PTGSTPIF	—	0000
IEC0	0820	—	DMA1IE	AD1IE	U1TXIE	U1RXIE	SPI1IE	SPI1EIE	T3IE	T2IE	OC2IE	IC2IE	DMA0IE	T1IE	OC1IE	IC1IE	INT0IE	0000
IEC1	0822	U2TXIE	U2RXIE	INT2IE	T5IE	T4IE	OC4IE	OC3IE	DMA2IE	IC8IE	IC7IE	AD2IE	INT1IE	CNIE	CMP1IE	MI2C1IE	SI2C1IE	0000
IEC2	0824	T6IE	—	PMPIE ⁽¹⁾	OC8IE	OC7IE	OC6IE	OC5IE	IC6IE	IC5IE	IC4IE	IC3IE	DMA3IE	C1IE	C1RXIE	SPI2IE	SPI2EIE	0000
IEC3	0826	FLT1IE	RTCCIE ⁽²⁾	—	DCIIE	DCIEIE	QE1IE	PSEMIIE	C2IE	C2RXIE	INT4IE	INT3IE	T9IE	T8IE	MI2C2IE	SI2C2IE	T7IE	0000
IEC4	0828	—	—	CTMUIE	FLT4IE	QE2IE	FLT3IE	PSESMIE	—	C2TXIE	C1TXIE	—	—	CRCIE	U2EIE	U1EIE	FLT2IE	0000
IEC5	082A	PWM2IE	PWM1IE	—	—	SPI3IE	SPI3EIE	U4TXIE	U4RXIE	U4EIE	—	—	—	U3TXIE	U3RXIE	U3EIE	—	0000
IEC6	082C	—	—	—	—	—	—	—	—	—	—	—	—	PWM6IE	PWM5IE	PWM4IE	PWM3IE	0000
IEC8	0830	JTAGIE	ICDIE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IEC9	0832	—	—	—	—	—	—	—	—	—	PTG3IE	PTG2IE	PTG1IE	PTG0IE	PTGWDTIE	PTGSTPIE	—	0000
IPC0	0840	—	T1IP2	T1IP1	T1IP0	—	OC1IP2	OC1IP1	OC1IP0	—	IC1IP2	IC1IP1	IC1IP0	—	INT0IP2	INT0IP1	INT0IP0	4444
IPC1	0842	—	T2IP2	T2IP1	T2IP0	—	OC2IP2	OC2IP1	OC2IP0	—	IC2IP2	IC2IP1	IC2IP0	—	DMA0IP2	DMA0IP1	DMA0IP0	4444
IPC2	0844	—	U1RXIP2	U1RXIP1	U1RXIP0	—	SPI1IP2	SPI1IP1	SPI1IP0	—	SPI1EIP2	SPI1EIP1	SPI1EIP0	—	T3IP2	T3IP1	T3IP0	4444
IPC3	0846	—	—	—	—	—	DMA1IP2	DMA1IP1	DMA1IP0	—	AD1IP2	AD1IP1	AD1IP0	—	U1TXIP2	U1TXIP1	U1TXIP0	4444
IPC4	0848	—	CNIP2	CNIP1	CNIP0	—	CMP1IP2	CMP1IP1	CMP1IP0	—	MI2C1IP2	MI2C1IP1	MI2C1IP0	—	SI2C1IP2	SI2C1IP1	SI2C1IP0	4444
IPC5	084A	—	IC8IP2	IC8IP1	IC8IP0	—	IC7IP2	IC7IP1	IC7IP0	—	AD2IP2	AD2IP1	AD2IP0	—	INT1IP2	INT1IP1	INT1IP0	4444
IPC6	084C	—	T4IP2	T4IP1	T4IP0	—	OC4IP2	OC4IP1	OC4IP0	—	OC3IP2	OC3IP1	OC3IP0	—	DMA2IP2	DMA2IP1	DMA2IP0	4444
IPC7	084E	—	U2TXIP2	U2TXIP1	U2TXIP0	—	U2RXIP2	U2RXIP1	U2RXIP0	—	INT2IP2	INT2IP1	INT2IP0	—	T5IP2	T5IP1	T5IP0	4444
IPC8	0850	—	C1IP2	C1IP1	C1IP0	—	C1RXIP2	C1RXIP1	C1RXIP0	—	SPI2IP2	SPI2IP1	SPI2IP0	—	SPI2EIP2	SPI2EIP1	SPI2EIP0	4444
IPC9	0852	—	IC5IP2	IC5IP1	IC5IP0	—	IC4IP2	IC4IP1	IC4IP0	—	IC3IP2	IC3IP1	IC3IP0	—	DMA3IP2	DMA3IP1	DMA3IP0	4444
IPC10	0854	—	OC7IP2	OC7IP1	OC7IP0	—	OC6IP2	OC6IP1	OC6IP0	—	OC5IP2	OC5IP1	OC5IP0	—	IC6IP2	IC6IP1	IC6IP0	4444

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: The PMPIF/PMPIE/PMPIP_x flags are not available on 44-pin devices.

Note 2: The RTCCIF/RTCCIE/RTCCIP_x flags are not available on 44-pin devices.

TABLE 4-3: INTERRUPT CONTROLLER REGISTER MAP FOR dsPIC33EPXXXGM3XX DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
INTCON1	08C0	NSTDIS	OVAERR	OVBERR	COVAERR	COVBERR	OVATE	OVBT	COVTE	SFTACERR	DIV0ERR	DMACERR	MATHERR	ADDRERR	STKERR	OSCFail	—	0000
INTCON2	08C2	GIE	DISI	SWTRAP	—	—	—	—	—	—	—	—	—	—	INT2EP	INT1EP	INT0EP	0000
INTCON3	08C4	—	—	—	—	—	—	—	—	—	—	DAE	DOOVR	—	—	—	—	0000
INTCON4	08C6	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SGHT	0000
IFS0	0800	—	DMA1IF	AD1IF	U1TXIF	U1RXIF	SPI1IF	SPI1EIF	T3IF	T2IF	OC2IF	IC2IF	DMA0IF	T1IF	OC1IF	IC1IF	INT0IF	0000
IFS1	0802	U2TXIF	U2RXIF	INT2IF	T5IF	T4IF	OC4IF	OC3IF	DMA2IF	IC8IF	IC7IF	AD2IF	INT1IF	CNIF	CMPIF	MI2C1IF	SI2C1IF	0000
IFS2	0804	T6IF	—	PMPIF ⁽¹⁾	OC8IF	OC7IF	OC6IF	OC5IF	IC6IF	IC5IF	IC4IF	IC3IF	DMA3IF	—	—	SPI2IF	SPI2EIF	0000
IFS3	0806	FLT1IF	RTCCIF ⁽²⁾	—	DCIIF	DCIEIF	QE1IF	PSEMIF	—	—	INT4IF	INT3IF	T9IF	T8IF	MI2C2IF	SI2C2IF	T7IF	0000
IFS4	0808	—	—	CTMUIF	FLT4IF	QE12IF	FLT3IF	PSESMIF	—	—	—	—	—	CRCIF	U2EIF	U1EIF	FLT2IF	0000
IFS5	080A	PWM2IF	PWM1IF	—	—	SPI3IF	SPI3EIF	U4TXIF	U4RXIF	U4EIF	—	—	—	U3TXIF	U3RXIF	U3EIF	—	0000
IFS6	080C	—	—	—	—	—	—	—	—	—	—	—	—	PWM6IF	PWM5IF	PWM4IF	PWM3IF	0000
IFS8	0810	JTAGIF	ICDIF	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IFS9	0812	—	—	—	—	—	—	—	—	—	PTG3IF	PTG2IF	PTG1IF	PTG0IF	PTGWDTIF	PTGSTIEIF	—	0000
IEC0	0820	—	DMA1IE	AD1IE	U1TXIE	U1RXIE	SPI1IE	SPI1EIE	T3IE	T2IE	OC2IE	IC2IE	DMA0IE	T1IE	OC1IE	IC1IE	INT0IE	0000
IEC1	0822	U2TXIE	U2RXIE	INT2IE	T5IE	T4IE	OC4IE	OC3IE	DMA2IE	IC8IE	IC7IE	AD2IE	INT1IE	CNIE	CMPIE	MI2C1IE	SI2C1IE	0000
IEC2	0824	T6IE	—	PMPIE ⁽¹⁾	OC8IE	OC7IE	OC6IE	OC5IE	IC6IE	IC5IE	IC4IE	IC3IE	DMA3IE	—	—	SPI2IE	SPI2EIE	0000
IEC3	0826	FLT1IE	RTCCIE ⁽²⁾	—	DCIE	DCIEIE	QE1IE	PSEMIE	—	—	INT4IE	INT3IE	T9IE	T8IE	MI2C2IE	SI2C2IE	T7IE	0000
IEC4	0828	—	—	CTMUIE	FLT4IE	QE12IE	FLT3IE	PSESMIE	—	—	—	—	—	CRCIE	U2EIE	U1EIE	FLT2IE	0000
IEC5	082A	PWM2IE	PWM1IE	—	—	SPI3IE	SPI3EIE	U4TXIE	U4RXIE	U4EIE	—	—	—	U3TXIE	U3RXIE	U3EIE	—	0000
IEC6	082C	—	—	—	—	—	—	—	—	—	—	—	—	PWM6IE	PWM5IE	PWM4IE	PWM3IE	0000
IEC8	0830	JTAGIE	ICDIE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000
IEC9	0832	—	—	—	—	—	—	—	—	—	PTG3IE	PTG2IE	PTG1IE	PTG0IE	PTGWDTIE	PTGSTIEIE	—	0000
IPC0	0840	—	T1IP2	T1IP1	T1IP0	—	OC1IP2	OC1IP1	OC1IP0	—	IC1IP2	IC1IP1	IC1IP0	—	INT0IP2	INT0IP1	INT0IP0	4444
IPC1	0842	—	T2IP2	T2IP1	T2IP0	—	OC2IP2	OC2IP1	OC2IP0	—	IC2IP2	IC2IP1	IC2IP0	—	DMA0IP2	DMA0IP1	DMA0IP0	4444
IPC2	0844	—	U1RXIP2	U1RXIP1	U1RXIP0	—	SPI1IP2	SPI1IP1	SPI1IP0	—	SPI1EIP2	SPI1EIP1	SPI1EIP0	—	T3IP2	T3IP1	T3IP0	4444
IPC3	0846	—	—	—	—	—	DMA1IP2	DMA1IP1	DMA1IP0	—	AD1IP2	AD1IP1	AD1IP0	—	U1TXIP2	U1TXIP1	U1TXIP0	4444
IPC4	0848	—	CNIP2	CNIP1	CNIP0	—	CMPIP2	CMPIP1	CMPIP0	—	MI2C1IP2	MI2C1IP1	MI2C1IP0	—	SI2C1IP2	SI2C1IP1	SI2C1IP0	4444
IPC5	084A	—	IC8IP2	IC8IP1	IC8IP0	—	IC7IP2	IC7IP1	IC7IP0	—	AD2IP2	AD2IP1	AD2IP0	—	INT1IP2	INT1IP1	INT1IP0	4444
IPC6	084C	—	T4IP2	T4IP1	T4IP0	—	OC4IP2	OC4IP1	OC4IP0	—	OC3IP2	OC3IP1	OC3IP0	—	DMA2IP2	DMA2IP1	DMA2IP0	4444
IPC7	084E	—	U2TXIP2	U2TXIP1	U2TXIP0	—	U2RXIP2	U2RXIP1	U2RXIP0	—	INT2IP2	INT2IP1	INT2IP0	—	T5IP2	T5IP1	T5IP0	4444
IPC8	0850	—	—	—	—	—	—	—	—	—	SPI2IP2	SPI2IP1	SPI2IP0	—	SPI2EIP2	SPI2EIP1	SPI2EIP0	4444
IPC9	0852	—	IC5IP2	IC5IP1	IC5IP0	—	IC4IP2	IC4IP1	IC4IP0	—	IC3IP2	IC3IP1	IC3IP0	—	DMA3IP2	DMA3IP1	DMA3IP0	4444
IPC10	0854	—	OC7IP2	OC7IP1	OC7IP0	—	OC6IP2	OC6IP1	OC6IP0	—	OC5IP2	OC5IP1	OC5IP0	—	IC6IP2	IC6IP1	IC6IP0	4444

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: The PMPIF/PMPIE/PMPIP flags are not available on 44-pin devices.

Note 2: The RTCCIF/RTCCIE/RTCCIP flags are not available on 44-pin devices.

4.3.2 EXTENDED X DATA SPACE

The lower portion of the base address space range, between 0x0000 and 0x7FFF, is always accessible regardless of the contents of the Data Space Page registers. It is indirectly addressable through the register indirect instructions. It can be regarded as being located in the default EDS Page 0 (i.e., EDS address range of 0x000000 to 0x007FFF with the base address bit, EA<15> = 0, for this address range). However, Page 0 cannot be accessed through the upper 32 Kbytes, 0x8000 to 0xFFFF, of Base Data Space, in combination with DSRPAG = 0x000 or DSWPAG = 0x000. Consequently, DSRPAG and DSWPAG are initialized to 0x001 at Reset.

- Note 1:** DSxPAG should not be used to access Page 0. An EDS access with DSxPAG set to 0x000 will generate an address error trap.

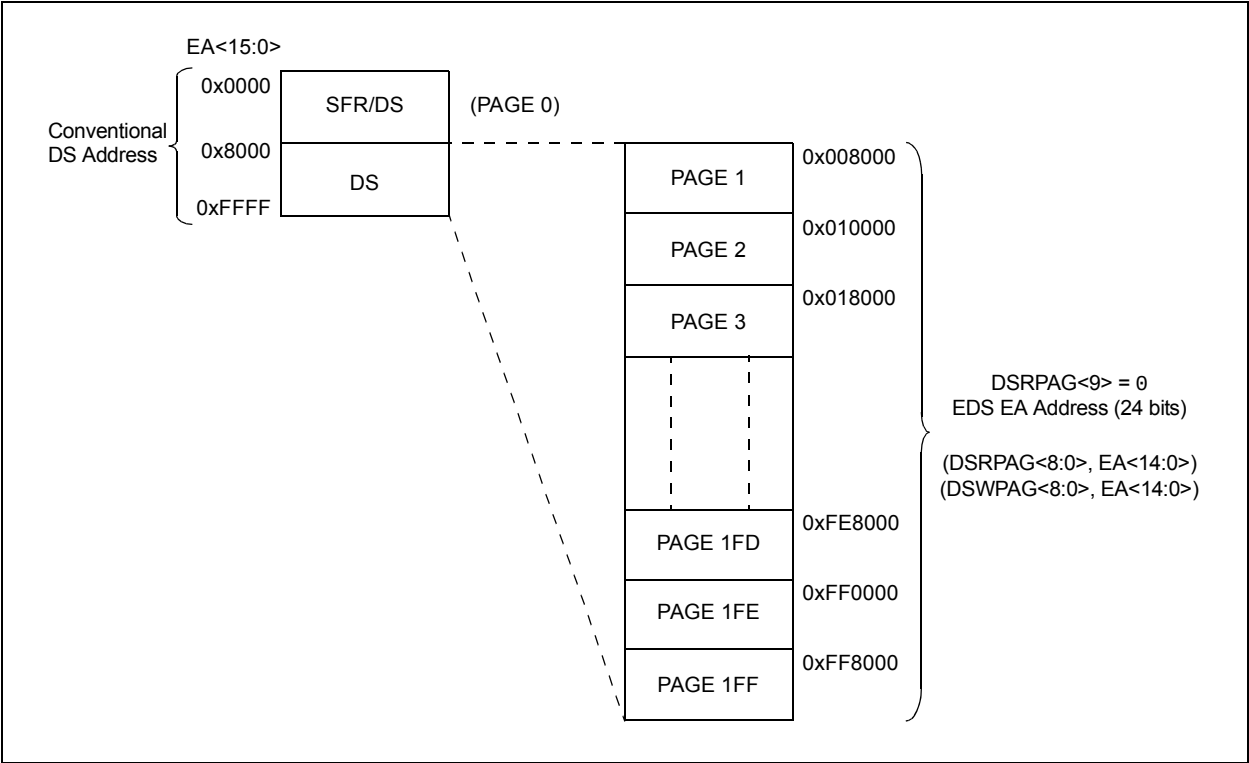
2: Clearing the DSxPAG in software has no effect.

The remaining pages, including both EDS and PSV pages, are only accessible using the DSRPAG or DSWPAG register, in combination with the upper 32 Kbytes, 0x8000 to 0xFFFF, of the base address, where the base address bit, EA<15> = 1.

For example, when DSRPAG = 0x001 or DSWPAG = 0x001, accesses to the upper 32 Kbytes, 0x8000 to 0xFFFF, of the Data Space will map to the EDS address range of 0x008000 to 0x00FFFF. When DSRPAG = 0x002 or DSWPAG = 0x002, accesses to the upper 32 Kbytes of the Data Space will map to the EDS address range of 0x010000 to 0x017FFF and so on, as shown in the EDS memory map in Figure 4-11.

For more information on the PSV page access, using Data Space Page registers, refer to the “**Program Space Visibility from Data Space**” section in “**Program Memory**” (DS70613) of the “dsPIC33/PIC24 Family Reference Manual”.

FIGURE 4-11: EDS MEMORY MAP



5.2 RTSP Operation

RTSP allows the user application to erase a single page of memory, program a row and to program two instruction words at a time. See Table 1 in the “dsPIC33EPXXXGM3XX/6XX/7XX Product Family” section for the page sizes of each device.

The Flash program memory array is organized into rows of 64 instructions or 192 bytes. RTSP allows the user application to erase a page of program memory, which consists of eight rows (512 instructions) at a time, and to program one row or two adjacent words at a time. The 8-row erase pages and single row write rows are edge-aligned, from the beginning of program memory, on boundaries of 1536 bytes and 192 bytes, respectively.

For more information on erasing and programming Flash memory, refer to the “dsPIC33/PIC24 Family Reference Manual”, “Flash Programming” (DS70609).

5.3 Programming Operations

A complete programming sequence is necessary for programming or erasing the internal Flash in RTSP mode. The processor stalls (waits) until the programming operation is finished.

For erase and program times, refer to Parameters D137a and D137b (Page Erase Time), and D138a and D138b (Word Write Cycle Time), in Table 33-13.

Setting the WR bit (NVMCON<15>) starts the operation and the WR bit is automatically cleared when the operation is finished.

5.3.1 PROGRAMMING ALGORITHM FOR FLASH PROGRAM MEMORY

Programmers can program two adjacent words (24 bits x 2) of program Flash memory at a time on every other word address boundary (0x000002, 0x000006, 0x00000A, etc.). To do this, it is necessary to erase the page that contains the desired address of the location the user wants to change. Programmers can also program a row of data (64 instruction words/192 bytes) at a time using the row programming feature present in these devices. For row programming, the source data is fetched directly from the data memory (RAM) on these devices. Two new registers have been provided to point to the RAM location where the source data resides. The page that has the row to be programmed must first be erased before the programming operation.

For protection against accidental operations, the write initiate sequence for NVMKEY must be used to allow any erase or program operation to proceed. After the programming command has been executed, the user application must wait for the programming time until programming is complete. The two instructions following the start of the programming sequence should be NOPs.

Refer to the “dsPIC33/PIC24 Family Reference Manual”, “Flash Programming” (DS70609) for details and code examples on programming using RTSP.

5.4 Control Registers

Six SFRs are used to read and write the program Flash memory: NVMCON, NVMKEY, NVMADR, NVMADRU, NVMSRCADRL and NVMSRCADRH.

The NVMCON register (Register 5-1) controls which blocks are to be erased, which memory type is to be programmed and the start of the programming cycle.

NVMKEY (Register 5-4) is a write-only register that is used for write protection. To start a programming or erase sequence, the user application must consecutively write 0x55 and 0xAA to the NVMKEY register.

There are two NVM Address registers: NVMADRU and NVMADR. These two registers, when concatenated, form the 24-bit Effective Address (EA) of the selected word for programming operations, or the selected page for erase operations.

The NVMADRU register is used to hold the upper 8 bits of the EA, while the NVMADR register is used to hold the lower 16 bits of the EA.

The NVMSRCADRH and NVMSRCADRL registers are used to hold the source address of the data in the data memory that needs to be written to Flash memory.

TABLE 7-1: INTERRUPT VECTOR DETAILS

Interrupt Source	Vector #	IRQ #	IVT Address	Interrupt Bit Location		
				Flag	Enable	Priority
Highest Natural Order Priority						
INT0 – External Interrupt 0	8	0	0x000014	IFS0<0>	IEC0<0>	IPC0<2:0>
IC1 – Input Capture 1	9	1	0x000016	IFS0<1>	IEC0<1>	IPC0<6:4>
OC1 – Output Compare 1	10	2	0x000018	IFS0<2>	IEC0<2>	IPC0<10:8>
T1 – Timer1	11	3	0x00001A	IFS0<3>	IEC0<3>	IPC0<14:12>
DMA0 – DMA Channel 0	12	4	0x00001C	IFS0<4>	IEC0<4>	IPC1<2:0>
IC2 – Input Capture 2	13	5	0x00001E	IFS0<5>	IEC0<5>	IPC1<6:4>
OC2 – Output Compare 2	14	6	0x000020	IFS0<6>	IEC0<6>	IPC1<10:8>
T2 – Timer2	15	7	0x000022	IFS0<7>	IEC0<7>	IPC1<14:12>
T3 – Timer3	16	8	0x000024	IFS0<8>	IEC0<8>	IPC2<2:0>
SPI1E – SPI1 Error	17	9	0x000026	IFS0<9>	IEC0<9>	IPC2<6:4>
SPI1 – SPI1 Transfer Done	18	10	0x000028	IFS0<10>	IEC0<10>	IPC2<10:8>
U1RX – UART1 Receiver	19	11	0x00002A	IFS0<11>	IEC0<11>	IPC2<14:12>
U1TX – UART1 Transmitter	20	12	0x00002C	IFS0<12>	IEC0<12>	IPC3<2:0>
AD1 – ADC1 Convert Done	21	13	0x00002E	IFS0<13>	IEC0<13>	IPC3<6:4>
DMA1 – DMA Channel 1	22	14	0x000030	IFS0<14>	IEC0<14>	IPC3<10:8>
Reserved	23	15	0x000032	—	—	—
SI2C1 – I2C1 Slave Event	24	16	0x000034	IFS1<0>	IEC1<0>	IPC4<2:0>
MI2C1 – I2C1 Master Event	25	17	0x000036	IFS1<1>	IEC1<1>	IPC4<6:4>
CMP1 – Comparator Combined Event	26	18	0x000038	IFS1<2>	IEC1<2>	IPC4<10:8>
CN – Input Change Interrupt	27	19	0x00003A	IFS1<3>	IEC1<3>	IPC4<14:12>
INT1 – External Interrupt 1	28	20	0x00003C	IFS1<4>	IEC1<4>	IPC5<2:0>
AD2 – ADC2 Convert Done	29	21	0x00003E	IFS1<5>	IEC1<5>	IPC5<6:4>
IC7 – Input Capture 7	30	22	0x000040	IFS1<6>	IEC1<6>	IPC5<10:8>
IC8 – Input Capture 8	31	23	0x000042	IFS1<7>	IEC1<7>	IPC5<14:12>
DMA2 – DMA Channel 2	32	24	0x000044	IFS1<8>	IEC1<8>	IPC6<2:0>
OC3 – Output Compare 3	33	25	0x000046	IFS1<9>	IEC1<9>	IPC6<6:4>
OC4 – Output Compare 4	34	26	0x000048	IFS1<10>	IEC1<10>	IPC6<10:8>
T4 – Timer4	35	27	0x00004A	IFS1<11>	IEC1<11>	IPC6<14:12>
T5 – Timer5	36	28	0x00004C	IFS1<12>	IEC1<12>	IPC7<2:0>
INT2 – External Interrupt 2	37	29	0x00004E	IFS1<13>	IEC1<13>	IPC7<6:4>
U2RX – UART2 Receiver	38	30	0x000050	IFS1<14>	IEC1<14>	IPC7<10:8>
U2TX – UART2 Transmitter	39	31	0x000052	IFS1<15>	IEC1<15>	IPC7<14:12>
SPI2E – SPI2 Error	40	32	0x000054	IFS2<0>	IEC2<0>	IPC8<2:0>
SPI2 – SPI2 Transfer Done	41	33	0x000056	IFS2<1>	IEC2<1>	IPC8<6:4>
C1RX – CAN1 RX Data Ready ⁽¹⁾	42	34	0x000058	IFS2<2>	IEC2<2>	IPC8<10:8>
C1 – CAN1 Event ⁽¹⁾	43	35	0x00005A	IFS2<3>	IEC2<3>	IPC8<14:12>
DMA3 – DMA Channel 3	44	36	0x00005C	IFS2<4>	IEC2<4>	IPC9<2:0>
IC3 – Input Capture 3	45	37	0x00005E	IFS2<5>	IEC2<5>	IPC9<6:4>
IC4 – Input Capture 4	46	38	0x000060	IFS2<6>	IEC2<6>	IPC9<10:8>
IC5 – Input Capture 5	47	39	0x000062	IFS2<7>	IEC2<7>	IPC9<14:12>
IC6 – Input Capture 6	48	40	0x000064	IFS2<8>	IEC2<8>	IPC10<2:0>

Note 1: This interrupt source is available on dsPIC33EPXXXGM6XX/7XX devices only.

2: This interrupt source is not available on 44-pin devices.

TABLE 7-1: INTERRUPT VECTOR DETAILS (CONTINUED)

Interrupt Source	Vector #	IRQ #	IVT Address	Interrupt Bit Location		
				Flag	Enable	Priority
SPI3E – SPI3 Error	98	90	0x0000C8	IFS5<10>	IEC5<10>	IPC22<10:8>
SPI3 – SPI3 Transfer Done	99	91	0x0000CA	IFS5<11>	IEC5<11>	IPC22<14:12>
Reserved	100-101	92-93	0x0000CC-0x0000CE	—	—	—
PWM1 – PWM Generator 1	102	94	0x0000D0	IFS5<14>	IEC5<14>	IPC23<10:8>
PWM2 – PWM Generator 2	103	95	0x0000D2	IFS5<15>	IEC5<15>	IPC23<14:12>
PWM3 – PWM Generator 3	104	96	0x0000D4	IFS6<0>	IEC6<0>	IPC24<2:0>
PWM4 – PWM Generator 4	105	97	0x0000D6	IFS6<1>	IEC6<1>	IPC24<6:4>
PWM5 – PWM Generator 5	106	98	0x0000D8	IFS6<2>	IEC6<2>	IPC24<10:8>
PWM6 – PWM Generator 6	107	99	0x0000DA	IFS6<3>	IEC6<3>	IPC24<14:12>
Reserved	108-149	100-141	0x0000DC-0x00012E	—	—	—
ICD – ICD Application	150	142	0x000142	IFS8<14>	IEC8<14>	IPC35<10:8>
JTAG – JTAG Programming	151	143	0x000130	IFS8<15>	IEC8<15>	IPC35<14:12>
Reserved	152	144	0x000134	—	—	—
PTGSTEP – PTG Step	153	145	0x000136	IFS9<1>	IEC9<1>	IPC36<6:4>
PTGWDT – PTG Watchdog Time-out	154	146	0x000138	IFS9<2>	IEC9<2>	IPC36<10:8>
PTG0 – PTG Interrupt 0	155	147	0x00013A	IFS9<3>	IEC9<3>	IPC36<14:12>
PTG1 – PTG Interrupt 1	156	148	0x00013C	IFS9<4>	IEC9<4>	IPC37<2:0>
PTG2 – PTG Interrupt 2	157	149	0x00013E	IFS9<5>	IEC9<5>	IPC37<6:4>
PTG3 – PTG Interrupt 3	158	150	0x000140	IFS9<6>	IEC9<6>	IPC37<10:8>
Reserved	159-245	151-245	0x000142-0x0001FE	—	—	—
Lowest Natural Order Priority						

- Note 1:** This interrupt source is available on dsPIC33EPXXXGM6XX/7XX devices only.
Note 2: This interrupt source is not available on 44-pin devices.

dsPIC33EPXXXGM3XX/6XX/7XX

REGISTER 9-3: PLLFBD: PLL FEEDBACK DIVISOR REGISTER⁽¹⁾

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	PLLDIV<8>
bit 15							bit 8

R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0
PLLDIV<7:0>							
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-9

Unimplemented: Read as '0'

bit 8-0

PLLDIV<8:0>: PLL Feedback Divisor bits (also denoted as 'M', PLL multiplier)

11111111 = 513

•

•

•

000110000 = 50 (default)

•

•

•

000000010 = 4

000000001 = 3

000000000 = 2

Note 1: This register is reset only on a Power-on Reset (POR).

dsPIC33EPXXXGM3XX/6XX/7XX

REGISTER 9-5: REFOCON: REFERENCE OSCILLATOR CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ROON	—	ROSSLP	ROSEL	RODIV3 ⁽¹⁾	RODIV2 ⁽¹⁾	RODIV1 ⁽¹⁾	RODIV0 ⁽¹⁾
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15 **ROON:** Reference Oscillator Output Enable bit
 1 = Reference oscillator output is enabled on the REFCLK pin⁽²⁾
 0 = Reference oscillator output is disabled
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **ROSSLP:** Reference Oscillator Run in Sleep bit
 1 = Reference oscillator output continues to run in Sleep
 0 = Reference oscillator output is disabled in Sleep
- bit 12 **ROSEL:** Reference Oscillator Source Select bit
 1 = Oscillator crystal is used as the reference clock
 0 = System clock is used as the reference clock
- bit 11-8 **RODIV<3:0>:** Reference Oscillator Divider bits⁽¹⁾
 1111 = Reference clock divided by 32,768
 1110 = Reference clock divided by 16,384
 1101 = Reference clock divided by 8,192
 1100 = Reference clock divided by 4,096
 1011 = Reference clock divided by 2,048
 1010 = Reference clock divided by 1,024
 1001 = Reference clock divided by 512
 1000 = Reference clock divided by 256
 0111 = Reference clock divided by 128
 0110 = Reference clock divided by 64
 0101 = Reference clock divided by 32
 0100 = Reference clock divided by 16
 0011 = Reference clock divided by 8
 0010 = Reference clock divided by 4
 0001 = Reference clock divided by 2
 0000 = Reference clock
- bit 7-0 **Unimplemented:** Read as '0'

- Note 1:** The reference oscillator output must be disabled (ROON = 0) before writing to these bits.
Note 2: This pin is remappable. See **Section 11.4 “Peripheral Pin Select (PPS)”** for more information.

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13.1 Timer Control Registers

REGISTER 13-1: TxCON (T2CON, T4CON, T6CON AND T8CON) CONTROL REGISTER

R/W-0	U-0	R/W-0	U-0	U-0	U-0	U-0	U-0
TON	—	TSIDL	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0
—	TGATE	TCKPS1	TCKPS0	T32	—	TCS ⁽¹⁾	—
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **TON:** Timerx On bit

When T32 = 1:

1 = Starts 32-bit Timerx/y

0 = Stops 32-bit Timerx/y

When T32 = 0:

1 = Starts 16-bit Timerx

0 = Stops 16-bit Timerx

bit 14 **Unimplemented:** Read as '0'

bit 13 **TSIDL:** Timerx Stop in Idle Mode bit

1 = Discontinues module operation when device enters Idle mode

0 = Continues module operation in Idle mode

bit 12-7 **Unimplemented:** Read as '0'

bit 6 **TGATE:** Timerx Gated Time Accumulation Enable bit

When TCS = 1:

This bit is ignored.

When TCS = 0:

1 = Gated time accumulation is enabled

0 = Gated time accumulation is disabled

bit 5-4 **TCKPS<1:0>:** Timerx Input Clock Prescale Select bits

11 = 1:256

10 = 1:64

01 = 1:8

00 = 1:1

bit 3 **T32:** 32-Bit Timer Mode Select bit

1 = Timerx and Timery form a single 32-bit timer

0 = Timerx and Timery act as two 16-bit timers

bit 2 **Unimplemented:** Read as '0'

bit 1 **TCS:** Timerx Clock Source Select bit⁽¹⁾

1 = External clock is from pin, TxCK (on the rising edge)

0 = Internal clock (Fp)

bit 0 **Unimplemented:** Read as '0'

Note 1: The TxCK pin is not available on all timers. Refer to the “Pin Diagrams” section for the available pins.

REGISTER 16-12: PDCx: PWMx GENERATOR DUTY CYCLE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PDCx<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PDCx<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 **PDCx<15:0>**: PWMx Generator # Duty Cycle Value bits

REGISTER 16-13: SDCx: PWMx SECONDARY DUTY CYCLE REGISTER⁽¹⁾

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SDCx<15:8>							
bit 15				bit 8			

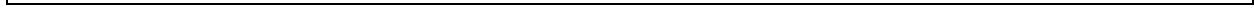
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SDCx<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-0 **SDCx<15:0>**: Secondary Duty Cycle bits for PWMxL Output Pin bits

Note 1: The SDCx register is used in Independent PWM mode only. When used in Independent PWM mode, the SDCx register controls the PWMxL duty cycle.



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REGISTER 24-3: DCICON3: DCI CONTROL REGISTER 3

r-0	r-0	r-0	r-0	R/W-0	R/W-0	R/W-0	R/W-0
r	r	r	r	BCG<11:8>			
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
BCG<7:0>							
bit 7							bit 0

Legend:	r = Reserved bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-12 **Reserved:** Read as '0'

bit 11-0 **BCG<11:0>:** DCI Bit Clock Generator Control bits

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REGISTER 25-12: PTGQPTR: PTG STEP QUEUE POINTER REGISTER⁽¹⁾

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15				bit 8			

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	PTGQPTR<4:0>				
bit 7				bit 0			

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-5 **Unimplemented:** Read as '0'

bit 4-0 **PTGQPTR<4:0>:** PTG Step Queue Pointer Register bits
This register points to the currently active Step command in the step queue.

Note 1: This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

REGISTER 25-13: PTGQUEx: PTG STEP QUEUE REGISTER x (x = 0-15)^(1,3)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STEP(2x + 1)<7:0> ⁽²⁾							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STEP(2x)<7:0> ⁽²⁾							
bit 7				bit 0			

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
-n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 15-8 **STEP(2x + 1)<7:0>:** PTG Step Queue Pointer Register bits⁽²⁾
A queue location for storage of the STEP(2x + 1) command byte.

bit 7-0 **STEP(2x)<7:0>:** PTG Step Queue Pointer Register bits⁽²⁾
A queue location for storage of the STEP(2x) command byte.

Note 1: This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

2: Refer to Table 25-1 for the Step command encoding.

3: The Step registers maintain their values on any type of Reset.

25.3 Step Commands and Format

TABLE 25-1: PTG STEP COMMAND FORMAT

Step Command Byte:			
STEPx<7:0>			
CMD<3:0>		OPTION<3:0>	
bit 7	bit 4	bit 3	bit 0

bit 7-4	CMD<3:0>	Step Command	Command Description
	0000	PTGCTRL	Execute control command as described by OPTION<3:0>
	0001	PTGADD	Add contents of PTGADJ register to target register as described by OPTION<3:0>
		PTGCOPY	Copy contents of PTGHOLD register to target register as described by OPTION<3:0>
	001x	PTGSTRB	Copy the value contained in CMD0:OPTION<3:0> to the CH0SA<4:0> bits (AD1CHS0<4:0>)
	0100	PTGWHI	Wait for a low-to-high edge input from selected PTG trigger input as described by OPTION<3:0>
	0101	PTGWLO	Wait for a high-to-low edge input from selected PTG trigger input as described by OPTION<3:0>
	0110	Reserved	Reserved
	0111	PTGIRQ	Generate individual interrupt request as described by OPTION<3:0>
	100x	PTGTRIG	Generate individual trigger output as described by <<CMD0>:OPTION<3:0>>
	101x	PTGJMP	Copy the value indicated in <<CMD0>:OPTION<3:0>> to the Queue Pointer (PTGQPTR) and jump to that step queue
	110x	PTGJMPC0	PTGC0 = PTGC0LIM: Increment the Queue Pointer (PTGQPTR)
			PTGC0 ≠ PTGC0LIM: Increment Counter 0 (PTGC0) and copy the value indicated in <<CMD0>:OPTION<3:0>> to the Queue Pointer (PTGQPTR) and jump to that step queue
	111x	PTGJMPC1	PTGC1 = PTGC1LIM: Increment the Queue Pointer (PTGQPTR)
			PTGC1 ≠ PTGC1LIM: Increment Counter 1 (PTGC1) and copy the value indicated in <<CMD0>:OPTION<3:0>> to the Queue Pointer (PTGQPTR) and jump to that step queue

Note 1: All reserved commands or options will execute but have no effect (i.e., execute as a NOP instruction).

2: Refer to Table 25-2 for the trigger output descriptions.

26.1.2 OP AMP CONFIGURATION B

Figure 26-6 shows a typical inverting amplifier circuit with the output of the op amp (OAxOUT) externally routed to a separate analog input pin (ANy) on the device. This op amp configuration is slightly different in terms of the op amp output and the ADCx input connection, therefore, RINT1 is not included in the transfer function. However, this configuration requires the designer to externally route the op amp output (OAxOUT) to another analog input pin (ANy). See Table 33-52 in **Section 33.0 “Electrical Characteristics”** for the typical value of RINT1. Table 33-57 and Table 33-58 in **Section 33.0 “Electrical Characteristics”** describe the minimum sample time (TSAMP) requirements for the ADCx module in this configuration.

Figure 26-6 also defines the equation to be used to calculate the expected voltage at point, VOAxOUT. This is the typical inverting amplifier equation.

26.2 Op Amp/Comparator Resources

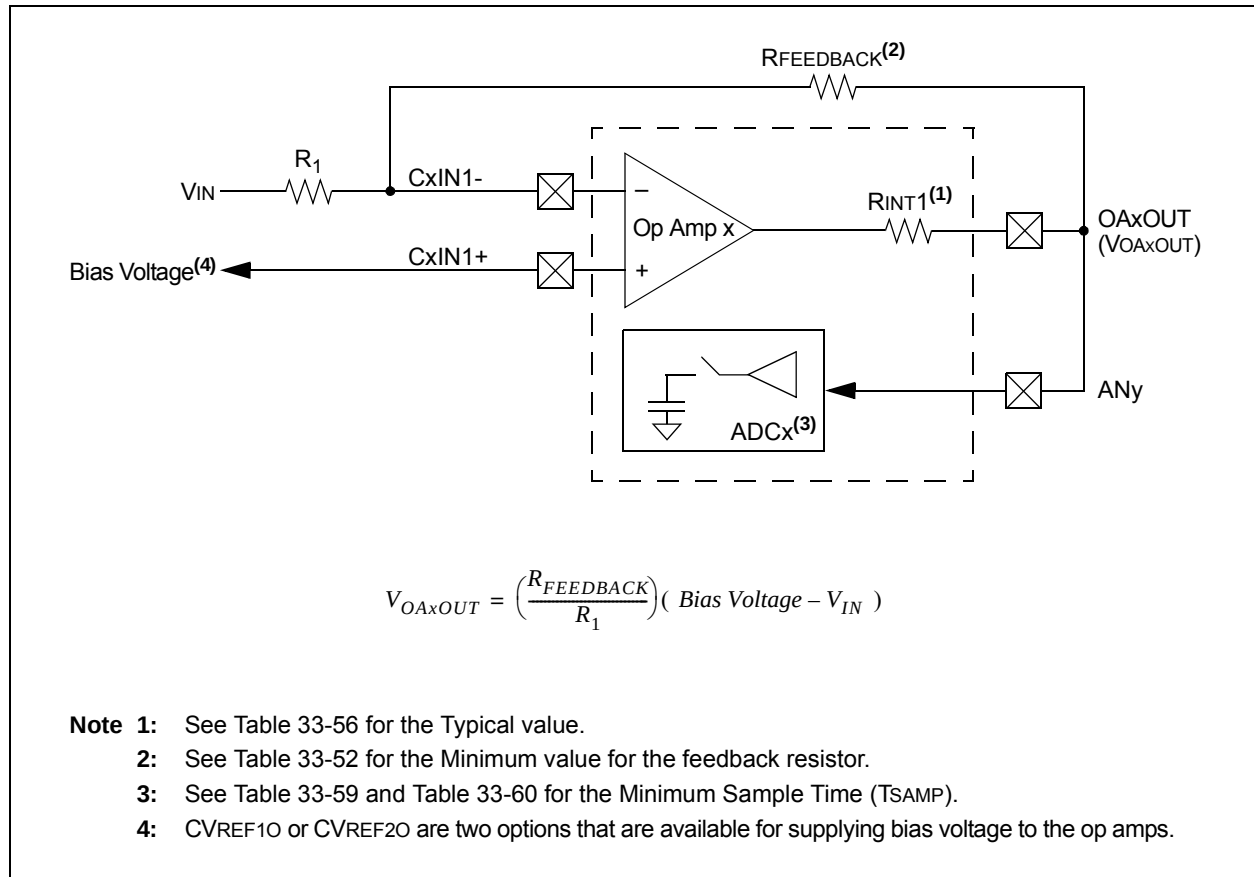
Many useful resources are provided on the main product page of the Microchip web site for the devices listed in this data sheet. This product page, which can be accessed using this link, contains the latest updates and additional information.

Note: In the event you are not able to access the product page using the link above, enter this URL in your browser:
<http://www.microchip.com/wwwproducts/Devices.aspx?dDocName=en555464>

26.2.1 KEY RESOURCES

- “Op Amp/Comparator” (DS70000357) in the “dsPIC33/PIC24 Family Reference Manual”
- Code Samples
- Application Notes
- Software Libraries
- Webinars
- All Related “dsPIC33/PIC24 Family Reference Manual” Sections
- Development Tools

FIGURE 26-6: OP AMP CONFIGURATION B



NOTES:

REGISTER 27-2: PADCFG1: PAD CONFIGURATION CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	RTSECSEL ⁽¹⁾	PMPTTL
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-2 **Unimplemented:** Read as '0'

bit 1 **RTSECSEL:** RTCC Seconds Clock Output Select bit⁽¹⁾

1 = RTCC seconds clock is selected for the RTCC pin

0 = RTCC alarm pulse is selected for the RTCC pin

bit 0 Not used by the RTCC module.

Note 1: To enable the actual RTCC output, the RTCOE bit (RCFGCAL<10>) must be set.

30.5 Watchdog Timer (WDT)

For dsPIC33EPXXXGM3XX/6XX/7XX devices, the WDT is driven by the LPRC oscillator. When the WDT is enabled, the clock source is also enabled.

30.5.1 PRESCALER/POSTSCALER

The nominal WDT clock source from LPRC is 32 kHz. This feeds a prescaler that can be configured for either 5-bit (divide-by-32) or 7-bit (divide-by-128) operation. The prescaler is set by the WDTPRE Configuration bit. With a 32 kHz input, the prescaler yields a WDT time-out period (TWDT), as shown in Parameter SY12 in Table 33-21.

A variable postscaler divides down the WDT prescaler output and allows for a wide range of time-out periods. The postscaler is controlled by the WDTPOST<3:0> Configuration bits (FWDT<3:0>), which allow the selection of 16 settings, from 1:1 to 1:32,768. Using the prescaler and postscaler, time-out periods ranging from 1 ms to 131 seconds can be achieved.

The WDT, prescaler and postscaler are reset:

- On any device Reset
- On the completion of a clock switch, whether invoked by software (i.e., setting the OSWEN bit after changing the NOSCx bits) or by hardware (i.e., Fail-Safe Clock Monitor)
- When a PWRSAV instruction is executed (i.e., Sleep or Idle mode is entered)
- When the device exits Sleep or Idle mode to resume normal operation
- By a CLRWDT instruction during normal execution

Note: The CLRWDT and PWRSAV instructions clear the prescaler and postscaler counts when executed.

30.5.2 SLEEP AND IDLE MODES

If the WDT is enabled, it continues to run during Sleep or Idle modes. When the WDT time-out occurs, the device wakes the device and code execution continues from where the PWRSAV instruction was executed. The corresponding SLEEP or IDLE bit (RCON<3,2>) needs to be cleared in software after the device wakes up.

30.5.3 ENABLING WDT

The WDT is enabled or disabled by the FWDTEN Configuration bit in the FWDT Configuration register. When the FWDTEN Configuration bit is set, the WDT is always enabled.

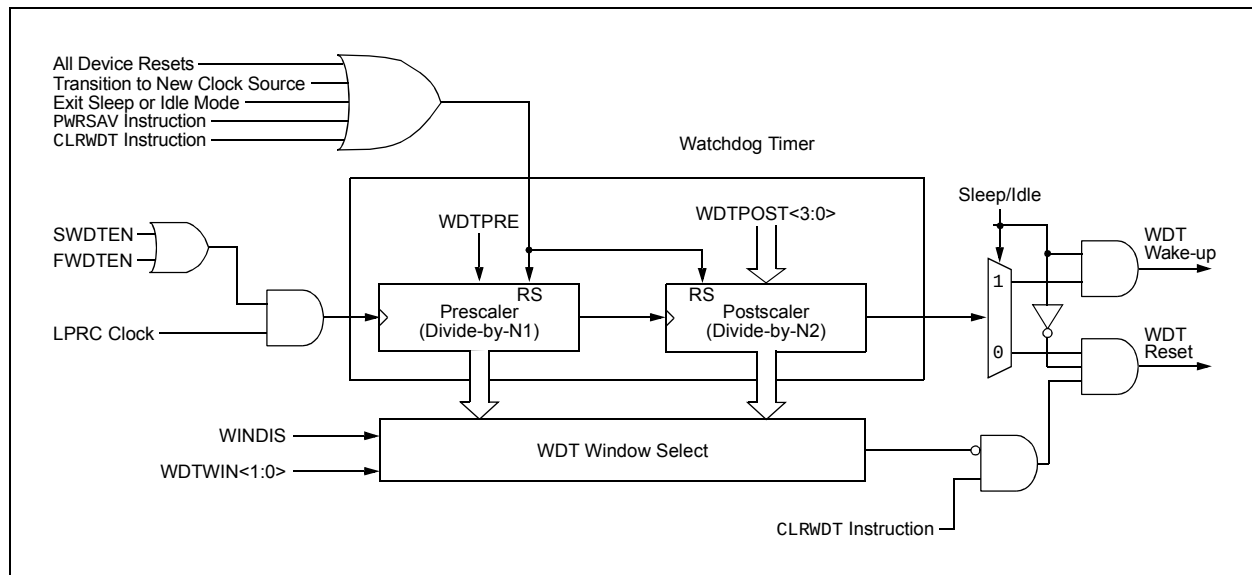
The WDT can be optionally controlled in software when the FWDTEN Configuration bit has been programmed to '0'. The WDT is enabled in software by setting the SWDTEN control bit (RCON<5>). The SWDTEN control bit is cleared on any device Reset. The software WDT option allows the user application to enable the WDT for critical code segments and disable the WDT during non-critical segments for maximum power savings.

The WDT flag bit, WDTO (RCON<4>), is not automatically cleared following a WDT time-out. To detect subsequent WDT events, the flag must be cleared in software.

30.5.4 WDT WINDOW

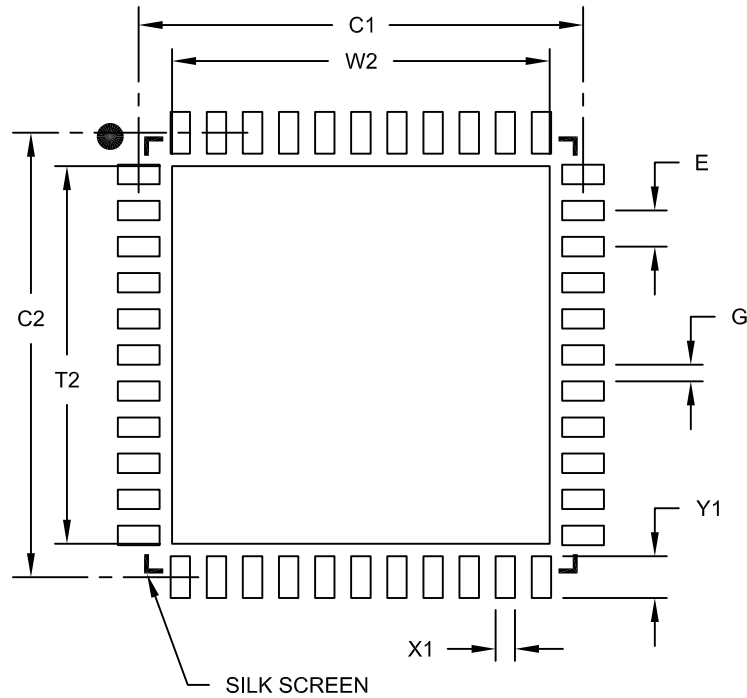
The Watchdog Timer has an optional Windowed mode enabled by programming the WINDIS bit in the WDT Configuration register (FWDT<6>). In the Windowed mode (WINDIS = 0), the WDT should be cleared based on the settings in the programmable Watchdog Timer Window select bits (WDTWIN<1:0>).

FIGURE 30-2: WDT BLOCK DIAGRAM



44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Optional Center Pad Width	W2			6.60
Optional Center Pad Length	T2			6.60
Contact Pad Spacing	C1		8.00	
Contact Pad Spacing	C2		8.00	
Contact Pad Width (X44)	X1			0.35
Contact Pad Length (X44)	Y1			0.85
Distance Between Pads	G	0.25		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2103B