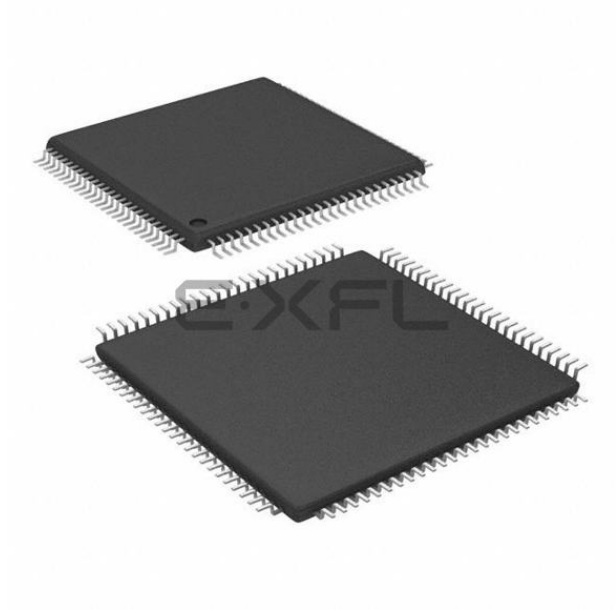
Microchip Technology - DSPIC33EP512GM310T-I/PF Datasheet



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Number of I/O	85
Program Memory Size	512KB (170K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	-
Data Converters	A/D 49x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
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Supplier Device Package	100-TQFP (14x14)
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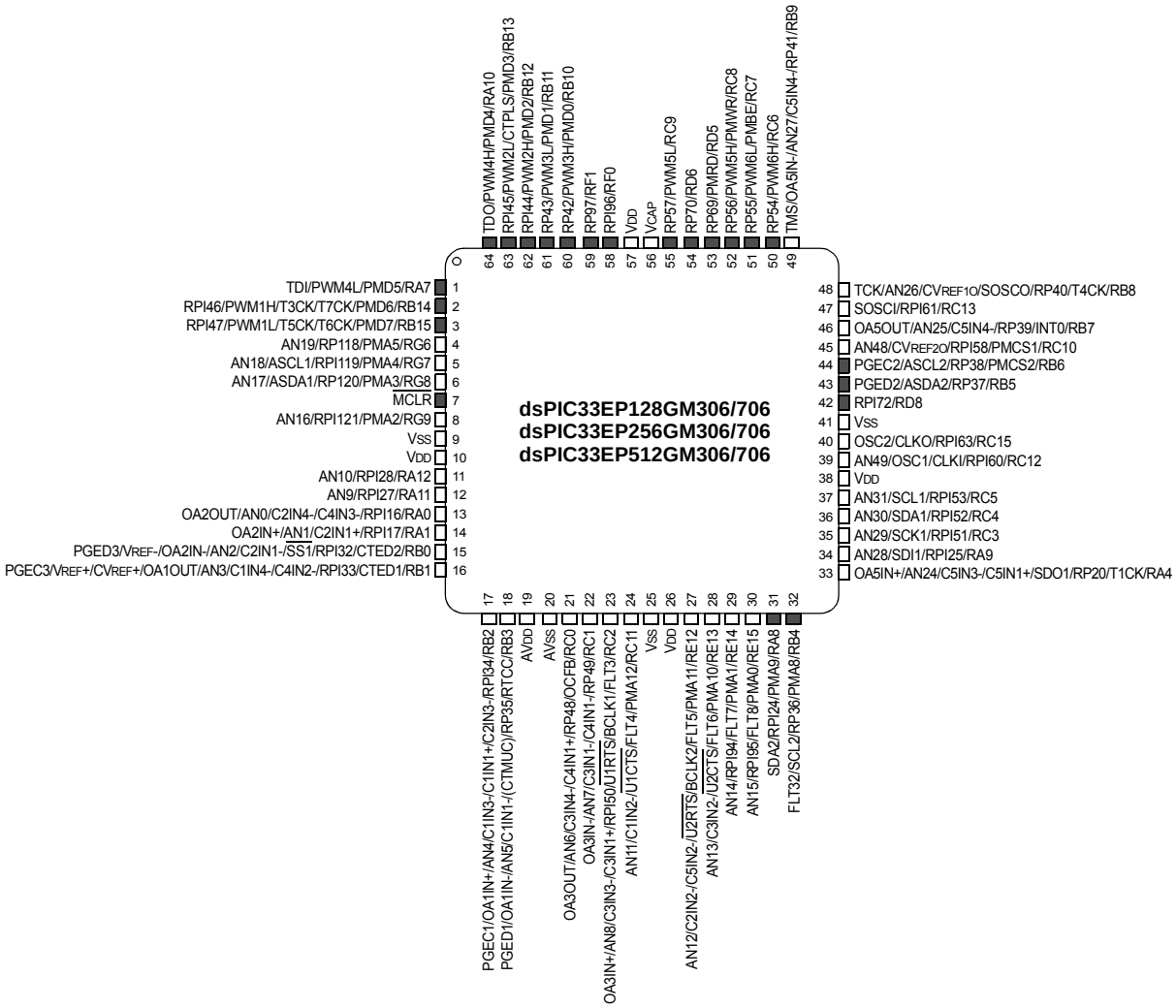
Pin Diagrams (Continued)

64-Pin TQFP(1,2,3)

■ = Pins are up to 5V tolerant



Note 1: The RPn/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 "Peripheral Pin Select (PPS)"** for available peripherals and for information on limitations.

2: Every I/O port pin (RAx-RGx) can be used as a Change Notification pin (CNAx-CNGx). See **Section 11.0 "I/O Ports"** for more information.

3: This pin is not available as an input when OPMODE (CMxCON<10>) = 1.

2.5 ICSP Pins

The PGECx and PGEDx pins are used for ICSP and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

Pull-up resistors, series diodes and capacitors on the PGECx and PGEDx pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin Voltage Input High (V_{IH}) and Voltage Input Low (V_{IL}) requirements.

Ensure that the "Communication Channel Select" (i.e., PGECx/PGEDx pins) programmed into the device matches the physical connections for the ICSP to MPLAB® PICkit™ 3, MPLAB ICD 3, or MPLAB REAL ICE™.

For more information on MPLAB ICD 2, ICD 3 and REAL ICE connection requirements, refer to the following documents that are available on the Microchip web site:

- *"Using MPLAB® ICD 3"* (poster) DS51765
- *"MPLAB® ICD 3 Design Advisory"* DS51764
- *"MPLAB® REAL ICE™ In-Circuit Emulator User's Guide"* DS51616
- *"Using MPLAB® REAL ICE™ In-Circuit Emulator"* (poster) DS51749

2.6 External Oscillator Pins

Many DSCs have options for at least two oscillators: a high-frequency primary oscillator and a low-frequency secondary oscillator. For details, see **Section 9.0 "Oscillator Configuration"** for details.

The oscillator circuit should be placed on the same side of the board as the device. Also, place the oscillator circuit close to the respective oscillator pins, not exceeding one-half inch (12 mm) distance between them. The load capacitors should be placed next to the oscillator itself, on the same side of the board. Use a grounded copper pour around the oscillator circuit to isolate them from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed. A suggested layout is shown in Figure 2-3.

FIGURE 2-3: SUGGESTED PLACEMENT OF THE OSCILLATOR CIRCUIT

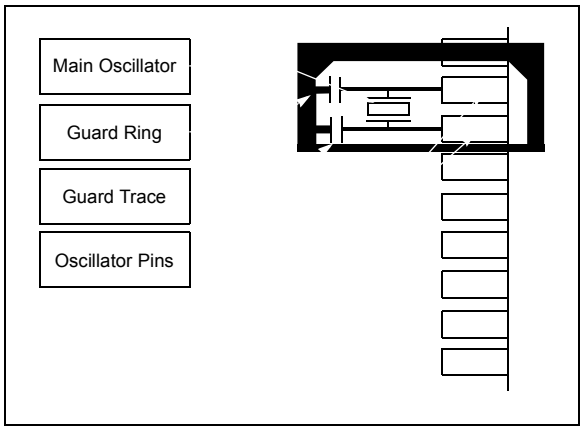


TABLE 4-8: PWM REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PTCON	0C00	PTEN	—	PTSIDL	SESTAT	SEIEN	EIPU	SYNCPOL	SYNCOEN	SYNCEN	SYNCSRC2	SYNCSRC1	SYNCSRC0	SEVTPS3	SEVTPS2	SEVTPS1	SEVTPS0	0000
PTCON2	0C02	—	—	—	—	—	—	—	—	—	—	—	—	—	PCLKDIV<2:0>			0000
PTPER	0C04	PTPER<15:0>																00F8
SEVTCMP	0C06	SEVTCMP<15:0>																0000
MDC	0C0A	MDC<15:0>																0000
STCON	0C0E	—	—	—	SESTAT	SEIEN	EIPU	SYNCPOL	SYNCOEN	SYNCEN	SYNCSRC2	SYNCSRC1	SYNCSRC0	SEVTPS3	SEVTPS2	SEVTPS1	SEVTPS0	0000
STCON2	0C10	—	—	—	—	—	—	—	—	—	—	—	—	—	PCLKDIV<2:0>			0000
STPER	0C12	STPER<15:0>																0000
SSEVTCMP	0C14	SSEVTCMP<15:0>																0000
CHOP	0C1A	CHPCLKEN	—	—	—	—	—	CHOPCLK9	CHOPCLK8	CHOPCLK7	CHOPCLK6	CHOPCLK5	CHOPCLK4	CHOPCLK3	CHOPCLK2	CHOPCLK1	CHOPCLK0	0000
PWMKEY	0C1E	PWMKEY<15:0>																0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-9: PWM GENERATOR 1 REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PWMCON1	0C20	FLTSTAT	CLSTAT	TRGSTAT	FLTIEN	CLIEN	TRGIEN	ITB	MDCS	DTC1	DTC0	DTCP	—	MTBS	CAM	XPRES	IUE	0000
IOCON1	0C22	PENH	PENL	POLH	POLL	PMOD1	PMOD0	OVRENH	OVRENL	OVRDAT1	OVRDAT0	FLTDAT1	FLTDAT0	CLDAT1	CLDAT0	SWAP	OSYNC	C000
FCLCON1	0C24	IFLTMOD	CLSRC4	CLSRC3	CLSRC2	CLSRC1	CLSRC0	CLPOL	CLMOD	FLTSRC4	FLTSRC3	FLTSRC2	FLTSRC1	FLTSRC0	FLTPOL	FLTMOD1	FLTMOD0	0000
PDC1	0C26	PDC1<15:0>																FFF8
PHASE1	0C28	PHASE1<15:0>																0000
DTR1	0C2A	—	—	DTR1<13:0>														0000
ALTDTR1	0C2C	—	—	ALTDTR1<13:0>														0000
SDC1	0C2E	SDC1<15:0>																0000
SPHASE1	0C30	SPHASE1<15:0>																0000
TRIG1	0C32	TRGCMP<15:0>																0000
TRGCON1	0C34	TRGDIV3	TRGDIV2	TRGDIV1	TRGDIV0	—	—	—	—	—	—	TRGSTRT5	TRGSTRT4	TRGSTRT3	TRGSTRT2	TRGSTRT1	TRGSTRT0	0000
PWMCAP1	0C38	PWMCAP1<15:0>																0000
LEBCON1	0C3A	PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	—	—	—	—	BCH	BCL	BPHH	BPHL	BPLH	BPLL	0000
LEBDLY1	0C3C	—	—	—	—	LEB<11:0>												0000
AUXCON1	0C3E	—	—	—	—	BLANKSEL3	BLANKSEL2	BLANKSEL1	BLANKSEL0	—	—	CHOPSEL3	CHOPSEL2	CHOPSEL1	CHOPSEL0	CHOPHEN	CHOPLEN	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-17: I2C1 AND I2C2 REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
I2C1RCV	0200	—	—	—	—	—	—	—	—	I2C1 Receive Register								0000
I2C1TRN	0202	—	—	—	—	—	—	—	—	I2C1 Transmit Register								00FF
I2C1BRG	0204	Baud Rate Generator Register																0000
I2C1CON	0206	I2CEN	—	I2CSIDL	SCLREL	IPMIEN	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	1000
I2C1STAT	0208	ACKSTAT	TRSTAT	—	—	—	BCL	GCSTAT	ADD10	IWCOL	I2COV	D_A	P	S	R_W	RBF	TBF	0000
I2C1ADD	020A	—	—	—	—	—	—	I2C1 Address Register										0000
I2C1MSK	020C	—	—	—	—	—	—	I2C1 Address Mask Register										0000
I2C2RCV	0210	—	—	—	—	—	—	—	—	I2C2 Receive Register								0000
I2C2TRN	0212	—	—	—	—	—	—	—	—	I2C2 Transmit Register								00FF
I2C2BRG	0214	Baud Rate Generator Register																0000
I2C2CON	0216	I2CEN	—	I2CSIDL	SCLREL	IPMIEN	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	1000
I2C2STAT	0218	ACKSTAT	TRSTAT	—	—	—	BCL	GCSTAT	ADD10	IWCOL	I2COV	D_A	P	S	R_W	RBF	TBF	0000
I2C2ADD	021A	—	—	—	—	—	—	I2C2 Address Register										0000
I2C2MSK	021C	—	—	—	—	—	—	I2C2 Address Mask Register										0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-18: UART1 AND UART2 REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
U1MODE	0220	UARTEN	—	USIDL	IREN	RTSMD	—	UEN1	UEN0	WAKE	LPBACK	ABAUD	URXINV	BRGH	PDSEL1	PDSEL0	STSEL	0000
U1STA	0222	UTXISEL1	UTXINV	UTXISEL0	—	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL1	URXISEL0	ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
U1TXREG	0224	—	—	—	—	—	—	—	UART1 Transmit Register									xxxx
U1RXREG	0226	—	—	—	—	—	—	—	UART1 Receive Register									0000
U1BRG	0228	Baud Rate Generator Prescaler																0000
U2MODE	0230	UARTEN	—	USIDL	IREN	RTSMD	—	UEN1	UEN0	WAKE	LPBACK	ABAUD	URXINV	BRGH	PDSEL1	PDSEL0	STSEL	0000
U2STA	0232	UTXISEL1	UTXINV	UTXISEL0	—	UTXBRK	UTXEN	UTXBF	TRMT	URXISEL1	URXISEL0	ADDEN	RIDLE	PERR	FERR	OERR	URXDA	0110
U2TXREG	0234	—	—	—	—	—	—	—	UART2 Transmit Register									xxxx
U2RXREG	0236	—	—	—	—	—	—	—	UART2 Receive Register									0000
U2BRG	0238	Baud Rate Generator Prescaler																0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-32: PERIPHERAL PIN SELECT OUTPUT REGISTER MAP FOR dsPIC33EPXXXGM310/710 DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
RPOR0	0680	—	—	RP35R<5:0>						—	—	RP20R<5:0>						0000
RPOR1	0682	—	—	RP37R<5:0>						—	—	RP36R<5:0>						0000
RPOR2	0684	—	—	RP39R<5:0>						—	—	RP38R<5:0>						0000
RPOR3	0686	—	—	RP41R<5:0>						—	—	RP40R<5:0>						0000
RPOR4	0688	—	—	RP43R<5:0>						—	—	RP42R<5:0>						0000
RPOR5	068A	—	—	RP49R<5:0>						—	—	RP48R<5:0>						0000
RPOR6	068C	—	—	RP55R<5:0>						—	—	RP54R<5:0>						0000
RPOR7	068E	—	—	RP57R<5:0>						—	—	RP56R<5:0>						0000
RPOR8	0690	—	—	RP70R<5:0>						—	—	RP69R<5:0>						0000
RPOR9	0692	—	—	RP97R<5:0>						—	—	RP81R<5:0>						0000
RPOR10	0694	—	—	RP118R<5:0>						—	—	RP113R<5:0>						0000
RPOR11	0696	—	—	RPR125R<5:0>						—	—	RPR120R<5:0>						0000
RPOR12	0698	—	—	RPR127R<5:0>						—	—	RPR126R<5:0>						0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-49: PORTB REGISTER MAP FOR dsPIC33EPXXXGM310/710 DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISB	0E10	TRISB<15:0>																DF9F
PORTB	0E12	RB<15:0>																xxxx
LATB	0E14	LATB<15:0>																xxxx
ODCB	0E16	ODCB<15:0>																0000
CNENB	0E18	CNIEB<15:0>																0000
CNPUB	0E1A	CNPUB<15:0>																0000
CNPDB	0E1C	CNPDB<15:0>																0000
ANSELB	0E1E	—	—	—	—	—	—	ANSB<9:7>			—	—	—	ANSB<3:0>				010F

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-50: PORTB REGISTER MAP FOR dsPIC33EPXXXGM306/706 DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISB	0E10	TRISB<15:0>																DF9F
PORTB	0E12	RB<15:0>																xxxx
LATB	0E14	LATB<15:0>																xxxx
ODCB	0E16	ODCB<15:0>																0000
CNENB	0E18	CNIEB<15:0>																0000
CNPUB	0E1A	CNPUB<15:0>																0000
CNPDB	0E1C	CNPDB<15:0>																0000
ANSELB	0E1E	—	—	—	—	—	—	ANSB<9:7>			—	—	—	ANSB<3:0>				010F

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-51: PORTB REGISTER MAP FOR dsPIC33EPXXXGM304/604 DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISB	0E10	TRISB<15:0>																FFFF
PORTB	0E12	RB<15:0>																xxxx
LATB	0E14	LATB<15:0>																xxxx
ODCB	0E16	ODCB<15:0>																0000
CNENB	0E18	CNIEB<15:0>																0000
CNPUB	0E1A	CNPUB<15:0>																0000
CNPDB	0E1C	CNPDB<15:0>																0000
ANSELB	0E1E	—	—	—	—	—	—	ANSB<9:7>			—	—	—	ANSB<3:0>				010F

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

4.7.1 DATA ACCESS FROM PROGRAM MEMORY USING TABLE INSTRUCTIONS

The TBLRDL and TBLWTL instructions offer a direct method of reading or writing the lower word of any address within the Program Space without going through Data Space. The TBLRDH and TBLWTH instructions are the only method to read or write the upper 8 bits of a Program Space word as data.

The PC is incremented by two for each successive 24-bit program word. This allows program memory addresses to directly map to Data Space addresses. Program memory can thus be regarded as two 16-bit-wide word address spaces, residing side by side, each with the same address range. TBLRDL and TBLWTL access the space that contains the least significant data word. TBLRDH and TBLWTH access the space that contains the upper data byte.

Two table instructions are provided to move byte or word-sized (16-bit) data to and from Program Space. Both function as either byte or word operations.

- TBLRDL (Table Read Low):
  - In Word mode, this instruction maps the lower word of the Program Space location (P<15:0>) to a data address (D<15:0>)
  - In Byte mode, either the upper or lower byte of the lower program word is mapped to the lower byte of a data address. The upper byte is selected when Byte Select is '1'; the lower byte is selected when it is '0'.
- TBLRDH (Table Read High):
  - In Word mode, this instruction maps the entire upper word of a program address (P<23:16>) to a data address. The 'phantom' byte (D<15:8>) is always '0'.
  - In Byte mode, this instruction maps the upper or lower byte of the program word to D<7:0> of the data address in the TBLRDL instruction. The data is always '0' when the upper 'phantom' byte is selected (Byte Select = 1).

In a similar fashion, two table instructions, TBLWTH and TBLWTL, are used to write individual bytes or words to a Program Space address. The details of their operation are explained in **Section 5.0 "Flash Program Memory"**.

For all table operations, the area of program memory space to be accessed is determined by the Table Page register (TBLPAG). TBLPAG covers the entire program memory space of the device, including user application and configuration spaces. When TBLPAG<7> = 0, the table page is located in the user memory space. When TBLPAG<7> = 1, the page is located in configuration space.

FIGURE 4-17: ACCESSING PROGRAM MEMORY WITH TABLE INSTRUCTIONS

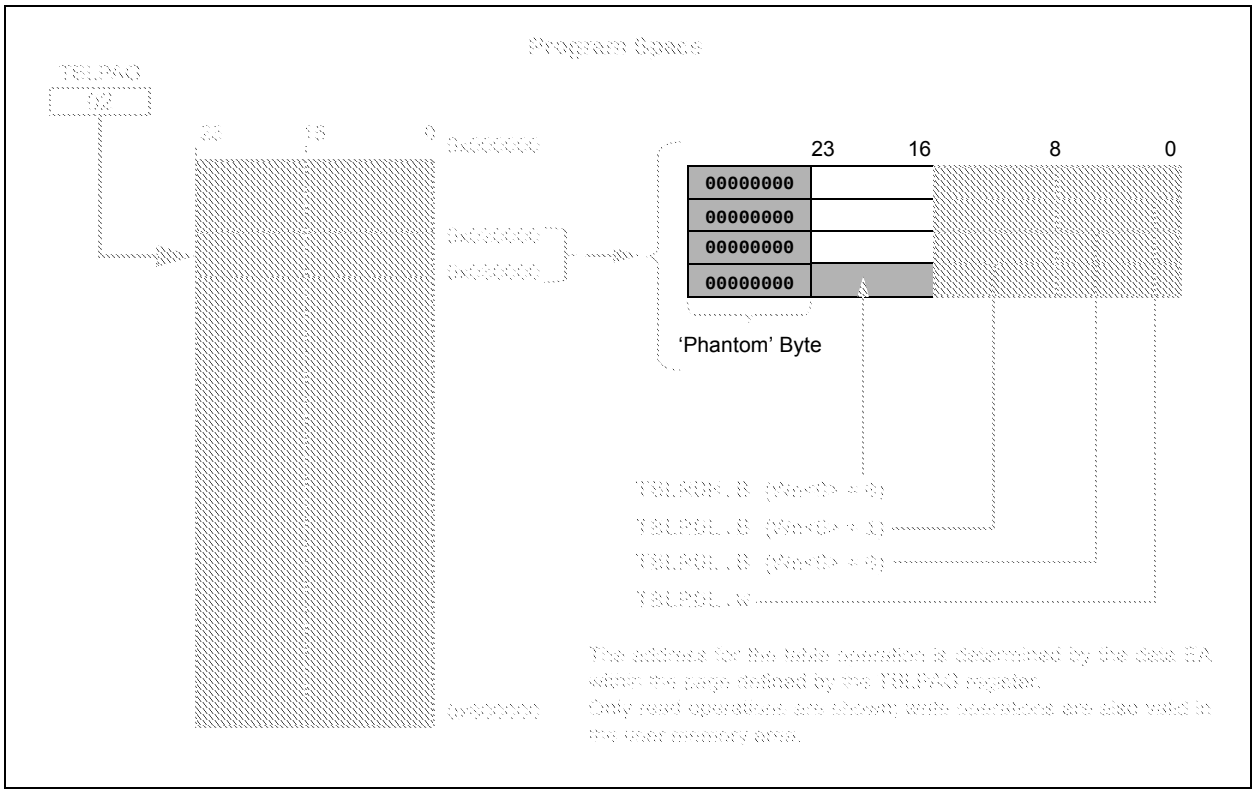
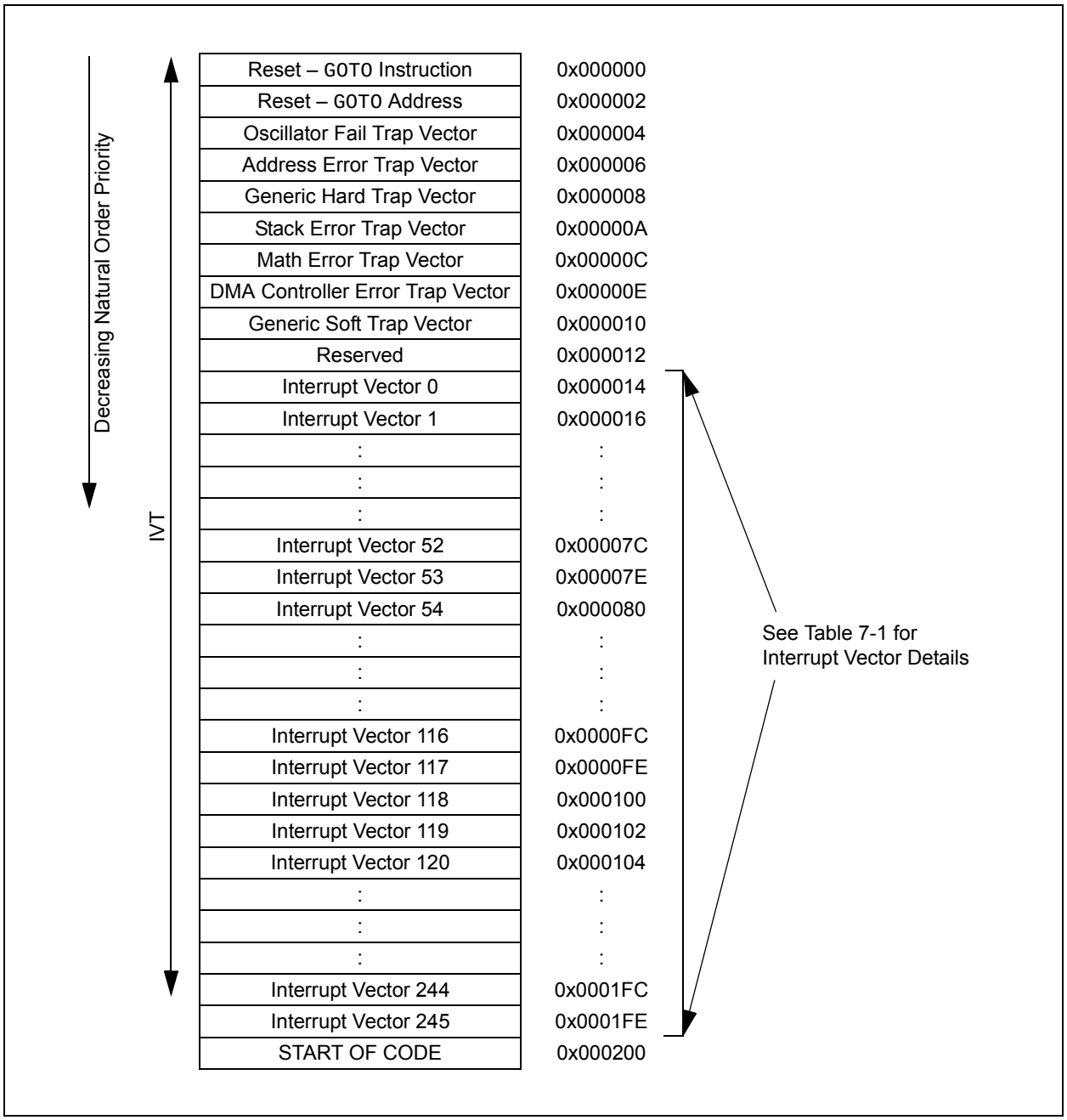


FIGURE 7-1: dsPIC33EPXXXGM3XX/6XX/7XX INTERRUPT VECTOR TABLE



REGISTER 8-12: DMARQC: DMA REQUEST COLLISION STATUS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
—	—	—	—	RQCOL3	RQCOL2	RQCOL1	RQCOL0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-4 **Unimplemented:** Read as ‘0’

bit 3 **RQCOL3:** Channel 3 Transfer Request Collision Flag bit
1 = User FORCE and interrupt-based request collision are detected
0 = No request collision is detected

bit 2 **RQCOL2:** Channel 2 Transfer Request Collision Flag bit
1 = User FORCE and interrupt-based request collision are detected
0 = No request collision is detected

bit 1 **RQCOL1:** Channel 1 Transfer Request Collision Flag bit
1 = User FORCE and interrupt-based request collision are detected
0 = No request collision is detected

bit 0 **RQCOL0:** Channel 0 Transfer Request Collision Flag bit
1 = User FORCE and interrupt-based request collision are detected
0 = No request collision is detected

9.0 OSCILLATOR CONFIGURATION

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGM3XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"Oscillator"** (DS70580), which is available from the Microchip web site (www.microchip.com).

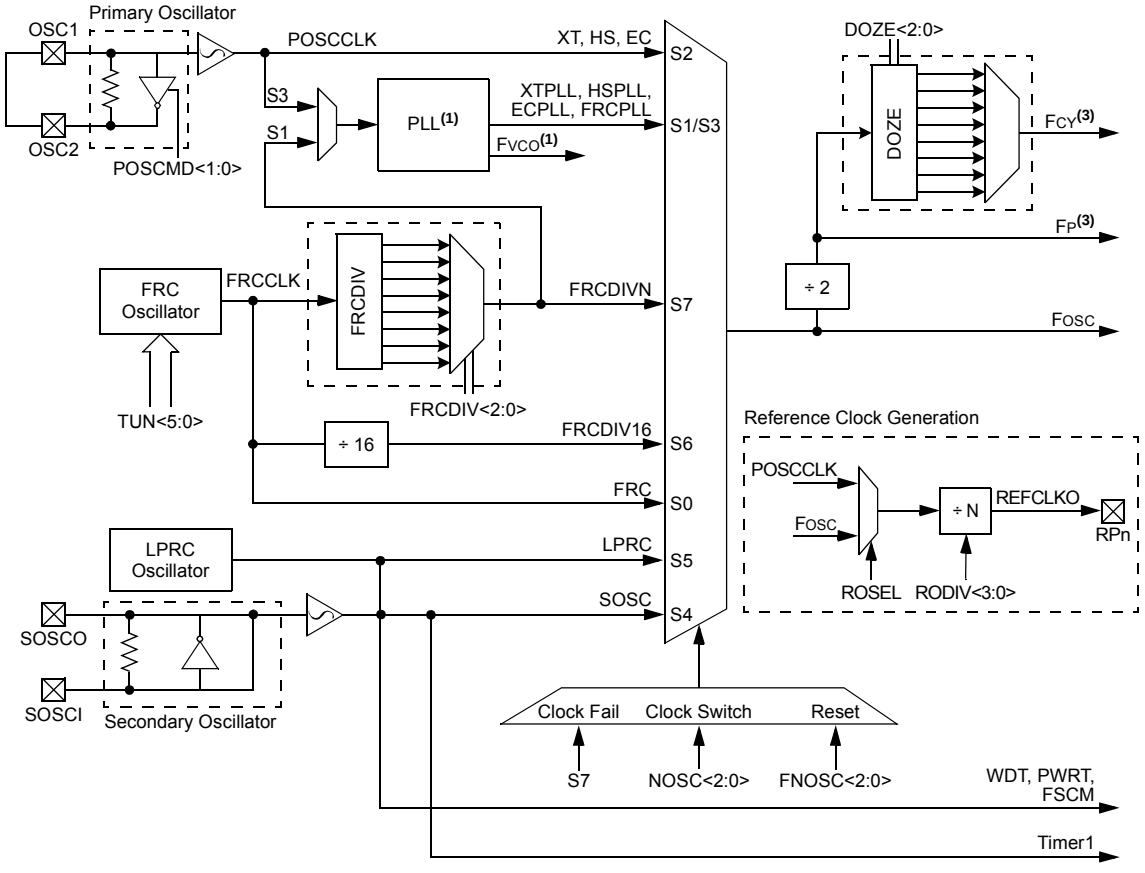
2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGM3XX/6XX/7XX oscillator system provides:

- On-chip Phase-Locked Loop (PLL) to boost internal operating frequency on select internal and external oscillator sources
- On-the-fly clock switching between various clock sources
- Doze mode for system power savings
- Fail-Safe Clock Monitor (FSCM) that detects clock failure and permits safe application recovery or shutdown
- Configuration bits for clock source selection

A simplified diagram of the oscillator system is shown in Figure 9-1.

FIGURE 9-1: OSCILLATOR SYSTEM DIAGRAM



Note 1: See Figure 9-2 for PLL and FVCO details.

2: If the oscillator is used with XT or HS modes, an external parallel resistor with the value of 1 MΩ must be connected.

3: The term, FP, refers to the clock source for all peripherals, while FCY refers to the clock source for the CPU. Throughout this document, FCY and FP are used interchangeably, except in the case of Doze mode. FP and FCY will be different when Doze mode is used with a doze ratio of 1:2 or lower.

TABLE 9-1: CONFIGURATION BIT VALUES FOR CLOCK SELECTION

Oscillator Mode	Oscillator Source	POSCMD<1:0>	FNOSC<2:0>	See Notes
Fast RC Oscillator with Divide-by-N (FRCDIVN)	Internal	xx	111	**1, 2**
Fast RC Oscillator with Divide-by-16 (FRCDIV16)	Internal	xx	110	**1**
Low-Power RC Oscillator (LPRC)	Internal	xx	101	**1**
Secondary (Timer1) Oscillator (SOSC)	Secondary	xx	100	**1**
Primary Oscillator (HS) with PLL (HSPLL)	Primary	10	011	
Primary Oscillator (XT) with PLL (XTPLL)	Primary	01	011	
Primary Oscillator (EC) with PLL (ECPLL)	Primary	00	011	**1**
Primary Oscillator (HS)	Primary	10	010	
Primary Oscillator (XT)	Primary	01	010	
Primary Oscillator (EC)	Primary	00	010	**1**
Fast RC Oscillator (FRC) with Divide-by-N and PLL (FRCPLL)	Internal	xx	001	**1**
Fast RC Oscillator (FRC)	Internal	xx	000	**1**

Note 1: OSC2 pin function is determined by the OSCIOFNC Configuration bit.

2: This is the default oscillator mode for an unprogrammed (erased) device.

REGISTER 11-3: RPINR3: PERIPHERAL PIN SELECT INPUT REGISTER 3

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	T2CKR<6:0>						
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-7 **Unimplemented:** Read as ‘0’

bit 6-0 **T2CKR<6:0>:** Assign Timer2 External Clock (T2CK) to the Corresponding RPn pin bits (see Table 11-2 for input pin selection numbers)

1111100 = Input tied to RPI124
•
•
•
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

REGISTER 11-8: RPINR11: PERIPHERAL PIN SELECT INPUT REGISTER 11

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	OCFAR<6:0>						
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-7 **Unimplemented:** Read as ‘0’

bit 6-0 **OCFAR<6:0>:** Assign Output Compare Fault A (OCFA) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

1111100 = Input tied to RPI124
•
•
•
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

NOTES:

REGISTER 21-15: CxBUFPNT4: CANx FILTERS 12-15 BUFFER POINTER REGISTER 4

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F15BP3	F15BP2	F15BP1	F15BP0	F14BP3	F14BP2	F14BP1	F14BP0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F13BP3	F13BP2	F13BP1	F13BP0	F12BP3	F12BP2	F12BP1	F12BP0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-12 **F15BP<3:0>:** RX Buffer Mask for Filter 15 bits
1111 = Filter hits received in RX FIFO buffer
1110 = Filter hits received in RX Buffer 14
•
•
•
0001 = Filter hits received in RX Buffer 1
0000 = Filter hits received in RX Buffer 0

bit 11-8 **F14BP<3:0>:** RX Buffer Mask for Filter 14 bits (same values as bits 15-12)

bit 7-4 **F13BP<3:0>:** RX Buffer Mask for Filter 13 bits (same values as bits 15-12)

bit 3-0 **F12BP<3:0>:** RX Buffer Mask for Filter 12 bits (same values as bits 15-12)

REGISTER 21-20: CxRXMnSID: CANx ACCEPTANCE FILTER MASK n STANDARD IDENTIFIER REGISTER (n = 0-2)

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3
bit 15							bit 8

R/W-x	R/W-x	R/W-x	U-0	R/W-x	U-0	R/W-x	R/W-x
SID2	SID1	SID0	—	MIDE	—	EID17	EID16
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-5 **SID<10:0>:** Standard Identifier bits
1 = Includes bit, SIDx, in filter comparison
0 = Bit, SIDx, is a don't care in filter comparison

bit 4 **Unimplemented:** Read as '0'

bit 3 **MIDE:** Identifier Receive Mode bit
1 = Matches only message types (standard or extended address) that correspond to the EXIDE bit in the filter
0 = Matches either standard or extended address message if filters match (i.e., if (Filter SIDx) = (Message SIDx) or if (Filter SIDx/EIDx) = (Message SIDx/EIDx))

bit 2 **Unimplemented:** Read as '0'

bit 1-0 **EID<17:16>:** Extended Identifier bits
1 = Includes bit, EIDx, in filter comparison
0 = Bit, EIDx, is a don't care in filter comparison

REGISTER 21-21: CxRXMnEID: CANx ACCEPTANCE FILTER MASK n EXTENDED IDENTIFIER REGISTER (n = 0-2)

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
EID<15:8>							
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
EID<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-0 **EID<15:0>:** Extended Identifier bits
1 = Includes bit, EIDx, in filter comparison
0 = Bit, EIDx, is a don't care in filter comparison

REGISTER 23-6: ADxCHS0: ADCx INPUT CHANNEL 0 SELECT REGISTER(3) (CONTINUED)

bit 7 **CH0NA:** Channel 0 Negative Input Select for Sample MUXA bit
1 = Channel 0 negative input is AN1(1)
0 = Channel 0 negative input is VREFL

bit 6 **Unimplemented:** Read as '0'

bit 5-0 **CH0SA<5:0>:** Channel 0 Positive Input Select for Sample MUXA bits(1,4,5)
111111 = Channel 0 positive input is (AN63) unconnected
111110 = Channel 0 positive input is (AN62) the CTMU temperature voltage
111101 = Channel 0 positive input is (AN61) reserved
•
•
•
110010 = Channel 0 positive input is (AN50) reserved
110001 = Channel 0 positive input is AN49
110000 = Channel 0 positive input is AN48
101111 = Channel 0 positive input is AN47
101110 = Channel 0 positive input is AN46
•
•
•
011010 = Channel 0 positive input is AN26
011001 = Channel 0 positive input is AN25 or Op Amp 5 output voltage(2)
011000 = Channel 0 positive input is AN24
•
•
•
000111 = Channel 0 positive input is AN7
000110 = Channel 0 positive input is AN6 or Op Amp 3 output voltage(2)
000101 = Channel 0 positive input is AN5
000100 = Channel 0 positive input is AN4
000011 = Channel 0 positive input is AN3 or Op Amp 1 output voltage(2)
000010 = Channel 0 positive input is AN2
000001 = Channel 0 positive input is AN1
000000 = Channel 0 positive input is AN0 or Op Amp 2 output voltage(2)

Note 1: AN0 through AN7 are repurposed when comparator and op amp functionality are enabled. See Figure 23-1 to determine how enabling a particular op amp or comparator affects selection choices for Channels 1, 2 and 3.

2: If the op amp is selected (OPMODE bit (CMxCON<10>) = 1), the OAx input is used; otherwise, the ANx input is used.

3: See the **"Pin Diagrams"** section for the available analog channels for each device.

4: Analog input selections for ADC1 are shown here. AN32-AN63 selections are not available for ADC2. The CH0SB5 and CH0SA5 bits are 'Reserved' for ADC2 and should be programmed to '0'.

5: Analog inputs, AN32-AN49, are available only when the ADCx is working in 10-bit mode.

TABLE 33-11: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param.	**Symbol**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
DO10	VOL	**Output Low Voltage** 4x Sink Driver Pins(1)	—	—	0.4	V	VDD = 3.3V, IOL ≤ 6 mA, -40°C ≤ TA ≤ +85°C, IOL ≤ 5 mA, +85°C < TA ≤ +125°C
		Output Low Voltage 8x Sink Driver Pins(2)	—	—	0.4	V	VDD = 3.3V, IOL ≤ 12 mA, -40°C ≤ TA ≤ +85°C, IOL ≤ 8 mA, +85°C < TA ≤ +125°C
DO20	VOH	**Output High Voltage** 4x Source Driver Pins(1)	2.4	—	—	V	IOH ≥ -10 mA, VDD = 3.3V
		Output High Voltage 8x Source Driver Pins(2)	2.4	—	—	V	IOH ≥ -15 mA, VDD = 3.3V
DO20A	VOH1	**Output High Voltage** 4x Source Driver Pins(1)	1.5	—	—	V	IOH ≥ -14 mA, VDD = 3.3V
			2.0	—	—		IOH ≥ -12 mA, VDD = 3.3V
			3.0	—	—		IOH ≥ -7 mA, VDD = 3.3V
		Output High Voltage 8x Source Driver Pins(2)	1.5	—	—	V	IOH ≥ -22 mA, VDD = 3.3V
			2.0	—	—		IOH ≥ -18 mA, VDD = 3.3V
			3.0	—	—		IOH ≥ -10 mA, VDD = 3.3V

Note 1: Includes all I/O pins that are not 8x Sink Driver pins (see below).

2: Includes the following pins:
For 44-pin devices: RA3, RA4, RA7, RA9, RA10, RB7, RB<15:9>, RC1 and RC<9:3>
For 64-pin devices: RA4, RA7, RA<10:9>, RB7, RB<15:9>, RC1, RC<9:3>, RC15 and RG<8:7>
For 100-pin devices: RA4, RA7, RA9, RA10, RB7, RB<15:9>, RC1, RC<9:3>, RC15, RD<3:1> and RG<8:6>

TABLE 33-12: ELECTRICAL CHARACTERISTICS: BOR

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min.(1)**	**Typ.**	**Max.**	**Units**	**Conditions**
BO10	VBOR	BOR Event on VDD Transition High-to-Low	2.7	—	2.95	V	VDD **(Note 2, Note 3)**
PO10	VPOR	POR Event on VDD Transition High-to-Low	1.75	—	1.95	V	**(Note 2)**

Note 1: Parameters are for design guidance only and are not tested in manufacturing.

2: The VBOR specification is relative to VDD.

3: The device is functional at VBORMIN < VDD < VDDMIN. Analog modules: ADC, op amp/comparator and comparator voltage reference will have degraded performance. Device functionality is tested but not characterized.

TABLE 34-8: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +150°C				
Param.	**Symbol**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
HDO10	VOL	**Output Low Voltage** 4x Sink Driver Pins(2)	—	—	0.4	V	IOL ≤ 5 mA, VDD = 3.3V **(Note 1)**
		Output Low Voltage 8x Sink Driver Pins(3)	—	—	0.4	V	IOL ≤ 8 mA, VDD = 3.3V **(Note 1)**
HDO20	VOH	**Output High Voltage** 4x Source Driver Pins(2)	2.4	—	—	V	IOH ≥ -10 mA, VDD = 3.3V **(Note 1)**
		Output High Voltage 8x Source Driver Pins(3)	2.4	—	—	V	IOH ≥ 15 mA, VDD = 3.3V **(Note 1)**
HDO20A	VOH1	**Output High Voltage** 4x Source Driver Pins(2)	1.5	—	—	V	IOH ≥ -3.9 mA, VDD = 3.3V **(Note 1)**
			2.0	—	—		IOH ≥ -3.7 mA, VDD = 3.3V **(Note 1)**
			3.0	—	—		IOH ≥ -2 mA, VDD = 3.3V **(Note 1)**
		Output High Voltage 8x Source Driver Pins(3)	1.5	—	—	V	IOH ≥ -7.5 mA, VDD = 3.3V **(Note 1)**
			2.0	—	—		IOH ≥ -6.8 mA, VDD = 3.3V **(Note 1)**
			3.0	—	—		IOH ≥ -3 mA, VDD = 3.3V **(Note 1)**

Note 1: Parameters are characterized, but not tested.

2: Includes all I/O pins that are not 8x Sink Driver pins (see below).

3: Includes the following pins:
For 44-pin devices: RA3, RA4, RA7, RA9, RA10, RB7, RB<15:9>, RC1 and RC<9:3>
For 64-pin devices: RA4, RA7, RA<10:9>, RB7, RB<15:9>, RC1, RC<9:3>, RC15 and RG<8:7>
For 100-pin devices: RA4, RA7, RA9, RA10, RB7, RB<15:9>, RC1, RC<9:3>, RC15, RD<3:1> and RG<8:6>

TABLE 34-9: DC CHARACTERISTICS: PROGRAM MEMORY

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +150°C				
Param.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
		Program Flash Memory					
HD130	EP	Cell Endurance	10,000	—	—	E/W	-40°C to +150°C(2)
HD134	TRETD	Characteristic Retention	20	—	—	Year	1000 E/W cycles or less and no other specifications are violated

Note 1: These parameters are assured by design, but are not characterized or tested in manufacturing.

2: Programming of the Flash memory is allowed up to +150°C.

TABLE 34-11: PLL CLOCK TIMING SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +150°C				
Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
HOS53	DCLK	CLKO Stability (Jitter)(1)	-5	0.5	5	%	Measured over 100 ms period

Note 1: These parameters are characterized by similarity, but are not tested in manufacturing. This specification is based on clock cycle by clock cycle measurements. To calculate the effective jitter for individual time bases or communication clocks use this formula:

$$Peripheral\ Clock\ Jitter = \frac{DCLK}{\sqrt{\left(\frac{FOSC}{Peripheral\ Bit\ Rate\ Clock}\right)}}$$

For example: FOSC = 32 MHz, DCLK = 5%, SPIx bit rate clock (i.e., SCKx) is 2 MHz.

$$SPI\ SCK\ Jitter = \left\lfloor \frac{DCLK}{\sqrt{\left(\frac{32\ MHz}{2\ MHz}\right)}} \right\rfloor = \left\lfloor \frac{5\%}{\sqrt{16}} \right\rfloor = \left\lfloor \frac{5\%}{4} \right\rfloor = 1.25\%$$

TABLE 34-12: INTERNAL FRC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +150°C					
Param No.	Characteristic	Min	Typ	Max	Units	Conditions	
	Internal FRC Accuracy @ FRC Frequency = 7.3728 MHz						
HF20	FRC	-3	—	+3	%	-40°C ≤ TA ≤ +150°C	VDD = 3.0-3.6V

TABLE 34-13: INTERNAL RC ACCURACY

AC CHARACTERISTICS		Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +150°C					
Param No.	Characteristic	Min	Typ	Max	Units	Conditions	
	LPRC @ 32.768 kHz(1,2)						
HF21	LPRC	-30	—	+30	%	-40°C ≤ TA ≤ +150°C	VDD = 3.0-3.6V

Note 1: Change of LPRC frequency as VDD changes.

2: LPRC accuracy impacts the Watchdog Timer Time-out Period (TWDT1). See **Section 30.5 "Watchdog Timer (WDT)"** for more information.