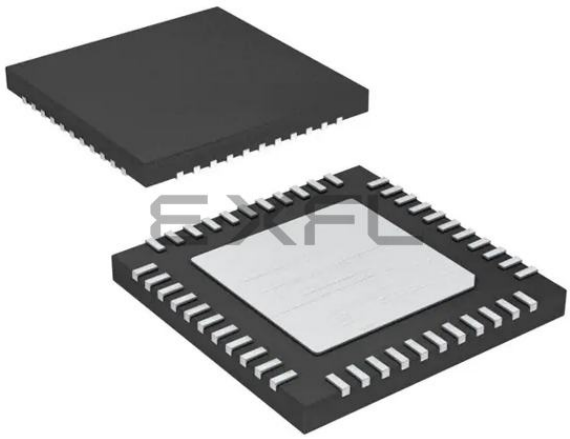

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## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | dsPIC |
| Core Size | 16-Bit |
| Speed | 70 MIPs |
| Connectivity | CANbus, I²C, IrDA, LINbus, QEI, SPI, UART/USART |
| Peripherals | Brown-out Detect/Reset, DMA, I²S, Motor Control PWM, POR, PWM, WDT |
| Number of I/O | 35 |
| Program Memory Size | 512KB (170K x 24) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 48K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 3.6V |
| Data Converters | A/D 18x10b/12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 44-VQFN Exposed Pad |
| Supplier Device Package | 44-QFN (8x8) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep512gm604-i-ml |

**TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)**

| Pin Name | Pin Type | Buffer Type | PPS | Description |
|---|---|---|---|---|
| PMA0 | I/O | TTL/ST | No | Parallel Master Port Address Bit 0 input (Buffered Slave modes) and output (Master modes). |
| PMA1 | I/O | TTL/ST | No | Parallel Master Port Address Bit 1 input (Buffered Slave modes) and output (Master modes). |
| PMA2-PMA13 | O | — | No | Parallel Master Port Address Bits 2-13 (Demultiplexed Master modes). |
| PMBE | O | — | No | Parallel Master Port Byte Enable strobe. |
| PMCS1, PMCS2 | O | — | No | Parallel Master Port Chip Select 1 and 2 strobe. |
| PMD0-PMD7 | I/O | TTL/ST | No | Parallel Master Port Data (Demultiplexed Master mode) or Address/Data (Multiplexed Master modes). |
| PMRD | O | — | No | Parallel Master Port Read strobe. |
| PMWR | O | — | No | Parallel Master Port Write strobe. |
| FLT1-FLT2(1) | I | ST | Yes | PWMx Fault Inputs 1 through 2. |
| FLT3-FLT8(1) | I | ST | No | PWMx Fault Inputs 3 through 8 |
| FLT32 | I | ST | No | PWMx Fault Input 32 |
| DTCMP1-DTCMP6(1) | I | ST | Yes | PWMx Dead-Time Compensation Inputs 1 through 6. |
| PWM1L-PWM6L(1) | O | — | No | PWMx Low Outputs 1 through 7. |
| PWM1H-PWM6H(1) | O | — | No | PWMx High Outputs 1 through 7. |
| SYNCI1(1), SYNCI2(1) | I | ST | Yes | PWMx Synchronization Input 1. |
| SYNCO1, SYNCO2(1) | O | — | Yes | PWMx Synchronization Outputs 1 and 2. |
| PGED1 | I/O | ST | No | Data I/O pin for Programming/Debugging Communication Channel 1. |
| PGEC1 | I | ST | No | Clock input pin for Programming/Debugging Communication Channel 1. |
| PGED2 | I/O | ST | No | Data I/O pin for Programming/Debugging Communication Channel 2. |
| PGEC2 | I | ST | No | Clock input pin for Programming/Debugging Communication Channel 2. |
| PGED3 | I/O | ST | No | Data I/O pin for Programming/Debugging Communication Channel 3. |
| PGEC3 | I | ST | No | Clock input pin for Programming/Debugging Communication Channel 3. |
| $\overline{MCLR}$ | I/P | ST | No | Master Clear (Reset) input. This pin is an active-low Reset to the device. |
| $AV_{DD}$(2) | P | P | No | Positive supply for analog modules. This pin must be connected at all times. |
| $AV_{SS}$ | P | P | No | Ground reference for analog modules. |
| $V_{DD}$ | P | — | No | Positive supply for peripheral logic and I/O pins. |
| $V_{CAP}$ | P | — | No | CPU logic filter capacitor connection. |
| $V_{SS}$ | P | — | No | Ground reference for logic and I/O pins. |
| $V_{REF+}$ | I | Analog | No | Analog voltage reference (high) input. |
| $V_{REF-}$ | I | Analog | No | Analog voltage reference (low) input. |

**Legend:** CMOS = CMOS compatible input or output; Analog = Analog input; P = Power
ST = Schmitt Trigger input with CMOS levels; O = Output; I = Input
PPS = Peripheral Pin Select; TTL = TTL input buffer

**Note 1:** This pin is not available on all devices. For more information, see the **"Pin Diagrams"** section for pin availability.

**2:** $AV_{DD}$ must be connected at all times.

**REGISTER 3-2: CORCON: CORE CONTROL REGISTER(3) (CONTINUED)**

bit 3 **IPL3:** CPU Interrupt Priority Level Status bit 3(2)
1 = CPU Interrupt Priority Level is greater than 7
0 = CPU Interrupt Priority Level is 7 or less

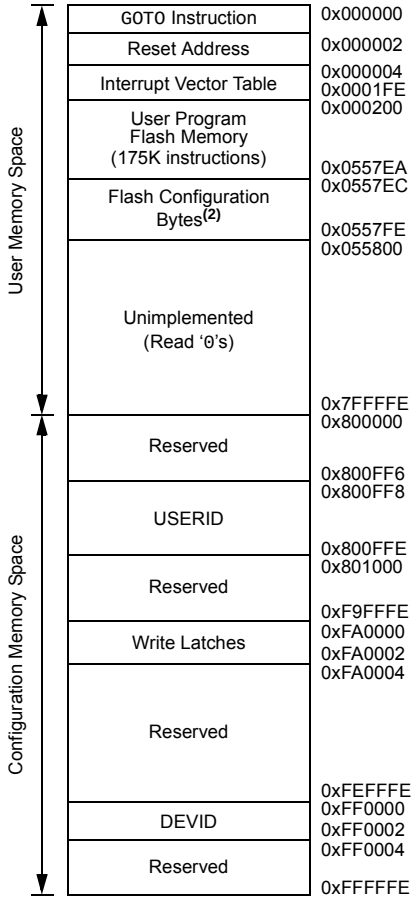
bit 2 **SFA:** Stack Frame Active Status bit
1 = Stack frame is active; W14 and W15 address 0x0000 to 0xFFFF, regardless of DSRPAG and DSWPAG values
0 = Stack frame is not active; W14 and W15 address of EDS or Base Data Space

bit 1 **RND:** Rounding Mode Select bit
1 = Biased (conventional) rounding is enabled
0 = Unbiased (convergent) rounding is enabled

bit 0 **IF:** Integer or Fractional Multiplier Mode Select bit
1 = Integer mode is enabled for DSP multiply
0 = Fractional mode is enabled for DSP multiply

**Note 1:** This bit is always read as '0'.
**2:** The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU Interrupt Priority Level.
**3:** Refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"CPU"** (DS70359) for more detailed information.

**FIGURE 4-3: PROGRAM MEMORY MAP FOR dsPIC33EP512GM3XX/6XX/7XX DEVICES(1)**




**Note 1:** Memory areas are not shown to scale.

**2:** On Reset, these bits are automatically copied into the device Configuration Shadow registers.

**TABLE 4-6: OUTPUT COMPARE REGISTER MAP**

| SFR Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| OC1CON1 | 0900 | — | — | OCSIDL | OCTSEL2 | OCTSEL1 | OCTSEL0 | — | ENFLTB | ENFLTA | — | OCFLTB | OCFLTA | TRIGMODE | OCM2 | OCM1 | OCM0 | 0000 |
| OC1CON2 | 0902 | FLTMD | FLTOUT | FLTTRIEN | OCINV | — | — | — | OC32 | OCTRIG | TRIGSTAT | OCTRIS | SYNCSEL4 | SYNCSEL3 | SYNCSEL2 | SYNCSEL1 | SYNCSEL0 | 000C |
| OC1RS | 0904 | Output Compare 1 Secondary Register | | | | | | | | | | | | | | | | xxxx |
| OC1R | 0906 | Output Compare 1 Register | | | | | | | | | | | | | | | | xxxx |
| OC1TMR | 0908 | Output Compare 1 Timer Value Register | | | | | | | | | | | | | | | | xxxx |
| OC2CON1 | 090A | — | — | OCSIDL | OCTSEL2 | OCTSEL1 | OCTSEL0 | — | ENFLTB | ENFLTA | — | OCFLTB | OCFLTA | TRIGMODE | OCM2 | OCM1 | OCM0 | 0000 |
| OC2CON2 | 090C | FLTMD | FLTOUT | FLTTRIEN | OCINV | — | — | — | OC32 | OCTRIG | TRIGSTAT | OCTRIS | SYNCSEL4 | SYNCSEL3 | SYNCSEL2 | SYNCSEL1 | SYNCSEL0 | 000C |
| OC2RS | 090E | Output Compare 2 Secondary Register | | | | | | | | | | | | | | | | xxxx |
| OC2R | 0910 | Output Compare 2 Register | | | | | | | | | | | | | | | | xxxx |
| OC2TMR | 0912 | Output Compare 2 Timer Value Register | | | | | | | | | | | | | | | | xxxx |
| OC3CON1 | 0914 | — | — | OCSIDL | OCTSEL2 | OCTSEL1 | OCTSEL0 | — | ENFLTB | ENFLTA | — | OCFLTB | OCFLTA | TRIGMODE | OCM2 | OCM1 | OCM0 | 0000 |
| OC3CON2 | 0916 | FLTMD | FLTOUT | FLTTRIEN | OCINV | — | — | — | OC32 | OCTRIG | TRIGSTAT | OCTRIS | SYNCSEL4 | SYNCSEL3 | SYNCSEL2 | SYNCSEL1 | SYNCSEL0 | 000C |
| OC3RS | 0918 | Output Compare 3 Secondary Register | | | | | | | | | | | | | | | | xxxx |
| OC3R | 091A | Output Compare 3 Register | | | | | | | | | | | | | | | | xxxx |
| OC3TMR | 091C | Output Compare 3 Timer Value Register | | | | | | | | | | | | | | | | xxxx |
| OC4CON1 | 091E | — | — | OCSIDL | OCTSEL2 | OCTSEL1 | OCTSEL0 | — | ENFLTB | ENFLTA | — | OCFLTB | OCFLTA | TRIGMODE | OCM2 | OCM1 | OCM0 | 0000 |
| OC4CON2 | 0920 | FLTMD | FLTOUT | FLTTRIEN | OCINV | — | — | — | OC32 | OCTRIG | TRIGSTAT | OCTRIS | SYNCSEL4 | SYNCSEL3 | SYNCSEL2 | SYNCSEL1 | SYNCSEL0 | 000C |
| OC4RS | 0922 | Output Compare 4 Secondary Register | | | | | | | | | | | | | | | | xxxx |
| OC4R | 0924 | Output Compare 4 Register | | | | | | | | | | | | | | | | xxxx |
| OC4TMR | 0926 | Output Compare 4 Timer Value Register | | | | | | | | | | | | | | | | xxxx |
| OC5CON1 | 0928 | — | — | OCSIDL | OCTSEL2 | OCTSEL1 | OCTSEL0 | — | ENFLTB | ENFLTA | — | OCFLTB | OCFLTA | TRIGMODE | OCM2 | OCM1 | OCM0 | 0000 |
| OC5CON2 | 092A | FLTMD | FLTOUT | FLTTRIEN | OCINV | — | — | — | OC32 | OCTRIG | TRIGSTAT | OCTRIS | SYNCSEL4 | SYNCSEL3 | SYNCSEL2 | SYNCSEL1 | SYNCSEL0 | 000C |
| OC5RS | 092C | Output Compare 5 Secondary Register | | | | | | | | | | | | | | | | xxxx |
| OC5R | 092E | Output Compare 5 Register | | | | | | | | | | | | | | | | xxxx |
| OC5TMR | 0930 | Output Compare 5 Timer Value Register | | | | | | | | | | | | | | | | xxxx |
| OC6CON1 | 0932 | — | — | OCSIDL | OCTSEL2 | OCTSEL1 | OCTSEL0 | — | ENFLTB | ENFLTA | — | OCFLTB | OCFLTA | TRIGMODE | OCM2 | OCM1 | OCM0 | 0000 |
| OC6CON2 | 0934 | FLTMD | FLTOUT | FLTTRIEN | OCINV | — | — | — | OC32 | OCTRIG | TRIGSTAT | OCTRIS | SYNCSEL4 | SYNCSEL3 | SYNCSEL2 | SYNCSEL1 | SYNCSEL0 | 000C |
| OC6RS | 0936 | Output Compare 6 Secondary Register | | | | | | | | | | | | | | | | xxxx |
| OC6R | 0938 | Output Compare 6 Register | | | | | | | | | | | | | | | | xxxx |
| OC6TMR | 093A | Output Compare 6 Timer Value Register | | | | | | | | | | | | | | | | xxxx |

**Legend:** x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**TABLE 4-33: PERIPHERAL PIN SELECT INPUT REGISTER MAP FOR dsPIC33EPXXXGM60X/7XX DEVICES**

| SFR Name | Addr. | Bit 15 | Bit 14 | Bit 13 | Bit 12 | Bit 11 | Bit 10 | Bit 9 | Bit 8 | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | All Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RPINR0 | 06A0 | — | INT1R<6:0> | | | | | | | — | — | — | — | — | — | — | — | 0000 |
| RPINR1 | 06A2 | — | — | — | — | — | — | — | — | — | INT2R<6:0> | | | | | | | 0000 |
| RPINR3 | 06A6 | — | — | — | — | — | — | — | — | — | T2CKR<6:0> | | | | | | | 0000 |
| RPINR7 | 06AE | — | IC2R<6:0> | | | | | | | — | IC1R<6:0> | | | | | | | 0000 |
| RPINR8 | 06B0 | — | IC4R<6:0> | | | | | | | — | IC3R<6:0> | | | | | | | 0000 |
| RPINR9 | 06B2 | — | IC6R<6:0> | | | | | | | — | IC5R<6:0> | | | | | | | 0000 |
| RPINR10 | 06B4 | — | IC8R<6:0> | | | | | | | — | IC7R<6:0> | | | | | | | 0000 |
| RPINR11 | 06B6 | — | — | — | — | — | — | — | — | — | OCFAR<6:0> | | | | | | | 0000 |
| RPINR12 | 06B8 | — | FLT2R<6:0> | | | | | | | — | FLT1R<6:0> | | | | | | | 0000 |
| RPINR14 | 06BC | — | QEB1R<6:0> | | | | | | | — | QEA1R<6:0> | | | | | | | 0000 |
| RPINR15 | 06BE | — | HOME1R<6:0> | | | | | | | — | INDX1R<6:0> | | | | | | | 0000 |
| RPINR16 | 06C0 | — | QEB2R<6:0> | | | | | | | — | QEA2R<6:0> | | | | | | | 0000 |
| RPINR17 | 06C2 | — | HOME2R<6:0> | | | | | | | — | INDX2R<6:0> | | | | | | | 0000 |
| RPINR18 | 06C4 | — | — | — | — | — | — | — | — | — | U1RXR<6:0> | | | | | | | 0000 |
| RPINR19 | 06C6 | — | — | — | — | — | — | — | — | — | U2RXR<6:0> | | | | | | | 0000 |
| RPINR22 | 06CC | — | SCK2R<6:0> | | | | | | | — | SDI2R<6:0> | | | | | | | 0000 |
| RPINR23 | 06CE | — | — | — | — | — | — | — | — | — | SS2R<6:0> | | | | | | | 0000 |
| RPINR24 | 06D0 | — | CSCKR<6:0> | | | | | | | — | CSDIR<6:0> | | | | | | | 0000 |
| RPINR25 | 06D2 | — | — | — | — | — | — | — | — | — | COFSR<6:0> | | | | | | | 0000 |
| RPINR26 | 06D4 | — | C2RXR<6:0> | | | | | | | — | C1RXR<6:0> | | | | | | | 0000 |
| RPINR27 | 06D6 | — | U3CTSR<6:0> | | | | | | | — | U3RXR<6:0> | | | | | | | 0000 |
| RPINR28 | 06D8 | — | U4CTSR<6:0> | | | | | | | — | U4RXR<6:0> | | | | | | | 0000 |
| RPINR29 | 06DA | — | SCK3R<6:0> | | | | | | | — | SDI3R<6:0> | | | | | | | 0000 |
| RPINR30 | 06DC | — | — | — | — | — | — | — | — | — | SS3R<6:0> | | | | | | | 0000 |
| RPINR37 | 06EA | — | SYNCI1R<6:0> | | | | | | | — | — | — | — | — | — | — | — | 0000 |
| RPINR38 | 06EC | — | DTCMP1R<6:0> | | | | | | | — | — | — | — | — | — | — | — | 0000 |
| RPINR39 | 06EE | — | DTCMP3R<6:0> | | | | | | | — | DTCMP2R<6:0> | | | | | | | 0000 |
| RPINR40 | 06F0 | — | DTCMP5R<6:0> | | | | | | | — | DTCMP4R<6:0> | | | | | | | 0000 |
| RPINR41 | 06F2 | — | — | — | — | — | — | — | — | — | DTCMP6R<6:0> | | | | | | | 0000 |

**Legend:** — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

**REGISTER 8-13: DMALCA: DMA LAST CHANNEL ACTIVE STATUS REGISTER**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | R-1 | R-1 | R-1 | R-1 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | LSTCH<3:0> | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-4 **Unimplemented:** Read as ‘0’

bit 3-0 **LSTCH<3:0>:** Last DMA Controller Channel Active Status bits

1111 = No DMA transfer has occurred since system Reset
1110 = Reserved
•
•
•
0100 = Reserved
0011 = Last data transfer was handled by Channel 3
0010 = Last data transfer was handled by Channel 2
0001 = Last data transfer was handled by Channel 1
0000 = Last data transfer was handled by Channel 0

## 10.3 Doze Mode

The preferred strategies for reducing power consumption are changing clock speed and invoking one of the power-saving modes. In some circumstances, this cannot be practical. For example, it may be necessary for an application to maintain uninterrupted synchronous communication, even while it is doing nothing else. Reducing system clock speed can introduce communication errors, while using a power-saving mode can stop communications completely.

Doze mode is a simple and effective alternative method to reduce power consumption while the device is still executing code. In this mode, the system clock continues to operate from the same source and at the same speed. Peripheral modules continue to be clocked at the same speed, while the CPU clock speed is reduced. Synchronization between the two clock domains is maintained, allowing the peripherals to access the SFRs while the CPU executes code at a slower rate.

Doze mode is enabled by setting the DOZEN bit (CLKDIV<11>). The ratio between peripheral and core clock speed is determined by the DOZE<2:0> bits (CLKDIV<14:12>). There are eight possible configurations, from 1:1 to 1:128, with 1:1 being the default setting.

Programs can use Doze mode to selectively reduce power consumption in event-driven applications. This allows clock-sensitive functions, such as synchronous communications, to continue without interruption while the CPU Idles, waiting for something to invoke an interrupt routine. An automatic return to full-speed CPU operation on interrupts can be enabled by setting the ROI bit (CLKDIV<15>). By default, interrupt events have no effect on Doze mode operation.

For example, suppose the device is operating at 20 MIPS and the CAN module has been configured for 500 kbps based on this device operating speed. If the device is placed in Doze mode with a clock frequency ratio of 1:4, the CAN module continues to communicate at the required bit rate of 500 kbps, but the CPU now starts executing instructions at a frequency of 5 MIPS.

## 10.4 Peripheral Module Disable

The Peripheral Module Disable (PMD) registers provide a method to disable a peripheral module by stopping all clock sources supplied to that module. When a peripheral is disabled, using the appropriate PMD control bit, the peripheral is in a minimum power consumption state. The control and status registers associated with the peripheral are also disabled, so writes to those registers do not have effect and read values are invalid.

A peripheral module is enabled only if both the associated bit in the PMD register is cleared and the peripheral is supported by the specific dsPIC® DSC variant. If the peripheral is present in the device, it is enabled in the PMD register by default.

| | |
|---|---|
| **Note:** | If a PMD bit is set, the corresponding module is disabled after a delay of one instruction cycle. Similarly, if a PMD bit is cleared, the corresponding module is enabled after a delay of one instruction cycle (assuming the module control registers are already configured to enable module operation). |

**REGISTER 11-6: RPINR9: PERIPHERAL PIN SELECT INPUT REGISTER 9**

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | IC6R<6:0> | | | | | | |
| bit 15 | | | | | | | bit 8 |

| U-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | IC5R<6:0> | | | | | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15 **Unimplemented:** Read as ‘0’

bit 14-8 **IC6R<6:0>:** Assign Input Capture 6 (IC6) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

1111100 = Input tied to RPI124
•
•
•
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

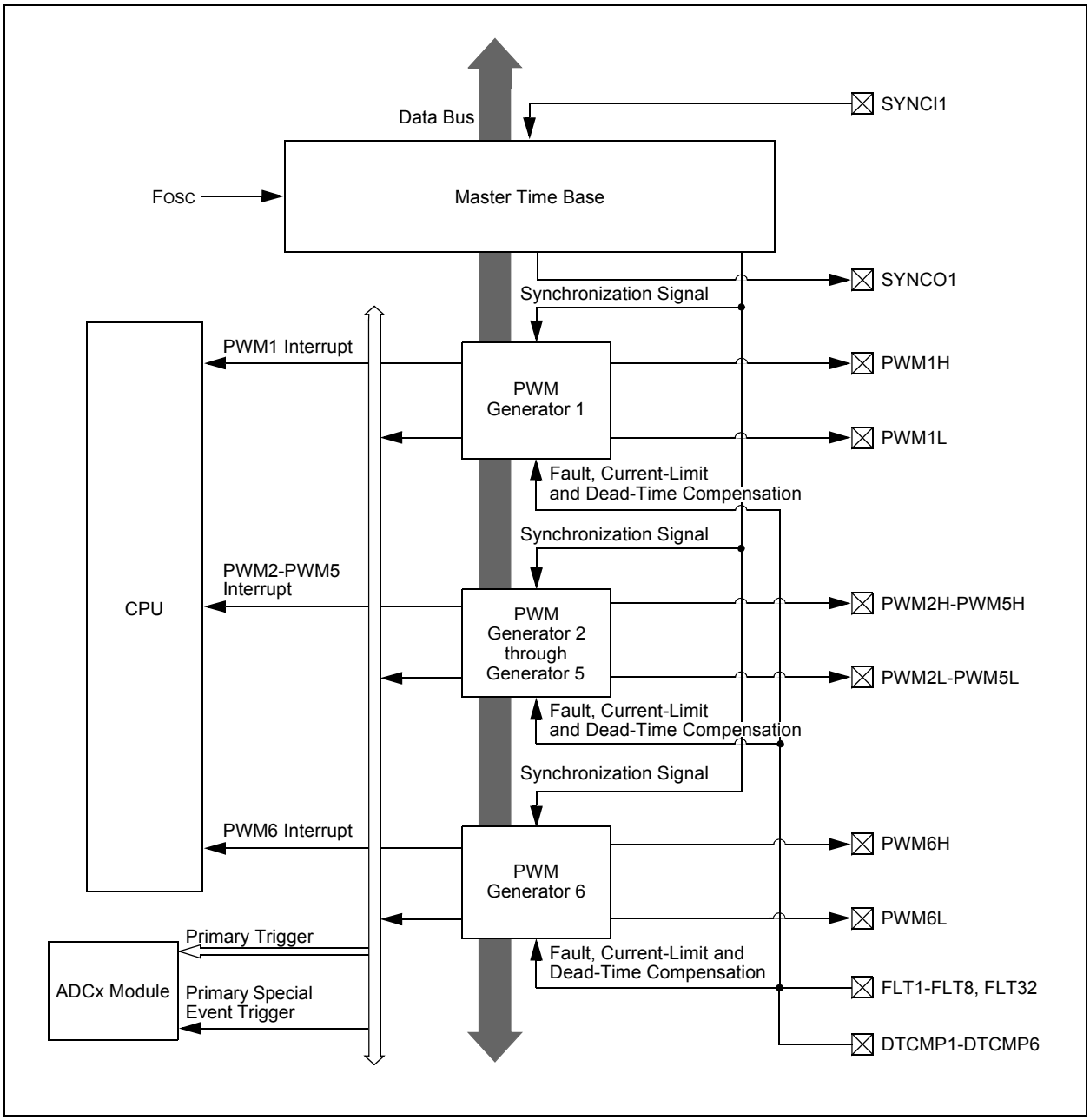
bit 7 **Unimplemented:** Read as ‘0’

bit 6-0 **IC5R<6:0>:** Assign Input Capture 5 (IC5) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

1111100 = Input tied to RPI124
•
•
•
0000001 = Input tied to CMP1
0000000 = Input tied to Vss

**NOTES:**

**FIGURE 16-1: HIGH-SPEED PWMx MODULE ARCHITECTURAL OVERVIEW**



**REGISTER 16-6: STCON2: PWMx SECONDARY MASTER CLOCK DIVIDER SELECT REGISTER 2**

| U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 | U-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | — | — | — |
| bit 15 | | | | | | | bit 8 |

| U-0 | U-0 | U-0 | U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 |
|---|---|---|---|---|---|---|---|
| — | — | — | — | — | PCLKDIV<2:0>(1) | | |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as ‘0’ | |
| -n = Value at POR | ‘1’ = Bit is set | ‘0’ = Bit is cleared | x = Bit is unknown |

bit 15-3 **Unimplemented:** Read as ‘0’

bit 2-0 **PCLKDIV<2:0>:** PWMx Input Clock Prescaler (Divider) Select bits(1)

111 = Reserved
110 = Divide-by-64
101 = Divide-by-32
100 = Divide-by-16
011 = Divide-by-8
010 = Divide-by-4
001 = Divide-by-2
000 = Divide-by-1, maximum PWMx timing resolution (power-on default)

**Note 1:** These bits should be changed only when PTEN = 0. Changing the clock selection during operation will yield unpredictable results.

**REGISTER 26-2: CMxCON: OP AMP/COMPARATOR x CONTROL REGISTER (x = 1, 2, 3 OR 5) (CONTINUED)**

bit 7-6 **EVPOL<1:0>:** Trigger/Event/Interrupt Polarity Select bits(3)

11 = Trigger/event/interrupt generated on any change of the comparator output (while CEVT = 0)

10 = Trigger/event/interrupt generated only on high-to-low transition of the polarity selected comparator output (while CEVT = 0)

If CPOL = 1 (inverted polarity):
Low-to-high transition of the comparator output.

If CPOL = 0 (non-inverted polarity):
High-to-low transition of the comparator output.

01 = Trigger/event/interrupt generated only on low-to-high transition of the polarity selected comparator output (while CEVT = 0)

If CPOL = 1 (inverted polarity):
High-to-low transition of the comparator output.

If CPOL = 0 (non-inverted polarity):
Low-to-high transition of the comparator output.

00 = Trigger/event/interrupt generation is disabled.

bit 5 **Unimplemented:** Read as '0'

bit 4 **CREF:** Comparator Reference Select bit (VIN+ input)(1)

1 = VIN+ input connects to internal CVREFIN voltage
0 = VIN+ input connects to CxIN1+ pin

bit 3-2 **Unimplemented:** Read as '0'

bit 1-0 **CCH<1:0>:** Op Amp/Comparator Channel Select bits(1)

11 = Inverting input of op amp/comparator connects to CxIN4- pin
10 = Inverting input of op amp/comparator connects to CxIN3- pin
01 = Inverting input of op amp/comparator connects to CxIN2- pin
00 = Inverting input of op amp/comparator connects to CxIN1- pin

**Note 1:** Inputs that are selected and not available will be tied to VSS. See the **"Pin Diagrams"** section for available inputs for each package.

**2:** The op amp and the comparator can be used simultaneously in these devices. The OPMODE bit only enables the op amp while the comparator is still functional.

**3:** After configuring the comparator, either for a high-to-low or low-to-high COUT transition (EVPOL<1:0> (CMxCON<7:6>) = 10 or 01), the Comparator Event bit, CEVT (CMxCON<9>), and the Comparator Combined Interrupt Flag, CMPIF (IFS1<2>), **must be cleared** before enabling the Comparator Interrupt Enable bit, CMPIE (IEC1<2>).

**TABLE 31-2: INSTRUCTION SET OVERVIEW (CONTINUED)**

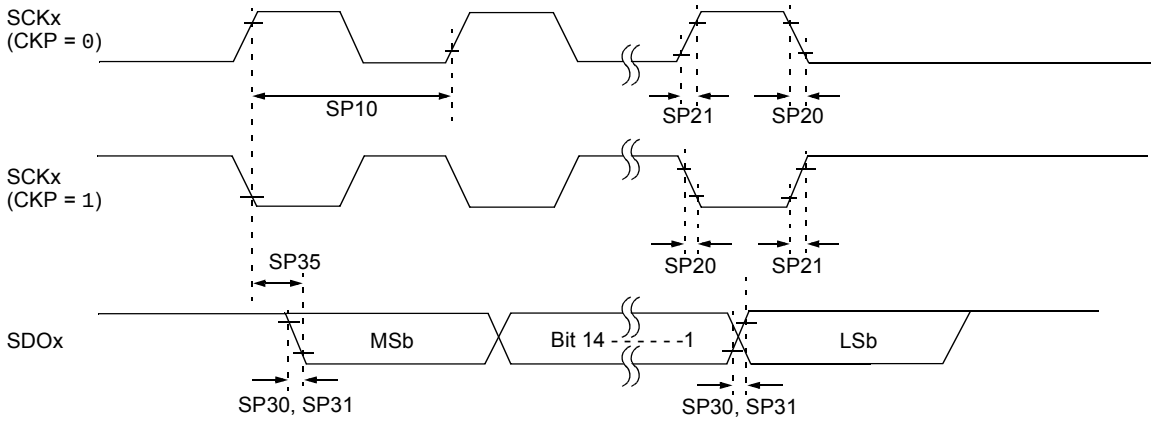
| Base Instr # | Assembly Mnemonic | Assembly Syntax | Description | # of Words | # of Cycles | Status Flags Affected |
|---|---|---|---|---|---|---|
| 53 | NEG | NEG Acc | Negate Accumulator | 1 | 1 | OA,OB,OAB, SA,SB,SAB |
| | | NEG f | f = $\overline{f}$ + 1 | 1 | 1 | C,DC,N,OV,Z |
| | | NEG f,WREG | WREG = $\overline{f}$ + 1 | 1 | 1 | C,DC,N,OV,Z |
| | | NEG Ws,Wd | Wd = $\overline{Ws}$ + 1 | 1 | 1 | C,DC,N,OV,Z |
| 54 | NOP | NOP | No Operation | 1 | 1 | None |
| | | NOPR | No Operation | 1 | 1 | None |
| 55 | POP | POP f | Pop f from Top-of-Stack (TOS) | 1 | 1 | None |
| | | POP Wdo | Pop from Top-of-Stack (TOS) to Wdo | 1 | 1 | None |
| | | POP.D Wnd | Pop from Top-of-Stack (TOS) to W(nd):W(nd + 1) | 1 | 2 | None |
| | | POP.S | Pop Shadow Registers | 1 | 1 | All |
| 56 | PUSH | PUSH f | Push f to Top-of-Stack (TOS) | 1 | 1 | None |
| | | PUSH Wso | Push Wso to Top-of-Stack (TOS) | 1 | 1 | None |
| | | PUSH.D Wns | Push W(ns):W(ns + 1) to Top-of-Stack (TOS) | 1 | 2 | None |
| | | PUSH.S | Push Shadow Registers | 1 | 1 | None |
| 57 | PWRSAV | PWRSAV #lit1 | Go into Sleep or Idle mode | 1 | 1 | WDTO,Sleep |
| 58 | RCALL | RCALL Expr | Relative Call | 1 | 4 | SFA |
| | | RCALL Wn | Computed Call | 1 | 4 | SFA |
| 59 | REPEAT | REPEAT #lit15 | Repeat Next Instruction lit15 + 1 times | 1 | 1 | None |
| | | REPEAT Wn | Repeat Next Instruction (Wn) + 1 times | 1 | 1 | None |
| 60 | RESET | RESET | Software device Reset | 1 | 1 | None |
| 61 | RETFIE | RETFIE | Return from interrupt | 1 | 6 (5) | SFA |
| 62 | RETLW | RETLW #lit10,Wn | Return with literal in Wn | 1 | 6 (5) | SFA |
| 63 | RETURN | RETURN | Return from Subroutine | 1 | 6 (5) | SFA |
| 64 | RLC | RLC f | f = Rotate Left through Carry f | 1 | 1 | C,N,Z |
| | | RLC f,WREG | WREG = Rotate Left through Carry f | 1 | 1 | C,N,Z |
| | | RLC Ws,Wd | Wd = Rotate Left through Carry Ws | 1 | 1 | C,N,Z |
| 65 | RLNC | RLNC f | f = Rotate Left (No Carry) f | 1 | 1 | N,Z |
| | | RLNC f,WREG | WREG = Rotate Left (No Carry) f | 1 | 1 | N,Z |
| | | RLNC Ws,Wd | Wd = Rotate Left (No Carry) Ws | 1 | 1 | N,Z |
| 66 | RRC | RRC f | f = Rotate Right through Carry f | 1 | 1 | C,N,Z |
| | | RRC f,WREG | WREG = Rotate Right through Carry f | 1 | 1 | C,N,Z |
| | | RRC Ws,Wd | Wd = Rotate Right through Carry Ws | 1 | 1 | C,N,Z |
| 67 | RRNC | RRNC f | f = Rotate Right (No Carry) f | 1 | 1 | N,Z |
| | | RRNC f,WREG | WREG = Rotate Right (No Carry) f | 1 | 1 | N,Z |
| | | RRNC Ws,Wd | Wd = Rotate Right (No Carry) Ws | 1 | 1 | N,Z |
| 68 | SAC | SAC Acc,#Slit4,Wdo | Store Accumulator | 1 | 1 | None |
| | | SAC.R Acc,#Slit4,Wdo | Store Rounded Accumulator | 1 | 1 | None |
| 69 | SE | SE Ws,Wnd | Wnd = sign-extended Ws | 1 | 1 | C,N,Z |
| 70 | SETM | SETM f | f = 0xFFFF | 1 | 1 | None |
| | | SETM WREG | WREG = 0xFFFF | 1 | 1 | None |
| | | SETM Ws | Ws = 0xFFFF | 1 | 1 | None |
| 71 | SFTAC | SFTAC Acc,Wn | Arithmetic Shift Accumulator by (Wn) | 1 | 1 | OA,OB,OAB, SA,SB,SAB |
| | | SFTAC Acc,#Slit6 | Arithmetic Shift Accumulator by Slit6 | 1 | 1 | OA,OB,OAB, SA,SB,SAB |

**Note:** Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

**TABLE 33-32: SPI2 AND SPI3 MAXIMUM DATA/CLOCK RATE SUMMARY**

| AC CHARACTERISTICS | | | Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | |
|---|---|---|---|---|---|---|
| **Maximum Data Rate** | **Master Transmit Only (Half-Duplex)** | **Master Transmit/Receive (Full-Duplex)** | **Slave Transmit/Receive (Full-Duplex)** | **CKE** | **CKP** | **SMP** |
| 15 MHz | Table 33-33 | — | — | 0,1 | 0,1 | 0,1 |
| 9 MHz | — | Table 33-34 | — | 1 | 0,1 | 1 |
| 9 MHz | — | Table 33-35 | — | 0 | 0,1 | 1 |
| 15 MHz | — | — | Table 33-36 | 1 | 0 | 0 |
| 11 MHz | — | — | Table 33-37 | 1 | 1 | 0 |
| 15 MHz | — | — | Table 33-38 | 0 | 1 | 0 |
| 11 MHz | — | — | Table 33-39 | 0 | 0 | 0 |

**FIGURE 33-15: SPI2 AND SPI3 MASTER MODE (HALF-DUPLEX, TRANSMIT ONLY, CKE = 0) TIMING CHARACTERISTICS**




**Note:** Refer to Figure 33-1 for load conditions.

**FIGURE 33-33: I2Cx BUS START/STOP BITS TIMING CHARACTERISTICS (SLAVE MODE)**

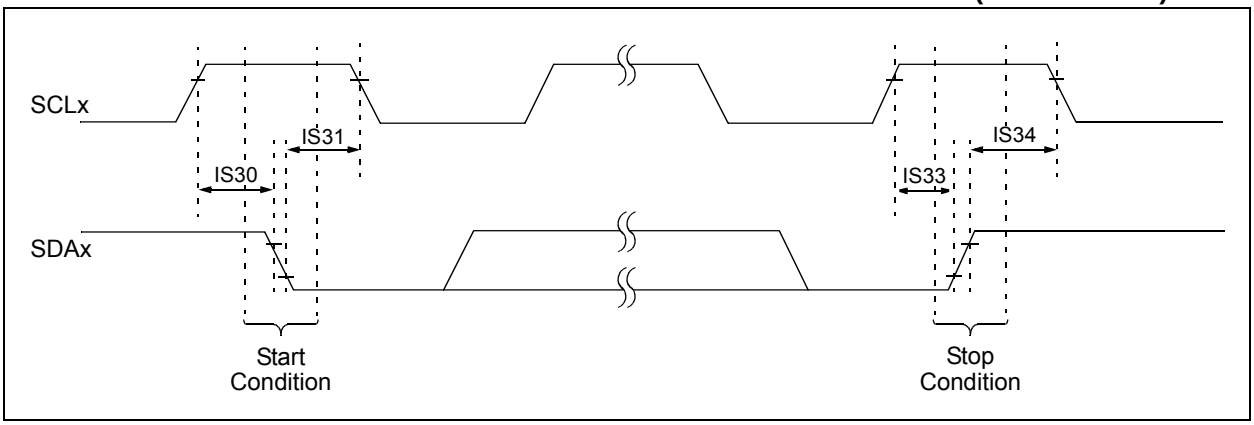



**FIGURE 33-34: I2Cx BUS DATA TIMING CHARACTERISTICS (SLAVE MODE)**

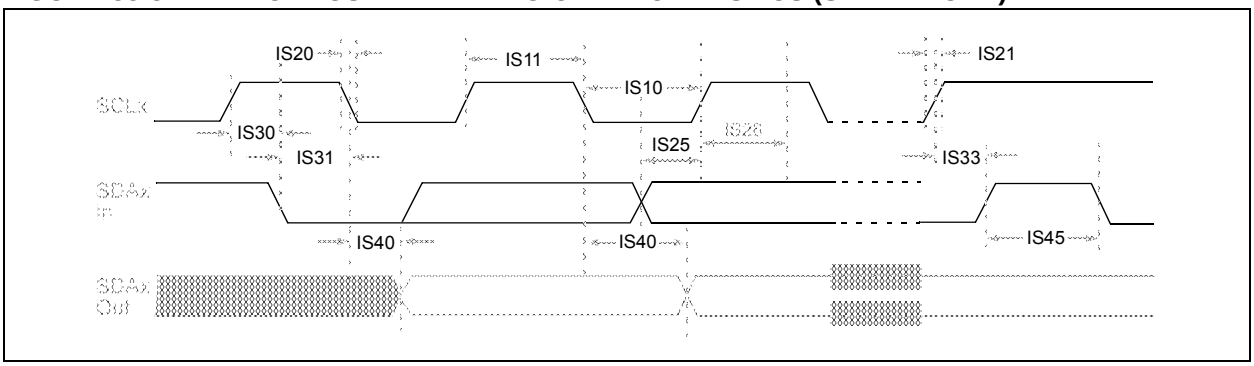


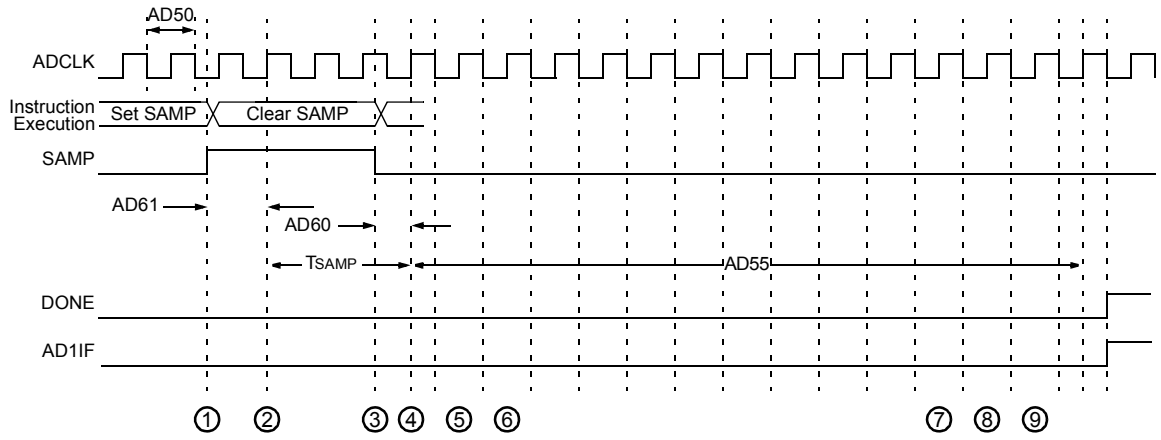
**TABLE 33-57: ADCx MODULE SPECIFICATIONS (12-BIT MODE)**

| AC CHARACTERISTICS | | | Standard Operating Conditions (see Note 1): 3.0V to 3.6V (unless otherwise stated)<br>Operating temperature -40°C ≤ TA ≤ +85°C for Industrial<br>-40°C ≤ TA ≤ +125°C for Extended | | | | |
|---|---|---|---|---|---|---|---|
| **Param No.** | **Symbol** | **Characteristic** | **Min.** | **Typ.** | **Max.** | **Units** | **Conditions** |
| **ADC Accuracy (12-Bit Mode) – VREF-** | | | | | | | |
| AD20a | Nr | Resolution | 12 data bits | | | bits | |
| AD21a | INL | Integral Nonlinearity | -3 | — | +3 | LSb | VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V **(Note 2)** |
| AD22a | DNL | Differential Nonlinearity | ≥ 1 | — | < 1 | LSb | VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V **(Note 2)** |
| AD23a | GERR | Gain Error | -10 | — | 10 | LSb | VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V **(Note 2)** |
| AD24a | EOFF | Offset Error | -5 | — | 5 | LSb | VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V **(Note 2)** |
| AD25a | — | Monotonicity | — | — | — | — | Guaranteed |
| **Dynamic Performance (12-Bit Mode)** | | | | | | | |
| AD30a | THD | Total Harmonic Distortion | — | — | -75 | dB | |
| AD31a | SINAD | Signal to Noise and Distortion | 68.5 | 69.5 | — | dB | |
| AD32a | SFDR | Spurious Free Dynamic Range | 80 | — | — | dB | |
| AD33a | FNYQ | Input Signal Bandwidth | — | — | 250 | kHz | |
| AD34a | ENOB | Effective Number of Bits | 11.09 | 11.3 | — | bits | |

**Note 1:** Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules: ADC, op amp/comparator and comparator voltage reference, will have degraded performance. Refer to Parameter BO10 in Table 33-12 for the minimum and maximum BOR values.

**2:** For all accuracy specifications, VINL = AVSS = VREFL = 0V and AVDD = VREFH = 3.6V.

**FIGURE 33-38: ADC1 CONVERSION (12-BIT MODE) TIMING CHARACTERISTICS (ASAM = 0, SSRC<2:0> = 000, SSRCG = 0)**




1 – Software sets AD1CON1. SAMP to start sampling.

2 – Sampling starts after discharge period. TSAMP is described in **"Analog-to-Digital Converter (ADC)"** (DS70621) of the *"dsPIC33/PIC24 Family Reference Manual"*.

3 – Software clears AD1CON1. SAMP to start conversion.

4 – Sampling ends, conversion sequence starts.

5 – Convert bit 11.

6 – Convert bit 10.

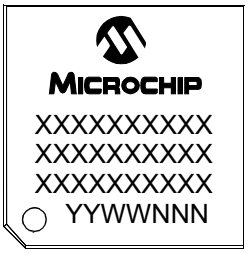
7 – Convert bit 1.

8 – Convert bit 0.

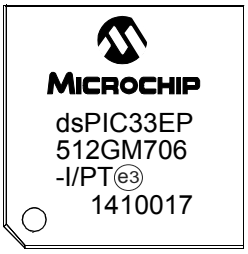
9 – One TAD for end of conversion.

### 35.1 Package Marking Information (Continued)

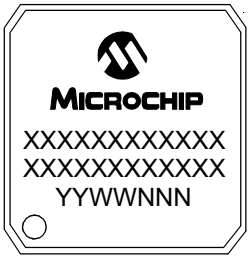
64-Lead TQFP (10x10x1 mm)




Example

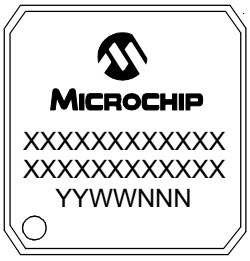



100-Lead TQFP (12x12x1 mm)



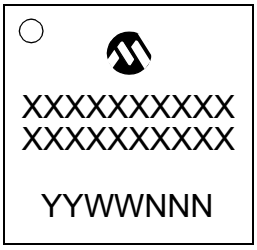

Example


100-Lead TQFP (14x14x1 mm)

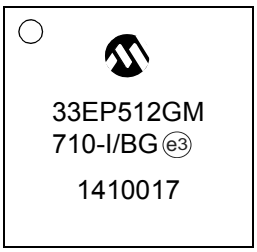



Example


121-Lead TFBGA (10x10x1.1 mm)




Example



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**NOTES:**