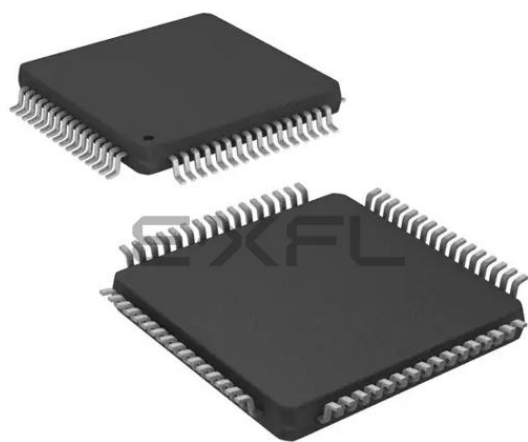




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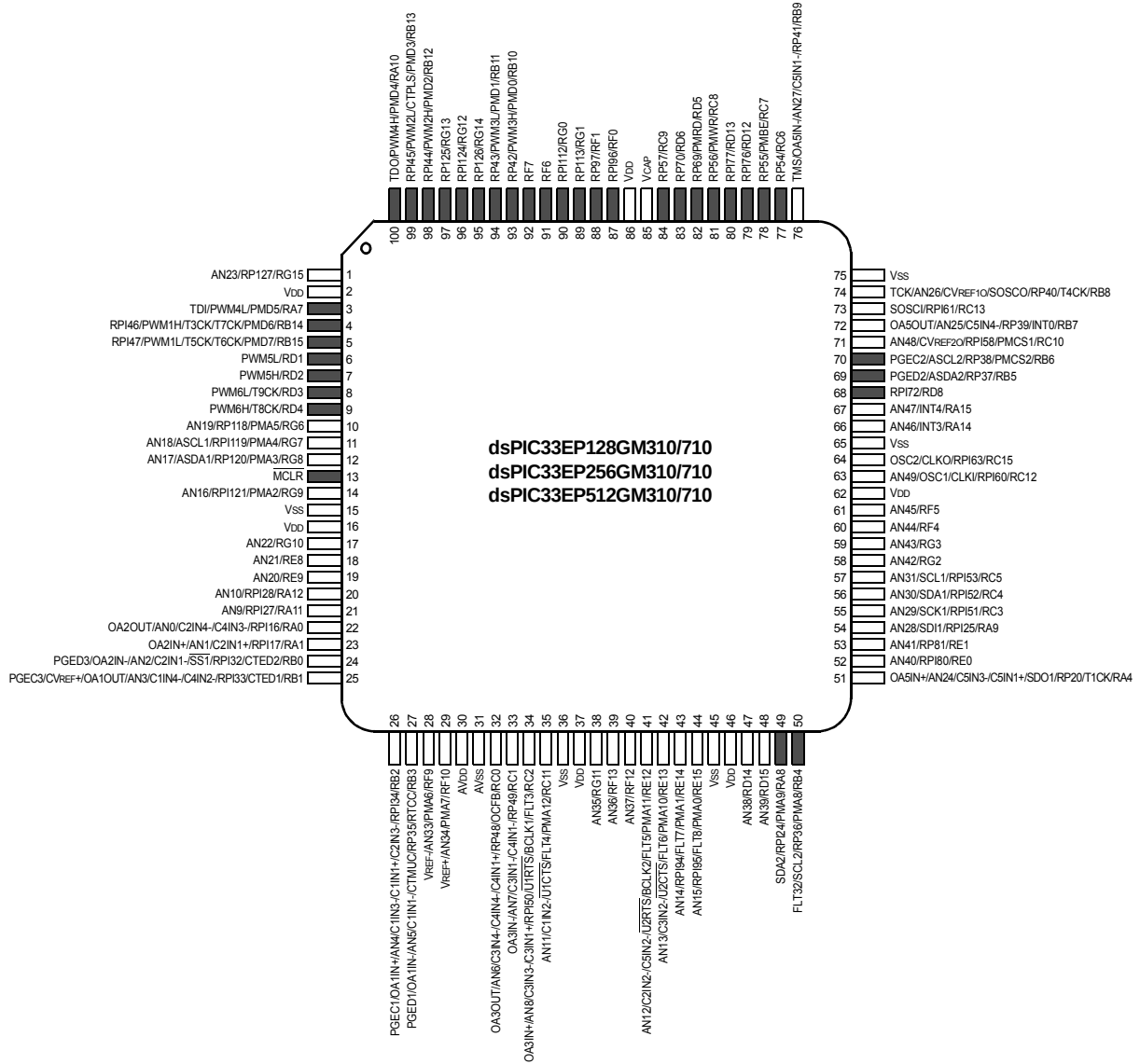
Details

Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	-
Connectivity	CANbus, I ² C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, Motor Control PWM, POR, PWM, WDT
Number of I/O	53
Program Memory Size	512KB (170K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	-
Data Converters	A/D 30x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	64-TQFP
Supplier Device Package	64-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep512gm706-h-pt

Pin Diagrams (Continued)

100-Pin TQFP^(1,2,3)

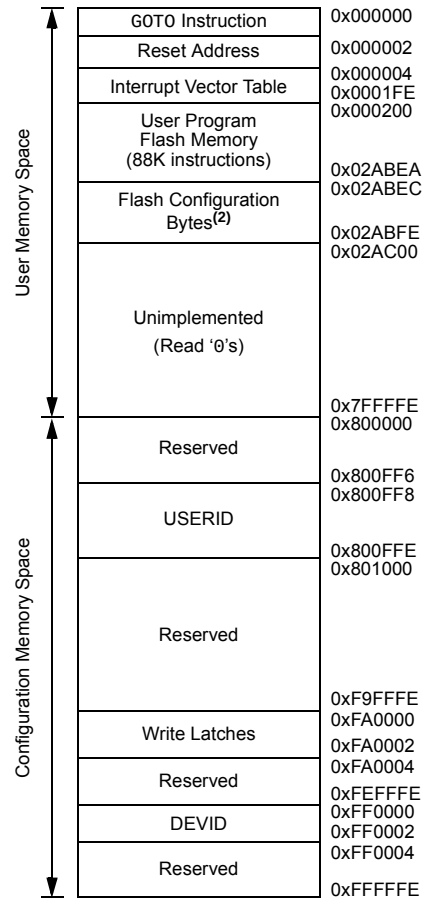
■ = Pins are up to 5V tolerant



- Note 1:** The RPN/RPIn pins can be used by any remappable peripheral with some limitation. See **Section 11.4 “Peripheral Pin Select (PPS)”** for available peripherals and for information on limitations.
- Note 2:** Every I/O port pin (RAX-RGx) can be used as a Change Notification pin (CNAX-CNGx). See **Section 11.0 “I/O Ports”** for more information.
- Note 3:** This pin is not available as an input when OPMODE (CMxCON<10>) = 1.

dsPIC33EPXXXGM3XX/6XX/7XX

FIGURE 4-2: PROGRAM MEMORY MAP FOR dsPIC33EP256GM3XX/6XX/7XX DEVICES⁽¹⁾



Note 1: Memory areas are not shown to scale.

Note 2: On Reset, these bits are automatically copied into the device Configuration Shadow registers.

TABLE 4-28: CAN2 REGISTER MAP WHEN WIN (C1CTRL<0>) = 1 FOR dsPIC33EPXXXGM60X/7XX DEVICES⁽¹⁾

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
	0500-051E	See definition when WIN = x																
C2BUFNT1	0520	F3BP3	F3BP2	F3BP1	F3BP0	F2BP3	F2BP2	F2BP1	F2BP0	F1BP3	F1BP2	F1BP1	F1BP0	F0BP3	F0BP2	F0BP1	F0BP0	0000
C2BUFNT2	0522	F7BP3	F7BP2	F7BP1	F7BP0	F6BP3	F6BP2	F6BP1	F6BP0	F5BP3	F5BP2	F5BP1	F5BP0	F4BP3	F4BP2	F4BP1	F4BP0	0000
C2BUFNT3	0524	F11BP3	F11BP2	F11BP1	F11BP0	F10BP3	F10BP2	F10BP1	F10BP0	F9BP3	F9BP2	F9BP1	F9BP0	F8BP3	F8BP2	F8BP1	F8BP0	0000
C2BUFNT4	0526	F15BP3	F15BP2	F15BP1	F15BP0	F14BP3	F14BP2	F14BP1	F14BP0	F13BP3	F13BP2	F13BP1	F13BP0	F12BP3	F12BP2	F12BP1	F12BP0	0000
C2RXM0SID	0530	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	MIDE	—	EID17	EID16	xxxx
C2RXM0EID	0532	EID<15:0>																xxxx
C2RXM1SID	0534	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	MIDE	—	EID17	EID16	xxxx
C2RXM1EID	0536	EID<15:0>																xxxx
C2RXM2SID	0538	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	MIDE	—	EID17	EID16	xxxx
C2RXM2EID	053A	EID<15:0>																xxxx
C2RXF0SID	0540	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	MIDE	—	EID17	EID16	xxxx
C2RXF0EID	0542	EID<15:0>																xxxx
C2RXF1SID	0544	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	MIDE	—	EID17	EID16	xxxx
C2RXF1EID	0546	EID<15:0>																xxxx
C2RXF2SID	0548	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	MIDE	—	EID17	EID16	xxxx
C2RXF2EID	054A	EID<15:0>																xxxx
C2RXF3SID	054C	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	MIDE	—	EID17	EID16	xxxx
C2RXF3EID	054E	EID<15:0>																xxxx
C2RXF4SID	0550	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	MIDE	—	EID17	EID16	xxxx
C2RXF4EID	0552	EID<15:0>																xxxx
C2RXF5SID	0554	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	MIDE	—	EID17	EID16	xxxx
C2RXF5EID	0556	EID<15:0>																xxxx
C2RXF6SID	0558	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	MIDE	—	EID17	EID16	xxxx
C2RXF6EID	055A	EID<15:0>																xxxx
C2RXF7SID	055C	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	MIDE	—	EID17	EID16	xxxx
C2RXF7EID	055E	EID<15:0>																xxxx
C2RXF8SID	0560	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	MIDE	—	EID17	EID16	xxxx
C2RXF8EID	0562	EID<15:0>																xxxx
C2RXF9SID	0564	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	MIDE	—	EID17	EID16	xxxx
C2RXF9EID	0566	EID<15:0>																xxxx
C2RXF10SID	0568	SID10	SID9	SID8	SID7	SID6	SID5	SID4	SID3	SID2	SID1	SID0	—	MIDE	—	EID17	EID16	xxxx
C2RXF10EID	056A	EID<15:0>																xxxx

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

Note 1: These registers are not present on dsPIC33EPXXXGM3XX devices.

FIGURE 4-15: BIT-REVERSED ADDRESSING EXAMPLE

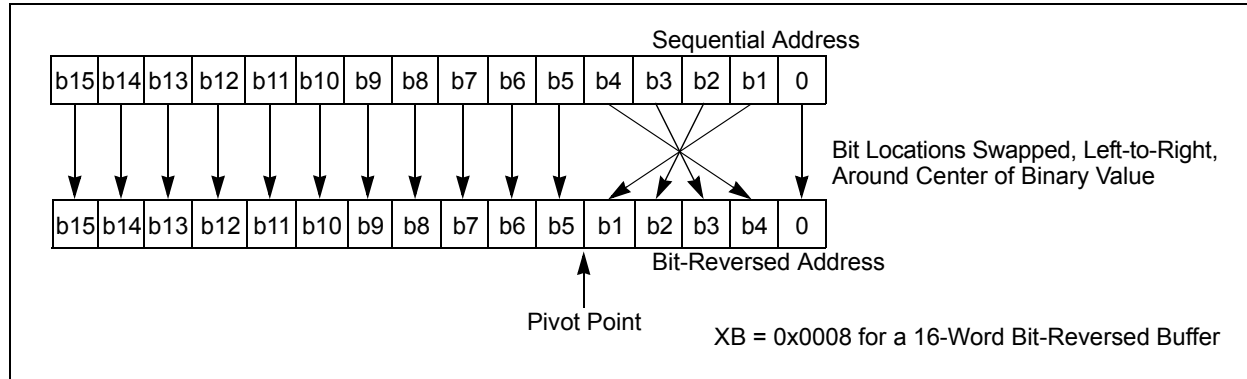


TABLE 4-67: BIT-REVERSED ADDRESSING SEQUENCE (16-ENTRY)

Normal Address					Bit-Reversed Address				
A3	A2	A1	A0	Decimal	A3	A2	A1	A0	Decimal
0	0	0	0	0	0	0	0	0	0
0	0	0	1	1	1	0	0	0	8
0	0	1	0	2	0	1	0	0	4
0	0	1	1	3	1	1	0	0	12
0	1	0	0	4	0	0	1	0	2
0	1	0	1	5	1	0	1	0	10
0	1	1	0	6	0	1	1	0	6
0	1	1	1	7	1	1	1	0	14
1	0	0	0	8	0	0	0	1	1
1	0	0	1	9	1	0	0	1	9
1	0	1	0	10	0	1	0	1	5
1	0	1	1	11	1	1	0	1	13
1	1	0	0	12	0	0	1	1	3
1	1	0	1	13	1	0	1	1	11
1	1	1	0	14	0	1	1	1	7
1	1	1	1	15	1	1	1	1	15

REGISTER 7-1: SR: CPU STATUS REGISTER⁽¹⁾

R/W-0	R/W-0	R/W-0	R/W-0	R/C-0	R/C-0	R-0	R/W-0
OA	OB	SA	SB	OAB	SAB	DA	DC
bit 15						bit 8	

R/W-0 ⁽³⁾	R/W-0 ⁽³⁾	R/W-0 ⁽³⁾	R-0	R/W-0	R/W-0	R/W-0	R/W-0
IPL2 ⁽²⁾	IPL1 ⁽²⁾	IPL0 ⁽²⁾	RA	N	OV	Z	C
bit 7						bit 0	

Legend:	C = Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-5 **IPL<2:0>:** CPU Interrupt Priority Level Status bits^(2,3)

111 = CPU Interrupt Priority Level is 7 (15); user interrupts are disabled
110 = CPU Interrupt Priority Level is 6 (14)
101 = CPU Interrupt Priority Level is 5 (13)
100 = CPU Interrupt Priority Level is 4 (12)
011 = CPU Interrupt Priority Level is 3 (11)
010 = CPU Interrupt Priority Level is 2 (10)
001 = CPU Interrupt Priority Level is 1 (9)
000 = CPU Interrupt Priority Level is 0 (8)

- Note 1:** For complete register details, see Register 3-1.
- 2:** The IPL<2:0> bits are concatenated with the IPL<3> bit (CORCON<3>) to form the CPU Interrupt Priority Level. The value in parentheses indicates the IPL if IPL<3> = 1. User interrupts are disabled when IPL<3> = 1.
- 3:** The IPL<2:0> Status bits are read-only when the NSTDIS bit (INTCON1<15>) = 1.

REGISTER 8-12: DMARQC: DMA REQUEST COLLISION STATUS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	R-0	R-0	R-0	R-0
—	—	—	—	RQCOL3	RQCOL2	RQCOL1	RQCOL0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-4 **Unimplemented:** Read as '0'

bit 3 **RQCOL3:** Channel 3 Transfer Request Collision Flag bit

1 = User FORCE and interrupt-based request collision are detected

0 = No request collision is detected

bit 2 **RQCOL2:** Channel 2 Transfer Request Collision Flag bit

1 = User FORCE and interrupt-based request collision are detected

0 = No request collision is detected

bit 1 **RQCOL1:** Channel 1 Transfer Request Collision Flag bit

1 = User FORCE and interrupt-based request collision are detected

0 = No request collision is detected

bit 0 **RQCOL0:** Channel 0 Transfer Request Collision Flag bit

1 = User FORCE and interrupt-based request collision are detected

0 = No request collision is detected

NOTES:

REGISTER 10-3: PMD3: PERIPHERAL MODULE DISABLE CONTROL REGISTER 3

R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
T9MD	T8MD	T7MD	T6MD	—	CMPMD	RTCCMD ⁽¹⁾	PMPMD
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CRCMD	DACMD	QE12MD	PWM2MD	U3MD	I2C3MD	I2C2MD	ADC2MD
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15 **T9MD:** Timer9 Module Disable bit
1 = Timer9 module is disabled
0 = Timer9 module is enabled
- bit 13 **T8MD:** Timer8 Module Disable bit
1 = Timer8 module is disabled
0 = Timer8 module is enabled
- bit 14 **T7MD:** Timer7 Module Disable bit
1 = Timer7 module is disabled
0 = Timer7 module is enabled
- bit 12 **T6MD:** Timer6 Module Disable bit
1 = Timer6 module is disabled
0 = Timer6 module is enabled
- bit 11 **Unimplemented:** Read as '0'
- bit 10 **CMPMD:** Comparator Module Disable bit
1 = Comparator module is disabled
0 = Comparator module is enabled
- bit 9 **RTCCMD:** RTCC Module Disable bit⁽¹⁾
1 = RTCC module is disabled
0 = RTCC module is enabled
- bit 8 **PMPMD:** PMP Module Disable bit
1 = PMP module is disabled
0 = PMP module is enabled
- bit 7 **CRCMD:** CRC Module Disable bit
1 = CRC module is disabled
0 = CRC module is enabled
- bit 6 **DACMD:** DAC Module Disable bit
1 = DAC module is disabled
0 = DAC module is enabled
- bit 5 **QE12MD:** QE12 Module Disable bit
1 = QE12 module is disabled
0 = QE12 module is enabled
- bit 4 **PWM2MD:** PWM2 Module Disable bit
1 = PWM2 module is disabled
0 = PWM2 module is enabled

Note 1: The RTCCMD bit is not available on 44-pin devices.

REGISTER 10-3: PMD3: PERIPHERAL MODULE DISABLE CONTROL REGISTER 3

bit 3	U3MD: UART3 Module Disable bit 1 = UART3 module is disabled 0 = UART3 module is enabled
bit 2	I2C3MD: I2C3 Module Disable bit 1 = I2C3 module is disabled 0 = I2C3 module is enabled
bit 1	I2C2MD: I2C2 Module Disable bit 1 = I2C2 module is disabled 0 = I2C2 module is enabled
bit 0	ADC2MD: ADC2 Module Disable bit 1 = ADC2 module is disabled 0 = ADC2 module is enabled

Note 1: The RTCCMD bit is not available on 44-pin devices.

REGISTER 11-24: RPINR30: PERIPHERAL PIN SELECT INPUT REGISTER 30

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	SS3R<6:0>						
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-7

Unimplemented: Read as '0'

bit 6-0

SS3R<6:0>: Assign SPI3 Slave Select Input ($\overline{SS3}$) to the Corresponding RPn/RPIn Pin bits (see Table 11-2 for input pin selection numbers)

1111111 = Input tied to RP124

•

•

•

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

REGISTER 16-19: IOCONx: PWMx I/O CONTROL REGISTER⁽²⁾ (CONTINUED)

- bit 1 **SWAP:** SWAP PWMxH and PWMxL Pins bit
 1 = PWMxH output signal is connected to the PWMxL pins; PWMxL output signal is connected to the PWMxH pins
 0 = PWMxH and PWMxL pins are mapped to their respective pins
- bit 0 **OSYNC:** Output Override Synchronization bit
 1 = Output overrides via the OVRDAT<1:0> bits are synchronized to the PWM time base
 0 = Output overrides via the OVDDAT<1:0> bits occur on the next CPU clock boundary

Note 1: These bits should not be changed after the PWMx module is enabled (PTEN = 1).

2: If the PWMLOCK Configuration bit (FOSCSEL<6>) is a '1', the IOCONx register can only be written after the unlock sequence has been executed.

REGISTER 16-20: TRIGx: PWMx PRIMARY TRIGGER COMPARE VALUE REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TRGCMP<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TRGCMP<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **TRGCMP<15:0>:** Trigger Control Value bits

When the primary PWMx functions in the local time base, this register contains the compare values that can trigger the ADCx module.

REGISTER 16-21: FCLCONx: PWMx FAULT CURRENT-LIMIT CONTROL REGISTER (CONTINUED)

bit 7-3	FLTSRC<4:0> : Fault Control Signal Source Select for PWMx Generator # bits 11111 = Fault 32 (default) 11110 = Reserved • • • 01100 = Op Amp/Comparator 5 01011 = Comparator 4 01010 = Op Amp/Comparator 3 01001 = Op Amp/Comparator 2 01000 = Op Amp/Comparator 1 00111 = Fault 8 00110 = Fault 7 00101 = Fault 6 00100 = Fault 5 00011 = Fault 4 00010 = Fault 3 00001 = Fault 2 00000 = Fault 1
bit 2	FLTPOL : Fault Polarity for PWMx Generator # bit ⁽¹⁾ 1 = The selected Fault source is active-low 0 = The selected Fault source is active-high
bit 1-0	FLTMOD<1:0> : Fault Mode for PWMx Generator # bits 11 = Fault input is disabled 10 = Reserved 01 = The selected Fault source forces the PWMxH, PWMxL pins to FLTDATx values (cycle) 00 = The selected Fault source forces the PWMxH, PWMxL pins to FLTDATx values (latched condition)

Note 1: These bits should be changed only when PTEN = 0. Changing the clock selection during operation will yield unpredictable results.

REGISTER 16-23: LEBDLYx: LEADING-EDGE BLANKING DELAY REGISTER x

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	LEB<11:8>			
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
LEB<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-12 **Unimplemented:** Read as '0'

bit 11-0 **LEB<11:0>:** Leading-Edge Blanking Delay for Current-Limit and Fault Inputs bits

18.0 SERIAL PERIPHERAL INTERFACE (SPI)

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGM3XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the “dsPIC33/PIC24 Family Reference Manual”, “Serial Peripheral Interface (SPI)” (DS70005185), which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The SPI module is a synchronous serial interface, useful for communicating with other peripheral or microcontroller devices. These peripheral devices can be serial EEPROMs, shift registers, display drivers, A/D Converters, etc. The SPI module is compatible with the Motorola® SPI and SIOP interfaces.

The dsPIC33EPXXXGM3XX/6XX/7XX device family offers three SPI modules on a single device. These modules, which are designated as SPI1, SPI2 and SPI3, are functionally identical. Each SPI module includes an eight-word FIFO buffer and allows DMA bus connections. When using the SPI module with DMA, FIFO operation can be disabled.

Note: In this section, the SPI modules are referred to together as SPIx, or separately as SPI1, SPI2 and SPI3. Special Function Registers follow a similar notation. For example, SPIxCON refers to the control register for the SPI1, SPI2 and SPI3 modules.

The SPI1 module uses dedicated pins which allow for a higher speed when using SPI1. The SPI2 and SPI3 modules take advantage of the Peripheral Pin Select (PPS) feature to allow for greater flexibility in pin configuration of these modules, but results in a lower maximum speed. See **Section 33.0 “Electrical Characteristics”** for more information.

The SPIx serial interface consists of four pins, as follows:

- SDIx: Serial Data Input
- SDOx: Serial Data Output
- SCKx: Shift Clock Input or Output
- $\overline{\text{SSx}}$ /FSYNCx: Active-Low Slave Select or Frame Synchronization I/O Pulse

The SPIx module can be configured to operate with two, three or four pins. In 3-pin mode, $\overline{\text{SSx}}$ is not used. In 2-pin mode, neither SDOx nor $\overline{\text{SSx}}$ is used.

Figure 18-1 illustrates the block diagram of the SPIx module in Standard and Enhanced modes.

REGISTER 18-1: SPIxSTAT: SPIx STATUS AND CONTROL REGISTER (CONTINUED)

- bit 1 **SPITBF:** SPIx Transmit Buffer Full Status bit
1 = Transmit has not yet started, SPIxTXB is full
0 = Transmit has started, SPIxTXB is empty
Standard Buffer Mode:
Automatically set in hardware when the core writes to the SPIxBUF location, loading SPIxTXB. Automatically cleared in hardware when the SPIx module transfers data from SPIxTXB to SPIxSR.
Enhanced Buffer Mode:
Automatically set in hardware when the CPU writes to the SPIxBUF location, loading the last available buffer location. Automatically cleared in hardware when a buffer location is available for a CPU write operation.
- bit 0 **SPIRBF:** SPIx Receive Buffer Full Status bit
1 = Receive is complete, SPIxRXB is full
0 = Receive is incomplete, SPIxRXB is empty
Standard Buffer Mode:
Automatically set in hardware when SPIx transfers data from SPIxSR to SPIxRXB. Automatically cleared in hardware when the core reads the SPIxBUF location, reading SPIxRXB.
Enhanced Buffer Mode:
Automatically set in hardware when SPIx transfers data from SPIxSR to the buffer, filling the last unread buffer location. Automatically cleared in hardware when a buffer location is available for a transfer from SPIxSR.

21.0 CONTROLLER AREA NETWORK (CAN) MODULE (dsPIC33EPXXXGM6XX/7XX DEVICES ONLY)

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGM3XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *“dsPIC33/PIC24 Family Reference Manual”*, **“Enhanced Controller Area Network (ECAN™)”** (DS70353), which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

21.1 Overview

The Controller Area Network (CAN) module is a serial interface, useful for communicating with other CAN modules or microcontroller devices. This interface/protocol was designed to allow communications within noisy environments. The dsPIC33EPXXXGM6XX/7XX devices contain two CAN modules.

The CAN module is a communication controller, implementing the CAN 2.0 A/B protocol, as defined in the BOSCH CAN specification. The module supports CAN 1.2, CAN 2.0A, CAN 2.0B Passive and CAN 2.0B Active versions of the protocol. The module implementation is a full CAN system. The CAN specification is not covered within this data sheet. The reader can refer to the BOSCH CAN specification for further details.

The CAN module features are as follows:

- Implementation of the CAN protocol, CAN 1.2, CAN 2.0A and CAN 2.0B
- Standard and Extended Data Frames
- 0-8 Bytes of Data Length
- Programmable Bit Rate, up to 1 Mbit/sec
- Automatic Response to Remote Transmission Requests
- Up to 8 Transmit Buffers with Application Specified Prioritization and Abort Capability (each buffer can contain up to 8 bytes of data)
- Up to 32 Receive Buffers (each buffer can contain up to 8 bytes of data)
- Up to 16 Full (Standard/Extended Identifier) Acceptance Filters
- Three Full Acceptance Filter Masks
- DeviceNet™ Addressing Support
- Programmable Wake-up Functionality with Integrated Low-Pass Filter
- Programmable Loopback mode supports Self-Test Operation
- Signaling via Interrupt Capabilities for all CAN Receiver and Transmitter Error States
- Programmable Clock Source
- Programmable Link to Input Capture 2 (IC2) module for Timestamping and Network Synchronization
- Low-Power Sleep and Idle modes

The CAN bus module consists of a protocol engine and message buffering/control. The CAN protocol engine handles all functions for receiving and transmitting messages on the CAN bus. Messages are transmitted by first loading the appropriate data registers. Status and errors can be checked by reading the appropriate registers. Any message detected on the CAN bus is checked for errors and then matched against filters to see if it should be received and stored in one of the receive registers.

REGISTER 23-1: ADxCON1: ADCx CONTROL REGISTER 1 (CONTINUED)

bit 7-5	SSRC<2:0>: Sample Clock Source Select bits If SSRCG = 1: 111 = Reserved 110 = PTGO15 primary trigger compare ends sampling and starts conversion⁽¹⁾ 101 = PTGO14 primary trigger compare ends sampling and starts conversion⁽¹⁾ 100 = PTGO13 primary trigger compare ends sampling and starts conversion⁽¹⁾ 011 = PTGO12 primary trigger compare ends sampling and starts conversion⁽¹⁾ 010 = PWM Generator 3 primary trigger compare ends sampling and starts conversion 001 = PWM Generator 2 primary trigger compare ends sampling and starts conversion 000 = PWM Generator 1 primary trigger compare ends sampling and starts conversion If SSRCG = 0: 111 = Internal counter ends sampling and starts conversion (auto-convert) 110 = CTMU ends sampling and starts conversion 101 = PWM secondary Special Event Trigger ends sampling and starts conversion 100 = Timer5 compare ends sampling and starts conversion 011 = PWM primary Special Event Trigger ends sampling and starts conversion 010 = Timer3 compare ends sampling and starts conversion 001 = Active transition on the INT0 pin ends sampling and starts conversion 000 = Clearing the Sample bit (SAMP) ends sampling and starts conversion (Manual mode)
bit 4	SSRCG: Sample Trigger Source Group bit See SSRC<2:0> for details.
bit 3	SIMSAM: Simultaneous Sample Select bit (only applicable when CHPS<1:0> = 01 or 1x) In 12-Bit Mode (AD12B = 1), SIMSAM is Unimplemented and is Read as '0': 1 = Samples CH0, CH1, CH2, CH3 simultaneously (when CHPS<1:0> = 1x), or samples CH0 and CH1 simultaneously (when CHPS<1:0> = 01) 0 = Samples multiple channels individually in sequence
bit 2	ASAM: ADCx Sample Auto-Start bit 1 = Sampling begins immediately after last conversion; SAMP bit is auto-set 0 = Sampling begins when SAMP bit is set
bit 1	SAMP: ADCx Sample Enable bit 1 = ADCx Sample-and-Hold amplifiers are sampling 0 = ADCx Sample-and-Hold amplifiers are holding If ASAM = 0, software can write '1' to begin sampling. Automatically set by hardware if ASAM = 1. If SSRC<2:0> = 000, software can write '0' to end sampling and start conversion. If SSRC<2:0> ≠ 000, automatically cleared by hardware to end sampling and start conversion.
bit 0	DONE: ADCx Conversion Status bit⁽²⁾ 1 = ADCx conversion cycle is completed. 0 = ADCx conversion has not started or is in progress Automatically set by hardware when A/D conversion is complete. Software can write '0' to clear DONE status (software not allowed to write '1'). Clearing this bit does NOT affect any operation in progress. Automatically cleared by hardware at the start of a new conversion.

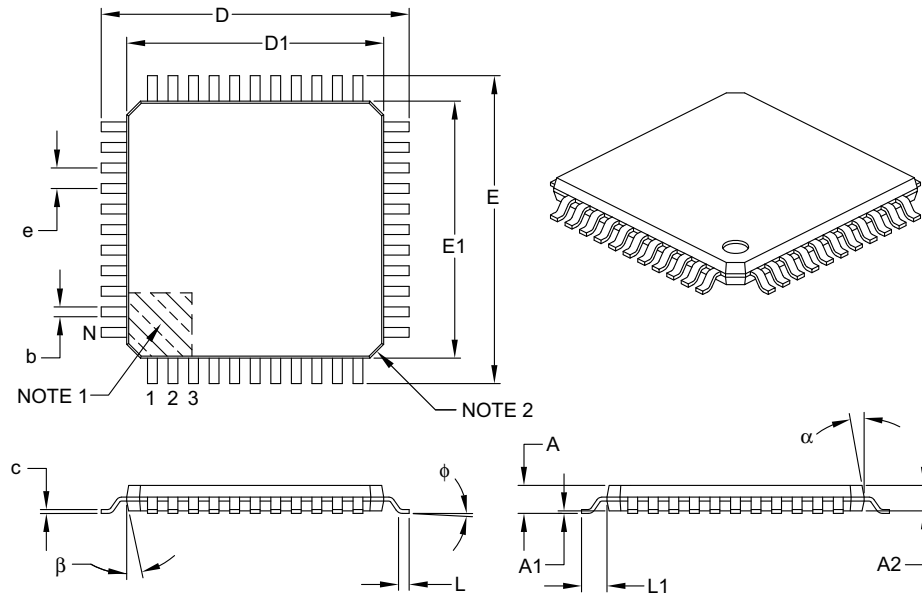
Note 1: See Section 25.0 "Peripheral Trigger Generator (PTG) Module" for information on this selection.

2: Do not clear the **DONE** bit in software if ADCx Sample Auto-Start bit is enabled (**ASAM** = 1).

35.2 Package Details

44-Lead Plastic Thin Quad Flatpack (PT) – 10x10x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N	44		
Lead Pitch	e	0.80 BSC		
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	–	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1	1.00 REF		
Foot Angle	φ	0°	3.5°	7°
Overall Width	E	12.00 BSC		
Overall Length	D	12.00 BSC		
Molded Package Width	E1	10.00 BSC		
Molded Package Length	D1	10.00 BSC		
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.30	0.37	0.45
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Chamfers at corners are optional; size may vary.
- Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-076B

dsPIC33EPXXXGM3XX/6XX/7XX

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PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

dsPIC 33 EP 512 GM7 10 T - I / PT XXX Microchip Trademark _____ Architecture _____ Core Family _____ Program Memory Size (Kbytes) _____ Product Group _____ Pin Count _____ Tape and Reel Flag (if applicable) _____ Temperature Range _____ Package _____ Pattern _____		Example: dsPIC33EP512GM710-I/PT: dsPIC33, Enhanced Performance, 512-Kbyte program memory, 100-pin, Industrial temperature, TQFP package.
Architecture: 33 = 16-Bit Digital Signal Controller Family: EP = Enhanced Performance Product Group: GM7 = General Purpose plus Motor Control Family Pin Count: 04 = 44-pin 06 = 64-pin 10 = 100/124-pin Temperature Range: I = -40°C to +85°C (Industrial) E = -40°C to +125°C (Extended) Package: BG = Plastic Thin Profile Ball Grid Array - (121-pin) 10x10 mm body (TFBGA) ML = Plastic Quad, No Lead Package - (44-pin) 8x8 mm body (QFN) MR = Plastic Quad, No Lead Package - (64-pin) 9x9 mm body (QFN) PT = Plastic Thin Quad Flatpack - (44-pin) 10x10 mm body (TQFP) PT = Plastic Thin Quad Flatpack - (64-pin) 10x10 mm body (TQFP) PT = Thin Quad Flatpack - (100-pin) 12x12x1 mm body (TQFP) PF = Thin Quad Flatpack - (100-pin) 14x14x1 mm body (TQFP)		