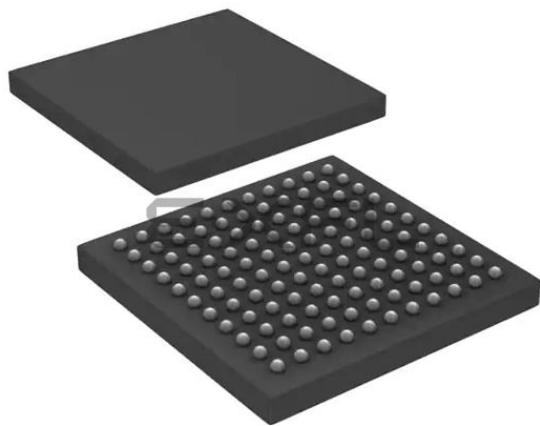




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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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Details

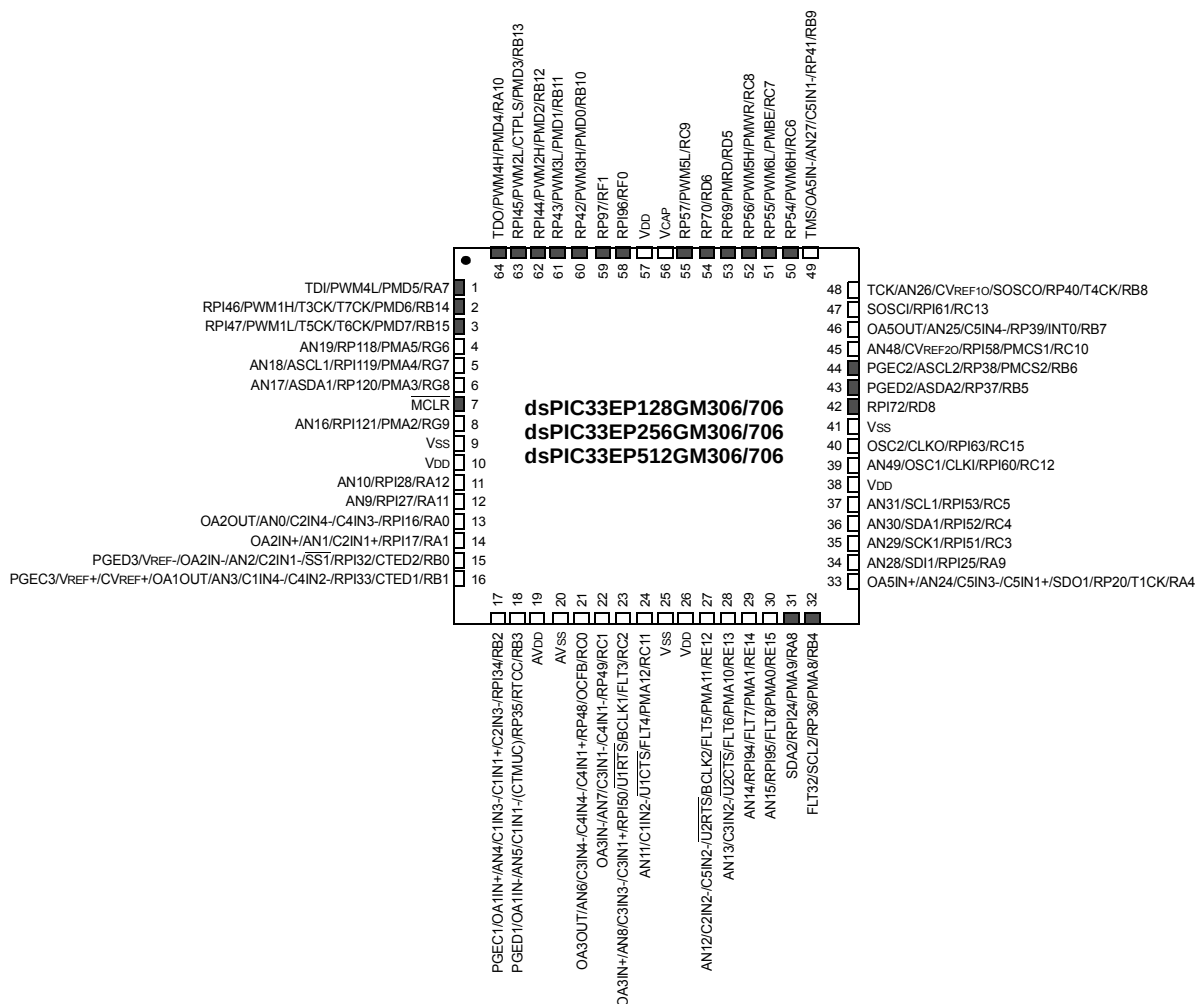
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	60 MIPS
Connectivity	CANbus, I ² C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, Motor Control PWM, POR, PWM, WDT
Number of I/O	85
Program Memory Size	512KB (170K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 49x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	121-TFBGA
Supplier Device Package	121-TFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep512gm710-e-bg

dsPIC33EPXXXGM3XX/6XX/7XX

Pin Diagrams (Continued)

64-Pin QFN^(1,2,3,4)

■ = Pins are up to 5V tolerant



- Note 1:** The RPN/RPIN pins can be used by any remappable peripheral with some limitation. See **Section 11.4 “Peripheral Pin Select (PPS)”** for available peripherals and for information on limitations.
- Note 2:** Every I/O port pin (RAX-RGX) can be used as a Change Notification pin (CNAX-CNGX). See **Section 11.0 “I/O Ports”** for more information.
- Note 3:** This pin is not available as an input when OPMODE (CMxCON<10>) = 1.
- Note 4:** The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to Vss externally.

TABLE 1-1: PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Type	Buffer Type	PPS	Description
U1CTS	I	ST	Yes	UART1 Clear-to-Send.
U1RTS	O	—	Yes	UART1 Ready-to-Send.
U1RX	I	ST	Yes	UART1 receive.
U1TX	O	—	Yes	UART1 transmit.
U2CTS	I	ST	Yes	UART2 Clear-to-Send.
U2RTS	O	—	Yes	UART2 Ready-to-Send.
U2RX	I	ST	Yes	UART2 receive.
U2TX	O	—	Yes	UART2 transmit.
U3CTS	I	ST	Yes	UART3 Clear-to-Send.
U3RTS	O	—	Yes	UART3 Ready-to-Send.
U3RX	I	ST	Yes	UART3 receive.
U3TX	O	—	Yes	UART3 transmit.
U4CTS	I	ST	Yes	UART4 Clear-to-Send.
U4RTS	O	—	Yes	UART4 Ready-to-Send.
U4RX	I	ST	Yes	UART4 receive.
U4TX	O	—	Yes	UART4 transmit.
SCK1	I/O	ST	No	Synchronous serial clock input/output for SPI1.
SDI1	I	ST	No	SPI1 data in.
SDO1	O	—	No	SPI1 data out.
SS1	I/O	ST	No	SPI1 slave synchronization or frame pulse I/O.
SCK2	I/O	ST	Yes	Synchronous serial clock input/output for SPI2.
SDI2	I	ST	Yes	SPI2 data in.
SDO2	O	—	Yes	SPI2 data out.
SS2	I/O	ST	Yes	SPI2 slave synchronization or frame pulse I/O.
SCK3	I/O	ST	Yes	Synchronous serial clock input/output for SPI3.
SDI3	I	ST	Yes	SPI3 data in.
SDO3	O	—	Yes	SPI3 data out.
SS3	I/O	ST	Yes	SPI3 slave synchronization or frame pulse I/O.
SCL1	I/O	ST	No	Synchronous serial clock input/output for I2C1.
SDA1	I/O	ST	No	Synchronous serial data input/output for I2C1.
ASCL1	I/O	ST	No	Alternate synchronous serial clock input/output for I2C1.
ASDA1	I/O	ST	No	Alternate synchronous serial data input/output for I2C1.
SCL2	I/O	ST	No	Synchronous serial clock input/output for I2C2.
SDA2	I/O	ST	No	Synchronous serial data input/output for I2C2.
ASCL2	I/O	ST	No	Alternate synchronous serial clock input/output for I2C2.
ASDA2	I/O	ST	No	Alternate synchronous serial data input/output for I2C2.
TMS	I	ST	No	JTAG Test mode select pin.
TCK	I	ST	No	JTAG test clock input pin.
TDI	I	ST	No	JTAG test data input pin.
TDO	O	—	No	JTAG test data output pin.

Legend: CMOS = CMOS compatible input or output Analog = Analog input P = Power
ST = Schmitt Trigger input with CMOS levels O = Output I = Input
PPS = Peripheral Pin Select TTL = TTL input buffer

- Note 1:** This pin is not available on all devices. For more information, see the “Pin Diagrams” section for pin availability.
- 2:** AVDD must be connected at all times.

dsPIC33EPXXXGM3XX/6XX/7XX

TABLE 7-1: INTERRUPT VECTOR DETAILS (CONTINUED)

Interrupt Source	Vector #	IRQ #	IVT Address	Interrupt Bit Location		
				Flag	Enable	Priority
OC5 – Output Compare 5	49	41	0x000066	IFS2<9>	IEC2<9>	IPC10<6:4>
OC6 – Output Compare 6	50	42	0x000068	IFS2<10>	IEC2<10>	IPC10<10:8>
OC7 – Output Compare 7	51	43	0x00006A	IFS2<11>	IEC2<11>	IPC10<14:12>
OC8 – Output Compare 8	52	44	0x00006C	IFS2<12>	IEC2<12>	IPC11<2:0>
PMP – Parallel Master Port ⁽²⁾	53	45	0x00006E	IFS2<13>	IEC2<13>	IPC11<6:4>
Reserved	54	46	0x000070	—	—	—
T6 – Timer6	55	47	0x000072	IFS2<15>	IEC2<15>	IPC11<14:12>
T7 – Timer7	56	48	0x000074	IFS3<0>	IEC3<0>	IPC12<2:0>
SI2C2 – I2C2 Slave Event	57	49	0x000076	IFS3<1>	IEC3<1>	IPC12<6:4>
MI2C2 – I2C2 Master Event	58	50	0x000078	IFS3<2>	IEC3<2>	IPC12<10:8>
T8 – Timer8	59	51	0x00007A	IFS3<3>	IEC3<3>	IPC12<14:12>
T9 – Timer9	60	52	0x00007C	IFS3<4>	IEC3<4>	IPC13<2:0>
INT3 – External Interrupt 3	61	53	0x00007E	IFS3<5>	IEC3<5>	IPC13<6:4>
INT4 – External Interrupt 4	62	54	0x000080	IFS3<6>	IEC3<6>	IPC13<10:8>
C2RX – CAN2 RX Data Ready ⁽¹⁾	63	55	0x000082	IFS3<7>	IEC3<7>	IPC13<14:12>
C2 – CAN2 Event ⁽¹⁾	64	56	0x000084	IFS3<8>	IEC3<8>	IPC14<2:0>
PSEM – PCPWM Primary Event	65	57	0x000086	IFS3<9>	IEC3<9>	IPC14<6:4>
QE11 – QE11 Position Counter Compare	66	58	0x000088	IFS3<10>	IEC3<10>	IPC14<10:8>
DCIE – DCI Fault Interrupt	67	59	0x00008A	IFS3<11>	IEC3<11>	IPC14<14:12>
DCI – DCI Transfer Done	68	60	0x00008C	IFS3<12>	IEC3<12>	IPC15<2:0>
Reserved	69	61	0x00008E	—	—	—
RTCC – Real-Time Clock and Calendar ⁽²⁾	70	62	0x000090	IFS3<14>	IEC3<14>	IPC15<10:8>
Reserved	71-72	63-64	0x000092-0x000094	—	—	—
U1E – UART1 Error Interrupt	73	65	0x000096	IFS4<1>	IEC4<1>	IPC16<6:4>
U2E – UART2 Error Interrupt	74	66	0x000098	IFS4<2>	IEC4<2>	IPC16<10:8>
CRC – CRC Generator Interrupt	75	67	0x00009A	IFS4<3>	IEC4<3>	IPC16<14:12>
Reserved	76-77	68-69	0x00009C-0x00009E	—	—	—
C1TX – CAN1 TX Data Request ⁽¹⁾	78	70	0x0000A0	IFS4<6>	IEC4<6>	IPC17<10:8>
C2TX – CAN2 TX Data Request ⁽¹⁾	79	71	0x0000A2	IFS4<7>	IEC4<7>	IPC17<14:12>
Reserved	80	72	0x0000A4	—	—	—
PSESM – PCPWM Secondary Event	81	73	0x0000A6	IFS4<9>	IEC4<9>	IPC18<6:4>
Reserved	82	74	0x0000A8	—	—	—
QE12 – QE12 Position Counter Compare	83	75	0x0000AA	IFS4<11>	IEC4<11>	IPC18<14:12>
Reserved	84	76	0x0000AC	—	—	—
CTMU – CTMU Interrupt	85	77	0x0000AE	IFS4<13>	IEC4<13>	IPC19<6:4>
Reserved	86-88	78-80	0x0000B0-0x0000B4	—	—	—
U3E – UART3 Error Interrupt	89	81	0x0000B6	IFS5<1>	IEC5<1>	IPC20<6:4>
U3RX – UART3 Receiver	90	82	0x0000B8	IFS5<2>	IEC5<2>	IPC20<10:8>
U3TX – UART3 Transmitter	91	83	0x0000BA	IFS5<3>	IEC5<3>	IPC20<14:12>
Reserved	92-94	84-86	0x0000BC-0x0000C0	—	—	—
U4E – UART4 Error Interrupt	95	87	0x0000C2	IFS5<7>	IEC5<7>	IPC21<14:12>
U4RX – UART4 Receiver	96	88	0x0000C4	IFS5<8>	IEC5<8>	IPC22<2:0>
U4TX – UART4 Transmitter	97	89	0x0000C6	IFS5<9>	IEC5<9>	IPC22<6:4>

Note 1: This interrupt source is available on dsPIC33EPXXXGM6XX/7XX devices only.

Note 2: This interrupt source is not available on 44-pin devices.

dsPIC33EPXXXGM3XX/6XX/7XX

REGISTER 8-3: DMAxSTAH: DMA CHANNEL x START ADDRESS REGISTER A (HIGH)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STA<23:16>							
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **STA<23:16>:** DMA Primary Start Address bits (source or destination)

REGISTER 8-4: DMAxSTAL: DMA CHANNEL x START ADDRESS REGISTER A (LOW)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STA<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STA<7:0>							
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **STA<15:0>:** DMA Primary Start Address bits (source or destination)

dsPIC33EPXXXGM3XX/6XX/7XX

REGISTER 9-5: REFOCON: REFERENCE OSCILLATOR CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ROON	—	ROSSLP	ROSEL	RODIV3 ⁽¹⁾	RODIV2 ⁽¹⁾	RODIV1 ⁽¹⁾	RODIV0 ⁽¹⁾
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15 **ROON:** Reference Oscillator Output Enable bit
 1 = Reference oscillator output is enabled on the REFCLK pin⁽²⁾
 0 = Reference oscillator output is disabled
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **ROSSLP:** Reference Oscillator Run in Sleep bit
 1 = Reference oscillator output continues to run in Sleep
 0 = Reference oscillator output is disabled in Sleep
- bit 12 **ROSEL:** Reference Oscillator Source Select bit
 1 = Oscillator crystal is used as the reference clock
 0 = System clock is used as the reference clock
- bit 11-8 **RODIV<3:0>:** Reference Oscillator Divider bits⁽¹⁾
 1111 = Reference clock divided by 32,768
 1110 = Reference clock divided by 16,384
 1101 = Reference clock divided by 8,192
 1100 = Reference clock divided by 4,096
 1011 = Reference clock divided by 2,048
 1010 = Reference clock divided by 1,024
 1001 = Reference clock divided by 512
 1000 = Reference clock divided by 256
 0111 = Reference clock divided by 128
 0110 = Reference clock divided by 64
 0101 = Reference clock divided by 32
 0100 = Reference clock divided by 16
 0011 = Reference clock divided by 8
 0010 = Reference clock divided by 4
 0001 = Reference clock divided by 2
 0000 = Reference clock
- bit 7-0 **Unimplemented:** Read as '0'

- Note 1:** The reference oscillator output must be disabled (ROON = 0) before writing to these bits.
Note 2: This pin is remappable. See **Section 11.4 “Peripheral Pin Select (PPS)”** for more information.

REGISTER 11-9: RPINR12: PERIPHERAL PIN SELECT INPUT REGISTER 12

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	FLT2R<6:0>						
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	FLT1R<6:0>						
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **FLT2R<6:0>:** Assign PWM Fault 2 (FLT2) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

1111100 = Input tied to RPI124

•

•

•

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **FLT1R<6:0>:** Assign PWM Fault 1 (FLT1) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)

1111100 = Input tied to RPI124

•

•

•

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

dsPIC33EPXXXGM3XX/6XX/7XX

REGISTER 11-10: RPINR14: PERIPHERAL PIN SELECT INPUT REGISTER 14

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	QEB1R<6:0>						
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	QEA1R<6:0>						
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **QEB1R<6:0>:** Assign QE11 Phase B (QEB1) to the Corresponding RPn Pin bits
(see Table 11-2 for input pin selection numbers)

1111100 = Input tied to RPI124

•
•
•

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **QEA1R<6:0>:** Assign QE11 Phase A (QEA1) to the Corresponding RPn Pin bits
(see Table 11-2 for input pin selection numbers)

1111100 = Input tied to RPI124

•
•
•

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

dsPIC33EPXXXGM3XX/6XX/7XX

REGISTER 11-27: RPINR39: PERIPHERAL PIN SELECT INPUT REGISTER 39

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	DTCMP3R<6:0>						
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	DTCMP2R<6:0>						
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14-8 **DTCMP3R<6:0>:** Assign PWM Dead-Time Compensation Input 3 to the Corresponding RPN Pin bits (see Table 11-2 for input pin selection numbers)

1111100 = Input tied to RPI124

•
•
•

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

bit 7 **Unimplemented:** Read as '0'

bit 6-0 **DTCMP2R<6:0>:** Assign PWM Dead-Time Compensation Input 2 to the Corresponding RPN Pin bits (see Table 11-2 for input pin selection numbers)

1111100 = Input tied to RPI124

•
•
•

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

REGISTER 11-30: RPOR0: PERIPHERAL PIN SELECT OUTPUT REGISTER 0

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP35R<5:0>					
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP20R<5:0>					
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

- bit 15-14 **Unimplemented:** Read as '0'
- bit 13-8 **RP35R<5:0>:** Peripheral Output Function is Assigned to RP35 Output Pin bits
(see Table 11-3 for peripheral function numbers)
- bit 7-6 **Unimplemented:** Read as '0'
- bit 5-0 **RP20R<5:0>:** Peripheral Output Function is Assigned to RP20 Output Pin bits
(see Table 11-3 for peripheral function numbers)

REGISTER 11-31: RPOR1: PERIPHERAL PIN SELECT OUTPUT REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP37R<5:0>					
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RP36R<5:0>					
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

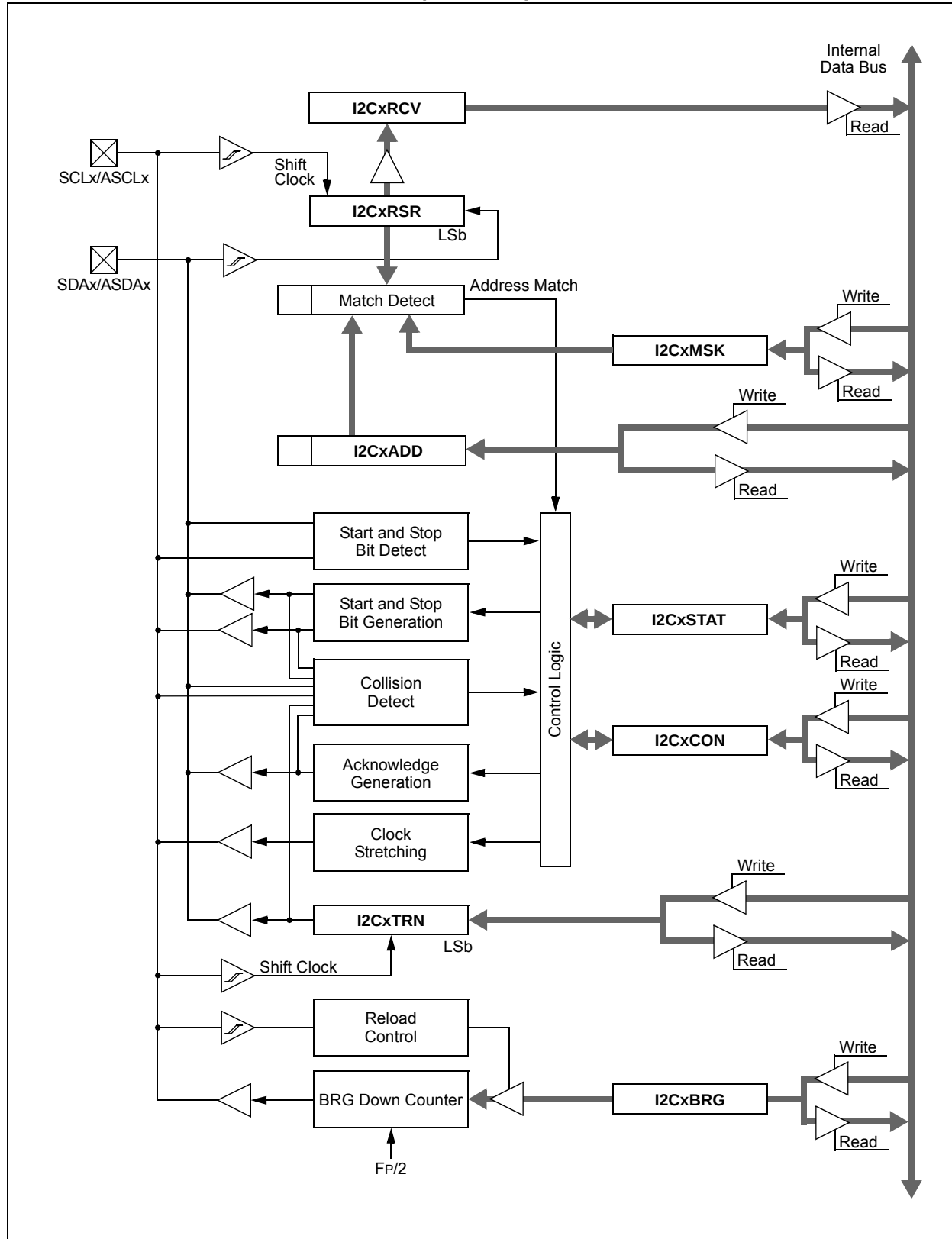
- bit 15-14 **Unimplemented:** Read as '0'
- bit 13-8 **RP37R<5:0>:** Peripheral Output Function is Assigned to RP37 Output Pin bits
(see Table 11-3 for peripheral function numbers)
- bit 7-6 **Unimplemented:** Read as '0'
- bit 5-0 **RP36R<5:0>:** Peripheral Output Function is Assigned to RP36 Output Pin bits
(see Table 11-3 for peripheral function numbers)

REGISTER 17-3: QEIXSTAT: QEIX STATUS REGISTER (CONTINUED)

- bit 2 **HOMIEN**: Home Input Event Interrupt Enable bit
 1 = Interrupt is enabled
 0 = Interrupt is disabled
- bit 1 **IDXIRQ**: Status Flag for Index Event Status bit
 1 = Index event has occurred
 0 = No index event has occurred
- bit 0 **IDXIEN**: Index Input Event Interrupt Enable bit
 1 = Interrupt is enabled
 0 = Interrupt is disabled

Note 1: This status bit is only applicable to PIMOD<2:0> = 011 and 100 modes.

FIGURE 19-1: I2Cx BLOCK DIAGRAM (x = 1 OR 2)



REGISTER 19-1: I2CxCON: I2Cx CONTROL REGISTER (CONTINUED)

bit 6	STREN: SCLx Clock Stretch Enable bit (when operating as I ² C slave) Used in conjunction with the SCLREL bit. 1 = Enables software or receives clock stretching 0 = Disables software or receives clock stretching
bit 5	ACKDT: Acknowledge Data bit (when operating as I ² C master, applicable during master receive) Value that is transmitted when the software initiates an Acknowledge sequence. 1 = Sends NACK during Acknowledge 0 = Sends ACK during Acknowledge
bit 4	ACKEN: Acknowledge Sequence Enable bit (when operating as I ² C master, applicable during master receive) 1 = Initiates Acknowledge sequence on SDAx and SCLx pins and transmits ACKDT data bit; hardware clears at the end of the master Acknowledge sequence 0 = Acknowledge sequence is not in progress
bit 3	RCEN: Receive Enable bit (when operating as I ² C master) 1 = Enables Receive mode for I ² C; hardware clears at the end of the eighth bit of a master receive data byte 0 = Receive sequence is not in progress
bit 2	PEN: Stop Condition Enable bit (when operating as I ² C master) 1 = Initiates Stop condition on SDAx and SCLx pins; hardware clears at the end of a master Stop sequence 0 = Stop condition is not in progress
bit 1	RSEN: Repeated Start Condition Enable bit (when operating as I ² C master) 1 = Initiates Repeated Start condition on SDAx and SCLx pins; hardware clears at the end of a master Repeated Start sequence 0 = Repeated Start condition is not in progress
bit 0	SEN: Start Condition Enable bit (when operating as I ² C master) 1 = Initiates Start condition on SDAx and SCLx pins; hardware clears at the end of a master Start sequence 0 = Start condition is not in progress

Note 1: When performing master operations, ensure that the IPMIEN bit is set to '0'.

REGISTER 25-3: PTGBTE: PTG BROADCAST TRIGGER ENABLE REGISTER^(1,2) (CONTINUED)

bit 4	OC1CS: Clock Source for OC1 bit 1 = Generates clock pulse when the broadcast command is executed 0 = Does not generate clock pulse when the broadcast command is executed
bit 3	OC4TSS: Trigger/Synchronization Source for OC4 bit 1 = Generates trigger/synchronization when the broadcast command is executed 0 = Does not generate trigger/synchronization when the broadcast command is executed
bit 2	OC3TSS: Trigger/Synchronization Source for OC3 bit 1 = Generates trigger/synchronization when the broadcast command is executed 0 = Does not generate trigger/synchronization when the broadcast command is executed
bit 1	OC2TSS: Trigger/Synchronization Source for OC2 bit 1 = Generates trigger/synchronization when the broadcast command is executed 0 = Does not generate trigger/synchronization when the broadcast command is executed
bit 0	OC1TSS: Trigger/Synchronization Source for OC1 bit 1 = Generates trigger/synchronization when the broadcast command is executed 0 = Does not generate trigger/synchronization when the broadcast command is executed

Note 1: This register is read-only when the PTG module is executing Step commands (PTGEN = 1 and PTGSTRT = 1).

2: This register is only used with the PTGCTRL OPTION = 1111 Step command.

FIGURE 26-3: USER-PROGRAMMABLE BLANKING FUNCTION BLOCK DIAGRAM

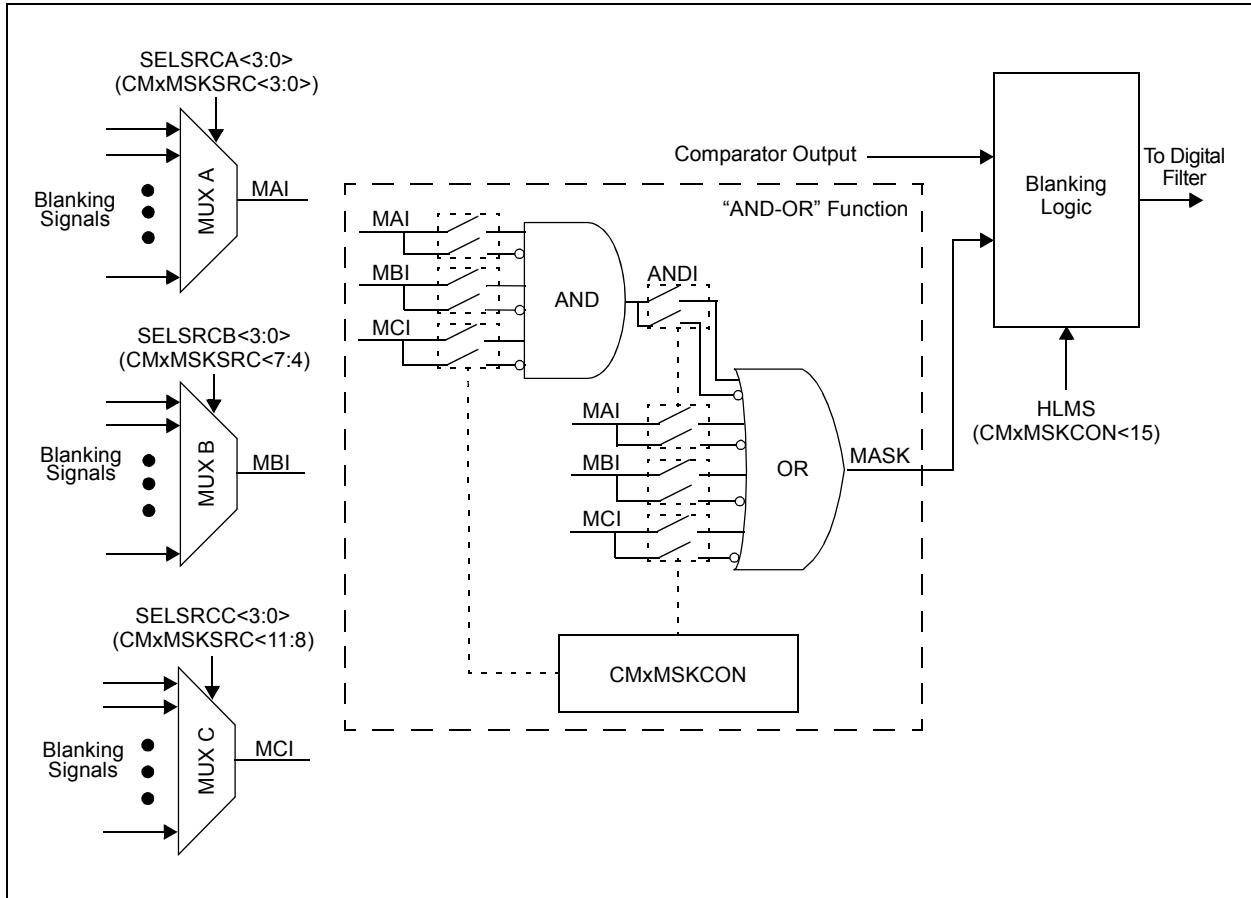
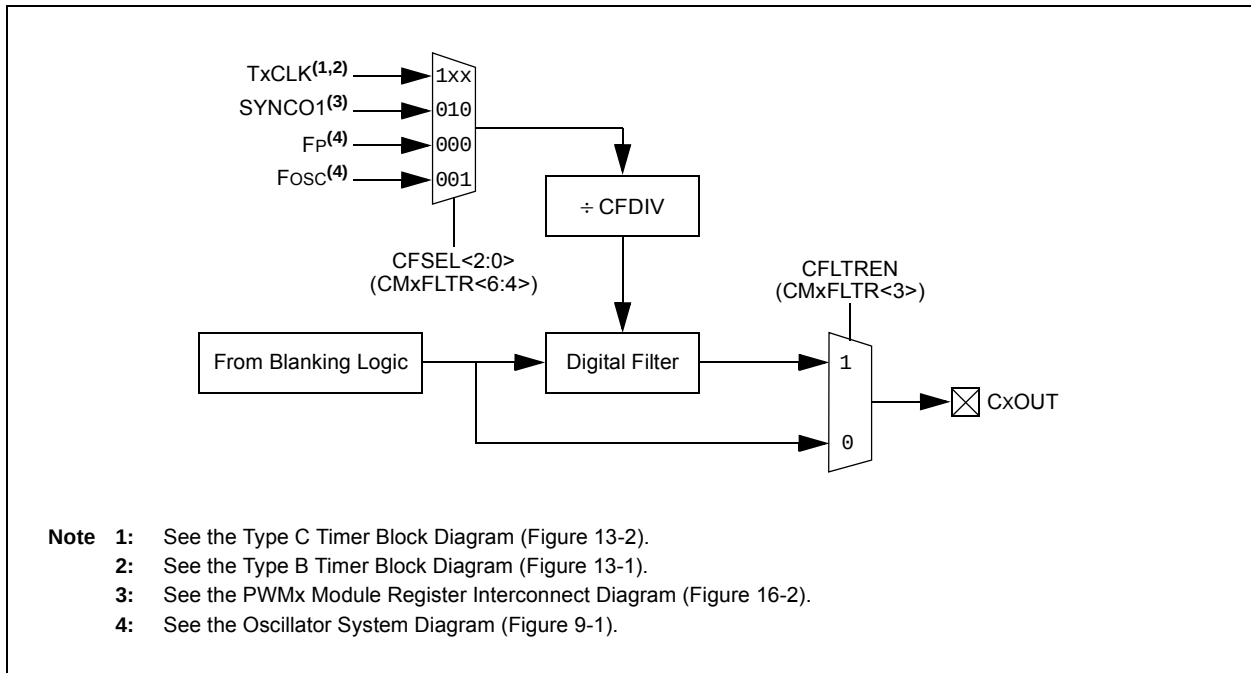


FIGURE 26-4: DIGITAL FILTER INTERCONNECT BLOCK DIAGRAM



REGISTER 26-4: CMxMSKSRC: COMPARATOR x MASK SOURCE SELECT CONTROL REGISTER (CONTINUED)

bit 3-0 **SELSRCA<3:0>**: Mask A Input Select bits

1111 = FLT4
1110 = FLT2
1101 = PTGO19
1100 = PTGO18
1011 = PWM6H
1010 = PWM6L
1001 = PWM5H
1000 = PWM5L
0111 = PWM4H
0110 = PWM4L
0101 = PWM3H
0100 = PWM3L
0011 = PWM2H
0010 = PWM2L
0001 = PWM1H
0000 = PWM1L

dsPIC33EPXXXGM3XX/6XX/7XX

TABLE 30-2: CONFIGURATION BITS DESCRIPTION (CONTINUED)

Bit Field	Description
WDTPRE	Watchdog Timer Prescaler bit 1 = 1:128 0 = 1:32
WDTPOST<3:0>	Watchdog Timer Postscaler bits 1111 = 1:32,768 1110 = 1:16,384 • • • 0001 = 1:2 0000 = 1:1
WDTWIN<1:0>	Watchdog Timer Window Select bits 11 = WDT Window is 25% of WDT Period 10 = WDT Window is 37.5% of WDT Period 01 = WDT Window is 50% of WDT Period 00 = WDT Window is 75% of WDT Period
ALTI2C1	Alternate I2C1 Pins bit 1 = I2C1 is mapped to the SDA1/SCL1 pins 0 = I2C1 is mapped to the ASDA1/ASCL1 pins
ALTI2C2	Alternate I2C2 Pins bit 1 = I2C2 is mapped to the SDA2/SCL2 pins 0 = I2C2 is mapped to the ASDA2/ASCL2 pins
BOREN	Brown-out Reset (BOR) Detection Enable bit 1 = BOR is enabled 0 = BOR is disabled
JTAGEN	JTAG Enable bit 1 = JTAG is enabled 0 = JTAG is disabled
ICS<1:0>	ICD Communication Channel Select bits 11 = Communicates on PGEC1 and PGED1 10 = Communicates on PGEC2 and PGED2 01 = Communicates on PGEC3 and PGED3 00 = Reserved, do not use

Note 1: The Two-Speed Start-up is not enabled when EC mode is used since the EC clocks will be ready immediately.

TABLE 33-13: DC CHARACTERISTICS: PROGRAM MEMORY

DC CHARACTERISTICS			Standard Operating Conditions: V_{BOR} (min)V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended				
Param No.	Symbol	Characteristic	Min	Typ ⁽¹⁾	Max	Units	Conditions
Program Flash Memory							
D130	EP	Cell Endurance	10,000	—	—	E/W	-40°C to $+125^{\circ}\text{C}$
D131	VPR	VDD for Read	V_{BORMIN}	—	3.6	V	
D132b	VPEW	VDD for Self-Timed Write	3.0	—	3.6	V	
D134	TRETD	Characteristic Retention	20	—	—	Year	Provided no other specifications are violated, -40°C to $+125^{\circ}\text{C}$
D135	IDDP	Supply Current During Programming	—	10	—	mA	
D138a	TWW	Word Write Cycle Time	46.5	46.9	47.4	μs	TWW = 346 FRC cycles, $T_A = +85^{\circ}\text{C}$ (Note 2)
D138b	TWW	Word Write Cycle Time	46.0	—	47.9	μs	TWW = 346 FRC cycles, $T_A = +125^{\circ}\text{C}$ (Note 2)
D136a	TPE	Row Write Time	0.667	0.673	0.680	ms	TRW = 4965 FRC cycles, $T_A = +85^{\circ}\text{C}$ (Note 2)
D136b	TPE	Row Write Time	0.660	—	0.687	ms	TRW = 4965 FRC cycles, $T_A = +125^{\circ}\text{C}$ (Note 2)
D137a	TPE	Page Erase Time	19.6	20	20.1	ms	TPE = 146893 FRC cycles, $T_A = +85^{\circ}\text{C}$ (Note 2)
D137b	TPE	Page Erase Time	19.5	—	20.3	ms	TPE = 146893 FRC cycles, $T_A = +125^{\circ}\text{C}$ (Note 2)

Note 1: Data in “Typ” column is at 3.3V, $+25^{\circ}\text{C}$ unless otherwise stated.

- 2:** Other conditions: FRC = 7.3728 MHz, $TUN<5:0> = b'011111$ (for Min), $TUN<5:0> = b'100000$ (for Max). This parameter depends on the FRC accuracy (see Table 33-19) and the value of the FRC Oscillator Tuning register.

FIGURE 33-13: QEAX/QEBx INPUT CHARACTERISTICS

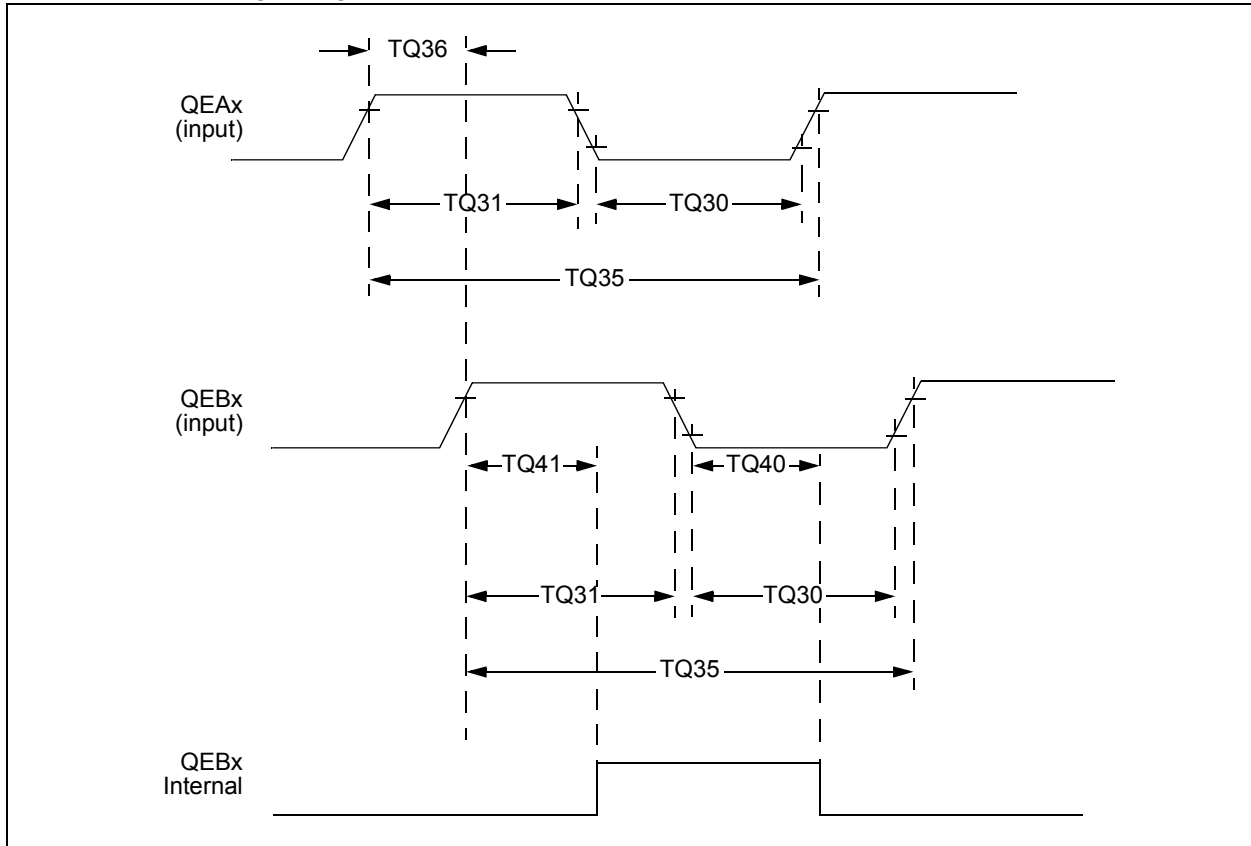


TABLE 33-30: QUADRATURE DECODER TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended			
Param No.	Symbol	Characteristic ⁽¹⁾	Typ. ⁽²⁾	Max.	Units	Conditions
TQ30	TQuL	Quadrature Input Low Time	6 Tcy	—	ns	
TQ31	TQuH	Quadrature Input High Time	6 Tcy	—	ns	
TQ35	TQuIN	Quadrature Input Period	12 Tcy	—	ns	
TQ36	TQuP	Quadrature Phase Period	3 Tcy	—	ns	
TQ40	TQuFL	Filter Time to Recognize Low with Digital Filter	3 * N * Tcy	—	ns	N = 1, 2, 4, 16, 32, 64, 128 and 256 (Note 3)
TQ41	TQuFH	Filter Time to Recognize High with Digital Filter	3 * N * Tcy	—	ns	N = 1, 2, 4, 16, 32, 64, 128 and 256 (Note 3)

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typical" column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

3: N = Index Channel Digital Filter Clock Divide Select bits. Refer to the "dsPIC33/PIC24 Family Reference Manual", "Quadrature Encoder Interface (QE)" (DS70601). Please see the Microchip web site for the latest "dsPIC33/PIC24 Family Reference Manual" sections.

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