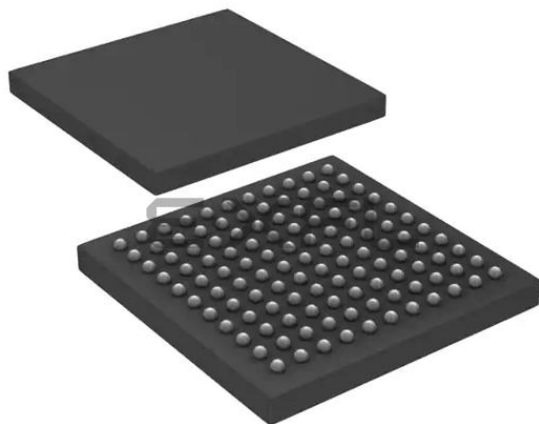




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Details

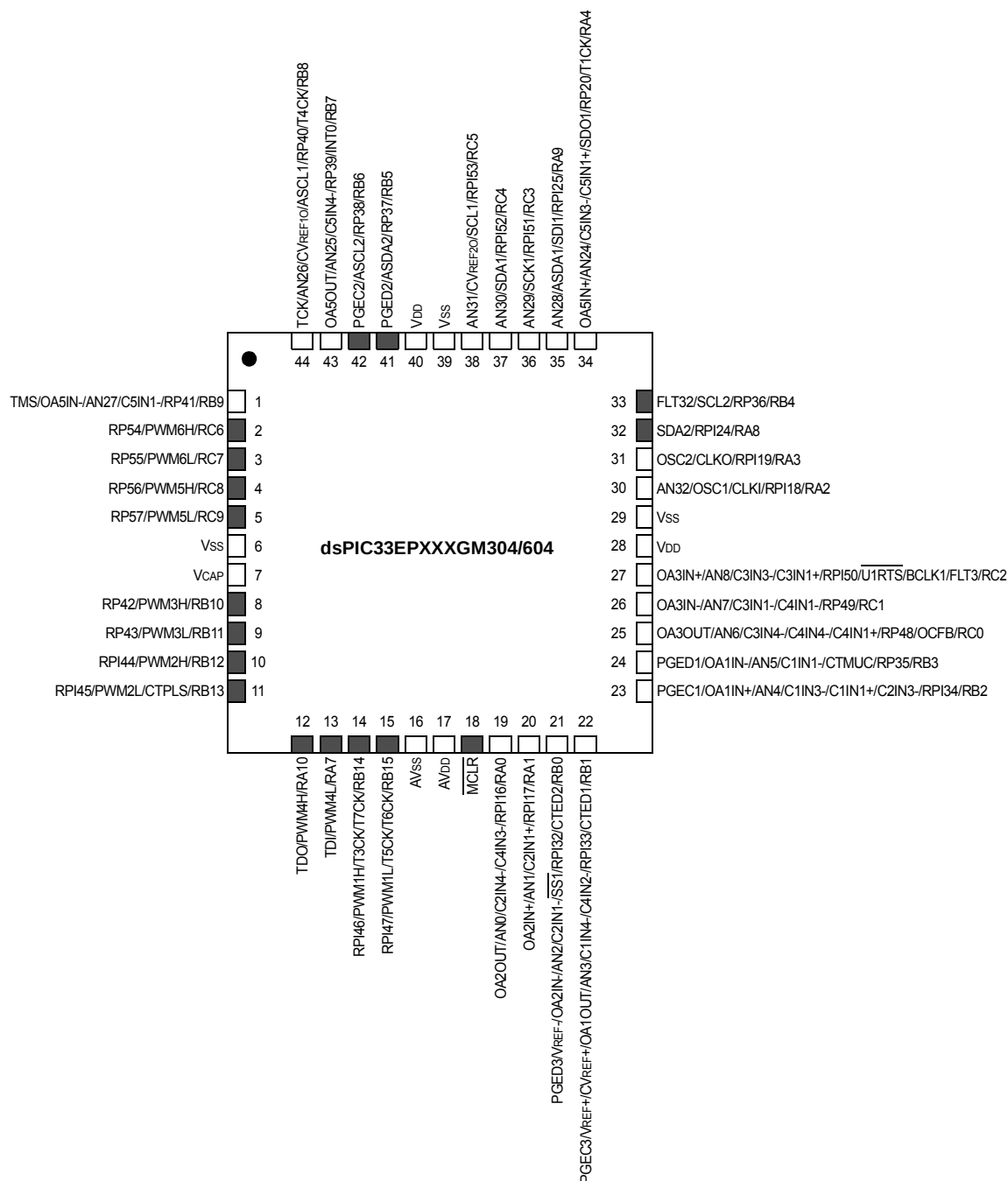
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	-
Connectivity	CANbus, I ² C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, Motor Control PWM, POR, PWM, WDT
Number of I/O	85
Program Memory Size	512KB (170K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	-
Data Converters	A/D 49x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	121-TFBGA
Supplier Device Package	121-TFBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep512gm710-h-bg

dsPIC33EPXXXGM3XX/6XX/7XX

Pin Diagrams (Continued)

44-Pin QFN^(1,2,3)

■ = Pins are up to 5V tolerant



- Note**
- 1: The RPN/RPIN pins can be used by any remappable peripheral with some limitation. See **Section 11.4 “Peripheral Pin Select (PPS)”** for available peripherals and for information on limitations.
 - 2: Every I/O port pin (RAX-RGX) can be used as a Change Notification pin (CNAX-CNGX). See **Section 11.0 “I/O Ports”** for more information.
 - 3: The metal pad at the bottom of the device is not connected to any pins and is recommended to be connected to VSS externally.

dsPIC33EPXXXGM3XX/6XX/7XX

FIGURE 4-2: PROGRAM MEMORY MAP FOR dsPIC33EP256GM3XX/6XX/7XX DEVICES⁽¹⁾

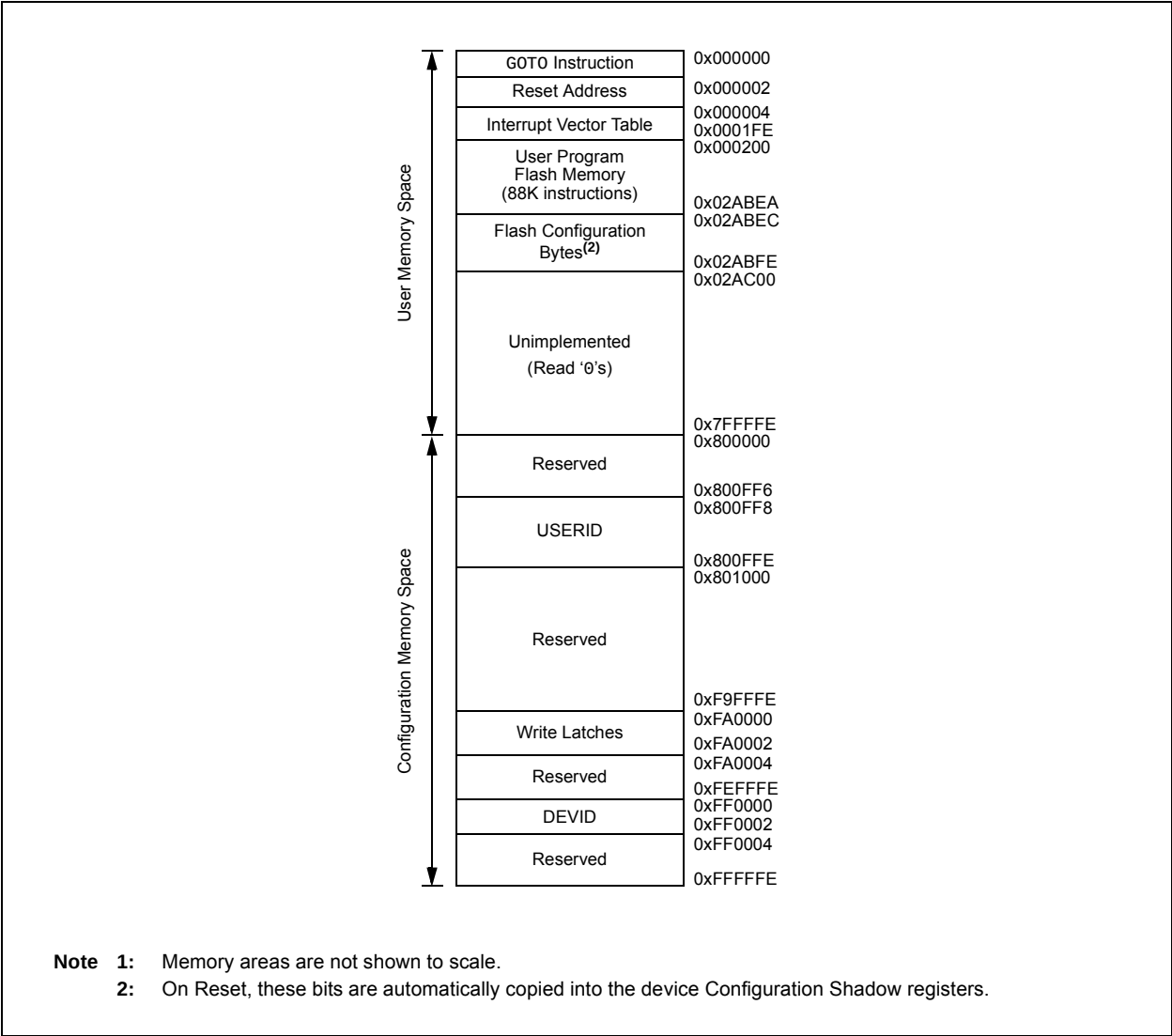
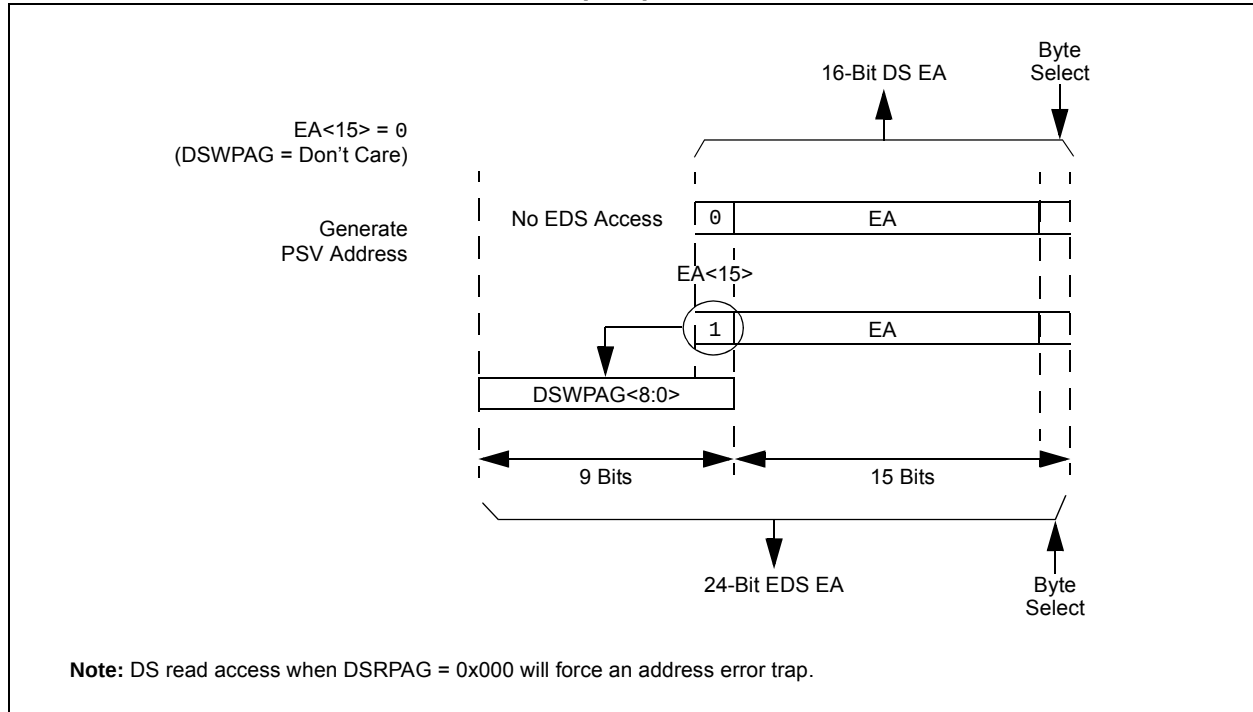


FIGURE 4-9: EXTENDED DATA SPACE (EDS) WRITE ADDRESS GENERATION



The paged memory scheme provides access to multiple 32-Kbyte windows in the EDS and PSV memory. The Data Space Page registers, DSxPAG, in combination with the upper half of the Data Space address, can provide up to 16 Mbytes of additional address space in the EDS and 8 Mbytes (DSRPAG only) of PSV address space. The paged data memory space is shown in Figure 4-10.

The Program Space (PS) can be accessed with a DSRPAG of 0x200 or greater. Only reads from PS are supported using the DSRPAG. Writes to PS are not supported, so DSWPAG is dedicated to DS, including EDS only. The Data Space and EDS can be read from, and written to, using DSRPAG and DSWPAG, respectively.

dsPIC33EPXXXGM3XX/6XX/7XX

REGISTER 5-4: NVMKEY: NONVOLATILE MEMORY KEY REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

W-0	W-0	W-0	W-0	W-0	W-0	W-0	W-0
NVMKEY<7:0>							
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **NVMKEY<7:0>:** NVM Key Register (write-only) bits

REGISTER 5-5: NVMSRCADRH: NONVOLATILE DATA MEMORY UPPER ADDRESS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
NVMSRCADRH<23:16>							
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-8 **Unimplemented:** Read as '0'

bit 7-0 **NVMSRCADRH<23:16>:** Nonvolatile Data Memory Upper Address bits

dsPIC33EPXXXGM3XX/6XX/7XX

REGISTER 11-19: RPINR25: PERIPHERAL PIN SELECT INPUT REGISTER 25

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	COFSR<6:0>						
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 15-7
- bit 6-0
- Unimplemented: Read as '0'

COFSR<6:0>: Assign DCI Frame Sync Input (COFS) to the Corresponding RPN Pin bits (see Table 11-2 for input pin selection numbers)

1111100 = Input tied to RPI124

-
 -
 -

0000001 = Input tied to CMP1

0000000 = Input tied to Vss

15.0 OUTPUT COMPARE

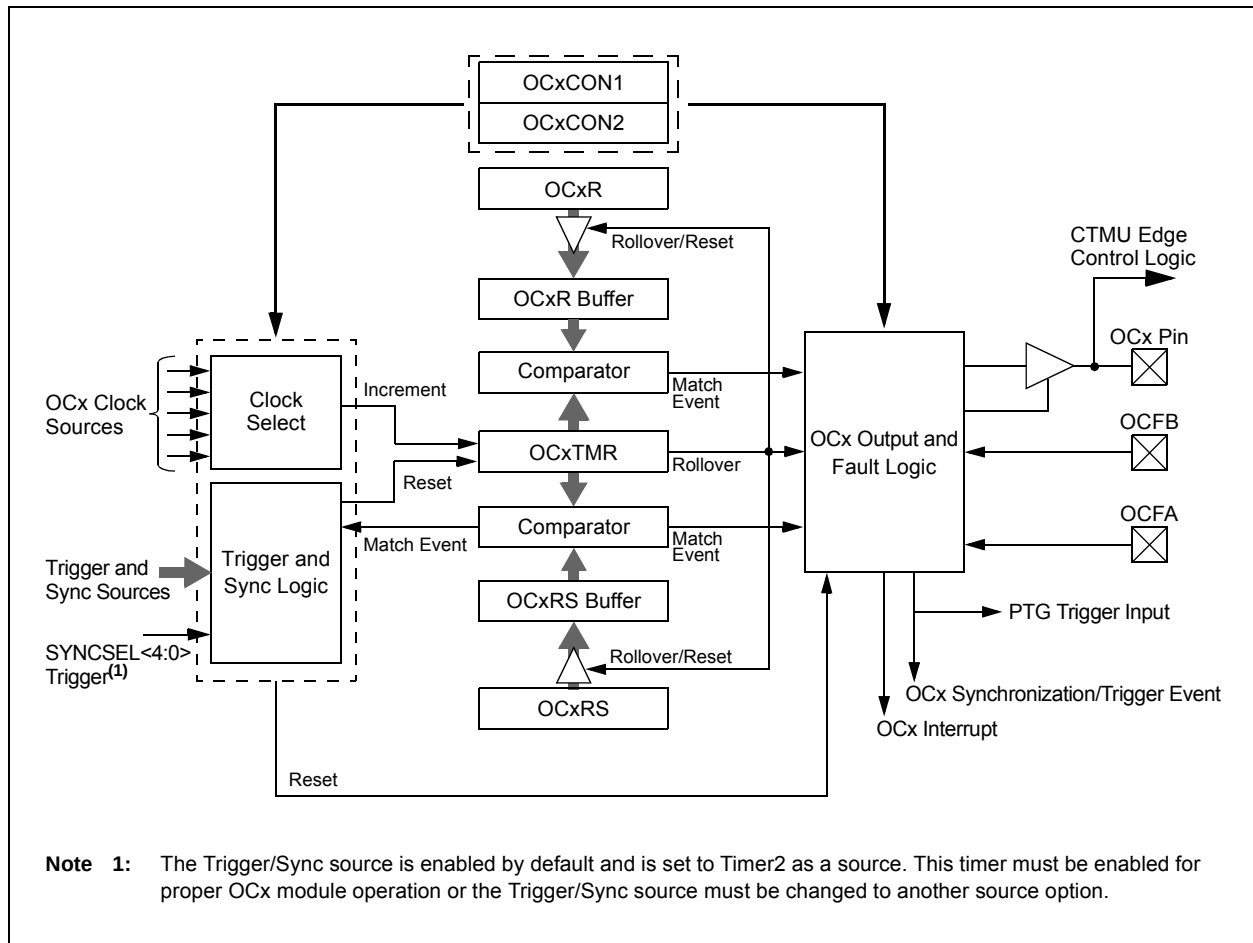
Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGM3XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the “dsPIC33/PIC24E Family Reference Manual”, “Output Compare” (DS70005157), which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 “Memory Organization”** in this data sheet for device-specific register and bit information.

The output compare module can select one of eight available clock sources for its time base. The module compares the value of the timer with the value of one or two Compare registers depending on the operating mode selected. The state of the output pin changes when the timer value matches the Compare register value. The output compare module generates either a single output pulse, or a sequence of output pulses, by changing the state of the output pin on the compare match events. The output compare module can also generate interrupts on compare match events and trigger DMA data transfers.

Note: See the “dsPIC33/PIC24 Family Reference Manual”, “Output Compare” (DS70005157) for OCxR and OCxRS register restrictions.

FIGURE 15-1: OUTPUT COMPARE x MODULE BLOCK DIAGRAM



dsPIC33EPXXXGM3XX/6XX/7XX

REGISTER 21-8: CxEC: CANx TRANSMIT/RECEIVE ERROR COUNT REGISTER

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
TERRCNT7	TERRCNT6	TERRCNT5	TERRCNT4	TERRCNT3	TERRCNT2	TERRCNT1	TERRCNT0
bit 15							bit 8

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
RERRCNT7	RERRCNT6	RERRCNT5	RERRCNT4	RERRCNT3	RERRCNT2	RERRCNT1	RERRCNT0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-8 **TERRCNT<7:0>**: Transmit Error Count bits

bit 7-0 **RERRCNT<7:0>**: Receive Error Count bits

REGISTER 21-9: CxCFG1: CANx BAUD RATE CONFIGURATION REGISTER 1

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
SJW1	SJW0	BRP5	BRP4	BRP3	BRP2	BRP1	BRP0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-8 **Unimplemented**: Read as '0'

bit 7-6 **SJW<1:0>**: Synchronization Jump Width bits

11 = Length is 4 x Tq

10 = Length is 3 x Tq

01 = Length is 2 x Tq

00 = Length is 1 x Tq

bit 5-0 **BRP<5:0>**: Baud Rate Prescaler bits

11 1111 = TQ = 2 x 64 x 1/FCAN

•

•

•

00 0010 = TQ = 2 x 3 x 1/FCAN

00 0001 = TQ = 2 x 2 x 1/FCAN

00 0000 = TQ = 2 x 1 x 1/FCAN

dsPIC33EPXXXGM3XX/6XX/7XX

REGISTER 21-15: CxBUFNT4: CANx FILTERS 12-15 BUFFER POINTER REGISTER 4

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F15BP3	F15BP2	F15BP1	F15BP0	F14BP3	F14BP2	F14BP1	F14BP0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
F13BP3	F13BP2	F13BP1	F13BP0	F12BP3	F12BP2	F12BP1	F12BP0
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-12 **F15BP<3:0>**: RX Buffer Mask for Filter 15 bits

1111 = Filter hits received in RX FIFO buffer

1110 = Filter hits received in RX Buffer 14

•

•

•

0001 = Filter hits received in RX Buffer 1

0000 = Filter hits received in RX Buffer 0

bit 11-8 **F14BP<3:0>**: RX Buffer Mask for Filter 14 bits (same values as bits 15-12)

bit 7-4 **F13BP<3:0>**: RX Buffer Mask for Filter 13 bits (same values as bits 15-12)

bit 3-0 **F12BP<3:0>**: RX Buffer Mask for Filter 12 bits (same values as bits 15-12)

23.3 ADCx Control Registers

REGISTER 23-1: ADxCON1: ADCx CONTROL REGISTER 1

R/W-0	U-0	R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0
ADON	—	ADSIDL	ADDMABM	—	AD12B	FORM1	FORM0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0, HC, HS	R/C-0, HC, HS
SSRC2	SSRC1	SSRC0	SSRCG	SIMSAM	ASAM	SAMP	DONE ⁽²⁾
bit 7							bit 0

Legend:	C = Clearable bit	U = Unimplemented bit, read as '0'	
R = Readable bit	W = Writable bit	HS = Hardware Settable bit	HC = Hardware Clearable bit
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

- bit 15 **ADON:** ADCx Operating Mode bit
1 = ADCx module is operating
0 = ADCx is off
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **ADSIDL:** ADCx Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode
- bit 12 **ADDMABM:** ADCx DMA Buffer Build Mode bit
1 = DMA buffers are written in the order of conversion; the module provides an address to the DMA channel that is the same as the address used for the non-DMA stand-alone buffer
0 = DMA buffers are written in Scatter/Gather mode; the module provides a Scatter/Gather address to the DMA channel based on the index of the analog input and the size of the DMA buffer
- bit 11 **Unimplemented:** Read as '0'
- bit 10 **AD12B:** 10-Bit or 12-Bit ADCx Operation Mode bit
1 = 12-bit, 1-channel ADCx operation
0 = 10-bit, 4-channel ADCx operation
- bit 9-8 **FORM<1:0>:** Data Output Format bits
For 10-Bit Operation:
11 = Signed fractional (DOUT = sddd dddd dd00 0000, where s = .NOT.d<9>)
10 = Fractional (DOUT = dddd dddd dd00 0000)
01 = Signed integer (DOUT = ssss sssd dddd dddd, where s = .NOT.d<9>)
00 = Integer (DOUT = 0000 00dd dddd dddd)
For 12-Bit Operation:
11 = Signed fractional (DOUT = sddd dddd dddd 0000, where s = .NOT.d<11>)
10 = Fractional (DOUT = dddd dddd dddd 0000)
01 = Signed integer (DOUT = ssss sddd dddd dddd, where s = .NOT.d<11>)
00 = Integer (DOUT = 0000 dddd dddd dddd)

- Note 1:** See Section 25.0 “Peripheral Trigger Generator (PTG) Module” for information on this selection.
- Note 2:** Do not clear the DONE bit in software if ADCx Sample Auto-Start bit is enabled (ASAM = 1).

REGISTER 23-8: ADxCSSL: ADCx INPUT SCAN SELECT REGISTER LOW^(1,2)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CSS<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CSS<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **CSS<15:0>**: ADCx Input Scan Selection bits

1 = Selects ANx for input scan

0 = Skips ANx for input scan

Note 1: On devices with less than 16 analog inputs, all bits in this register can be selected by the user application. However, inputs selected for scan without a corresponding input on the device convert VREFL.

2: CSSx = ANx, where 'x' = 0-15.

dsPIC33EPXXXGM3XX/6XX/7XX

REGISTER 24-5: RSCON: DCI RECEIVE SLOT CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
RSE<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
RSE<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **RSE<15:0>**: DCI Receive Slot Enable bits
1 = CSDI data is received during Individual Time Slot n
0 = CSDI data is ignored during Individual Time Slot n

REGISTER 24-6: TSCON: DCI TRANSMIT SLOT CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TSE<15:8>							
bit 15				bit 8			

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
TSE<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

bit 15-0 **TSE<15:0>**: DCI Transmit Slot Enable Control bits
1 = Transmit buffer contents are sent during Individual Time Slot n
0 = CSDO pin is tri-stated or driven to logic '0' during the individual time slot, depending on the state of the CSDOM bit

REGISTER 26-5: CMxMSKCON: COMPARATOR x MASK GATING CONTROL REGISTER

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
HLMS	—	OCEN	OCNEN	OBEN	OBNEN	OAEN	OANEN
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
NAGS	PAGS	ACEN	ACNEN	ABEN	ABNEN	AAEN	AANEN
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

- bit 15 **HLMS:** High or Low-Level Masking Select bit
1 = The masking (blanking) function will prevent any asserted ('0') comparator signal from propagating
0 = The masking (blanking) function will prevent any asserted ('1') comparator signal from propagating
- bit 14 **Unimplemented:** Read as '0'
- bit 13 **OCEN:** OR Gate C Input Enable bit
1 = MCI is connected to the OR gate
0 = MCI is not connected to the OR gate
- bit 12 **OCNEN:** OR Gate C Input Inverted Enable bit
1 = Inverted MCI is connected to the OR gate
0 = Inverted MCI is not connected to the OR gate
- bit 11 **OBEN:** OR Gate B Input Enable bit
1 = MBI is connected to the OR gate
0 = MBI is not connected to the OR gate
- bit 10 **OBNEN:** OR Gate B Input Inverted Enable bit
1 = Inverted MBI is connected to the OR gate
0 = Inverted MBI is not connected to the OR gate
- bit 9 **OAEN:** OR Gate A Input Enable bit
1 = MAI is connected to the OR gate
0 = MAI is not connected to the OR gate
- bit 8 **OANEN:** OR Gate A Input Inverted Enable bit
1 = Inverted MAI is connected to the OR gate
0 = Inverted MAI is not connected to the OR gate
- bit 7 **NAGS:** AND Gate Output Inverted Enable bit
1 = Inverted ANDI is connected to the OR gate
0 = Inverted ANDI is not connected to the OR gate
- bit 6 **PAGS:** AND Gate Output Enable bit
1 = ANDI is connected to the OR gate
0 = ANDI is not connected to the OR gate
- bit 5 **ACEN:** AND Gate C Input Enable bit
1 = MCI is connected to the AND gate
0 = MCI is not connected to the AND gate
- bit 4 **ACNEN:** AND Gate C Input Inverted Enable bit
1 = Inverted MCI is connected to the AND gate
0 = Inverted MCI is not connected to the AND gate

30.2 User ID Words

dsPIC33EPXXXGM3XX/6XX/7XX devices contain four User ID Words, located at addresses, 0x800FF8 through 0x800FFE. The User ID Words can be used for storing product information, such as serial numbers, system manufacturing dates, manufacturing lot numbers and other application-specific information.

The User ID Words register map is shown in Table 30-3.

TABLE 30-3: USER ID WORDS REGISTER MAP

File Name	Address	Bits<23:16>	Bits<15:0>
FUID0	0x800FF8	—	UID0
FUID1	0x800FFA	—	UID1
FUID2	0x800FFC	—	UID2
FUID3	0x800FFE	—	UID3

Legend: — = unimplemented, read as '1'.

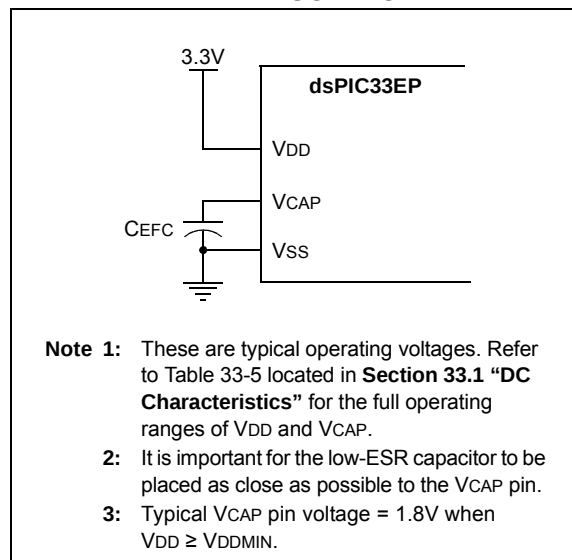
30.3 On-Chip Voltage Regulator

All of the dsPIC33EPXXXGM3XX/6XX/7XX devices power their core digital logic at a nominal 1.8V. This can create a conflict for designs that are required to operate at a higher typical voltage, such as 3.3V. To simplify system design, all devices in the dsPIC33EPXXXGM3XX/6XX/7XX family incorporate an on-chip regulator that allows the device to run its core logic from VDD.

The regulator provides power to the core from the other VDD pins. A low-ESR (less than 1 Ohm) capacitor (such as tantalum or ceramic) must be connected to the VCAP pin (Figure 30-1). This helps to maintain the stability of the regulator. The recommended value for the filter capacitor is provided in Table 33-5, located in Section 33.0 “Electrical Characteristics”.

Note: It is important for the low-ESR capacitor to be placed as close as possible to the VCAP pin.

FIGURE 30-1: CONNECTIONS FOR THE ON-CHIP VOLTAGE REGULATOR^(1,2,3)



30.4 Brown-out Reset (BOR)

The Brown-out Reset (BOR) module is based on an internal voltage reference circuit that monitors the regulated supply voltage, VCAP. The main purpose of the BOR module is to generate a device Reset when a brown-out condition occurs. Brown-out conditions are generally caused by glitches on the AC mains (for example, missing portions of the AC cycle waveform due to bad power transmission lines or voltage sags due to excessive current draw when a large inductive load is turned on).

A BOR generates a Reset pulse, which resets the device. The BOR selects the clock source, based on the device Configuration bit values (FNOSC<2:0> and POSCMD<1:0>).

If an oscillator mode is selected, the BOR activates the Oscillator Start-up Timer (OST). The system clock is held until OST expires. If the PLL is used, the clock is held until the LOCK bit (OSCCON<5>) is '1'.

Concurrently, the Power-up Timer (PWRT) Time-out (TPWRT) is applied before the internal Reset is released. If TPWRT = 0 and a crystal oscillator is being used, then a nominal delay of TFSCM is applied. The total delay in this case is TFSCM. Refer to Parameter SY35 in Table 33-21 of Section 33.0 “Electrical Characteristics” for specific TFSCM values.

The BOR Status bit (RCON<1>) is set to indicate that a BOR has occurred. The BOR circuit continues to operate while in Sleep or Idle mode and resets the device should VDD fall below the BOR threshold voltage.

TABLE 31-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Base Instr #	Assembly Mnemonic	Assembly Syntax	Description	# of Words	# of Cycles	Status Flags Affected
8	BSW	BSW.C ws, Wb	Write C bit to Ws<Wb>	1	1	None
		BSW.Z ws, Wb	Write Z bit to Ws<Wb>	1	1	None
9	BTG	BTG f, #bit4	Bit Toggle f	1	1	None
		BTG ws, #bit4	Bit Toggle Ws	1	1	None
10	BTSC	BTSC f, #bit4	Bit Test f, Skip if Clear	1	1 (2 or 3)	None
		BTSC ws, #bit4	Bit Test Ws, Skip if Clear	1	1 (2 or 3)	None
11	BTSS	BTSS f, #bit4	Bit Test f, Skip if Set	1	1 (2 or 3)	None
		BTSS ws, #bit4	Bit Test Ws, Skip if Set	1	1 (2 or 3)	None
12	BTST	BTST f, #bit4	Bit Test f	1	1	Z
		BTST.C ws, #bit4	Bit Test Ws to C	1	1	C
		BTST.Z ws, #bit4	Bit Test Ws to Z	1	1	Z
		BTST.C ws, Wb	Bit Test Ws<Wb> to C	1	1	C
		BTST.Z ws, Wb	Bit Test Ws<Wb> to Z	1	1	Z
13	BTSTS	BTSTS f, #bit4	Bit Test then Set f	1	1	Z
		BTSTS.C ws, #bit4	Bit Test Ws to C, then Set	1	1	C
		BTSTS.Z ws, #bit4	Bit Test Ws to Z, then Set	1	1	Z
14	CALL	CALL lit23	Call subroutine	2	4	SFA
		CALL Wn	Call indirect subroutine	1	4	SFA
		CALL.L Wn	Call indirect subroutine (long address)	1	4	SFA
15	CLR	CLR f	f = 0x0000	1	1	None
		CLR WREG	WREG = 0x0000	1	1	None
		CLR ws	Ws = 0x0000	1	1	None
		CLR Acc, Wx, Wxd, Wy, Wyd, AWB	Clear Accumulator	1	1	OA, OB, SA, SB
16	CLRWD	CLRWD	Clear Watchdog Timer	1	1	WDTO, Sleep
17	COM	COM f	f = $\bar{f}$	1	1	N, Z
		COM f, WREG	WREG = $\bar{f}$	1	1	N, Z
		COM ws, Wd	Wd = $\overline{Ws}$	1	1	N, Z
18	CP	CP f	Compare f with WREG	1	1	C, DC, N, OV, Z
		CP Wb, #lit8	Compare Wb with lit8	1	1	C, DC, N, OV, Z
		CP Wb, Ws	Compare Wb with Ws (Wb – Ws)	1	1	C, DC, N, OV, Z
19	CP0	CP0 f	Compare f with 0x0000	1	1	C, DC, N, OV, Z
		CP0 ws	Compare Ws with 0x0000	1	1	C, DC, N, OV, Z
20	CPB	CPB f	Compare f with WREG, with Borrow	1	1	C, DC, N, OV, Z
		CPB Wb, #lit8	Compare Wb with lit8, with Borrow	1	1	C, DC, N, OV, Z
		CPB Wb, Ws	Compare Wb with Ws, with Borrow (Wb – Ws – C)	1	1	C, DC, N, OV, Z
21	CPSEQ	CPSEQ Wb, Wn	Compare Wb with Wn, skip if =	1	1 (2 or 3)	None
	CPBEQ	CPBEQ Wb, Wn, Expr	Compare Wb with Wn, branch if =	1	1 (5)	None
22	CPSGT	CPSGT Wb, Wn	Compare Wb with Wn, skip if >	1	1 (2 or 3)	None
	CPBGT	CPBGT Wb, Wn, Expr	Compare Wb with Wn, branch if >	1	1 (5)	None
23	CPSLT	CPSLT Wb, Wn	Compare Wb with Wn, skip if <	1	1 (2 or 3)	None
	CPBLT	CPBLT Wb, Wn, Expr	Compare Wb with Wn, branch if <	1	1 (5)	None
24	CPSNE	CPSNE Wb, Wn	Compare Wb with Wn, skip if ≠	1	1 (2 or 3)	None
	CPBNE	CPBNE Wb, Wn, Expr	Compare Wb with Wn, branch if ≠	1	1 (5)	None

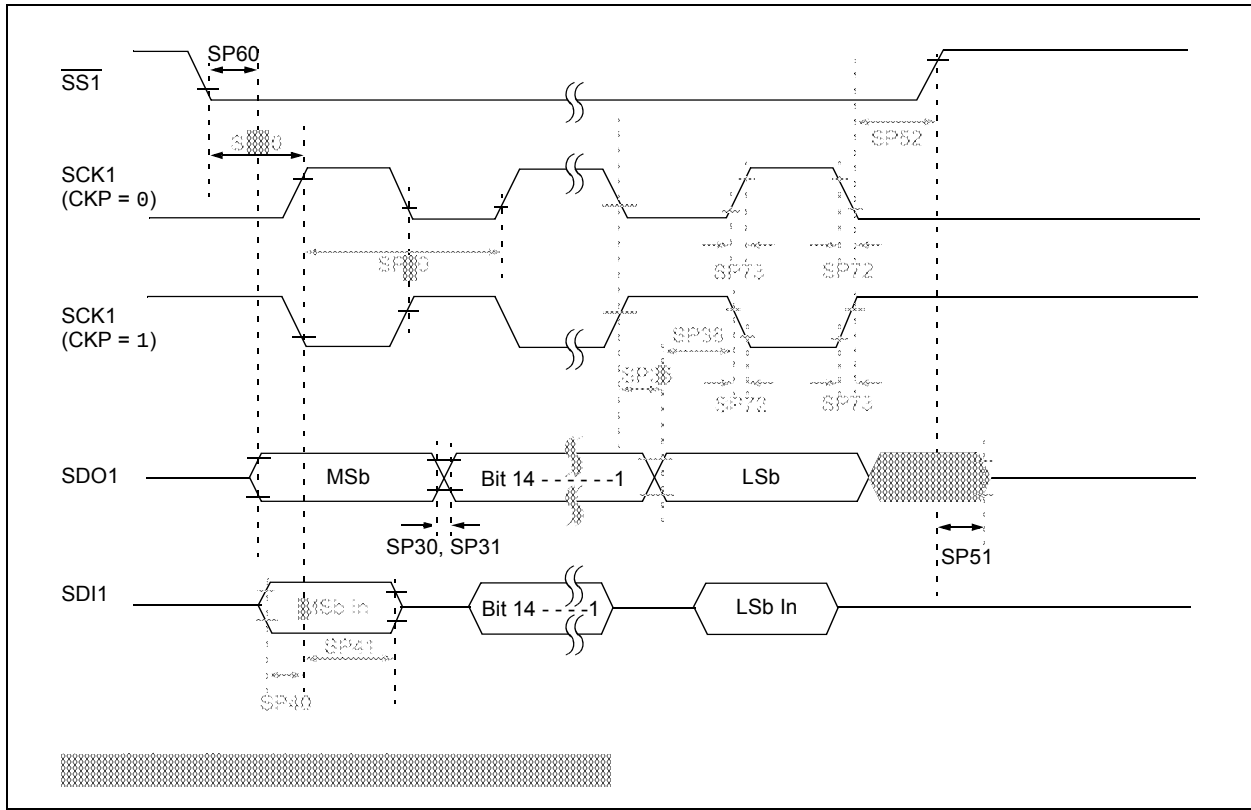
Note: Read and Read-Modify-Write (e.g., bit operations and logical operations) on non-CPU SFRs incur an additional instruction cycle.

TABLE 33-10: DC CHARACTERISTICS: I/O PIN INPUT SPECIFICATIONS (CONTINUED)

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for Industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for Extended				
Param No.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
DI50	I _{IL}	Input Leakage Current^(1,2) I/O Pins 5V Tolerant ⁽³⁾	-1	—	+1	μA	V _{SS} ≤ V _{PIN} ≤ 5V, Pin at high-impedance
DI51		I/O Pins Not 5V Tolerant ⁽³⁾	-1	—	+1	μA	V _{SS} ≤ V _{PIN} ≤ V _{DD} , Pin at high-impedance, $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$
DI51a		I/O Pins Not 5V Tolerant ⁽³⁾	-1	—	+1	μA	Analog pins shared with external reference pins, $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$
DI51b		I/O Pins Not 5V Tolerant ⁽³⁾	-1	—	+1	μA	V _{SS} ≤ V _{PIN} ≤ V _{DD} , Pin at high-impedance, $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$
DI51c		I/O Pins Not 5V Tolerant ⁽³⁾	-1	—	+1	μA	Analog pins shared with external reference pins, $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$
DI55		MCLR	-5	—	+5	μA	V _{SS} ≤ V _{PIN} ≤ V _{DD}
DI56		OSC1	-5	—	+5	μA	V _{SS} ≤ V _{PIN} ≤ V _{DD} , XT and HS modes

- Note 1:** The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current can be measured at different input voltages.
- 2:** Negative current is defined as current sourced by the pin.
- 3:** See the “Pin Diagrams” section for the 5V tolerant I/O pins.
- 4:** V_{IL} source < (V_{SS} – 0.3). Characterized but not tested.
- 5:** Non-5V tolerant pins V_{IH} source > (V_{DD} + 0.3), 5V tolerant pins V_{IH} source > 5.5V. Characterized but not tested.
- 6:** Digital 5V tolerant pins cannot tolerate any “positive” input injection current from input sources > 5.5V.
- 7:** Non-zero injection currents can affect the ADC results by approximately 4-6 counts.
- 8:** Any number and/or combination of I/O pins not excluded under I_{ICL} or I_{ICH} conditions are permitted provided the mathematical “absolute instantaneous” sum of the input injection currents from all pins do not exceed the specified limit. Characterized but not tested.

FIGURE 33-27: SPI1 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 0, SMP = 0)
TIMING CHARACTERISTICS



dsPIC33EPXXXGM3XX/6XX/7XX

TABLE 33-48: I2Cx BUS DATA TIMING REQUIREMENTS (MASTER MODE)

AC CHARACTERISTICS				Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Param No.	Symbol	Characteristic ⁽⁴⁾		Min. ⁽¹⁾	Max.	Units	Conditions
IM10	TLO:SCL	Clock Low Time	100 kHz mode	Tcy/2 (BRG + 2)	—	μs	
			400 kHz mode	Tcy/2 (BRG + 2)	—	μs	
			1 MHz mode ⁽²⁾	Tcy/2 (BRG + 2)	—	μs	
IM11	THI:SCL	Clock High Time	100 kHz mode	Tcy/2 (BRG + 2)	—	μs	
			400 kHz mode	Tcy/2 (BRG + 2)	—	μs	
			1 MHz mode ⁽²⁾	Tcy/2 (BRG + 2)	—	μs	
IM20	TF:SCL	SDAx and SCLx Fall Time	100 kHz mode	—	300	ns	Cb is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 Cb	300	ns	
			1 MHz mode ⁽²⁾	—	100	ns	
IM21	TR:SCL	SDAx and SCLx Rise Time	100 kHz mode	—	1000	ns	Cb is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1 Cb	300	ns	
			1 MHz mode ⁽²⁾	—	300	ns	
IM25	TSU:DAT	Data Input Setup Time	100 kHz mode	250	—	ns	
			400 kHz mode	100	—	ns	
			1 MHz mode ⁽²⁾	40	—	ns	
IM26	THD:DAT	Data Input Hold Time	100 kHz mode	0	—	μs	
			400 kHz mode	0	0.9	μs	
			1 MHz mode ⁽²⁾	0.2	—	μs	
IM30	TSU:STA	Start Condition Setup Time	100 kHz mode	Tcy/2 (BRG + 2)	—	μs	Only relevant for Repeated Start condition
			400 kHz mode	Tcy/2 (BRG + 2)	—	μs	
			1 MHz mode ⁽²⁾	Tcy/2 (BRG + 2)	—	μs	
IM31	THD:STA	Start Condition Hold Time	100 kHz mode	Tcy/2 (BRG + 2)	—	μs	After this period, the first clock pulse is generated
			400 kHz mode	Tcy/2 (BRG + 2)	—	μs	
			1 MHz mode ⁽²⁾	Tcy/2 (BRG + 2)	—	μs	
IM33	TSU:STO	Stop Condition Setup Time	100 kHz mode	Tcy/2 (BRG + 2)	—	μs	
			400 kHz mode	Tcy/2 (BRG + 2)	—	μs	
			1 MHz mode ⁽²⁾	Tcy/2 (BRG + 2)	—	μs	
IM34	THD:STO	Stop Condition Hold Time	100 kHz mode	Tcy/2 (BRG + 2)	—	μs	
			400 kHz mode	Tcy/2 (BRG + 2)	—	μs	
			1 MHz mode ⁽²⁾	Tcy/2 (BRG + 2)	—	μs	
IM40	TAA:SCL	Output Valid From Clock	100 kHz mode	—	3500	ns	
			400 kHz mode	—	1000	ns	
			1 MHz mode ⁽²⁾	—	400	ns	
IM45	TBF:SDA	Bus Free Time	100 kHz mode	4.7	—	μs	Time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	μs	
			1 MHz mode ⁽²⁾	0.5	—	μs	
IM50	CB	Bus Capacitive Loading		—	400	pF	
IM51	TPGD	Pulse Gobbler Delay		65	390	ns	(Note 3)

Note 1: BRG is the value of the I²C Baud Rate Generator. Refer to the “dsPIC33/PIC24 Family Reference Manual”, “Inter-Integrated Circuit™ (I²C™)” (DS70000195). Please see the Microchip web site for the latest “dsPIC33E/PIC24E Family Reference Manual” sections.

2: Maximum pin capacitance = 10 pF for all I2Cx pins (for 1 MHz mode only).

3: Typical value for this parameter is 130 ns.

4: These parameters are characterized, but not tested in manufacturing.

TABLE 33-58: ADCx MODULE SPECIFICATIONS (10-BIT MODE)

AC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) ⁽¹⁾ Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	Symbol	Characteristic	Min.	Typ.	Max.	Units	Conditions
ADC Accuracy (10-Bit Mode)							
AD20b	Nr	Resolution	10 Data Bits			bits	
AD21b	INL	Integral Nonlinearity	-0.625	—	0.625	LSb	-40°C ≤ TA ≤ +85°C (Note 2)
			-1.5	—	1.5	LSb	+85°C < TA ≤ +125°C (Note 2)
AD22b	DNL	Differential Nonlinearity	-0.25	—	0.25	LSb	-40°C ≤ TA ≤ +85°C (Note 2)
			-0.25	—	0.25	LSb	+85°C < TA ≤ +125°C (Note 2)
AD23b	GERR	Gain Error	-2.5	—	2.5	LSb	-40°C ≤ TA ≤ +85°C (Note 2)
			-2.5	—	2.5	LSb	+85°C < TA ≤ +125°C (Note 2)
AD24b	EOFF	Offset Error	-1.25	—	1.25	LSb	-40°C ≤ TA ≤ +85°C (Note 2)
			-1.25	—	1.25	LSb	+85°C < TA ≤ +125°C (Note 2)
AD25b	—	Monotonicity	—	—	—	—	Guaranteed
Dynamic Performance (10-Bit Mode)							
AD30b	THD	Total Harmonic Distortion ⁽³⁾	—	64	—	dB	
AD31b	SINAD	Signal to Noise and Distortion ⁽³⁾	—	57	—	dB	
AD32b	SFDR	Spurious Free Dynamic Range ⁽³⁾	—	72	—	dB	
AD33b	FNYQ	Input Signal Bandwidth ⁽³⁾	—	550	—	kHz	
AD34b	ENOB	Effective Number of Bits ⁽³⁾	—	9.4	—	bits	

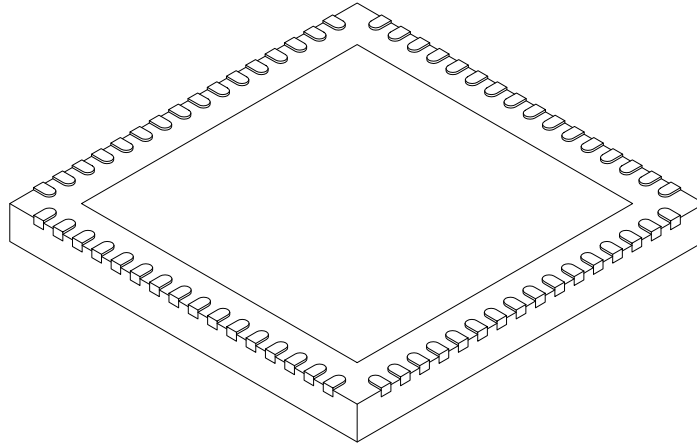
Note 1: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules: ADC, op amp/comparator and comparator voltage reference, may have degraded performance. Refer to Parameter BO10 in Table 33-12 for the minimum and maximum BOR values.

2: For all accuracy specifications, VINL = AVSS = VREFL = 0V and AVDD = VREFH = 3.6V.

3: Parameters are characterized but not tested in manufacturing.

64-Lead Plastic Quad Flat, No Lead Package (MR) – 9x9x0.9 mm Body [QFN] With 7.15 x 7.15 Exposed Pad

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N	64		
Pitch	e	0.50 BSC		
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3	0.20 REF		
Overall Width	E	9.00 BSC		
Exposed Pad Width	E2	7.05	7.15	7.50
Overall Length	D	9.00 BSC		
Exposed Pad Length	D2	7.05	7.15	7.50
Contact Width	b	0.18	0.25	0.30
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Package is saw singulated.
- Dimensioning and tolerancing per ASME Y14.5M.
BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-149C Sheet 2 of 2

dsPIC33EPXXXGM3XX/6XX/7XX

Program Address Space	37	Peripheral Pin Select Input (dsPIC33EPGM60X/7XX Devices)	76
Memory Map for dsPIC33EP128GM3XX/6XX/7XX Devices	37	Peripheral Pin Select Input (dsPIC33EPXXXGM3XX Devices)	77
Memory Map for dsPIC33EP256GM3XX/6XX/7XX Devices	38	Peripheral Pin Select Output (dsPIC33EPXXXGM304/604 Devices)	74
Memory Map for dsPIC33EP512GM3XX/6XX/7XX Devices	39	Peripheral Pin Select Output (dsPIC33EPXXXGM306/706 Devices)	74
Program Memory		Peripheral Pin Select Output (dsPIC33EPXXXGM310/710 Devices)	75
Organization	40	PMD (dsPIC33EPXXXGM3XX Devices)	80
Reset Vector	40	PMD (dsPIC33EPXXXGM6XX/7XX Devices)	79
Program Space		PORTA (dsPIC33EPXXXGM304/604 Devices)	84
Address Construction	101	PORTA (dsPIC33EPXXXGM306/706 Devices)	84
Data Access from Program Memory Using Table Instructions	102	PORTA (dsPIC33EPXXXGM310/710 Devices)	84
Table Read Instructions		PORTB (dsPIC33EPXXXGM304/604 Devices)	85
TBLRDH	102	PORTB (dsPIC33EPXXXGM306/706 Devices)	85
TBLRDL	102	PORTB (dsPIC33EPXXXGM310/710 Devices)	85
Programmable CRC		PORTC (dsPIC33EPXXXGM304/604 Devices)	86
Control Registers	407	PORTC (dsPIC33EPXXXGM306/706 Devices)	86
Overview	406	PORTC (dsPIC33EPXXXGM310/710 Devices)	86
Setup Examples	406	PORTD (dsPIC33EPXXXGM306/706 Devices)	87
Programmable Cyclic Redundancy Check (CRC)		PORTD (dsPIC33EPXXXGM310/710 Devices)	87
Generator	405	PORTE (dsPIC33EPXXXGM306/706 Devices)	88
PTG		PORTE (dsPIC33EPXXXGM310/710 Devices)	87
Control Registers	351	PORTF (dsPIC33EPXXXGM306/706 Devices)	88
Introduction	349	PORTF (dsPIC33EPXXXGM310/710 Devices)	88
Output Descriptions	364	PORTG (dsPIC33EPXXXGM306/706 Devices)	89
Step Commands and Format	361	PORTG (dsPIC33EPXXXGM310/710 Devices)	89
Q		Programmable CRC	73
Quadrature Encoder Interface (QEI)	257	PTG	56
Control Registers	259	PWM	57
R		PWM Generator 1	57
Real-Time Clock and Calendar (RTCC)	383	PWM Generator 2	58
Referenced Sources	13	PWM Generator 3	58
Register		PWM Generator 4	59
PTGADJ (PTG Adjust)	359	PWM Generator 5	59
PTGL0 (PTG Literal 0)	359	PWM Generator 6	60
PTGQPTR (PTG Step Queue Pointer)	360	QE1	61
PTGQUEX (PTG Step Queue x)	360	QE2	62
Register Maps		Real-Time Clock and Calendar	82
ADC1 and ADC2	66	Reference Clock	78
CAN1 (When WIN (C1CTRL) = 0 or 1)	68	SPI1, SPI2 and SPI3	64
CAN1 (When WIN (C1CTRL) = 0)	68	System Control	78
CAN1 (When WIN (C1CTRL) = 1)	69	Timers	52
CAN2 (When WIN (C1CTRL) = 0 or 1)	70	UART1 and UART2	63
CAN2 (When WIN (C1CTRL) = 0)	71	UART3 and UART4	64
CAN2 (When WIN (C1CTRL) = 1)	72	Registers	
Configuration Byte	412	ADxCHS0 (ADCx Input Channel 0 Select)	338
CPU Core	46	ADxCHS123 (ADCx Input Channel 1, 2, 3 Select)	337
CTMU	82	ADxCON1 (ADCx Control 1)	331
DCI	65	ADxCON2 (ADCx Control 2)	333
DMA Controller	83	ADxCON3 (ADCx Control 3)	335
I2C1 and I2C2	63	ADxCON4 (ADCx Control 4)	336
Input Capture 1-8	53	ADxCSSH (ADCx Input Scan Select High)	340
Interrupt Controller (dsPIC33EPXXXGM3XX Devices)	50	ADxCSSL (ADCx Input Scan Select Low)	342
Interrupt Controller (dsPIC33EPXXXGM6XX/7XX Devices)	48	ALCFGRPT (Alarm Configuration)	388
JTAG Interface	82	ALRMVAL (Alarm Minutes and Seconds Value, ALRMPTR = 00)	393
NVM	78	ALRMVAL (Alarm Month and Day Value, ALRMPTR = 10)	391
Op Amp/Comparator	81	ALRMVAL (Alarm Weekday and Hours Value, ALRMPTR = 01)	392
Output Compare	54	ALTDTRx (PWMx Alternate Dead-Time)	246
Pad Configuration	89		
Parallel Master/Slave Port	79		