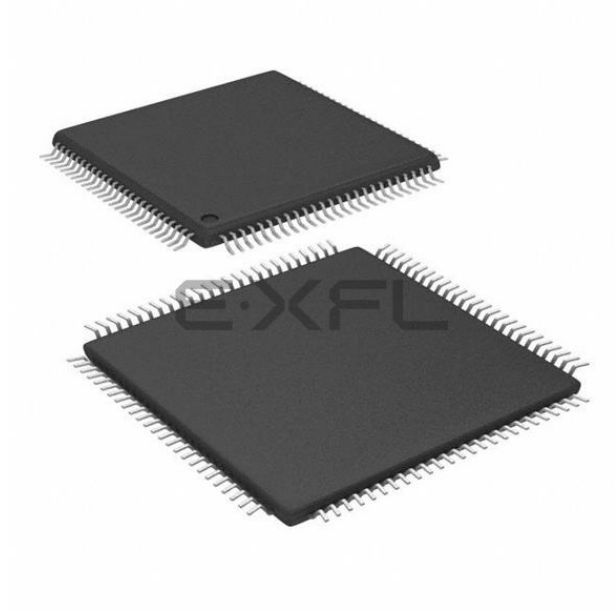
Microchip Technology - DSPIC33EP512GM710-H/PT Datasheet



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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	-
Connectivity	CANbus, I²C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, Motor Control PWM, POR, PWM, WDT
Number of I/O	85
Program Memory Size	512KB (170K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	-
Data Converters	A/D 49x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 150°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep512gm710-h-pt

2.5 ICSP Pins

The PGECx and PGEDx pins are used for ICSP and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of Ohms, not to exceed 100 Ohms.

Pull-up resistors, series diodes and capacitors on the PGECx and PGEDx pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin Voltage Input High (V_{IH}) and Voltage Input Low (V_{IL}) requirements.

Ensure that the "Communication Channel Select" (i.e., PGECx/PGEDx pins) programmed into the device matches the physical connections for the ICSP to MPLAB® PICkit™ 3, MPLAB ICD 3, or MPLAB REAL ICE™.

For more information on MPLAB ICD 2, ICD 3 and REAL ICE connection requirements, refer to the following documents that are available on the Microchip web site:

- *"Using MPLAB® ICD 3"* (poster) DS51765
- *"MPLAB® ICD 3 Design Advisory"* DS51764
- *"MPLAB® REAL ICE™ In-Circuit Emulator User's Guide"* DS51616
- *"Using MPLAB® REAL ICE™ In-Circuit Emulator"* (poster) DS51749

2.6 External Oscillator Pins

Many DSCs have options for at least two oscillators: a high-frequency primary oscillator and a low-frequency secondary oscillator. For details, see **Section 9.0 "Oscillator Configuration"** for details.

The oscillator circuit should be placed on the same side of the board as the device. Also, place the oscillator circuit close to the respective oscillator pins, not exceeding one-half inch (12 mm) distance between them. The load capacitors should be placed next to the oscillator itself, on the same side of the board. Use a grounded copper pour around the oscillator circuit to isolate them from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed. A suggested layout is shown in Figure 2-3.

FIGURE 2-3: SUGGESTED PLACEMENT OF THE OSCILLATOR CIRCUIT

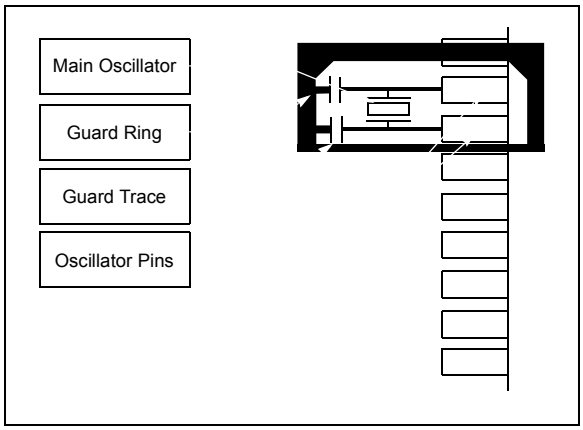
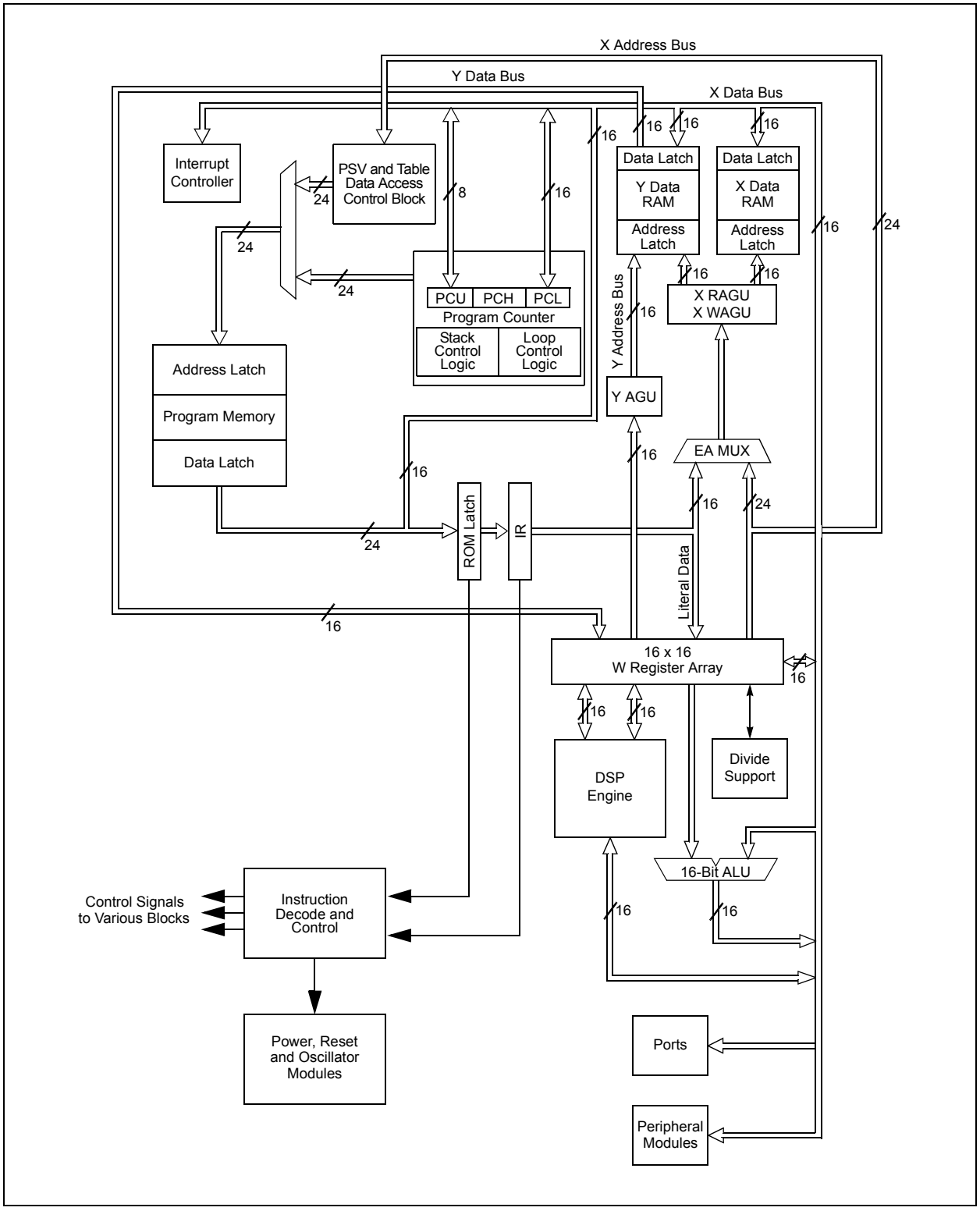


FIGURE 3-1: dsPIC33EPXXXGM3XX/6XX/7XX CPU BLOCK DIAGRAM



3.6 CPU Control Registers

REGISTER 3-1: SR: CPU STATUS REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/C-0	R/C-0	R-0	R/W-0
OA	OB	SA(3)	SB(3)	OAB	SAB	DA	DC
bit 15							bit 8

R/W-0(2)	R/W-0(2)	R/W-0(2)	R-0	R/W-0	R/W-0	R/W-0	R/W-0
IPL2(1)	IPL1(1)	IPL0(1)	RA	N	OV	Z	C
bit 7							bit 0

Legend:	C = Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **OA:** Accumulator A Overflow Status bit
1 = Accumulator A has overflowed
0 = Accumulator A has not overflowed

bit 14 **OB:** Accumulator B Overflow Status bit
1 = Accumulator B has overflowed
0 = Accumulator B has not overflowed

bit 13 **SA:** Accumulator A Saturation 'Sticky' Status bit(3)
1 = Accumulator A is saturated or has been saturated at some time
0 = Accumulator A is not saturated

bit 12 **SB:** Accumulator B Saturation 'Sticky' Status bit(3)
1 = Accumulator B is saturated or has been saturated at some time
0 = Accumulator B is not saturated

bit 11 **OAB:** OA || OB Combined Accumulator Overflow Status bit
1 = Accumulator A or B has overflowed
0 = Neither Accumulator A or B has overflowed

bit 10 **SAB:** SA || SB Combined Accumulator 'Sticky' Status bit
1 = Accumulator A or B is saturated or has been saturated at some time
0 = Neither Accumulator A or B is saturated

bit 9 **DA:** DO Loop Active bit
1 = DO loop in progress
0 = DO loop not in progress

bit 8 **DC:** MCU ALU Half Carry/$\overline{\text{Borrow}}$ bit
1 = A carry-out from the 4th low-order bit (for byte-sized data) or 8th low-order bit (for word-sized data) of the result occurred
0 = No carry-out from the 4th low-order bit (for byte-sized data) or 8th low-order bit (for word-sized data) of the result occurred

Note 1: The IPL<2:0> bits are concatenated with the IPL<3> bit (CORCON<3>) to form the CPU Interrupt Priority Level. The value in parentheses indicates the IPL, if IPL<3> = 1. User interrupts are disabled when IPL<3> = 1.

2: The IPL<2:0> Status bits are read-only when the NSTDIS bit (INTCON1<15>) = 1.

3: A data write to the SR register can modify the SA and SB bits by either a data write to SA and SB or by clearing the SAB bit. To avoid a possible SA or SB bit write race condition, the SA and SB bits should not be modified using bit operations.

REGISTER 3-1: SR: CPU STATUS REGISTER (CONTINUED)

bit 7-5 **IPL<2:0>:** CPU Interrupt Priority Level Status bits(1,2)

111 = CPU Interrupt Priority Level is 7 (15); user interrupts are disabled
110 = CPU Interrupt Priority Level is 6 (14)
101 = CPU Interrupt Priority Level is 5 (13)
100 = CPU Interrupt Priority Level is 4 (12)
011 = CPU Interrupt Priority Level is 3 (11)
010 = CPU Interrupt Priority Level is 2 (10)
001 = CPU Interrupt Priority Level is 1 (9)
000 = CPU Interrupt Priority Level is 0 (8)

bit 4 **RA:** REPEAT Loop Active bit

1 = REPEAT loop is in progress
0 = REPEAT loop is not in progress

bit 3 **N:** MCU ALU Negative bit

1 = Result was negative
0 = Result was non-negative (zero or positive)

bit 2 **OV:** MCU ALU Overflow bit

This bit is used for signed arithmetic (2's complement). It indicates an overflow of the magnitude that causes the sign bit to change state.
1 = Overflow occurred for signed arithmetic (in this arithmetic operation)
0 = No overflow occurred

bit 1 **Z:** MCU ALU Zero bit

1 = An operation that affects the Z bit has set it at some time in the past
0 = The most recent operation that affects the Z bit has cleared it (i.e., a non-zero result)

bit 0 **C:** MCU ALU Carry/$\overline{\text{Borrow}}$ bit

1 = A carry-out from the Most Significant bit (MSb) of the result occurred
0 = No carry-out from the Most Significant bit of the result occurred

Note 1: The IPL<2:0> bits are concatenated with the IPL<3> bit (CORCON<3>) to form the CPU Interrupt Priority Level. The value in parentheses indicates the IPL, if IPL<3> = 1. User interrupts are disabled when IPL<3> = 1.

2: The IPL<2:0> Status bits are read-only when the NSTDIS bit (INTCON1<15>) = 1.

3: A data write to the SR register can modify the SA and SB bits by either a data write to SA and SB or by clearing the SAB bit. To avoid a possible SA or SB bit write race condition, the SA and SB bits should not be modified using bit operations.

TABLE 4-58: PORTE REGISTER MAP FOR dsPIC33EPXXXGM306/706 DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISE	0E40	TRISE<15:12>				—	—	—	—	—	—	—	—	—	—	—	—	F000
PORTE	0E42	RE<15:12>				—	—	—	—	—	—	—	—	—	—	—	—	xxxx
LATE	0E44	LATE<15:12>				—	—	—	—	—	—	—	—	—	—	—	—	xxxx
ODCE	0E46	ODCE<15:12>				—	—	—	—	—	—	—	—	—	—	—	—	0000
CNENE	0E48	CNIEE<15:12>				—	—	—	—	—	—	—	—	—	—	—	—	0000
CNPUE	0E4A	CNPUE<15:12>				—	—	—	—	—	—	—	—	—	—	—	—	0000
CNPDE	0E4C	CNPDE<15:12>				—	—	—	—	—	—	—	—	—	—	—	—	0000
ANSELE	0E4E	ANSE<15:12>				—	—	—	—	—	—	—	—	—	—	—	—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-59: PORTF REGISTER MAP FOR dsPIC33EPXXXGM310/710 DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISF	0E50	—	—	TRISF<13:12>		—	TRISF<10:9>		—	TRISF<7:4>				—	—	TRISF<1:0>		F303
PORTF	0E52	—	—	RF<13:12>		—	RF<10:9>		—	RF<7:4>				—	—	RF<1:0>		xxxx
LATF	0E54	—	—	LATF<13:12>		—	LATF<10:9>		—	LATF<7:4>				—	—	LATF<1:0>		xxxx
ODCF	0E56	—	—	ODCF<13:12>		—	ODCF<10:9>		—	ODCF<7:4>				—	—	ODCF<1:0>		0000
CNENF	0E58	—	—	CNIEF<13:12>		—	CNIEF<10:9>		—	CNIEF<7:4>				—	—	CNIEF<1:0>		0000
CNPUF	0E5A	—	—	CNPUF<13:12>		—	CNPUF<10:9>		—	CNPUF<7:4>				—	—	CNPUF<1:0>		0000
CNPDF	0E5C	—	—	CNPDF<13:12>		—	CNPDF<10:9>		—	CNPDF<7:4>				—	—	CNPDF<1:0>		0000
ANSELF	0E4E	—	—	ANSF<13:12>		—	ANSF<10:9>		—	—	—	ANSF<5:4>		—	—	—	—	0000

Legend: x = unknown value on Reset, — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-60: PORTF REGISTER MAP FOR dsPIC33EPXXXGM306/706 DEVICES

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TRISF	0E50	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TRISF<1:0>		0003
PORTF	0E52	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RF<1:0>		xxxx
LATF	0E54	—	—	—	—	—	—	—	—	—	—	—	—	—	—	LATF<1:0>		xxxx
ODCF	0E56	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ODCF<1:0>		0000
CNENF	0E58	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CNIEF<1:0>		0000
CNPUF	0E5A	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CNPUF<1:0>		0000
CNPDF	0E5C	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0000

Legend: x = unknown value on Reset; — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 9-1: CONFIGURATION BIT VALUES FOR CLOCK SELECTION

Oscillator Mode	Oscillator Source	POSCMD<1:0>	FNOSC<2:0>	See Notes
Fast RC Oscillator with Divide-by-N (FRCDIVN)	Internal	xx	111	**1, 2**
Fast RC Oscillator with Divide-by-16 (FRCDIV16)	Internal	xx	110	**1**
Low-Power RC Oscillator (LPRC)	Internal	xx	101	**1**
Secondary (Timer1) Oscillator (SOSC)	Secondary	xx	100	**1**
Primary Oscillator (HS) with PLL (HSPLL)	Primary	10	011	
Primary Oscillator (XT) with PLL (XTPLL)	Primary	01	011	
Primary Oscillator (EC) with PLL (ECPLL)	Primary	00	011	**1**
Primary Oscillator (HS)	Primary	10	010	
Primary Oscillator (XT)	Primary	01	010	
Primary Oscillator (EC)	Primary	00	010	**1**
Fast RC Oscillator (FRC) with Divide-by-N and PLL (FRCPLL)	Internal	xx	001	**1**
Fast RC Oscillator (FRC)	Internal	xx	000	**1**

Note 1: OSC2 pin function is determined by the OSCIOFNC Configuration bit.

2: This is the default oscillator mode for an unprogrammed (erased) device.

REGISTER 9-2: CLKDIV: CLOCK DIVISOR REGISTER(2)

R/W-0	R/W-0	R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0
ROI	DOZE2(3)	DOZE1(3)	DOZE0(3)	DOZEN(1,4)	FRCDIV2	FRCDIV1	FRCDIV0
bit 15							bit 8

R/W-0	R/W-1	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PLLPOST1	PLLPOST0	—	PLLPRE4	PLLPRE3	PLLPRE2	PLLPRE1	PLLPRE0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **ROI:** Recover on Interrupt bit
1 = Interrupts will clear the DOZEN bit
0 = Interrupts will have no effect on the DOZEN bit

bit 14-12 **DOZE<2:0>:** Processor Clock Reduction Select bits(3)
111 = FCY divided by 128
110 = FCY divided by 64
101 = FCY divided by 32
100 = FCY divided by 16
011 = FCY divided by 8 (default)
010 = FCY divided by 4
001 = FCY divided by 2
000 = FCY divided by 1

bit 11 **DOZEN:** Doze Mode Enable bit(1,4)
1 = DOZE<2:0> field specifies the ratio between the peripheral clocks and the processor clocks
0 = Processor clock and peripheral clock ratio are forced to 1:1

bit 10-8 **FRCDIV<2:0>:** Internal Fast RC Oscillator Postscaler bits
111 = FRC divided by 256
110 = FRC divided by 64
101 = FRC divided by 32
100 = FRC divided by 16
011 = FRC divided by 8
010 = FRC divided by 4
001 = FRC divided by 2
000 = FRC divided by 1 (default)

bit 7-6 **PLLPOST<1:0>:** PLL VCO Output Divider Select bits (also denoted as 'N2', PLL postscaler)
11 = Output divided by 8
10 = Reserved
01 = Output divided by 4 (default)
00 = Output divided by 2

bit 5 **Unimplemented:** Read as '0'

Note 1: This bit is cleared when the ROI bit is set and an interrupt occurs.

2: This register resets only on a Power-on Reset (POR).

3: The DOZE<2:0> bits can only be written to when the DOZEN bit is clear. If DOZEN = 1, any writes to DOZE<2:0> are ignored.

4: The DOZEN bit cannot be set if DOZE<2:0> = 000. If DOZE<2:0> = 000, any attempt by user software to set the DOZEN bit is ignored.

TABLE 11-1: SELECTABLE INPUT SOURCES (MAPS INPUT TO FUNCTION)

Input Name(1)	Function Name	Register	Configuration Bits
External Interrupt 1	INT1	RPINR0	INT1R<6:0>
External Interrupt 2	INT2	RPINR1	INT2R<6:0>
Timer2 External Clock	T2CK	RPINR3	T2CKR<6:0>
Input Capture 1	IC1	RPINR7	IC1R<6:0>
Input Capture 2	IC2	RPINR7	IC2R<6:0>
Input Capture 3	IC3	RPINR8	IC3R<6:0>
Input Capture 4	IC4	RPINR8	IC4R<6:0>
Input Capture 5	IC5	RPINR9	IC5R<6:0>
Input Capture 6	IC6	RPINR9	IC6R<6:0>
Input Capture 7	IC7	RPINR10	IC7R<6:0>
Input Capture 8	IC8	RPINR10	IC8R<6:0>
Output Compare Fault A	OCFA	RPINR11	OCFAR<6:0>
PWM Fault 1	FLT1	RPINR12	FLT1R<6:0>
PWM Fault 2	FLT2	RPINR12	FLT2R<6:0>
QEI1 Phase A	QEA1	RPINR14	QEA1R<6:0>
QEI1 Phase B	QEB1	RPINR14	QEB1R<6:0>
QEI1 Index	INDX1	RPINR 15	INDX1R<6:0>
QEI1 Home	HOME1	RPINR15	HOM1R<6:0>
QEI2 Phase A	QEA2	RPINR16	QEA2R<6:0>
QEI2 Phase B	QEB2	RPINR16	QEB2R<6:0>
QEI2 Index	INDX2	RPINR17	INDX2R<6:0>
QEI2 Home	HOME2	RPINR17	HOM2R<6:0>
UART1 Receive	U1RX	RPINR18	U1RXR<6:0>
UART2 Receive	U2RX	RPINR19	U2RXR<6:0>
SPI2 Data Input	SDI2	RPINR22	SDI2R<6:0>
SPI2 Clock Input	SCK2	RPINR22	SCK2R<6:0>
SPI2 Slave Select	$\overline{SS2}$	RPINR23	SS2R<6:0>
DCI Data Input	CSDI	RPINR24	CSDIR>6:0>
DCI Clock Input	CSCK	RPINR24	CSCKR<6:0>
DCI Frame Synchronization Input	COFS	RPINR25	COFSR<6:0>
CAN1 Receive(2)	C1RX	RPINR26	C1RXR<6:0>
CAN2 Receive(2)	C2RX	RPINR26	C2RXR<6:0>
UART3 Receive	U3RX	RPINR27	U3RXR<6:0>
UART3 Clear-to-Send	$\overline{U3CTS}$	RPINR27	U3CTSR<6:0>
UART4 Receive	U4RX	RPINR28	U4RXR<6:0>
UART4 Clear-to-Send	$\overline{U4CTS}$	RPINR28	U4CTSR<6:0>
SPI3 Data Input	SDI3	RPINR29	SDI3R<6:0>
SPI3 Clock Input	SCK3	RPINR29	SCK3R<6:0>
SPI3 Slave Select	$\overline{SS3}$	RPINR 30	SS3R<6:0>

Note 1: Unless otherwise noted, all inputs use the Schmitt Trigger input buffers.

2: This input is available on dsPIC33EPXXXGM6XX/7XX devices only.

12.0 TIMER1

Note 1: This data sheet summarizes the features of the dsPIC33EPXXXGM3XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"Timers"** (DS70362), which is available from the Microchip web site (www.microchip.com).

2: Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The Timer1 module is a 16-bit timer that can operate as a free-running, interval timer/counter.

The Timer1 module has the following unique features over other timers:

- Can be operated in Asynchronous Counter mode from an external clock source
- The external clock input (T1CK) can optionally be synchronized to the internal device clock and the clock synchronization is performed after the prescaler

A block diagram of Timer1 is shown in Figure 12-1.

The Timer1 module can operate in one of the following modes:

- Timer mode
- Gated Timer mode
- Synchronous Counter mode
- Asynchronous Counter mode

In Timer and Gated Timer modes, the input clock is derived from the internal instruction cycle clock (FCY). In Synchronous and Asynchronous Counter modes, the input clock is derived from the external clock input at the T1CK pin.

The Timer modes are determined by the following bits:

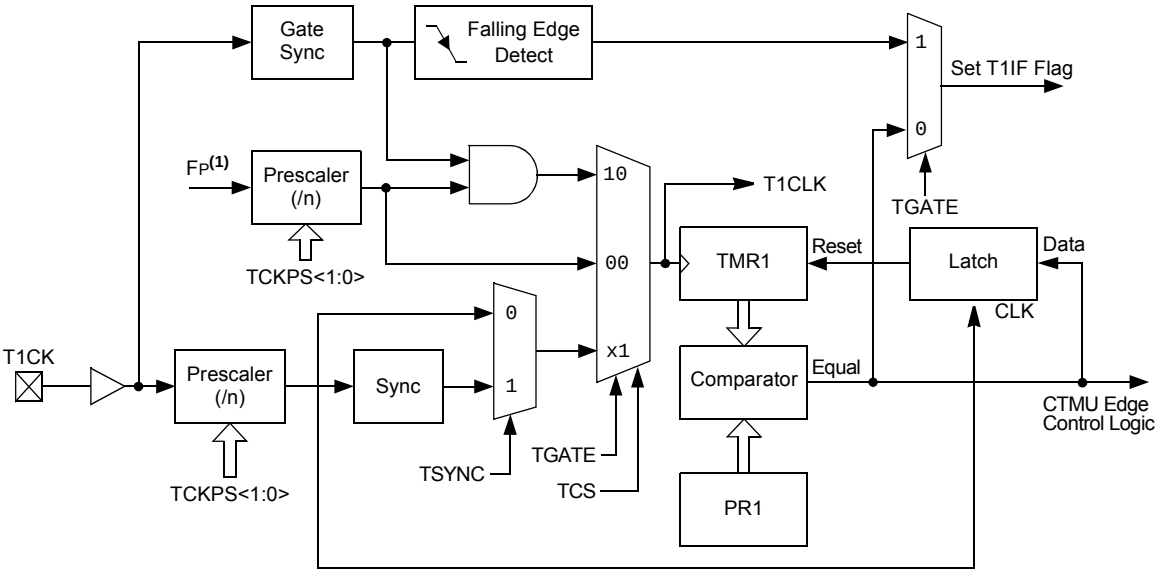
- Timer Clock Source Control bit (TCS): T1CON<1>
- Timer Synchronization Control bit (TSYNC): T1CON<2>
- Timer Gate Control bit (TGATE): T1CON<6>

Timer control bit settings for different operating modes are given in the Table 12-1.

TABLE 12-1: TIMER MODE SETTINGS

Mode	TCS	TGATE	TSYNC
Timer	0	0	x
Gated Timer	0	1	x
Synchronous Counter	1	x	1
Asynchronous Counter	1	x	0

FIGURE 12-1: 16-BIT TIMER1 MODULE BLOCK DIAGRAM



Note 1: FP is the peripheral clock.

REGISTER 23-6: ADxCHS0: ADCx INPUT CHANNEL 0 SELECT REGISTER(3)

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CH0NB	—	CH0SB5(1,4,5)	CH0SB4(1,5)	CH0SB3(1,5)	CH0SB2(1,5)	CH0SB1(1,5)	CH0SB0(1,5)
bit 15							bit 8

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CH0NA	—	CH0SA5(1,4,5)	CH0SA4(1,5)	CH0SA3(1,5)	CH0SA2(1,5)	CH0SA1(1,5)	CH0SA0(1,5)
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **CH0NB:** Channel 0 Negative Input Select for Sample MUXB bit
1 = Channel 0 negative input is AN1(1)
0 = Channel 0 negative input is VREFL

bit 14 **Unimplemented:** Read as '0'

bit 13-8 **CH0SB<5:0>:** Channel 0 Positive Input Select for Sample MUXB bits(1,4,5)
111111 = Channel 0 positive input is (AN63) unconnected
111110 = Channel 0 positive input is (AN62) the CTMU temperature voltage
111101 = Channel 0 positive input is (AN61) reserved
•
•
•
110010 = Channel 0 positive input is (AN50) reserved
110001 = Channel 0 positive input is AN49
110000 = Channel 0 positive input is AN48
101111 = Channel 0 positive input is AN47
101110 = Channel 0 positive input is AN46
•
•
•
011010 = Channel 0 positive input is AN26
011001 = Channel 0 positive input is AN25 or Op Amp 5 output voltage(2)
011000 = Channel 0 positive input is AN24
•
•
•
000111 = Channel 0 positive input is AN7
000110 = Channel 0 positive input is AN6 or Op Amp 3 output voltage(2)
000101 = Channel 0 positive input is AN5
000100 = Channel 0 positive input is AN4
000011 = Channel 0 positive input is AN3 or Op Amp 1 output voltage(2)
000010 = Channel 0 positive input is AN2
000001 = Channel 0 positive input is AN1
000000 = Channel 0 positive input is AN0 or Op Amp 2 output voltage(2)

Note 1: AN0 through AN7 are repurposed when comparator and op amp functionality are enabled. See Figure 23-1 to determine how enabling a particular op amp or comparator affects selection choices for Channels 1, 2 and 3.

2: If the op amp is selected (OPMODE bit (CMxCON<10>) = 1), the OAx input is used; otherwise, the ANx input is used.

3: See the **"Pin Diagrams"** section for the available analog channels for each device.

4: Analog input selections for ADC1 are shown here. AN32-AN63 selections are not available for ADC2. The CH0SB5 and CH0SA5 bits are 'Reserved' for ADC2 and should be programmed to '0'.

5: Analog inputs, AN32-AN49, are available only when the ADCx is working in 10-bit mode.

REGISTER 25-1: PTGCST: PTG CONTROL/STATUS REGISTER (CONTINUED)

bit 1-0 **PTGITM<1:0>:** PTG Input Trigger Command Operating Mode bits(1)

11 = Single level detect with step delay is not executed on exit of command (regardless of PTGCTRL command)
10 = Single level detect with step delay is executed on exit of command
01 = Continuous edge detect with step delay is not executed on exit of command (regardless of PTGCTRL command)
00 = Continuous edge detect with step delay is executed on exit of command

Note 1: These bits apply to the PTGWHI and PTGWLO commands only.

2: This bit is only used with the PTGCTRL Step command software trigger option.

Most instructions are a single word. Certain double-word instructions are designed to provide all the required information in these 48 bits. In the second word, the 8 MSbs are '0's. If this second word is executed as an instruction (by itself), it executes as a NOP.

The double-word instructions execute in two instruction cycles.

Most single-word instructions are executed in a single instruction cycle, unless a conditional test is true, or the Program Counter is changed as a result of the instruction, or a PSV or Table Read is performed. In these cases, the execution takes multiple instruction cycles with the additional instruction cycle(s) executed as a NOP. Certain instructions that involve skipping over the subsequent instruction require either two or three cycles if the skip is performed, depending on whether the instruction being skipped is a single-word or two-word instruction. Moreover, double-word moves require two cycles.

Note: For more details on the instruction set, refer to the *"16-bit MCU and DSC Programmer's Reference Manual"* (DS70157).

TABLE 31-1: SYMBOLS USED IN OPCODE DESCRIPTIONS

Field	Description
#text	Means literal defined by "text"
(text)	Means "content of text"
[text]	Means "the location addressed by text"
{ }	Optional field or operation
a ∈ {b, c, d}	a is selected from the set of values b, c, d
<n:m>	Register bit field
.b	Byte mode selection
.d	Double-Word mode selection
.S	Shadow register select
.w	Word mode selection (default)
Acc	One of two accumulators {A, B}
AWB	Accumulator write back destination address register ∈ {W13, [W13]+ = 2}
bit4	4-bit bit selection field (used in word addressed instructions) ∈ {0...15}
C, DC, N, OV, Z	MCU Status bits: Carry, Digit Carry, Negative, Overflow, Sticky Zero
Expr	Absolute address, label or expression (resolved by the linker)
f	File register address ∈ {0x0000...0x1FFF}
lit1	1-bit unsigned literal ∈ {0,1}
lit4	4-bit unsigned literal ∈ {0...15}
lit5	5-bit unsigned literal ∈ {0...31}
lit8	8-bit unsigned literal ∈ {0...255}
lit10	10-bit unsigned literal ∈ {0...255} for Byte mode, {0:1023} for Word mode
lit14	14-bit unsigned literal ∈ {0...16384}
lit16	16-bit unsigned literal ∈ {0...65535}
lit23	23-bit unsigned literal ∈ {0...8388608}; LSb must be '0'
None	Field does not require an entry, can be blank
OA, OB, SA, SB	DSP Status bits: ACCA Overflow, ACCB Overflow, ACCA Saturate, ACCB Saturate
PC	Program Counter
Slit10	10-bit signed literal ∈ {-512...511}
Slit16	16-bit signed literal ∈ {-32768...32767}
Slit6	6-bit signed literal ∈ {-16...16}
Wb	Base W register ∈ {W0...W15}
Wd	Destination W register ∈ { Wd, [Wd], [Wd++], [Wd--], [++Wd], [--Wd] }
Wdo	Destination W register ∈ { Wnd, [Wnd], [Wnd++], [Wnd--], [++Wnd], [--Wnd], [Wnd+Wb] }
Wm,Wn	Dividend, Divisor Working register pair (direct addressing)

TABLE 33-13: DC CHARACTERISTICS: PROGRAM MEMORY

DC CHARACTERISTICS			Standard Operating Conditions: VBOR (min)V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
		Program Flash Memory					
D130	EP	Cell Endurance	10,000	—	—	E/W	-40°C to +125°C
D131	VPR	VDD for Read	VBORMIN	—	3.6	V	
D132b	VPEW	VDD for Self-Timed Write	3.0	—	3.6	V	
D134	TRETD	Characteristic Retention	20	—	—	Year	Provided no other specifications are violated, -40°C to +125°C
D135	IDDP	Supply Current During Programming	—	10	—	mA	
D138a	TWW	Word Write Cycle Time	46.5	46.9	47.4	µs	TWW = 346 FRC cycles, TA = +85°C **(Note 2)**
D138b	TWW	Word Write Cycle Time	46.0	—	47.9	µs	TWW = 346 FRC cycles, TA = +125°C **(Note 2)**
D136a	TPE	Row Write Time	0.667	0.673	0.680	ms	TRW = 4965 FRC cycles, TA = +85°C **(Note 2)**
D136b	TPE	Row Write Time	0.660	—	0.687	ms	TRW = 4965 FRC cycles, TA = +125°C **(Note 2)**
D137a	TPE	Page Erase Time	19.6	20	20.1	ms	TPE = 146893 FRC cycles, TA = +85°C **(Note 2)**
D137b	TPE	Page Erase Time	19.5	—	20.3	ms	TPE = 146893 FRC cycles, TA = +125°C **(Note 2)**

Note 1: Data in “Typ” column is at 3.3V, +25°C unless otherwise stated.

2: Other conditions: FRC = 7.3728 MHz, TUN<5:0> = b'011111 (for Min), TUN<5:0> = b'100000 (for Max). This parameter depends on the FRC accuracy (see Table 33-19) and the value of the FRC Oscillator Tuning register.

FIGURE 33-20: SPI2 AND SPI3 SLAVE MODE (FULL-DUPLEX, CKE = 1, CKP = 1, SMP = 0) TIMING CHARACTERISTICS

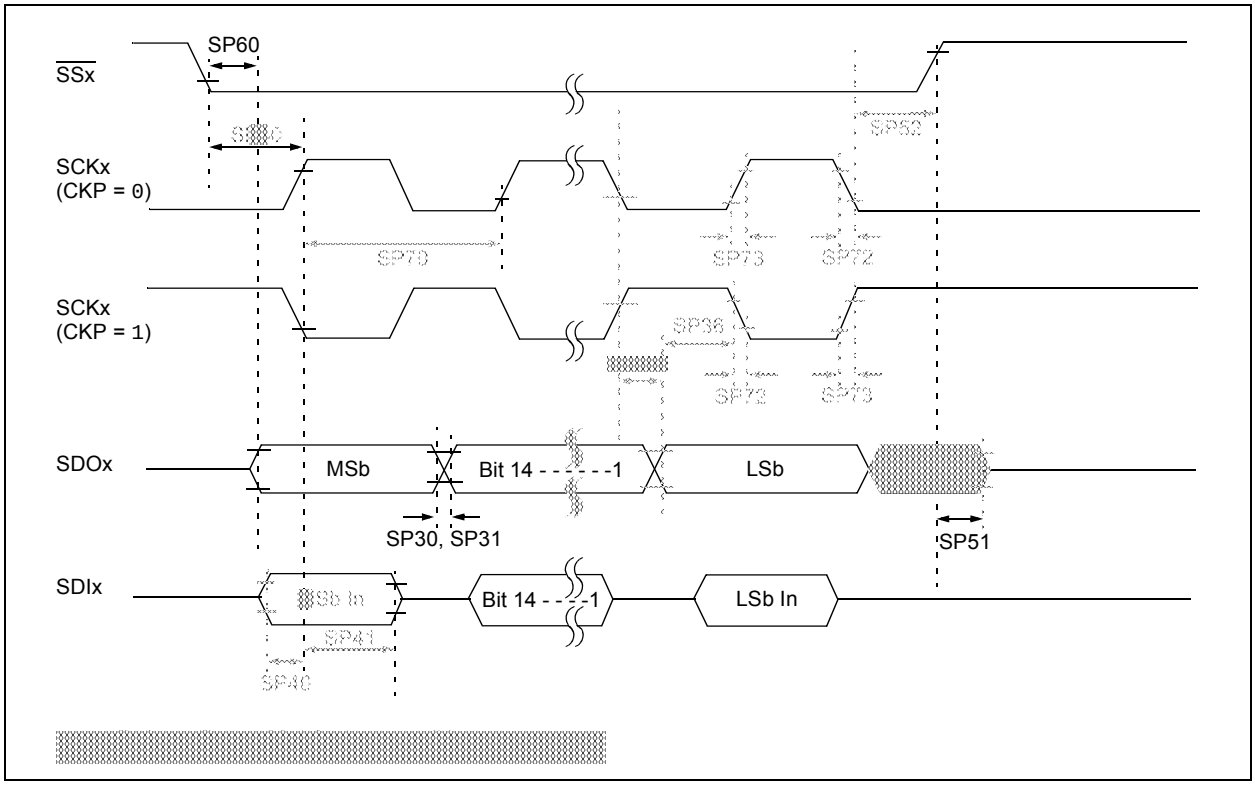


TABLE 33-55: CTMU CURRENT SOURCE SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
CTMU Current Source							
CTMUI1	IOUT1	Base Range	280	550	830	nA	CTMUICON<9:8> = 01
CTMUI2	IOUT2	10x Range	2.8	5.5	8.3	µA	CTMUICON<9:8> = 10
CTMUI3	IOUT3	100x Range	28	55	83	µA	CTMUICON<9:8> = 11
CTMUI4	IOUT4	1000x Range	280	550	830	µA	CTMUICON<9:8> = 00
CTMUFV1	VF		—	0.77	—	V	
CTMUFV2	VFVR		—	-1.38	—	mV/°C	

Note 1: Nominal value at center point of current trim range (CTMUICON<15:10> = 000000).

FIGURE 33-37: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS

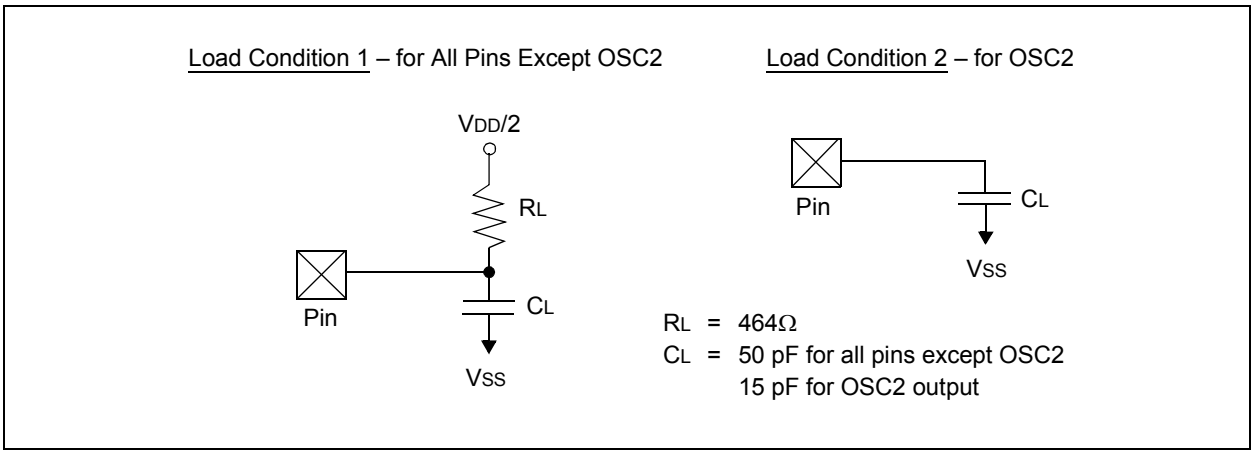


TABLE 33-56: ADCx MODULE SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions (see Note 1): 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Device Supply							
AD01	AVDD	Module VDD Supply	Greater of: VDD – 0.3 or 3.0	—	Lesser of: VDD + 0.3 or 3.6	V	
AD02	AVSS	Module VSS Supply	VSS – 0.3	—	VSS + 0.3	V	
Reference Inputs							
AD05	VREFH	Reference Voltage High	AVSS + 2.7	—	AVDD	V	**(Note 1)** VREFH = VREF+, VREFL = VREF-
AD05a			3.0	—	3.6	V	VREFH = AVDD, VREFL = AVSS = 0
AD06	VREFL	Reference Voltage Low	AVSS	—	AVDD – 2.7	V	**(Note 1)**
AD06a			0	—	0	V	VREFH = AVDD, VREFL = AVSS = 0
AD07	VREF	Absolute Reference Voltage	2.7	—	3.6	V	VREF = VREFH – VREFL
AD08	IREF	Current Drain	— —	— —	10 600	μA μA	ADC off ADC on
AD09	IAD	Operating Current	— —	5 2	— —	mA mA	ADC operating in 10-bit mode **(Note 1)** ADC operating in 12-bit mode **(Note 1)**
Analog Input							
AD12	VINH	Input Voltage Range, VINH	VINL	—	VREFH	V	This voltage reflects Sample-and-Hold Channels 0, 1, 2 and 3 (CH0-CH3), positive input
AD13	VINL	Input Voltage Range, VINL	VREFL	—	AVSS + 1V	V	This voltage reflects Sample-and-Hold Channels 0, 1, 2 and 3 (CH0-CH3), negative input
AD17	RIN	Recommended Impedance of Analog Voltage Source	—	—	200	Ω	Impedance to achieve maximum performance of ADC

Note 1: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules: ADC, op amp/comparator and comparator voltage reference, will have degraded performance. Refer to Parameter BO10 in Table 33-12 for the minimum and maximum BOR values.

TABLE 33-57: ADCx MODULE SPECIFICATIONS (12-BIT MODE)

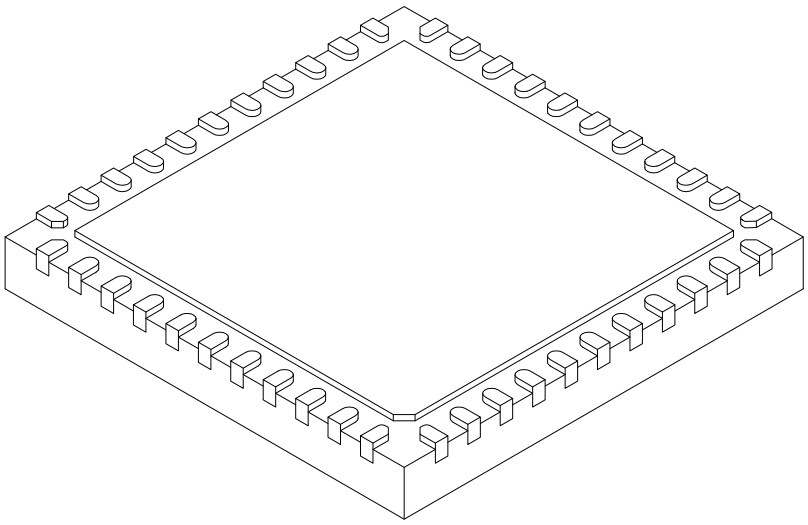
AC CHARACTERISTICS			Standard Operating Conditions (see Note 1): 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
ADC Accuracy (12-Bit Mode) – VREF-							
AD20a	Nr	Resolution	12 data bits			bits	
AD21a	INL	Integral Nonlinearity	-3	—	+3	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V **(Note 2)**
AD22a	DNL	Differential Nonlinearity	≥ 1	—	< 1	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V **(Note 2)**
AD23a	GERR	Gain Error	-10	—	10	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V **(Note 2)**
AD24a	EOFF	Offset Error	-5	—	5	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3.6V **(Note 2)**
AD25a	—	Monotonicity	—	—	—	—	Guaranteed
Dynamic Performance (12-Bit Mode)							
AD30a	THD	Total Harmonic Distortion	—	—	-75	dB	
AD31a	SINAD	Signal to Noise and Distortion	68.5	69.5	—	dB	
AD32a	SFDR	Spurious Free Dynamic Range	80	—	—	dB	
AD33a	FNYQ	Input Signal Bandwidth	—	—	250	kHz	
AD34a	ENOB	Effective Number of Bits	11.09	11.3	—	bits	

Note 1: Device is functional at VBORMIN < VDD < VDDMIN, but will have degraded performance. Device functionality is tested, but not characterized. Analog modules: ADC, op amp/comparator and comparator voltage reference, will have degraded performance. Refer to Parameter BO10 in Table 33-12 for the minimum and maximum BOR values.

2: For all accuracy specifications, VINL = AVSS = VREFL = 0V and AVDD = VREFH = 3.6V.

44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		44	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Width	E		8.00 BSC	
Exposed Pad Width	E2	6.25	6.45	6.60
Overall Length	D		8.00 BSC	
Exposed Pad Length	D2	6.25	6.45	6.60
Terminal Width	b	0.20	0.30	0.35
Terminal Length	L	0.30	0.40	0.50
Terminal-to-Exposed-Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

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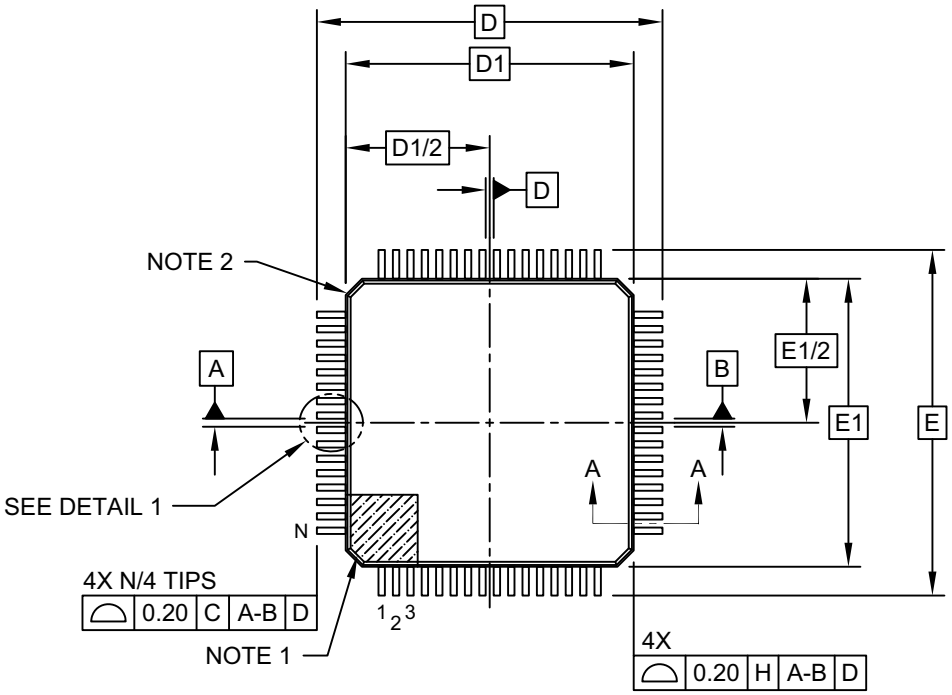
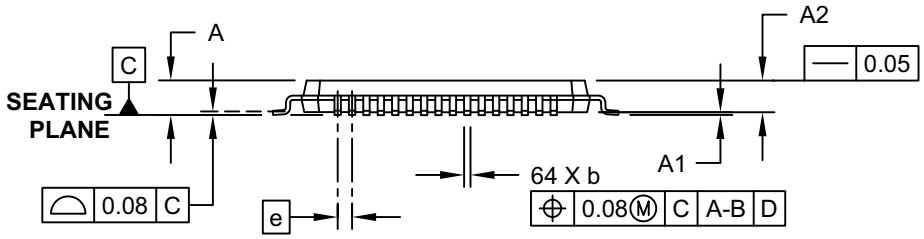
64-Lead Plastic Thin Quad Flatpack (PT)-10x10x1 mm Body, 2.00 mm Footprint [TQFP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

Microchip Technology Drawing C04-085C Sheet 1 of 2

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