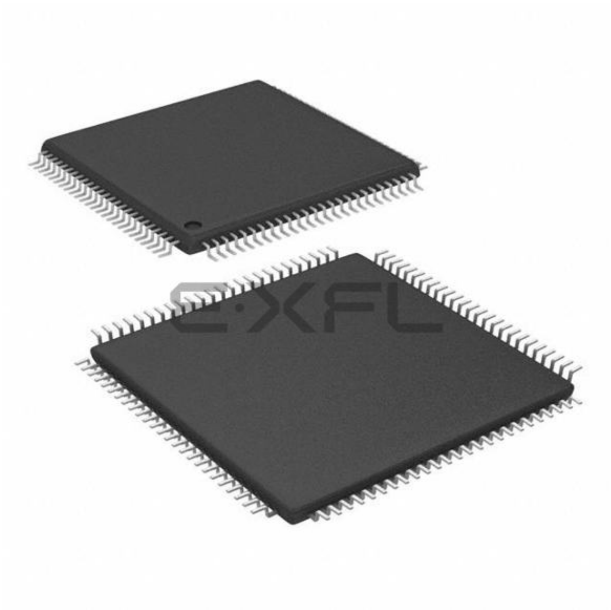
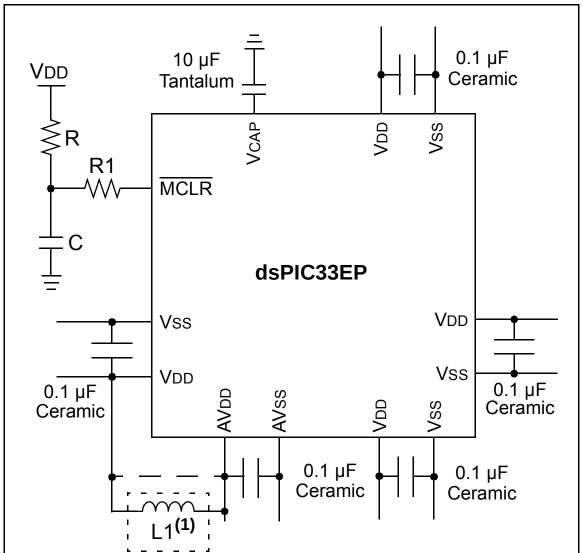


Details	
Product Status	Active
Core Processor	dsPIC
Core Size	16-Bit
Speed	70 MIPs
Connectivity	CANbus, I²C, IrDA, LINbus, QEI, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I²S, Motor Control PWM, POR, PWM, WDT
Number of I/O	85
Program Memory Size	512KB (170K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	-
Data Converters	A/D 49x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-TQFP
Supplier Device Package	100-TQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/dspic33ep512gm710t-i-pf

FIGURE 2-1: RECOMMENDED MINIMUM CONNECTION



Note 1: As an option, instead of a hard-wired connection, an inductor (L1) can be substituted between VDD and AVDD to improve ADC noise rejection. The inductor impedance should be less than 1Ω and the inductor capacity greater than 10 mA.

Where:

$$f = \frac{F_{CNV}}{2}$$ (i.e., ADC Conversion Rate/2)

$$f = \frac{1}{(2\pi\sqrt{LC})}$$

$$L = \left(\frac{1}{(2\pi f\sqrt{C})}\right)^2$$

2.2.1 TANK CAPACITORS

On boards with power traces running longer than six inches in length, it is suggested to use a tank capacitor for integrated circuits including DSCs to supply a local power source. The value of the tank capacitor should be determined based on the trace resistance that connects the power supply source to the device, and the maximum current drawn by the device in the application. In other words, select the tank capacitor so that it meets the acceptable voltage sag at the device. Typical values range from 4.7 µF to 47 µF.

2.3 CPU Logic Filter Capacitor Connection (VCAP)

A low-ESR (< 1 Ohms) capacitor is required on the VCAP pin, which is used to stabilize the voltage regulator output voltage. The VCAP pin must not be connected to VDD, and must have a capacitor greater than 4.7 µF (10 µF is recommended), 16V connected to ground. The type can be ceramic or tantalum. See **Section 33.0 "Electrical Characteristics"** for additional information.

The placement of this capacitor should be close to the VCAP pin. It is recommended that the trace length not exceeds one-quarter inch (6 mm). See **Section 30.3 "On-Chip Voltage Regulator"** for details.

2.4 Master Clear (MCLR) Pin

The MCLR pin provides two specific device functions:

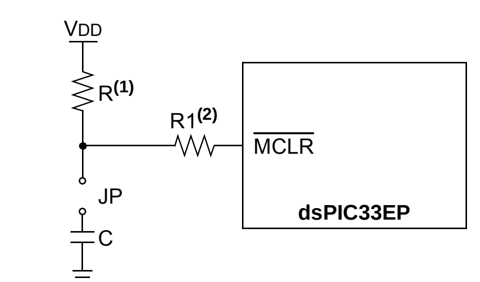
- Device Reset
- Device Programming and Debugging.

During device programming and debugging, the resistance and capacitance that can be added to the pin must be considered. Device programmers and debuggers drive the MCLR pin. Consequently, specific voltage levels (VIH and VIL) and fast signal transitions must not be adversely affected. Therefore, specific values of R and C will need to be adjusted based on the application and PCB requirements.

For example, as shown in Figure 2-2, it is recommended that the capacitor, C, be isolated from the MCLR pin during programming and debugging operations.

Place the components as shown in Figure 2-2 within one-quarter inch (6 mm) from the MCLR pin.

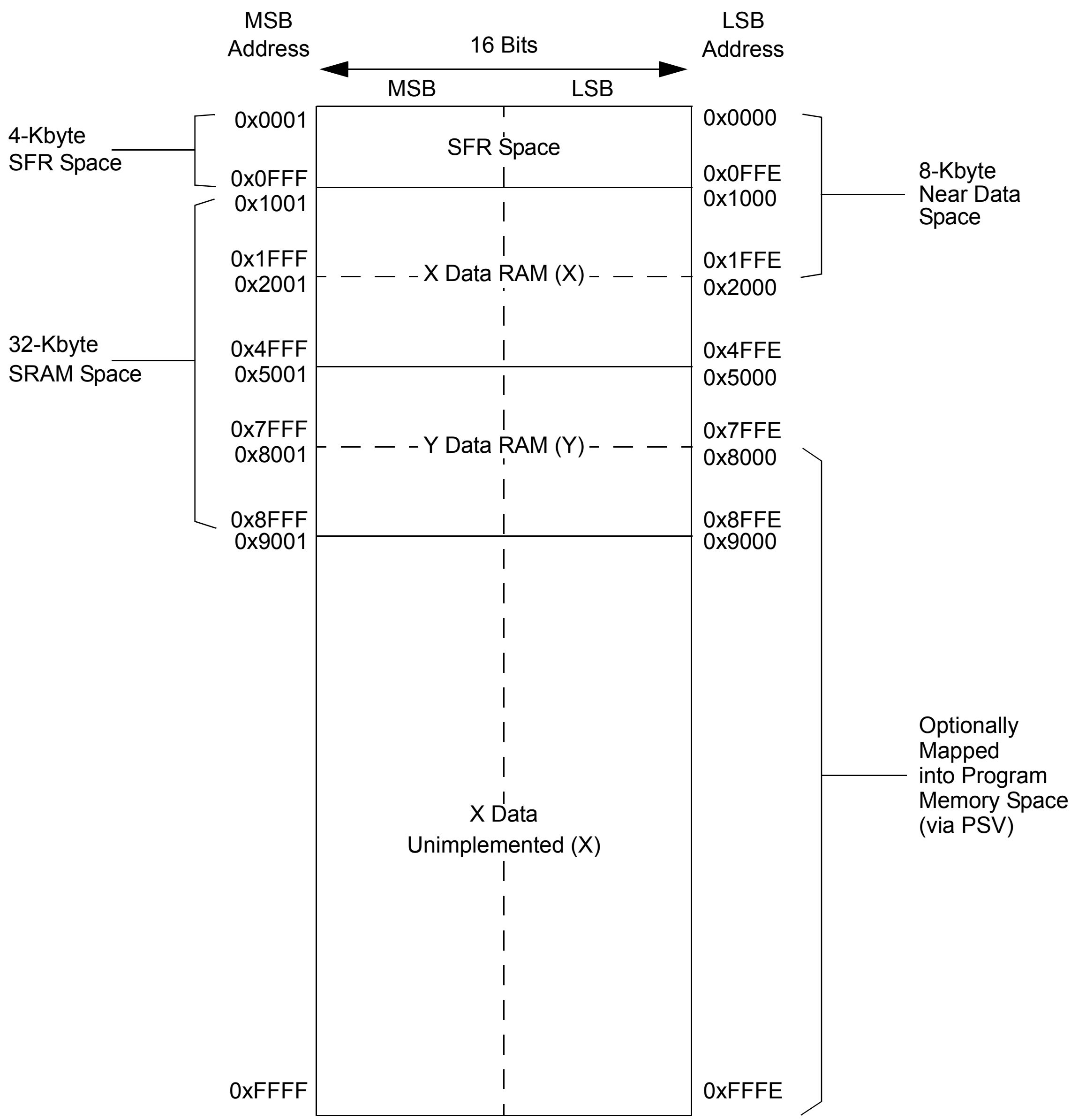
FIGURE 2-2: EXAMPLE OF MCLR PIN CONNECTIONS



Note 1: R ≤ 10 kΩ is recommended. A suggested starting value is 10 kΩ. Ensure that the MCLR pin VIH and VIL specifications are met.

2: R1 ≤ 470Ω will limit any current flowing into MCLR from the external capacitor, C, in the event of MCLR pin breakdown due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS). Ensure that the MCLR pin VIH and VIL specifications are met.

FIGURE 4-6: DATA MEMORY MAP FOR 256-KBYTE DEVICES



Note: Memory areas are not shown to scale.

TABLE 4-7: PTG REGISTER MAP

SFR Name	Addr.	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
PTGCST	0AC0	PTGEN	—	PTGSIDL	PTGTOGL	—	PTGSWT	PTGSSEN	PTGIVIS	PTGSTRT	PTGWDTO	—	—	—	—	PTGITM1	PTGITM0	0000
PTGCON	0AC2	PTGCLK2	PTGCLK1	PTGCLK0	PTGDIV4	PTGDIV3	PTGDIV2	PTGDIV1	PTGDIV0	PTGPWD3	PTGPWD2	PTGPWD1	PTGPWD0	—	PTGWDT2	PTGWDT1	PTGWDT0	0000
PTGBTE	0AC4	ADCTS4	ADCTS3	ADCTS2	ADCTS1	IC4TSS	IC3TSS	IC2TSS	IC1TSS	OC4CS	OC3CS	OC2CS	OC1CS	OC4TSS	OC3TSS	OC2TSS	OC1TSS	0000
PTGHOLD	0AC6	PTGHOLD<15:0>																0000
PTGT0LIM	0AC8	PTGT0LIM<15:0>																0000
PTGT1LIM	0ACA	PTGT1LIM<15:0>																0000
PTGSDLIM	0ACC	PTGSDLIM<15:0>																0000
PTGC0LIM	0ACE	PTGC0LIM<15:0>																0000
PTGC1LIM	0AD0	PTGC1LIM<15:0>																0000
PTGADJ	0AD2	PTGADJ<15:0>																0000
PTGL0	0AD4	PTGL0<15:0>																0000
PTGQPTR	0AD6	—	—	—	—	—	—	—	—	—	—	—	PTGQPTR<4:0>					0000
PTGQUE0	0AD8	STEP1<7:0>								STEP0<7:0>								0000
PTGQUE1	0ADA	STEP3<7:0>								STEP2<7:0>								0000
PTGQUE2	0ADC	STEP5<7:0>								STEP4<7:0>								0000
PTGQUE3	0ADE	STEP7<7:0>								STEP6<7:0>								0000
PTGQUE4	0AE0	STEP9<7:0>								STEP8<7:0>								0000
PTGQUE5	0AE2	STEP11<7:0>								STEP10<7:0>								0000
PTGQUE6	0AE4	STEP13<7:0>								STEP12<7:0>								0000
PTGQUE7	0AE6	STEP15<7:0>								STEP14<7:0>								0000
PTGQUE8	0x0AE8	STEP17<7:0>								STEP16<7:0>								0000
PTGQUE9	0x0AEA	STEP19<7:0>								STEP18<7:0>								0000
PTGQUE10	0x0AEC	STEP21<7:0>								STEP20<7:0>								0000
PTGQUE11	0x0AEE	STEP23<7:0>								STEP22<7:0>								0000
PTGQUE12	0x0AF0	STEP25<7:0>								STEP24<7:0>								0000
PTGQUE13	0x0AF2	STEP27<7:0>								STEP26<7:0>								0000
PTGQUE14	0x0AF4	STEP29<7:0>								STEP28<7:0>								0000
PTGQUE15	0x0AF6	STEP31<7:0>								STEP30<7:0>								0000

Legend: x = unknown value on Reset; — = unimplemented, read as ‘0’. Reset values are shown in hexadecimal.

5.2 RTSP Operation

RTSP allows the user application to erase a single page of memory, program a row and to program two instruction words at a time. See Table 1 in the **"dsPIC33EPXXXGM3XX/6XX/7XX Product Family"** section for the page sizes of each device.

The Flash program memory array is organized into rows of 64 instructions or 192 bytes. RTSP allows the user application to erase a page of program memory, which consists of eight rows (512 instructions) at a time, and to program one row or two adjacent words at a time. The 8-row erase pages and single row write rows are edge-aligned, from the beginning of program memory, on boundaries of 1536 bytes and 192 bytes, respectively.

For more information on erasing and programming Flash memory, refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"Flash Programming"** (DS70609).

5.3 Programming Operations

A complete programming sequence is necessary for programming or erasing the internal Flash in RTSP mode. The processor stalls (waits) until the programming operation is finished.

For erase and program times, refer to Parameters D137a and D137b (Page Erase Time), and D138a and D138b (Word Write Cycle Time), in Table 33-13.

Setting the WR bit (NVMCON<15>) starts the operation and the WR bit is automatically cleared when the operation is finished.

5.3.1 PROGRAMMING ALGORITHM FOR FLASH PROGRAM MEMORY

Programmers can program two adjacent words (24 bits x 2) of program Flash memory at a time on every other word address boundary (0x000002, 0x000006, 0x00000A, etc.). To do this, it is necessary to erase the page that contains the desired address of the location the user wants to change. Programmers can also program a row of data (64 instruction words/ 192 bytes) at a time using the row programming feature present in these devices. For row programming, the source data is fetched directly from the data memory (RAM) on these devices. Two new registers have been provided to point to the RAM location where the source data resides. The page that has the row to be programmed must first be erased before the programming operation.

For protection against accidental operations, the write initiate sequence for NVMKEY must be used to allow any erase or program operation to proceed. After the programming command has been executed, the user application must wait for the programming time until programming is complete. The two instructions following the start of the programming sequence should be NOPs.

Refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"Flash Programming"** (DS70609) for details and code examples on programming using RTSP.

5.4 Control Registers

Six SFRs are used to read and write the program Flash memory: NVMCON, NVMKEY, NVMADR, NVMADRU, NVMSRCADRL and NVMSRCADRH.

The NVMCON register (Register 5-1) controls which blocks are to be erased, which memory type is to be programmed and the start of the programming cycle.

NVMKEY (Register 5-4) is a write-only register that is used for write protection. To start a programming or erase sequence, the user application must consecutively write 0x55 and 0xAA to the NVMKEY register.

There are two NVM Address registers: NVMADRU and NVMADR. These two registers, when concatenated, form the 24-bit Effective Address (EA) of the selected word for programming operations, or the selected page for erase operations.

The NVMADRU register is used to hold the upper 8 bits of the EA, while the NVMADR register is used to hold the lower 16 bits of the EA.

The NVMSRCADRH and NVMSRCADRL registers are used to hold the source address of the data in the data memory that needs to be written to Flash memory.

REGISTER 8-7: DMAxPAD: DMA CHANNEL x PERIPHERAL ADDRESS REGISTER(1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PAD<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PAD<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **PAD<15:0>:** DMA Peripheral Address Register bits

Note 1: If the channel is enabled (i.e., active), writes to this register may result in unpredictable behavior of the DMA channel and should be avoided.

REGISTER 8-8: DMAxCNT: DMA CHANNEL x TRANSFER COUNT REGISTER(1)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	CNT<13:8>(2)					
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CNT<7:0>(2)							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13-0 **CNT<13:0>:** DMA Transfer Count Register bits(2)

Note 1: If the channel is enabled (i.e., active), writes to this register may result in unpredictable behavior of the DMA channel and should be avoided.

2: The number of DMA transfers = CNT<13:0> + 1.

REGISTER 11-4: RPINR7: PERIPHERAL PIN SELECT INPUT REGISTER 7

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	IC2R<6:0>						
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	IC1R<6:0>						
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as ‘0’

bit 14-8 **IC2R<6:0>:** Assign Input Capture 2 (IC2) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)
1111100 = Input tied to RPI124
•
•
•
0000001 = Input tied to CMP1
0000000 = Input tied to VSS

bit 7 **Unimplemented:** Read as ‘0’

bit 6-0 **IC1R<6:0>:** Assign Input Capture 1 (IC1) to the Corresponding RPn Pin bits (see Table 11-2 for input pin selection numbers)
1111100 = Input tied to RPI124
•
•
•
0000001 = Input tied to CMP1
0000000 = Input tied to VSS

REGISTER 14-2: ICxCON2: INPUT CAPTURE x CONTROL REGISTER 2 (CONTINUED)

bit 4-0 **SYNCSEL<4:0>:** Input Source Select for Synchronization and Trigger Operation bits(4)

`11111` = Capture timer is unsynchronized
`11110` = Capture timer is unsynchronized
`11101` = Capture timer is unsynchronized
`11100` = CTMU trigger is the source for the capture timer synchronization
`11011` = ADC1 interrupt is the source for the capture timer synchronization(5)
`11010` = Analog Comparator 3 is the source for the capture timer synchronization(5)
`11001` = Analog Comparator 2 is the source for the capture timer synchronization(5)
`11000` = Analog Comparator 1 is the source for the capture timer synchronization(5)
`10111` = Input Capture 8 interrupt is the source for the capture timer synchronization
`10110` = Input Capture 7 interrupt is the source for the capture timer synchronization
`10101` = Input Capture 6 interrupt is the source for the capture timer synchronization
`10100` = Input Capture 5 interrupt is the source for the capture timer synchronization
`10011` = Input Capture 4 interrupt is the source for the capture timer synchronization
`10010` = Input Capture 3 interrupt is the source for the capture timer synchronization
`10001` = Input Capture 2 interrupt is the source for the capture timer synchronization
`10000` = Input Capture 1 interrupt is the source for the capture timer synchronization
`01111` = GP Timer5 is the source for the capture timer synchronization
`01110` = GP Timer4 is the source for the capture timer synchronization
`01101` = GP Timer3 is the source for the capture timer synchronization
`01100` = GP Timer2 is the source for the capture timer synchronization
`01011` = GP Timer1 is the source for the capture timer synchronization
`01010` = PTGx trigger is the source for the capture timer synchronization(6)
`01001` = Capture timer is unsynchronized
`01000` = Output Compare 8 is the source for the capture timer synchronization
`00111` = Output Compare 7 is the source for the capture timer synchronization
`00110` = Output Compare 6 is the source for the capture timer synchronization
`00101` = Output Compare 5 is the source for the capture timer synchronization
`00100` = Output Compare 4 is the source for the capture timer synchronization
`00011` = Output Compare 3 is the source for the capture timer synchronization
`00010` = Output Compare 2 is the source for the capture timer synchronization
`00001` = Output Compare 1 is the source for the capture timer synchronization
`00000` = Capture timer is unsynchronized

Note 1: The IC32 bit in both the Odd and Even ICx must be set to enable Cascade mode.
2: The input source is selected by the SYNCSEL<4:0> bits of the ICxCON2 register.
3: This bit is set by the selected input source (selected by SYNCSEL<4:0> bits); it can be read, set and cleared in software.
4: Do not use the ICx module as its own Sync or Trigger source.
5: This option should only be selected as a trigger source and not as a synchronization source.
6: Each Input Capture x module (ICx) has one PTG input source. See **Section 25.0 “Peripheral Trigger Generator (PTG) Module”** for more information.
PTGO8 = IC1, IC5
PTGO9 = IC2, IC6
PTGO10 = IC3, IC7
PTGO11 = IC4, IC8

16.0 HIGH-SPEED PWM MODULE

> **Note 1:** This data sheet summarizes the features of the dsPIC33EPXXXGM3XX/6XX/7XX family of devices. It is not intended to be a comprehensive reference source. To complement the information in this data sheet, refer to the "*dsPIC33/PIC24 Family Reference Manual*", **"High-Speed PWM"** (DS70645), which is available from the Microchip web site (www.microchip.com).
>
> **2:** Some registers and associated bits described in this section may not be available on all devices. Refer to **Section 4.0 "Memory Organization"** in this data sheet for device-specific register and bit information.

The dsPIC33EPXXXGM3XX/6XX/7XX devices support a dedicated Pulse-Width Modulation (PWM) module with up to 12 outputs.

The high-speed PWMx module consists of the following major features:

- Six PWM generators
- Two PWM outputs per PWM generator
- Individual period and duty cycle for each PWM pair
- Duty cycle, dead time, phase shift and a frequency resolution of 7.14 ns
- Independent Fault and current-limit inputs for six PWM outputs
- Redundant output
- Center-Aligned PWM mode
- Output override control
- Chop mode (also known as Gated mode)
- Special Event Trigger
- Prescaler for input clock
- PWMxL and PWMxH output pin swapping
- Independent PWM frequency, duty cycle and phase-shift changes for each PWM generator
- Dead-time compensation
- Enhanced Leading-Edge Blanking (LEB) functionality
- Frequency resolution enhancement
- PWM capture functionality

> **Note:** In Edge-Aligned PWM mode, the duty cycle, dead time, phase shift and frequency resolution are 7.14 ns.

The high-speed PWMx module contains up to six PWM generators. Each PWMx generator provides two PWM outputs: PWMxH and PWMxL. The master time base generator provides a synchronous signal as a common time base to synchronize the various PWM outputs. The individual PWM outputs are available on the output pins of the device. The input Fault signals and current-limit signals, when enabled, can monitor and protect the system by placing the PWM outputs into a known "safe" state.

Each PWMx can generate a trigger to the ADCx module to sample the analog signal at a specific instance during the PWM period. In addition, the high-speed PWMx module also generates a Special Event Trigger to the ADCx module, based on either of the two master time bases.

The high-speed PWMx module can synchronize itself with an external signal or can act as a synchronizing source to any external device. The SYNCI1 and SYNCI2 input pins that utilize PPS, can synchronize the high-speed PWMx module with an external signal. The SYNCO1 and SYNCO2 pins are output pins that provides a synchronous signal to an external device.

Figure 16-1 illustrates an architectural overview of the high-speed PWMx module and its interconnection with the CPU and other peripherals.

16.1 PWM Faults

The PWMx module incorporates multiple external Fault inputs, which include FLT1 and FLT2. The inputs are remappable using the PPS feature. FLT3 is available on 44-pin, 64-pin and 100-pin packages; FLT4 through FLT8 are available on specific pins on 64-pin and 100-pin packages, and FLT32, which has been implemented with Class B safety features, and is available on a fixed pin on all devices.

These Faults provide a safe and reliable way to safely shut down the PWM outputs when the Fault input is asserted.

16.1.1 PWM FAULTS AT RESET

During any Reset event, the PWMx module maintains ownership of the Class B Fault, FLT32. At Reset, this Fault is enabled in Latched mode to ensure the fail-safe power-up of the application. The application software must clear the PWM Fault before enabling the high-speed motor control PWMx module. To clear the Fault condition, the FLT32 pin must first be pulled high externally or the internal pull-up resistor in the CNPUx register can be enabled.

> **Note:** The Fault mode may be changed using the FLTMOD<1:0> bits (FCLCONx<1:0>), regardless of the state of FLT32.

REGISTER 16-22: LEBCONx: LEADING-EDGE BLANKING CONTROL REGISTER x

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0
PHR	PHF	PLR	PLF	FLTLEBEN	CLLEBEN	—	—
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	BCH(1)	BCL(1)	BPHH	BPHL	BPLH	BPLL
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **PHR:** PWMxH Rising Edge Trigger Enable bit
1 = Rising edge of PWMxH will trigger the Leading-Edge Blanking counter
0 = Leading-Edge Blanking ignores the rising edge of PWMxH

bit 14 **PHF:** PWMxH Falling Edge Trigger Enable bit
1 = Falling edge of PWMxH will trigger the Leading-Edge Blanking counter
0 = Leading-Edge Blanking ignores the falling edge of PWMxH

bit 13 **PLR:** PWMxL Rising Edge Trigger Enable bit
1 = Rising edge of PWMxL will trigger the Leading-Edge Blanking counter
0 = Leading-Edge Blanking ignores the rising edge of PWMxL

bit 12 **PLF:** PWMxL Falling Edge Trigger Enable bit
1 = Falling edge of PWMxL will trigger the Leading-Edge Blanking counter
0 = Leading-Edge Blanking ignores the falling edge of PWMxL

bit 11 **FLTLEBEN:** Fault Input Leading-Edge Blanking Enable bit
1 = Leading-Edge Blanking is applied to the selected Fault input
0 = Leading-Edge Blanking is not applied to the selected Fault input

bit 10 **CLLEBEN:** Current-Limit Leading-Edge Blanking Enable bit
1 = Leading-Edge Blanking is applied to the selected current-limit input
0 = Leading-Edge Blanking is not applied to the selected current-limit input

bit 9-6 **Unimplemented:** Read as ‘0’

bit 5 **BCH:** Blanking in Selected Blanking Signal High Enable bit(1)
1 = State blanking (of current-limit and/or Fault input signals) when selected blanking signal is high
0 = No blanking when selected blanking signal is high

bit 4 **BCL:** Blanking in Selected Blanking Signal Low Enable bit(1)
1 = State blanking (of current-limit and/or Fault input signals) when selected blanking signal is low
0 = No blanking when selected blanking signal is low

bit 3 **BPHH:** Blanking in PWMxH High Enable bit
1 = State blanking (of current-limit and/or Fault input signals) when PWMxH output is high
0 = No blanking when PWMxH output is high

bit 2 **BPHL:** Blanking in PWMxH Low Enable bit
1 = State blanking (of current-limit and/or Fault input signals) when PWMxH output is low
0 = No blanking when PWMxH output is low

bit 1 **BPLH:** Blanking in PWMxL High Enable bit
1 = State blanking (of current-limit and/or Fault input signals) when PWMxL output is high
0 = No blanking when PWMxL output is high

bit 0 **BPLL:** Blanking in PWMxL Low Enable bit
1 = State blanking (of current-limit and/or Fault input signals) when PWMxL output is low
0 = No blanking when PWMxL output is low

Note 1: The blanking signal is selected via the BLANKSELx bits in the AUXCONx register.

REGISTER 17-3: QEIxSTAT: QEIx STATUS REGISTER

U-0	U-0	HS, R/C-0	R/W-0	HS, R/C-0	R/W-0	HS, R/C-0	R/W-0
—	—	PCHEQIRQ	PCHEQIEN	PCLEQIRQ	PCLEQIEN	POSOVIRQ	POSOVIEN
bit 15							bit 8

HS, R/C-0	R/W-0	HS, R/C-0	R/W-0	HS, R/C-0	R/W-0	HS, R/C-0	R/W-0
PCIIRQ(1)	PCIIEN	VELOVIRQ	VELOVIEN	HOMIRQ	HOMIEN	IDXIRQ	IDXIEN
bit 7							bit 0

Legend:	HS = Hardware Settable bit	C = Clearable bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as ‘0’

bit 13 **PCHEQIRQ:** Position Counter Greater Than or Equal Compare Status bit
1 = POSxCNT ≥ QEIxGEC
0 = POSxCNT < QEIxGEC

bit 12 **PCHEQIEN:** Position Counter Greater Than or Equal Compare Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 11 **PCLEQIRQ:** Position Counter Less Than or Equal Compare Status bit
1 = POSxCNT ≤ QEIxLEC
0 = POSxCNT > QEIxLEC

bit 10 **PCLEQIEN:** Position Counter Less Than or Equal Compare Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 9 **POSOVIRQ:** Position Counter Overflow Status bit
1 = Overflow has occurred
0 = No overflow has occurred

bit 8 **POSOVIEN:** Position Counter Overflow Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 7 **PCIIRQ:** Position Counter (Homing) Initialization Process Complete Status bit(1)
1 = POSxCNT was reinitialized
0 = POSxCNT was not reinitialized

bit 6 **PCIIEN:** Position Counter (Homing) Initialization Process Complete interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 5 **VELOVIRQ:** Velocity Counter Overflow Status bit
1 = Overflow has occurred
0 = No overflow has occurred

bit 4 **VELOVIEN:** Velocity Counter Overflow Interrupt Enable bit
1 = Interrupt is enabled
0 = Interrupt is disabled

bit 3 **HOMIRQ:** Status Flag for Home Event Status bit
1 = Home event has occurred
0 = No home event has occurred

Note 1: This status bit is only applicable to PIMOD<2:0> = 011 and 100 modes.

REGISTER 17-10: INDXxHLD: INDEX COUNTER x HOLD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INDXHLD<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INDXHLD<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **INDXHLD<15:0>:** Holding Register for Reading and Writing INDXxCNT bits

REGISTER 17-11: QEIxICH: QEIx INITIALIZATION/CAPTURE HIGH WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
QEIIC<31:24>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
QEIIC<23:16>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **QEIIC<31:16>:** High Word Used to Form 32-Bit Initialization/Capture Register (QEIxIC) bits

REGISTER 17-12: QEIxICL: QEIx INITIALIZATION/CAPTURE LOW WORD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
QEIIC<15:8>							
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
QEIIC<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15-0 **QEIIC<15:0>:** Low Word Used to Form 32-Bit Initialization/Capture Register (QEIxIC) bits

REGISTER 18-2: SPIxCON1: SPIx CONTROL REGISTER 1 (CONTINUED)

bit 4-2 **SPRE<2:0>:** Secondary Prescale bits (Master mode)(3)

111 = Secondary prescale 1:1
110 = Secondary prescale 2:1
•
•
•
000 = Secondary prescale 8:1

bit 1-0 **PPRE<1:0>:** Primary Prescale bits (Master mode)(3)

11 = Primary prescale 1:1
10 = Primary prescale 4:1
01 = Primary prescale 16:1
00 = Primary prescale 64:1

Note 1: The CKE bit is not used in Framed SPI modes. Program this bit to '0' for Framed SPI modes (FRMEN = 1).
2: This bit must be cleared when FRMEN = 1.
3: Do not set both primary and secondary prescalers to the value of 1:1.

REGISTER 28-1: PMCON: PARALLEL MASTER PORT CONTROL REGISTER[3] (CONTINUED)

bit 3	**CS1P:** Chip Select 0 Polarity bit[1] `1` = Active-high (PMCS1/PMCS)[2] `0` = Active-low ($\overline{\text{PMCS1}}$/$\overline{\text{PMCS}}$)
bit 2	**BEP:** Byte Enable Polarity bit `1` = Byte enable is active-high (PMBE) `0` = Byte enable is active-low ($\overline{\text{PMBE}}$)
bit 1	**WRSP:** Write Strobe Polarity bit For Slave Modes and Master Mode 2 (PMMODE<9:8> = `00`, `01`, `10`): `1` = Write strobe is active-high (PMWR) `0` = Write strobe is active-low ($\overline{\text{PMWR}}$) For Master Mode 1 (PMMODE<9:8> = `11`): `1` = Enables strobe active-high (PMENB) `0` = Enables strobe active-low ($\overline{\text{PMENB}}$)
bit 0	**RDSP:** Read Strobe Polarity bit For Slave Modes and Master Mode 2 (PMMODE<9:8> = `00`, `01`, `10`): `1` = Read strobe is active-high (PMRD) `0` = Read strobe is active-low ($\overline{\text{PMRD}}$) For Master Mode 1 (PMMODE<9:8> = `11`): `1` = Enables strobe active-high (PMRD/PMWR) `0` = Enables strobe active-low ($\overline{\text{PMRD}}$/PMWR)

Note 1: These bits have no effect when their corresponding pins are used as address lines.
2: PMCS1 applies to Master mode and PMCS applies to Slave mode.
3: This register is not available on 44-pin devices.

33.0 ELECTRICAL CHARACTERISTICS

This section provides an overview of dsPIC33EPXXXGM3XX/6XX/7XX electrical characteristics. Additional information will be provided in future revisions of this document as it becomes available.

Absolute maximum ratings for the dsPIC33EPXXXGM3XX/6XX/7XX family are listed below. Exposure to these maximum rating conditions for extended periods may affect device reliability. Functional operation of the device at these or any other conditions above the parameters indicated in the operation listings of this specification is not implied.

Absolute Maximum Ratings

(See Note 1)

Ambient temperature under bias.......-40°C to +125°C
Storage temperature.......-65°C to +160°C
Voltage on VDD with respect to VSS.......-0.3V to +4.0V
Voltage on any pin that is not 5V tolerant with respect to VSS(3).......-0.3V to (VDD + 0.3V)
Voltage on any 5V tolerant pin with respect to VSS when VDD ≥ 3.0V(3).......-0.3V to +5.5V
Voltage on any 5V tolerant pin with respect to Vss when VDD < 3.0V(3).......-0.3V to +3.6V
Voltage on VCAP with respect to VSS.......1.62V to 1.98V
Maximum current out of VSS pin.......350 mA
Maximum current into VDD pin(2).......350 mA
Maximum current sunk by any I/O pin.......20 mA
Maximum current sourced by I/O pin.......18 mA
Maximum current sourced/sunk by all ports(2,4).......200 mA

Note 1: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

2: Maximum allowable current is a function of device maximum power dissipation (see Table 33-2).

3: See the **“Pin Diagrams”** section for the 5V tolerant pins.

4: Exceptions are: RA3, RA4, RA7, RA9, RA10, RB7-RB15, RC3, RC15, RD1-RD4, which are able to sink 30 mA and source 20 mA.

TABLE 33-7: DC CHARACTERISTICS: IDLE CURRENT (I_{IDLE})

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended			
Parameter No.	**Typ.(2)**	**Max.**	**Units**	**Conditions**		
Idle Current (I_{IDLE})(1)						
DC40d	1.5	8.0	mA	-40°C	3.3V	10 MIPS
DC40a	1.5	8.0	mA	+25°C		
DC40b	1.5	8.0	mA	+85°C		
DC40c	1.5	8.0	mA	+125°C		
DC41d	2.0	12.0	mA	-40°C	3.3V	20 MIPS
DC41a	2.0	12.0	mA	+25°C		
DC41b	2.0	12.0	mA	+85°C		
DC41c	2.0	12.0	mA	+125°C		
DC42d	5.5	15.0	mA	-40°C	3.3V	40 MIPS
DC42a	5.5	15.0	mA	+25°C		
DC42b	5.5	15.0	mA	+85°C		
DC42c	5.5	15.0	mA	+125°C		
DC43d	9.0	20.0	mA	-40°C	3.3V	60 MIPS
DC43a	9.0	20.0	mA	+25°C		
DC43b	9.0	20.0	mA	+85°C		
DC43c	9.0	20.0	mA	+125°C		
DC44d	10.0	25.0	mA	-40°C	3.3V	70 MIPS
DC44a	10.0	25.0	mA	+25°C		
DC44b	10.0	25.0	mA	+85°C		

Note 1: Base Idle current (I_{IDLE}) is measured as follows:

- CPU core is off, oscillator is configured in EC mode and external clock is active, OSC1 is driven with external square wave from rail-to-rail (EC clock overshoot/undershoot < 250 mV required)
- CLKO is configured as an I/O input pin in the Configuration Word
- All I/O pins are configured as outputs and driving low
- $\overline{MCLR}$ = VDD, WDT and FSCM are disabled
- No peripheral modules are operating or being clocked (defined PMDx bits are all ones)
- The NVMSIDL bit (NVMCON<12>) = `1` (i.e., Flash regulator is set to standby while the device is in Idle mode)
- The VREGSF bit (RCON<11>) = `0` (i.e., Flash regulator is set to standby while the device is in Sleep mode)
- JTAG is disabled

2: Data in the “Typical” column is at 3.3V, +25°C unless otherwise specified.

FIGURE 33-22: SPI2 AND SPI3 SLAVE MODE (FULL-DUPLEX, CKE = 0, CKP = 0, SMP = 0) TIMING CHARACTERISTICS

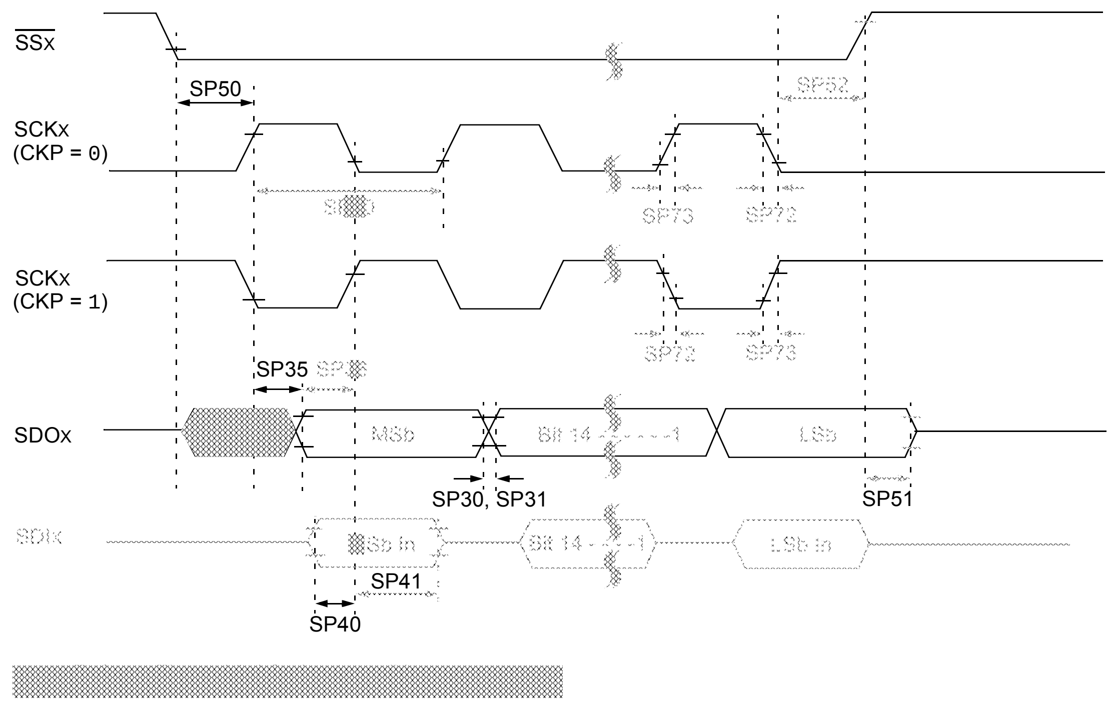


FIGURE 33-35: CANx MODULE I/O TIMING CHARACTERISTICS

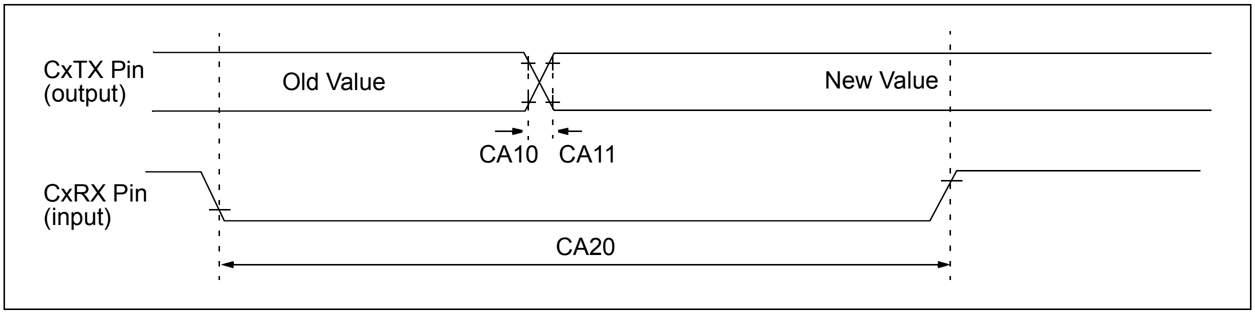


TABLE 33-50: CANx MODULE I/O TIMING REQUIREMENTS

AC CHARACTERISTICS			**Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
CA10	TIOF	Port Output Fall Time	—	—	—	ns	See Parameter DO32
CA11	TIOR	Port Output Rise Time	—	—	—	ns	See Parameter DO31
CA20	TCWF	Pulse Width to Trigger CAN Wake-up Filter	120	—	—	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in “Typical” column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

FIGURE 33-36: UARTx MODULE I/O TIMING CHARACTERISTICS

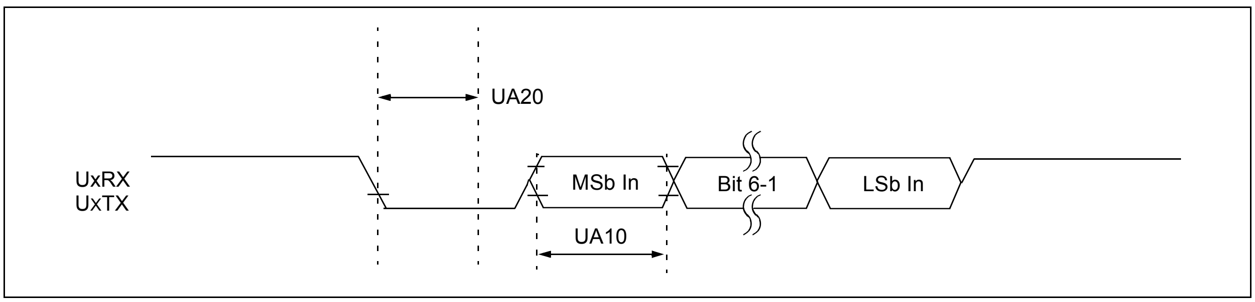


TABLE 33-51: UARTx MODULE I/O TIMING REQUIREMENTS

AC CHARACTERISTICS			**Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated)** Operating temperature -40°C ≤ TA ≤ +125°C				
Param No.	**Symbol**	**Characteristic(1)**	**Min.**	**Typ.(2)**	**Max.**	**Units**	**Conditions**
UA10	TUABAUD	UARTx Baud Time	66.67	—	—	ns	
UA11	FBAUD	UARTx Baud Frequency	—	—	15	Mbps	
UA20	TCWF	Start Bit Pulse Width to Trigger UARTx Wake-up	500	—	—	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in “Typical” column is at 3.3V, +25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

TABLE 34-8: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ T_A ≤ +150°C				
Param.	**Symbol**	**Characteristic**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
HDO10	V_{OL}	**Output Low Voltage** 4x Sink Driver Pins[(2)]	—	—	0.4	V	I_{OL} ≤ 5 mA, V_{DD} = 3.3V **(Note 1)**
		Output Low Voltage 8x Sink Driver Pins[(3)]	—	—	0.4	V	I_{OL} ≤ 8 mA, V_{DD} = 3.3V **(Note 1)**
HDO20	V_{OH}	**Output High Voltage** 4x Source Driver Pins[(2)]	2.4	—	—	V	I_{OH} ≥ -10 mA, V_{DD} = 3.3V **(Note 1)**
		Output High Voltage 8x Source Driver Pins[(3)]	2.4	—	—	V	I_{OH} ≥ 15 mA, V_{DD} = 3.3V **(Note 1)**
HDO20A	V_{OH1}	**Output High Voltage** 4x Source Driver Pins[(2)]	1.5	—	—	V	I_{OH} ≥ -3.9 mA, V_{DD} = 3.3V **(Note 1)**
			2.0	—	—		I_{OH} ≥ -3.7 mA, V_{DD} = 3.3V **(Note 1)**
			3.0	—	—		I_{OH} ≥ -2 mA, V_{DD} = 3.3V **(Note 1)**
		Output High Voltage 8x Source Driver Pins[(3)]	1.5	—	—	V	I_{OH} ≥ -7.5 mA, V_{DD} = 3.3V **(Note 1)**
			2.0	—	—		I_{OH} ≥ -6.8 mA, V_{DD} = 3.3V **(Note 1)**
			3.0	—	—		I_{OH} ≥ -3 mA, V_{DD} = 3.3V **(Note 1)**

Note 1: Parameters are characterized, but not tested.

2: Includes all I/O pins that are not 8x Sink Driver pins (see below).

3: Includes the following pins:
For 44-pin devices: RA3, RA4, RA7, RA9, RA10, RB7, RB<15:9>, RC1 and RC<9:3>
For 64-pin devices: RA4, RA7, RA<10:9>, RB7, RB<15:9>, RC1, RC<9:3>, RC15 and RG<8:7>
For 100-pin devices: RA4, RA7, RA9, RA10, RB7, RB<15:9>, RC1, RC<9:3>, RC15, RD<3:1> and RG<8:6>

TABLE 34-9: DC CHARACTERISTICS: PROGRAM MEMORY

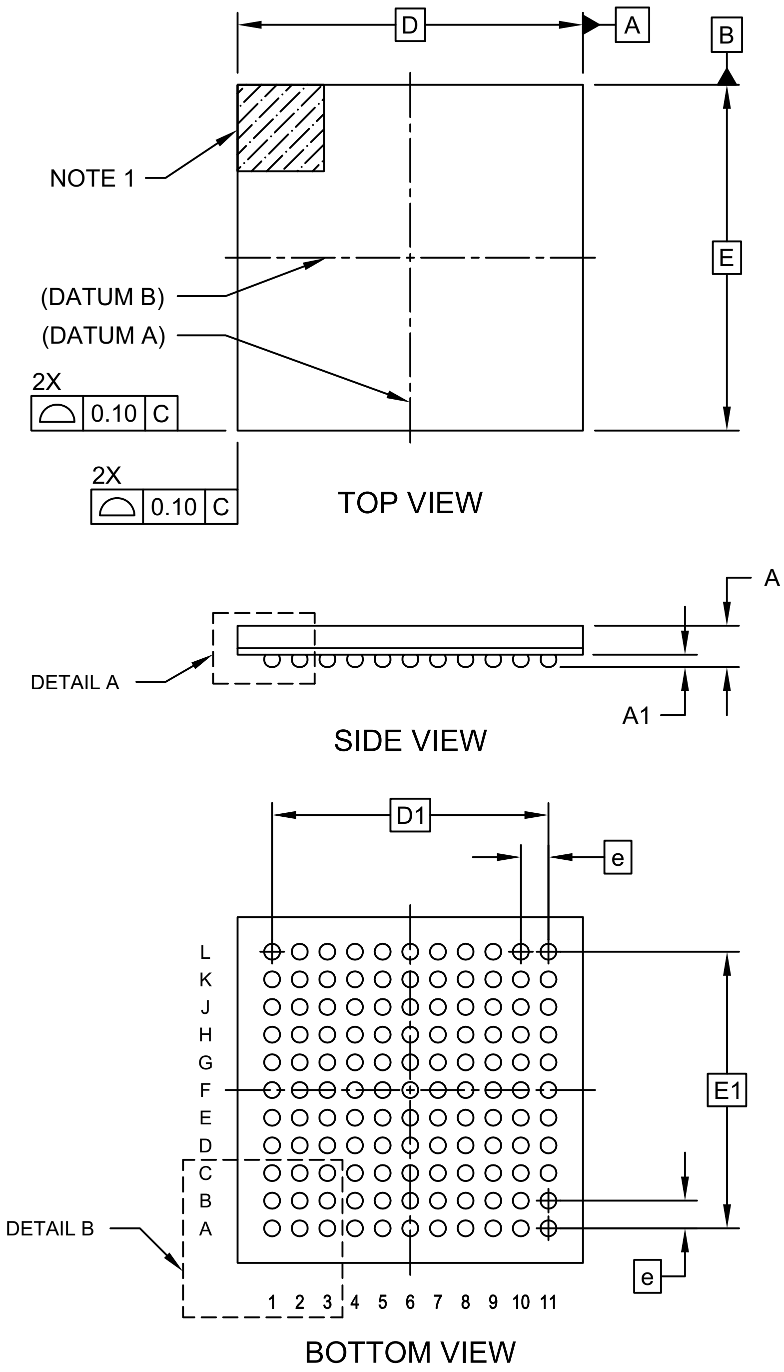
DC CHARACTERISTICS			Standard Operating Conditions: 3.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ T_A ≤ +150°C				
Param.	**Symbol**	**Characteristic[(1)]**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
		Program Flash Memory					
HD130	E_P	Cell Endurance	10,000	—	—	E/W	-40°C to +150°C[(2)]
HD134	T_{RETD}	Characteristic Retention	20	—	—	Year	1000 E/W cycles or less and no other specifications are violated

Note 1: These parameters are assured by design, but are not characterized or tested in manufacturing.

2: Programming of the Flash memory is allowed up to +150°C.

121-Ball Plastic Thin Profile Fine Pitch Ball Grid Array (BG) - 10x10x1.10 mm Body [TFBGA]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-148 Rev F Sheet 1 of 2