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Applications of "<u>Embedded - Microcontrollers</u>"

Details	
Product Status	Not For New Designs
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	SIO, UART/USART
Peripherals	LED, POR, Voltage Detect, WDT
Number of I/O	13
Program Memory Size	12KB (12K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	768 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-LSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21183sp-u0

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# R8C/18 Group, R8C/19 Group SINGLE-CHIP 16-BIT CMOS MCU

REJ03B0124-0140 Rev.1.40 Apr 14, 2006

### 1. Overview

These MCUs are fabricated using a high-performance silicon gate CMOS process, embedding the R8C/Tiny Series CPU core, and is packaged in a 20-pin molded-plastic LSSOP, SDIP or a 28-pin plastic molded-HWQFN. It implements sophisticated instructions for a high level of instruction efficiency. With 1 Mbyte of address space, they are capable of executing instructions at high speed.

Furthermore, the R8C/19 Group has on-chip data flash ROM (1 KB x 2 blocks).

The difference between the R8C/18 Group and R8C/19 Group is only the presence or absence of data flash ROM. Their peripheral functions are the same.

### 1.1 Applications

Electric household appliances, office equipment, housing equipment (sensors, security systems), general industrial equipment, audio equipment, etc.



### 1.2 Performance Overview

Table 1.1 outlines the Functions and Specifications for R8C/18 Group and Table 1.2 outlines the Functions and Specifications for R8C/19 Group.

Table 1.1 Functions and Specifications for R8C/18 Group

	Item	Specification
CPU	Number of fundamental	89 instructions
	instructions	
	Minimum instruction execution	50 ns (f(XIN) = 20 MHz, VCC = 3.0 to 5.5 V)
	time	100 ns (f(XIN) = 10 MHz, VCC = 2.7 to 5.5 V)
	Operation mode	Single-chip
	Address space	1 Mbyte
	Memory capacity	Refer to Table 1.3 Product Information for R8C/18
		Group
Peripheral	Ports	I/O ports: 13 pins (including LED drive port)
Functions		Input port: 3 pins
	LED drive ports	I/O ports: 4 pins
	Timers	Timer X: 8 bits × 1 channel, timer Z: 8 bits × 1 channel
		(Each timer equipped with 8-bit prescaler)
		Timer C: 16 bits x 1 channel
		(Input capture and output compare circuits)
	Serial interfaces	1 channel
		Clock synchronous serial I/O, UART
		1 channel
		UART
	Comparator	1-bit comparator: 1 circuit, 4 channels
	Watchdog timer	15 bits x 1 channel (with prescaler)
		Reset start selectable, count source protection mode
	Interrupts	Internal: 10 sources, External: 4 sources, Software: 4
		sources,
		Priority levels: 7 levels
	Clock generation circuits	2 circuits
		Main clock oscillation circuit (with on-chip feedback
		resistor)
		On-chip oscillator (high speed, low speed)
		High-speed on-chip oscillator has frequency
		adjustment function
	Oscillation stop detection	Main clock oscillation stop detection function
	function	
	Voltage detection circuit	On-chip
	Power-on reset circuit	On-chip On-chip
Electric	Supply voltage	VCC = 3.0 to 5.5 V (f(XIN) = 20 MHz)
Characteristics		VCC = 2.7  to  5.5  V  (f(XIN) = 10  MHz)
	Current consumption	Typ. 9 mA (VCC = 5.0 V, f(XIN) = 20 MHz, comparator stopped)
		Typ. 5 mA (VCC = 3.0V, f(XIN) = 10 MHz, comparator stopped)
		Typ. 35 μA (VCC = 3.0 V, wait mode, peripheral clock off)
		Typ. 0.7 $\mu$ A (VCC = 3.0 V, stop mode)
Flash Memory	Programming and erasure voltage	VCC = 2.7 to 5.5 V
	Programming and erasure	100 times
	endurance	
Operating Ambi	ent Temperature	-20 to 85°C
		-40 to 85°C (D version)
Package		20-pin molded-plastic LSSOP
		20-pin molded-plastic SDIP
		28-pin molded-plastic HWQFN

Table 1.4 Product Information for R8C/19 Group

### Current of Apr. 2006

Type No.	ROM C	apacity	RAM	Package Type	Remarks
Type No.	Program ROM	Data flash	Capacity	Fackage Type	Remarks
R5F21191SP	4 Kbytes	1 Kbyte x 2	384 bytes	PLSP0020JB-A	Flash memory version
R5F21192SP	8 Kbytes	1 Kbyte × 2	512 bytes	PLSP0020JB-A	
R5F21193SP	12 Kbytes	1 Kbyte × 2	768 bytes	PLSP0020JB-A	
R5F21194SP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLSP0020JB-A	
R5F21191DSP (D)	4 Kbytes	1 Kbyte × 2	384 bytes	PLSP0020JB-A	D version
R5F21192DSP (D)	8 Kbytes	1 Kbyte × 2	512 bytes	PLSP0020JB-A	
R5F21193DSP (D)	12 Kbytes	1 Kbyte x 2	768 bytes	PLSP0020JB-A	
R5F21194DSP (D)	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLSP0020JB-A	
R5F21191DD	4 Kbytes	1 Kbyte × 2	384 bytes	PRDP0020BA-A	Flash memory version
R5F21192DD	8 Kbytes	1 Kbyte × 2	512 bytes	PRDP0020BA-A	
R5F21193DD	12 Kbytes	1 Kbyte x 2	768 bytes	PRDP0020BA-A	
R5F21194DD	16 Kbytes	1 Kbyte × 2	1 Kbyte	PRDP0020BA-A	
R5F21192NP	8 Kbytes	1 Kbyte × 2	512 bytes	PWQN0028KA-B	Flash memory version
R5F21193NP	12 Kbytes	1 Kbyte × 2	768 bytes	PWQN0028KA-B	
R5F21194NP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PWQN0028KA-B	

(D): Under Development

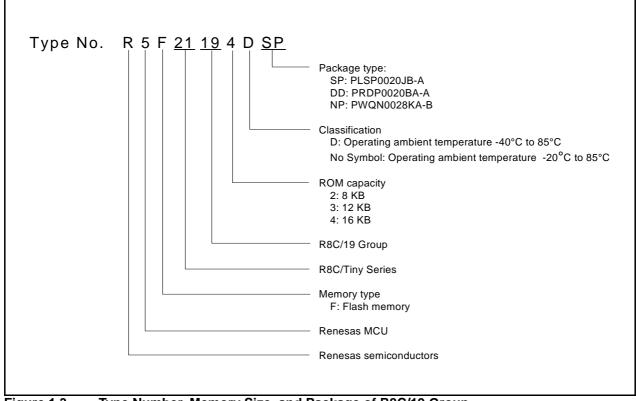


Figure 1.3 Type Number, Memory Size, and Package of R8C/19 Group

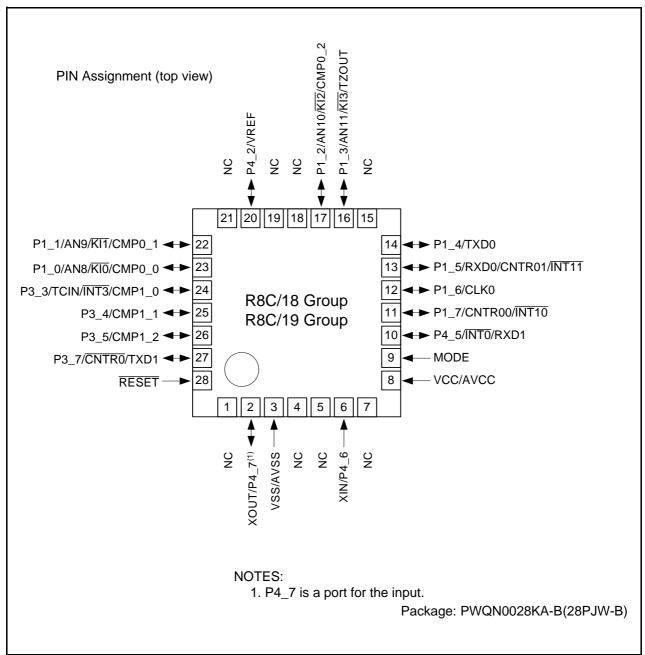


Figure 1.6 Pin Assignments for PWQN0028KA-B Package (Top View)

### 2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. R0, R1, R2, R3, A0, A1, and FB configure a register bank. There are two sets of register bank.

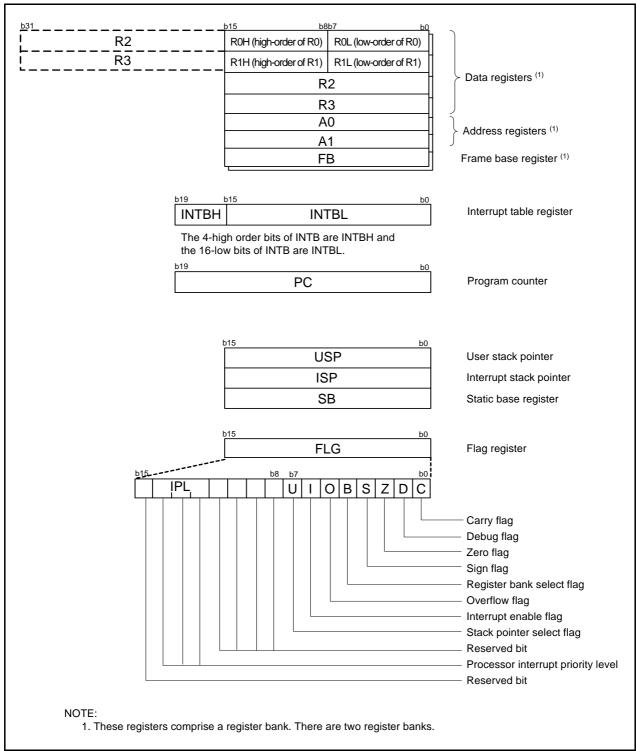


Figure 2.1 CPU Registers

### 2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

### 2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic and logic operations. A1 is analogous to A0. A1 can be combined with A0 and used as a 32-bit address register (A1A0).

### 2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

### 2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the start address of an interrupt vector table.

### 2.5 Program Counter (PC)

PC is 20 bits wide, indicates the address of the next instruction to be executed.

### 2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointer (SP), USP, and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

### 2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

### 2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

### 2.8.1 Carry Flag (C)

The C flag retains a carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

### 2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

### 2.8.3 **Zero Flag (Z)**

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

### 2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

### 2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

### 2.8.6 Overflow Flag (O)

The O flag is set to 1 when the operation results in an overflow; otherwise to 0.

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### 4. Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 4.1 to 4.4 list the special function registers.

Table 4.1 SFR Information (1)<sup>(1)</sup>

A -1-1	Devictor	Completel	A4
Address	Register	Symbol	After reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	00h
0005h	Processor Mode Register 1	PM1	00h
0006h	System Clock Control Register 0	CM0	01101000b
0007h	System Clock Control Register 1	CM1	00100000b
0008h			
0009h	Address Match Interrupt Enable Register	AIER	00h
000Ah	Protect Register	PRCR	00h
000Bh	1 Total Tragistal	TROR	0011
000Ch	Oscillation Stop Detection Register	OCD	00000100b
000Ch	Watchdog Timer Reset Register	WDTR	XXh
		WDTS	XXh
000Eh	Watchdog Timer Start Register		
000Fh	Watchdog Timer Control Register	WDC	00011111b
0010h	Address Match Interrupt Register 0	RMAD0	00h
0011h			00h
0012h			X0h
0013h			
0014h	Address Match Interrupt Register 1	RMAD1	00h
0015h			00h
0016h			X0h
0017h			
0018h			
0019h			
001Ah			
001Bh			
001Ch	Count Source Protection Mode Register	CSPR	00h
001Dh	Count Source Flotection wode Register	COFIC	0011
001Dh	<del> </del>	INITOE	001-
	INT0 Input Filter Select Register	INT0F	00h
001Fh			
0020h	High-Speed On-Chip Oscillator Control Register 0	HRA0	00h
0021h	High-Speed On-Chip Oscillator Control Register 1	HRA1	When shipping
0022h	High-Speed On-Chip Oscillator Control Register 2	HRA2	00h
0023h			
002Ah			
002Bh			
002Ch			
002Dh			
002Eh			
002En			
002FII			
	Valtana Datastina Danistas 4(2)	VCA1	00001000b
0031h	Voltage Detection Register 1 <sup>(2)</sup>	VCA1	00001000b
0032h	Voltage Detection Register 2 <sup>(2)</sup>	VCA2	00h <sup>(3)</sup>
			01000000b <sup>(4)</sup>
0033h			
0034h			
0035h			
0036h	Voltage Monitor 1 Circuit Control Register (2)	VW1C	0000X000b <sup>(3)</sup>
			0100X001b <sup>(4)</sup>
0037h	Voltage Monitor 2 Circuit Control Register (5)	VW2C	00h
	Voltage Monitor 2 Circuit Control Register (5)	V VVZO	OOH
0038h			
0039h			
003Ah			
003Bh			
003Ch			
003Dh			
003Eh			
003Fh			
	I .	l	1

### X: Undefined

- 1. The blank regions are reserved. Do not access locations in these regions.
- 2. Software reset, watchdog timer reset, and voltage monitor 2 reset do not affect this register.
- 3. After hardware reset.
- 4. After power-on reset or voltage monitor 1 reset.
- 5. Software reset, watchdog timer reset, and voltage monitor 2 reset do not affect b2 and b3.



SFR Information (2)<sup>(1)</sup> Table 4.2

Address	Register	Symbol	After reset
0040h	5	,	
0041h			
0042h			
0043h			
0044h			
0045h			
0046h			
0047h			
0048h			
0049h			
004Ah			
004Bh			
004Ch			
004Dh	Key Input Interrupt Control Register	KUPIC	XXXXX000b
004Eh	Comparator Conversion Interrupt Control Register	ADIC	XXXXX000b
004Fh			
0050h	Compare 1 Interrupt Control Register	CMP1IC	XXXXX000b
0051h	UART0 Transmit Interrupt Control Register	SOTIC	XXXXX000b
0052h	UARTO Receive Interrupt Control Register	SORIC	XXXXX000b
0053h	UART1 Transmit Interrupt Control Register	S1TIC	XXXXX000b
0054h	UART1 Receive Interrupt Control Register	S1RIC	XXXXX000b
0055h	Timor V Interrupt Central Pagister	TVIC	VVVVV000h
0056h 0057h	Timer X Interrupt Control Register	TXIC	XXXXX000b
0057h 0058h	Timer Z Interrupt Control Register	TZIC	XXXXX000b
0059h	-	INT1IC	XXXXX000b
	INT1 Interrupt Control Register		
005Ah	INT3 Interrupt Control Register	INT3IC	XXXXX000b
005Bh	Timer C Interrupt Control Register	TCIC	XXXXX000b
005Ch	Compare 0 Interrupt Control Register	CMP0IC	XXXXX000b
005Dh	INTO Interrupt Control Register	INT0IC	XX00X000b
005Eh			
005Fh			
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h 0068h			
0069h			
006Ah			
006Bh			
006Ch			
006Dh			
006Eh			
006Fh			
0070h			
0071h			
0072h			
0073h			
0074h			
0075h			
0076h			
0077h			
0078h			
0079h			
007Ah			
007Bh			
007Ch			
007Dh			
007Eh			
007Fh			

X: Undefined

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

SFR Information (4)<sup>(1)</sup> Table 4.4

DOCCOR	Address	Register	Symbol	After reset
0002h   0003h   0003	00C0h			
9003h				
00C4h         00C8h           00C8h         00C8h           00C7h         00C7h           00C7h         00C7h           00C2h         00C7h           00C2h         00C7h           00C7h         00C7h           00C7h         00C7h           00D9h         00D9h           00D9h <td></td> <td></td> <td></td> <td></td>				
0005h				
000C6h	00C4h			
00C7h         00C8h           00C8h         00C8h           00D0h         00D0h           00D1h         00D0h           00D2h         AD Control Register 0           00D5h         00D0h           00D7h         AD Control Register 0           00D8h         00D0h           00D8h         00D0h           00D8h         00D0h           00D8h         00D0h           00D0h         00D0h           00D0h         00D0h           00E0h         00D0h           00E0h         00C8h           00E3h         00F1 Port P3 Register           00E3h         Port P1 Register           00E3h         Port P3 Register           00E3h         Port P3 Register           00E3h         Port P3 Port P3 Register           00E4h         00E5h           00E5h         Port P3 Registe				
0005h   0005				
0005h   0006h   0006				
00Cbh         00Cbh           00Cbh         00Cbh           00Cbh         00Cbh           00Cbh         00Cbh           00D0bh         00D0bh           00D2h         00D3h           00D3h         AD Control Register 2           00D6h         ADCON0           00D8h         AD Control Register 0           00D8h         ADCON1           00D8h         ADCON1           00D8h         ADCON1           00D8h         ADCON1           00D8h         ADCON1           00D8h         ADCON1           00D8h         ODCh           00Eh         Port P1 Register           00Eh         Port P2 Register           00Eh         Port P3 Direction Register           00Eh         Port P3 Direction Register	00C9h			
00CCh         00CEh           00CCh         00CEh           00CCh         00CH           00D0h         00D0h           00D1h         00D1h           00D3h         00D3h           00D3h         AD Control Register 2           00D4h         AD Control Register 1           00D4h         AD Control Register 1           00D7h         AD Control Register 1           00D4h         AD CON1           00D4h         00D8h           00D4h         00D8h           00D4h         00D8h           00D4h         00D8h           00D4h         00D8h           00D4h         00D8h           00D5h         00D8h           00D6h         00D8h           00E0h         00D8h           00E1h         00E2h           00E2h         00E3h           00E3h         Port P1 Direction Register           00E4h         Port P3 Register         P3           00E4h         Port P4 Register         P4           00E4h         Port P4 Register         P4           00E4h         Port P4 Direction Register         PD3           00E6h         Port P4 Direction Regist				
000Cbh         00CFh           00Cbh         00CPh           00Cbh         00Ch           00Dlah         00Dlah           00Dlah         AD Control Register 2           00Dsh         AD Control Register 0           00Dsh         AD Control Register 1           00Dbh         AD Control Register 1           00Dsh         AD Control Register 1           00Dsh         ADCON1           00Dsh         00Dsh           00Esh         00Esh           00Esh         Port P1 Direction Register           00Esh         Port P3 Direction Register           00Esh         Port P4 Register           00Esh         Port P4 Register           00Esh         Port P5 Direction Register           00Esh         Port P5 Dir				
00CEh         00Ch           00DOh         00DOh           00D1h         00D3h           00D3h         00D3h           00D3h         AD Control Register 2           00D3h         AD Control Register 1           00D4h         AD COND           00D4h         AD COND           00D4h         00DAn           00D4h         00DAn           00D4h         00DAn           00D4h         00DAn           00D5h         00DAn           00D4h         00DAn           00D5h         00DAn           00E3h         00FD           00E3h         Pot P3 Register           00E4h         00E3h           00E5h         Pot P3 Direction Register         P3           00E4h         00E3h           00E4h         00E3h           00E4h         00E3h				
00CPh         00D0h         00D1h           00D1h         00D2h         00D0h           00D3h         AD Control Register 2         00h           00D3h         AD Control Register 0         00000h           00D3h         AD Control Register 1         00h           00D3h         AD Control Register 1         00h           00D3h         00D3h         00h           00D4h         00D4h         00h           00D4h         00D4h         00h           00D5h         00D6h         00h           00D6h         00D6h         00h           00D6h         00D6h         00h           00D6h         00D6h         00h           00E3h         00Fh         00h           00E3h         Port P1 Register         P1         XXh           00E3h         Port P3 Register         P3         XXh           00E3h         Port P3 Register         P3         00h           00E3h         Port P3 Register         P4         XXh           00E3h         Port P4 Direction Register         P3         00h           00E4h         Port P3 Direction Register         P4         00h           00E4h         Port				
00010h				
00D1h         00D2h           00D2h         0D0h           00D3h         AD Control Register 2         ADCON2         00h           00D5h         AD Control Register 0         ADCON0         000000XXb           00D7h         AD Control Register 1         ADCON1         00h           00D8h         00D0h         00h         00h           00D8h         00D0h         00D0h         00D0h           00D0h         00D0h         00D0h         00D0h           00D0h         00D0h         00D0h         00D0h           00D0h         00D0h         00D0h         00D0h           00D0h         00D0h         00D0h         00D0h           00D2h         00D0h         00D0h         00D0h           00D2h         00D0h         00D0h         00D0h           00E3h         Port P1 Register         P1         XXh           00E3h         Port P3 Register         P3         XXh           00E3h         Port P3 Register         P3         XXh           00E3h         Port P4 Direction Register         P3         00h           00E3h         Port P4 Direction Register         P4         00h           00E4h <t< td=""><td></td><td></td><td></td><td></td></t<>				
00D2h         00D4h         AD Control Register 2         ADCON2         00h           00D4h         AD Control Register 0         ADCON0         000000000000000000000000000000000000				
00D4h         AD Control Register 2         ADCON2         00h           00D5h         AD Control Register 0         ADCON0         000000XXXb           00D7h         AD Control Register 1         ADCON1         00h           00D8h         00D8h         00DA         00DA           00D8h         00DA         00DA         00DA           00D5h         00DBh         00DBh         00DBh           00D5h         00DBh         00DBh         00DBh           00D5h         00DBh         00DBh         00DBh           00D6h         00DBh         00DBh         00DBh           00E3h         Port P1 Register         P1         XXh           00E3h         Port P2 Bregister         P3         XXh           00E4h         P0T P3 Register         P3         XXh           00E4h         P0T P4 Register         P4         XXh           00E8h         P0T P4 Register				
00D4h         AD Control Register 2         ADCON2         00h           00D5h         AD Control Register 0         ADCON0         000000XXXb           00D7h         AD Control Register 1         ADCON1         00h           00D8h         00D8h         00DA         00DA           00D8h         00DA         00DA         00DA           00D5h         00DBh         00DBh         00DBh           00D5h         00DBh         00DBh         00DBh           00D5h         00DBh         00DBh         00DBh           00D6h         00DBh         00DBh         00DBh           00E3h         Port P1 Register         P1         XXh           00E3h         Port P2 Bregister         P3         XXh           00E4h         P0T P3 Register         P3         XXh           00E4h         P0T P4 Register         P4         XXh           00E8h         P0T P4 Register	00D3h			
00D6h         A/D Control Register 0         ADCON0         00000XXXb           00D7h         A/D Control Register 1         ADCON1         000h           00D8h         00DAh         00DAh         00DAh           00DBh         00DBh         00DBh         00DBh           00DCh         00DCh         00DCh         00DBh           00DDh         00DBh         00DBh         00DBh           00DFh         00DFh         00DBh         00DBh           00E1h         00E1h         00DBh         00DBh           00E2h         00E3h         00E3h         00DBh           00E3h         Port P1 Direction Register         PD1         00h           00E4h         00E3h         Port P3 Register         P3         XXh           00E6h         00E7h         00H         00E8h         00H           00E8h         Port P4 Register         P4         XXh           00E8h         Port P4 Direction Register         PD4         00h           00E8h         00E0h         00H         00H           00E8h         00E0h         00H         00H           00E0h         00E0h         00H         00H           00E0h <t< td=""><td>00D4h</td><td>A/D Control Register 2</td><td>ADCON2</td><td>00h</td></t<>	00D4h	A/D Control Register 2	ADCON2	00h
00DRh         A/D Control Register 1         00h           00D8h         00D9h           00DAh         00DBh           00DCh         00DCh           00DCh         00DCh           00DEh         00DEh           00Eh         00Eh           00Eh <t< td=""><td></td><td></td><td></td><td></td></t<>				
00D8h         00DAh           00DAh         00DAh           00DBh         00DCh           00DDh         00DDh           00DDh         00DDh           00DFh         00DFh           00DFh         00DFh           00E1h         Port P1 Register           00E2h         00E3h           00E3h         Port P1 Direction Register           00E3h         Port P2 Breston Register           00E6h         Port P3 Direction Register           00E8h         Port P4 Register           00E8h         Port P4 Direction Register           00E8h         Port P4 Direction Register           00E8h         Port P5 Direction Register           00E8h         Port P6 Direction Register           00E8h         Port P7 Direction Register           00E8h         Port P8 Direction Register           00E2h         Oberth           00E2h         Oberth           00E2h         Oberth           00E2h         Oberth           00E2h         Oberth           00F3h         Oberth           00F4h         Oberth           00F5h         Oberth           00F6h         Oberth <t< td=""><td>00D6h</td><td>A/D Control Register 0</td><td>ADCON0</td><td></td></t<>	00D6h	A/D Control Register 0	ADCON0	
00D9h         00DBh           00DBh         00DBh           00DCh         00DCh           00DEh         00DEh           00DFh         00DFh           00E1h         00E1h           00E2h         00E3h           00E3h         Port P1 Direction Register           00E3h         Port P2 Direction Register           00E3h         Port P3 Register           00E6h         Port P4 Register           00E7h         Port P4 Register           00E8h         Port P4 Register           00E8h         Port P4 Register           00E8h         Port P4 Direction Register           00E8h         Port P4 Direction Register           00E8h         Port P4 Direction Register           00E8h         Port P5 P4 Direction Register           00E8h         Port P6 Register           00E9h         Port P6 Register           00E9h         Port P6 Register           00E9h         Port P7 Register           00E9h         Port P8 Register           00F8h         Port P8 Register           00F8h         Port P8 Register           00F8h         Port P8 Register           00F8h         Port P8 Register <t< td=""><td></td><td>A/D Control Register 1</td><td>ADCON1</td><td>uun</td></t<>		A/D Control Register 1	ADCON1	uun
00DAh         00DBh           00DCh         00DCh           00DDh         00DBh           00DFh         00DFh           00E1h         00E1h           00E1h         00E1h           00E1h         00E1h           00E3h         00E3h           00E3h         Port P1 Direction Register           00E3h         Port P2 Register           00E6h         Port P3 Direction Register           00E8h         Port P4 Register           00E8h         Port P4 Register           00E8h         Port P4 Direction Register           00E9h         Ooh           00E1h         Ooh           00E2h         Ooh           00E2h         Ooh           00E2h         Ooh           00E3h         Ooh           00F8h         Ooh           00F8h         Ooh           00F8h         Ooh           00F8h         <				
00DBh         00DCh           00DCh         00DDh           00DFh         00E0h           00E0h         00E1h           00E2h         00E2h           00E2h         00E2h           00E2h         00E2h           00E3h         Port P1 Direction Register           00E3h         Port P3 Register           00E5h         Port P3 Direction Register           00E7h         Port P4 Register           00E8h         Port P4 Register           00E8h         Port P4 Direction Register           00E8h         Port P4 Direction Register           00E8h         Pot P4 Direction Register           00EBh         Do           00ECh         00E0h           00EDh         00E0h           00E7h         00F0h           00E7h         00F3h           00F3h         00F4h           00F3h         00F3h           00F6h         00F6h           00F7h         00F8h           00F8h         00F8h           00F9h         00F9h           00F9h         00F9h           00F9h         00F9h           00F9h         00F9h           00F9	00D9H			
OODCh OODED OODEN O				
OODDh OODEh OODEh OOED OOE1h OOE2h OOE3h OOE3h OOE3h OOE5h OOE5h OOE5h OOE6h OOE7h OOE7h OOE7h OOE7h OOE9h OOF9h OO				
00DFh         00E1h         Port P1 Register         P1         XXh           00E2h         00E3h         Port P1 Direction Register         PD1         00h           00E3h         Port P3 Register         P3         XXh           00E6h         00E7h         Port P3 Direction Register         PD3         00h           00E8h         Port P4 Register         P4         XXh           00E9h         P0         XXh         00E0           00EAh         P0rt P4 Direction Register         PD4         00h           00EBh         P0rt P4 Direction Register         PD4         00h           00EDh         00E0h         00h         00h           00ECh         00EDh         00h         00h           00EFh         00Fh         00Fh         00Fh           00F1h         00Fh         00Fh         00Fh           00F3h         00Fh         00Fh         00Fh           00F3h         00Fh         00Fh         00Fh           00F3h         00Fh         00Fh         00Fh           00F9h         00Fh         00Fh         00Fh         00Fh           00F9h         00Fh         00Fh         00Fh         00Fh	00DDh			
00E1h 00E3h         Port P1 Register         P1         XXh           00E3h 00E3h         Port P1 Direction Register         PD1         00h           00E4h 00E5h         P0T P3 Register         P3         XXh           00E6h 00E7h         Port P3 Direction Register         PD3         00h           00E8h 00E8h 00E8h         P0rt P4 Register         P4         XXh           00E9h 00E9h 00E0h         P0rt P4 Direction Register         PD4         00h           00E8h 00ECh 00E0h         P0rt P4 Direction Register         PD4         00h           00E9h 00E0h 00E0h 00E0h         P0rt P4 Direction Register         PD4         00h           00E1h 00E0h 00E0h 00E0h         P0rt P4 Direction Register         PD4         00h           00E1h 00F2h 00F3h 00F4h         P0rt P4 Direction Register         PD4         00h           00F3h 00F6h 00F6h 00F6h 00F6h         P0rt P4 Direction Register 0         P0rt P4 Direction Register 0         P0rt P4 Direction Register 0           00F8h 00F6h 00F6h         P0rt P4 Direction Register 0         PUR0         00XX0000b 00XX0000b           00F1h 00F6h         P0rt P4 Direction Register 0         PUR0         00XX0000b 00R Direction Register 0           00F1h 00F6h         P0rt P1 Dirive Capacity Control Register 0         PUR0         00XXX000b 00h	00DEh			
00E1h ODE2h         Port PR Register         P1         XXh           00E2h ODE3h         Port P1 Direction Register         PD1         00h           00E4h ODE6h         P0rt P3 Register         P3         XXh           00E6h ODE7h         Port P3 Direction Register         PD3         00h           00E8h P0rt P4 Register         P4         XXh           00E9h ODE8h P0rt P4 Direction Register         PD4         00h           00EAh P0rt P4 Direction Register         PD4         00h           00ED P1         P0F1 P4 Direction Register         PD4         00h           00ED P1         PD4         00h         00h           00ED P2         P0F2         00h				
00E2h         00E3h         Port P1 Direction Register         PD1         00h           00E4h         Port P3 Register         P3         XXh           00E6h         Port P3 Direction Register         PD3         00h           00E8h         Port P4 Register         P4         XXh           00E9h         00E0h         00h         00h           00E8h         Port P4 Direction Register         PD4         00h           00E0h         00E0h         00h         00h           00E0h         00E0h         00h         00h           00E0h         00E0h         00h         00h           00E0h         00E0h         00h         00h           00E1h         00E0h         00H         00H           00E2h         00E0h         00E0h         00E0h           00E1h         00E1h         00E1h         00E1h           00E2h         00E2h         00E2h         00E2h           00E3h         00E3h         00E3h         00E3h           00E4h         00E3h         00E3h         00E3h           00F3h         00F3h         00E3h         00E3h           00F3h         00F3h         00E3h         00E3h				V. 7.
00E3h         Port P1 Direction Register         PD1         00h           00E4h         Port P3 Register         P3         XXh           00E7h         Port P3 Direction Register         PD3         00h           00E8h         Port P4 Register         P4         XXh           00E9h         P0t         P0t         P0t           00EAh         Port P4 Direction Register         PD4         00h           00EBh         00ECh         00ED         00h           00ECh         00EDh         00EDh         00EDh           00EFh         00EFh         00EHh           00Fh         00Fh         00Fh		Port P1 Register	P1	XXh
00E4h         00E6h         Port P3 Register         P3         XXh           00E6h         Port P4 Direction Register         PD3         00h           00E8h         P0T P4 Register         P4         XXh           00E9h         00E0h         00h           00E8h         00h         00h           00EBh         00h         00h           00EDh         00EDh         00h           00EBh         00EDh         00EDh           00EBh         00EDh         00EDh           00EBh         00F0h         00EDh           00EPh         00F0h         00EDh           00F3h         00F3h         00F3h           00F4h         00F3h         00F3h           00F4h         00F3h         00F3h	00E2h	Dort D1 Direction Register	DD4	00h
00E6h         Port P3 Register           00E6h         Port P3 Direction Register           00E7h         Port P4 Register           00E8h         Port P4 Register           00E9h         Port P4 Direction Register           00EAh         Port P4 Direction Register           00EBh         O0           00ECh         O0           00ECh         O0EDh           00ECh         O0EDh           00ECh         O0ERH           00E7h         O0Foh           00F1h         O0Foh           00F2h         O0Foh           00F3h         O0Foh           00F6h         O0Foh           00F6h         O0Foh           00F6h         O0Foh           00F8h         O0Foh           00F8h         O0Foh           00F8h         O0Foh           00F9h         O0Foh           00F0h         Pull-Up Control Register 0           00F0h         Pull-Up Control Register 1           00F0h         Pull P1 Dive Capacity Control Register         Doh           00Feh         O0h           00Feh         O0h         O0h           00FFh         O0h         O0h </td <td></td> <td>  Fort F1 Direction Register</td> <td>וטיו</td> <td>OOT</td>		Fort F1 Direction Register	וטיו	OOT
00E6h         DOETh Port P3 Direction Register         PD3         00h           00E8h         Port P4 Register         P4         XXh           00E8h         00EAh         PD4         00h           00EBh         00         00         00           00EDh         00EBh         00         00           00EDh         00EBh         00         00           00EBh         00Fbh         00         00         00           00Eh         00Eh         00 </td <td></td> <td>L Port P3 Register</td> <td>P3</td> <td>XXh</td>		L Port P3 Register	P3	XXh
00E7h         Port P3 Direction Register         P9         00h           00E8h         Port P4 Register         P4         XXh           00E9h         ODEAh         Port P4 Direction Register         PD4         ODh           00EBh         ODECh         ODH         ODh           00ECh         ODECH         ODECH         ODECH           00EFh         ODECH         ODECH         ODECH           00F1h         ODF3h         ODECH         ODECH           00F3h         ODF3h         ODECH         ODECH           00F6h         ODF6h         ODECH         ODECH           00F8h         ODF8h         ODECH         ODECH           00F8h         ODECH         ODECH         ODECH           00F9h         ODECH         ODECH         ODECH           00F9h         ODECH         ODECH         ODECH           00F0h         DURO         ODXX0000b         DURO           00F0h         DURO         ODXX0000b         DURO           00F0h         DURO         ODXX0000b         DURO           00F0h         DURO         ODXX0000b         DURO           00F0h         DURO         ODXX0000b	00E6h	T or to trog.com	. •	70
00E9h 00E8h 00EBh 00ECh 00ECh 00EDh 00EEh 00EFh 00Fh 00Fh 00Fh 00Fh 00Fh 0			PD3	
00EAh         Port P4 Direction Register         PD4         00h           00EBh         00ECh         00EDh         00EDh <td>00E8h</td> <td>Port P4 Register</td> <td>P4</td> <td>XXh</td>	00E8h	Port P4 Register	P4	XXh
00EBh         00ECh           00EDh         00EFh           00EFh         00Fh           00Fh         00Fh           00Fh         00Fh           00F1h         00Fh           00F3h         00Fh           00F4h         00Fh           00Fh         Pull-Up Control Register 0           00Fh         Pull-Up Control Register 1           00Fh         Port P1 Drive Capacity Control Register           00Fh         Timer C Output Control Register           01B3h         Flash Memory Control Register 4           01B3h         Flash Memory Control Register 1           01B6h         FMR1           01B7h         Flash Memory Control Register 0				
00ECh         00EDh           00EFh         00Fh           00Fh         00Fh           00Fh         00Fh           00Fh         00Fh           00Fh         00Fh           00F3h         00Fh           00F6h         00Fh           00F7h         00Fh           00F9h         00Fh           00Fh         00Fh           00Fh         00Fh           00Fh         00Fh           00Fh         00Fh           00Fh         Pull-Up Control Register 0           00Fh         Pull-Up Control Register 1           00Fh         Port P1 Drive Capacity Control Register           00Fh         Drive Capacity Control Register           00Fh         Timer C Output Control Register           01B3h         Flash Memory Control Register 4         FMR4         01000000b           01B4h         01B5h         Flash Memory Control Register 1         FMR1         1000000xb           01B6h         Flash Memory Control Register 0         FMR0         00000001b		Port P4 Direction Register	PD4	00h
00EDh         00EEh           00EFh	00EBh			
00Eh         00Eh           00F0h	00ECII			
00EFh         00F0h           00F1h         00F1h           00F2h         00F3h           00F4h         00F4h           00F5h         00F6h           00F6h         00F7h           00F8h         00F8h           00F9h         00FAh           00FBh         00FBh           00FDh         Pull-Up Control Register 0           00FDh         Pull-Up Control Register 1           00FFh         Port P1 Drive Capacity Control Register           00FFh         Timer C Output Control Register           01B3h         Flash Memory Control Register 4           01B4h         FMR4           01B5h         Flash Memory Control Register 1           01B6h         FMR1           01B7h         Flash Memory Control Register 0				
00F0h         00F1h           00F2h         00F3h           00F4h         00F4h           00F5h         00F6h           00F7h         00F8h           00F9h         00F9h           00F8h         00F9h           00F0h         Pull-Up Control Register 0           00FDh         PUR0         00XX0000b           00FDh         Pull-Up Control Register 1         PUR1         XXXXXXX0Xb           00FEh         Port P1 Drive Capacity Control Register         DRR         00h           00FFh         Timer C Output Control Register         TCOUT         00h           01B3h         Flash Memory Control Register 4         FMR4         01000000b           01B4h         Flash Memory Control Register 1         FMR1         10000000b           01B6h         Flash Memory Control Register 0         FMR0         00000001b				
00F1h         00F2h           00F3h         00F4h           00F4h         00F5h           00F6h         00F7h           00F8h         00F9h           00F9h         00FAh           00FBh         00FBh           00FDh         Pull-Up Control Register 0           00FDh         Pull-Up Control Register 1           00FEh         Port P1 Drive Capacity Control Register           00FFh         Timer C Output Control Register           01B3h         Flash Memory Control Register 4           01B5h         Flash Memory Control Register 1           01B5h         Flash Memory Control Register 1           01B7h         Flash Memory Control Register 0           01B7h         Flash Memory Control Register 0           01B7h         Flash Memory Control Register 0	00F0h			
00F3h         00F4h           00F5h         00F6h           00F7h         00F8h           00F9h         00F9h           00F8h         00F9h           00F8h         00F9h           00F8h         00F9h           00FCh         Pull-Up Control Register 0         PUR0         00XX0000b           00FDh         Pull-Up Control Register 1         PUR1         XXXXXXXXXb           00FEh         Port P1 Drive Capacity Control Register         DRR         00h           00FFh         Timer C Output Control Register         TCOUT         00h           01B3h         Flash Memory Control Register 4         FMR4         01000000b           01B4h         01B5h         Flash Memory Control Register 1         FMR1         10000000xb           01B6h         01B7h         Flash Memory Control Register 0         FMR0         000000001b	00F1h			
00F4h         00F5h           00F6h         00F7h           00F8h         00F9h           00F9h         00F8h           00FBh         00FCh           00FCh         Pull-Up Control Register 0         PUR0         00XX0000b           00FDh         Pull-Up Control Register 1         PUR1         XXXXXXXXb           00FEh         Port P1 Drive Capacity Control Register         DRR         00h           00FFh         Timer C Output Control Register         TCOUT         00h           01B3h         Flash Memory Control Register 4         FMR4         01000000b           01B4h         01B5h         Flash Memory Control Register 1         FMR1         1000000Xb           01B6h         01B7h         Flash Memory Control Register 0         FMR0         000000001b	00F2h			
00F5h         00F6h           00F7h         00F8h           00F9h         00F9h           00FAh         00FBh           00FCh         Pull-Up Control Register 0         PUR0         00XX0000b           00FDh         Pull-Up Control Register 1         PUR1         XXXXXXXXX           00FEh         Port P1 Drive Capacity Control Register         DRR         00h           00FFh         Timer C Output Control Register         TCOUT         00h           01B3h         Flash Memory Control Register 4         FMR4         01000000b           01B4h         01B5h         Flash Memory Control Register 1         FMR1         1000000Xb           01B7h         Flash Memory Control Register 0         FMR0         00000001b				
00F6h         00F7h           00F8h         00F9h           00F9h         00FAh           00FBh         00FCh           00FCh         Pull-Up Control Register 0         PUR0         00XX0000b           00FDh         Pull-Up Control Register 1         PUR1         XXXXXXXXX           00FEh         Port P1 Drive Capacity Control Register         DRR         00h           00FFh         Timer C Output Control Register         TCOUT         00h           01B3h         Flash Memory Control Register 4         FMR4         01000000b           01B4h         01B5h         Flash Memory Control Register 1         FMR1         1000000Xb           01B6h         01B7h         Flash Memory Control Register 0         FMR0         00000001b	UUF4h			
00F7h         00F8h           00F9h         00F9h           00FAh         00FBh           00FBh         00FCh           00FCh         Pull-Up Control Register 0         PUR0         00XX0000b           00FDh         Pull-Up Control Register 1         PUR1         XXXXXXXXX           00FEh         Port P1 Drive Capacity Control Register         DRR         00h           00FFh         Timer C Output Control Register         TCOUT         00h           01B3h         Flash Memory Control Register 4         FMR4         01000000b           01B4h         01B5h         Flash Memory Control Register 1         FMR1         1000000Xb           01B6h         01B7h         Flash Memory Control Register 0         FMR0         00000001b				
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00F9h         00FAh           00FAh         00FBh           00FCh         Pull-Up Control Register 0         PUR0         00XX0000b           00FDh         Pull-Up Control Register 1         PUR1         XXXXXX0Xb           00FEh         Port P1 Drive Capacity Control Register         DRR         00h           00FFh         Timer C Output Control Register         TCOUT         00h           01B3h         Flash Memory Control Register 4         FMR4         010000000b           01B4h         01B5h         Flash Memory Control Register 1         FMR1         1000000Xb           01B6h         01B7h         Flash Memory Control Register 0         FMR0         00000001b				
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00FBh         00FCh         Pull-Up Control Register 0         PUR0         00XX0000b           00FDh         Pull-Up Control Register 1         PUR1         XXXXXX0Xb           00FEh         Port P1 Drive Capacity Control Register         DRR         00h           00FFh         Timer C Output Control Register         TCOUT         00h           01B3h         Flash Memory Control Register 4         FMR4         01000000b           01B4h         Flash Memory Control Register 1         FMR1         1000000Xb           01B6h         Flash Memory Control Register 0         FMR0         00000001b	00FAh			
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00FFh         Timer C Output Control Register         TCOUT         00h           01B3h         Flash Memory Control Register 4         FMR4         01000000b           01B4h         501B5h         Flash Memory Control Register 1         FMR1         1000000Xb           01B6h         701B6h         701B6h         700000001b           01B7h         Flash Memory Control Register 0         FMR0         00000001b	00FDh	Pull-Up Control Register 1		
01B3h         Flash Memory Control Register 4         FMR4         010000000b           01B4h         50         FMR1         1000000Xb           01B5h         Flash Memory Control Register 1         FMR1         1000000Xb           01B6h         01B7h         Flash Memory Control Register 0         FMR0         00000001b	UUFEh	Timer C Output Control Register		
01B4h         01B5h         Flash Memory Control Register 1         FMR1         1000000Xb           01B6h         01B7h         Flash Memory Control Register 0         FMR0         00000001b	UUFFN	Timer C Output Control Register	10001	UUII
01B4h         01B5h         Flash Memory Control Register 1         FMR1         1000000Xb           01B6h         01B7h         Flash Memory Control Register 0         FMR0         00000001b	01B3h	Flash Memory Control Register 4	I FMR4	I 01000000b
01B5h         Flash Memory Control Register 1         FMR1         1000000Xb           01B6h         01B7h         Flash Memory Control Register 0         FMR0         00000001b		aaanory control regional 4		0.000000
01B6h         01B7h         Flash Memory Control Register 0         FMR0         00000001b	01B5h	Flash Memory Control Register 1	FMR1	1000000Xb
01B7h Flash Memory Control Register 0 FMR0 00000001b	01B6h	-		
0FFFFh   Optional Function Select Register   OFS   (Note 2)	01B7h	Flash Memory Control Register 0	FMR0	00000001b
UFFFF   Optional Function Select Register   OFS   (Note 2)				
	0FFFFh	Optional Function Select Register	OFS	(Note 2)

### X: Undefined NOTES:

- The blank regions, 0100h to 01B2h and 01B8h to 02FFh are all reserved. Do not access locations in these regions.
   The OFS register cannot be changed by a program. Use a flash programmer to write to it.

### 5. Electrical Characteristics

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter	Condition	Rated Value	Unit
Vcc	Supply voltage	Vcc = AVcc	-0.3 to 6.5	V
AVcc	Analog supply voltage	Vcc = AVcc	-0.3 to 6.5	V
Vı	Input voltage		-0.3 to Vcc+0.3	V
Vo	Output voltage		-0.3 to Vcc+0.3	V
Pd	Power dissipation	Topr = 25°C	300	mW
Topr	Operating ambient temperature		-20 to 85 / -40 to 85 (D version)	°C
Tstg	Storage temperature		-65 to 150	°C

**Table 5.2** Recommended Operating Conditions

Cumbal	Do	Parameter			1144		
Symbol	Pa			Min.	Тур.	Max.	Unit
Vcc	Supply voltage			2.7	-	5.5	V
AVcc	Analog supply volt	age		-	Vcc	-	V
Vss	Supply voltage			-	0	-	V
AVss	Analog supply volt	age		-	0	-	V
VIH	Input "H" voltage			0.8Vcc	-	Vcc	V
VIL	Input "L" voltage			0	_	0.2Vcc	V
IOH(sum)	Peak sum output "H" current	Sum of all pins IOH (peak)		=	=	-60	mA
IOH(peak)	Peak output "H" cu	Peak output "H" current		-	-	-10	mA
IOH(avg)	Average output "H	Average output "H" current		-	-	-5	mA
IOL(sum)	Peak sum output "L" currents	Sum of all pins IOL (peak)		-	-	60	mA
IOL(peak)	Peak output "L"	Except P1_0 to P1_3		-	-	10	mA
	currents	P1_0 to P1_3	Drive capacity HIGH	-	-	30	mA
			Drive capacity LOW	-	-	10	mA
IOL(avg)	Average output	Except P1_0 to P1_3		=	-	5	mA
	"L" current	P1_0 to P1_3	Drive capacity HIGH	=	=	15	mA
			Drive capacity LOW	-	=	5	mA
f(XIN)	Main clock input o	scillation frequency	3.0 V ≤ Vcc ≤ 5.5 V	0	=	20	MHz
			2.7 V ≤ Vcc < 3.0 V	0	-	10	MHz

- 1. Vcc = 2.7 to 5.5 V at Topr = -20 to 85 °C / -40 to 85 °C, unless otherwise specified.
- 2. Typical values when average output current is 100 ms.

**Table 5.3** Comparator Characteristics

Symbol	Parameter	Conditions		Unit		
Symbol	Falanielei	Conditions	Min.	Тур.	Max.	Offic
=	Resolution		=	=	1	Bit
_	Absolute accuracy	$\phi AD = 10 \text{ MHz}^{(3)}$	-	-	±20	mV
tconv	Conversion time	$\phi AD = 10 \text{ MHz}^{(3)}$	1	-	_	μS
Vref	Reference voltage		0	=	AVcc	V
VIA	Analog input voltage		0	=	AVcc	V
_	Comparator conversion operating clock frequency <sup>(2)</sup>		1	_	10	MHz

### NOTES:

- 1. Vcc = 2.7 to 5.5 V at Topr = -20 to 85 °C / -40 to 85 °C, unless otherwise specified.
- 2. If f1 exceeds 10 MHz, divided f1 and ensure the comparator conversion operating clock frequency (φAD) is 10 MHz or below.
- 3. If AVcc is less than 4.2 V, divided f1 and ensure the comparator conversion operating clock frequency (\$\phiAD\$) is f1/2 or below.

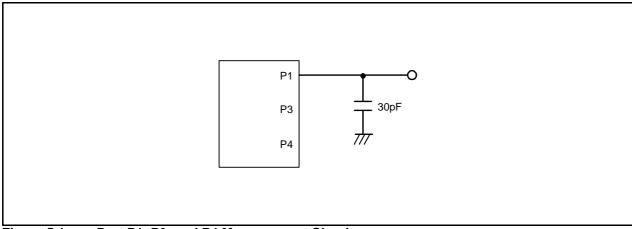


Figure 5.1 Port P1, P3, and P4 Measurement Circuit

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Table 5.4 Flash Memory (Program ROM) Electrical Characteristics

Cumbal	Parameter	Conditions		Unit		
Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
=	Program/erase endurance <sup>(2)</sup>	R8C/18 Group	100 <sup>(3)</sup>	=	=	times
		R8C/19 Group	1,000(3)	-	=	times
-	Byte program time		ī	50	400	μS
=	Block erase time		=	0.4	9	S
td(SR-SUS)	Time delay from suspend request until suspend		-	-	97+CPU clock × 6 cycles	μS
=	Interval from erase start/restart until following suspend request		650	=	-	μS
=	Interval from program start/restart until following suspend request		0	=	-	ns
=	Time from suspend until program/erase restart		=	=	3+CPU clock × 4 cycles	μS
_	Program, erase voltage		2.7	_	5.5	V
-	Read voltage		2.7	-	5.5	V
=	Program, erase temperature		0	-	60	°C
=	Data hold time <sup>(8)</sup>	Ambient temperature = 55 °C	20	_	_	year

#### NOTES:

- 1. Vcc = 2.7 to 5.5 V at Topr = 0 to 60 °C, unless otherwise specified.
- 2. Definition of programming/erasure endurance
  - The programming and erasure endurance is defined on a per-block basis.
  - If the programming and erasure endurance is n (n = 100 or 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one. However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
- 3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
- 4. If emergency processing is required, a suspend request can be generated independent of this characteristic. In that case the normal time delay to Suspend can be applied to the request. However, we recommend that a suspend request with an interval of less than 650 μs is only used once because, if the suspend state continues, erasure cannot operate and the incidence of erasure error rises.
- 5. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. In addition, averaging the number of erase operations between block A and block B can further reduce the effective number of rewrites. It is also advisable to retain data on the erase count of each block and limit the number of erase operations to a certain number.
- 6. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
- 7. Customers desiring programming/erasure failure rate information should contact their Renesas technical support representative.
- 8. The data hold time includes time that the power supply is off or the clock is not supplied.

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Table 5.10 High-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Descriptor	Condition	Standard			Lloit
Symbol	Parameter	Condition	Min.	Тур.	Max.	Unit
_	High-speed on-chip oscillator frequency when the reset is deasserted	VCC = 5.0 V, Topr = 25 °C	I	8	I	MHz
_	High-speed on-chip oscillator frequency temperature	0 to +60 °C/5 V ± 5 % <sup>(3)</sup>	7.76	-	8.24	MHz
	supply voltage dependence <sup>(2)</sup>	-20 to +85 °C/2.7 to 5.5 V(3)	7.68	_	8.32	MHz
		-40 to +85 °C/2.7 to 5.5 V <sup>(3)</sup>	7.44	-	8.32	MHz

### NOTES:

- 1. The measurement condition is Vcc = 5.0 V and  $T_{opr} = 25 \,^{\circ}\text{C}$ .
- 2. Refer to 10.6.4 High-Speed On-Chip Oscillator Clock for notes on high-speed on-chip oscillator clock.
- 3. The standard value shows when the HRA1 register is assumed as the value in shipping and the HRA2 register value is set to 00h.

**Table 5.11** Power Supply Circuit Timing Characteristics

Symbol	DI Parameter	Condition	Standard			Unit
Symbol		Condition	Min.	Тур.	Max.	Offic
td(P-R)	Time for internal power supply stabilization during power-on <sup>(2)</sup>		1	=	2000	μS
td(R-S)	STOP exit time <sup>(3)</sup>		=	-	150	μS

- 1. The measurement condition is Vcc = 2.7 to 5.5 V and  $T_{opr} = 25$  °C.
- 2. Waiting time until the internal power supply generation circuit stabilizes during power-on.
- 3. Time until CPU clock supply starts after the interrupt is acknowledged to exit stop mode.

Table 5.12 Electrical Characteristics (1) [Vcc = 5 V]

Symbol	Parameter Condit		dition	St	tandard		Unit	
Symbol	Fala	meter	Condition		Min.	Тур.	Max.	Unit
Vон	Output "H" voltage	Except Xout	Iон = -5 mA		Vcc - 2.0	_	Vcc	V
			Ιοн = -200 μΑ		Vcc - 0.3	-	Vcc	V
		Хоит	Drive capacity HIGH	Iон = -1 mA	Vcc - 2.0	=	Vcc	V
			Drive capacity LOW	ΙΟΗ = -500 μΑ	Vcc - 2.0	-	Vcc	V
Vol	Output "L" voltage	Except P1_0 to	IoL = 5 mA	-	_	1	2.0	V
		Р1_3, Хоит	IoL = 200 μA		_	1	0.45	V
		P1_0 to P1_3	Drive capacity HIGH	IOL = 15 mA	=	=	2.0	V
			Drive capacity LOW	IOL = 5 mA	=	1	2.0	V
			Drive capacity LOW	IOL = 200 μA	-	-	0.45	V
		Хоит	Drive capacity HIGH	IOL = 1 mA	=	=	2.0	V
			Drive capacity LOW	IOL = 500 μA	=	=	2.0	V
VT+-VT-	Hysteresis	INTO, INT1, INT2, INT3, KIO, KI1, KI2, KI3, CNTRO, CNTR1, TCIN, RXD0			0.2	-	1.0	V
		RESET			0.2	_	2.2	V
lін	Input "H" current	1	VI = 5 V		_	-	5.0	μА
lı∟	Input "L" current		VI = 0 V		-	_	-5.0	μА
RPULLUP	Pull-up resistance		VI = 0 V		30	50	167	kΩ
RfXIN	Feedback resistance	XIN			-	1.0	-	ΜΩ
fring-s	Low-speed on-chip o	scillator frequency			40	125	250	kHz
VRAM	RAM hold voltage		During stop mode		2.0	-	-	V

<sup>1.</sup> VCC = 4.2 to 5.5 V at Topr = -20 to 85 °C / -40 to 85 °C, f(XIN) = 20 MHz, unless otherwise specified.

### **Timing Requirements**

(Unless Otherwise Specified: Vcc = 5 V, Vss = 0 V at Ta = 25 °C) [Vcc = 5 V]

Table 5.14 XIN Input

Symbol	Parameter	Standard Min. Max.		Unit
	Faranietei			Unit
tc(XIN)	XIN input cycle time	50	-	ns
twh(xin)	XIN input "H" width	25	-	ns
twl(xin)	XIN input "L" width	25	-	ns

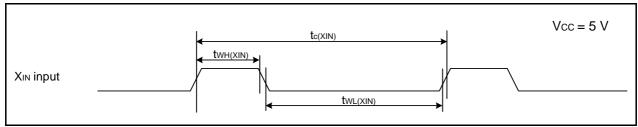


Figure 5.4 XIN Input Timing Diagram when Vcc = 5 V

Table 5.15 CNTR0 Input, CNTR1 Input, INT1 Input

Symbol	Parameter	Stan	dard	Unit
	Falanielei	Min.	Max.	Offic
tc(CNTR0)	CNTR0 input cycle time		-	ns
tWH(CNTR0)	CNTR0 input "H" width		-	ns
tWL(CNTR0)	CNTR0 input "L" width	40	=	ns

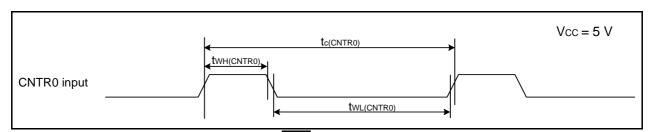


Figure 5.5 CNTR0 Input, CNTR1 Input, INT1 Input Timing Diagram when Vcc = 5 V

Table 5.16 TCIN Input, INT3 Input

Symbol	Parameter	Standard Min. Max.		Unit
	Faidilletei			Offic
tc(TCIN)	TCIN input cycle time	400 <sup>(1)</sup>	-	ns
tWH(TCIN)	TCIN input "H" width	200(2)	-	ns
tWL(TCIN)	TCIN input "L" width	200(2)	I	ns

- 1. When using timer C input capture mode, adjust the cycle time to (1/timer C count source frequency x 3) or above.
- 2. When using timer C input capture mode, adjust the pulse width to (1/timer C count source frequency x 1.5) or above.

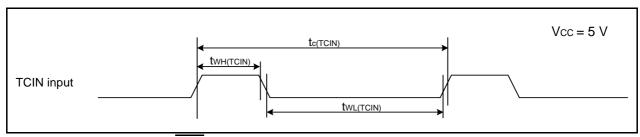


Figure 5.6 TCIN Input, INT3 Input Timing Diagram when Vcc = 5 V

Table	5.17	Serial	Interface
IUDIC	J. I 1	OCHA	michiacc

Symbol	Parameter	Stan	Unit	
	raianietei	Min.	Max.	Offic
tc(CK)	CLKi input cycle time	200	=	ns
tW(CKH)	CLKi input "H" width	100	=	ns
tW(CKL)	CLKi input "L" width	100	=	ns
td(C-Q)	TXDi output delay time	-	50	ns
th(C-Q)	TXDi hold time	0	-	ns
tsu(D-C)	RXDi input setup time	50	=	ns
th(C-D)	RXDi input hold time	90	-	ns

i = 0 or 1

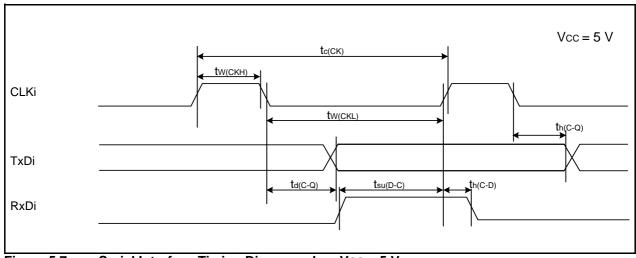


Figure 5.7 Serial Interface Timing Diagram when Vcc = 5 V

Table 5.18 External Interrupt INTO Input

Symbol	Parameter	Stan	dard	Unit
Syllibol	raianielei	Min.	Max.	Offic
tW(INH)	INTO input "H" width	250 <sup>(1)</sup>	-	ns
tW(INL)	INT0 input "L" width	250 <sup>(2)</sup>	-	ns

#### NOTES:

- 1. When selecting the digital filter by the INTO input filter select bit, use an INTO input HIGH width of either (1/digital filter clock frequency x 3) or the minimum value of standard, whichever is greater.
- 2. When selecting the digital filter by the INT0 input filter select bit, use an INT0 input LOW width of either (1/digital filter clock frequency x 3) or the minimum value of standard, whichever is greater.

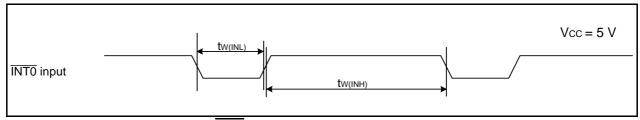
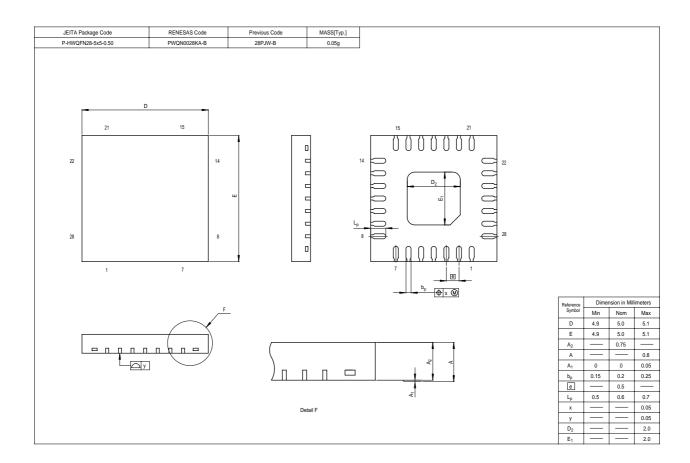


Figure 5.8 External Interrupt INTO Input Timing Diagram when Vcc = 5 V

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Electrical Characteristics (4) [Vcc = 3V] (Topr = -40 to 85 °C, unless otherwise specified.) **Table 5.20** 

Symbol	Parameter		Condition		Standard Max		
<b>C</b> y <b>C</b> O.	i didilioto.		Containen	Min.	Тур.	Max.	Unit
Icc	Power supply current (Vcc = 2.7 to 3.3 V) Single-chip mode, output pins are open,	High-speed mode	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	ı	8	13	mA
	other pins are Vss, comparator is stopped  XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	=	7	12	mA		
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	-	5	I	mA
		Medium- speed mode	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	l	3	l	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	=	2.5	-	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	_	1.6	-	mA
		High-speed on-chip oscillator mode	Main clock off High-speed on-chip oscillator on = 8 MHz Low-speed on-chip oscillator on = 125 kHz No division	-	3.5	7.5	mA
			Main clock off High-speed on-chip oscillator on = 8 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	ı	1.5	I	mA
		Low-speed on-chip oscillator mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8 FMR47 = 1		100	280	μА
		Wait mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = 0	=	37	74	μА
		Wait mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = 0	-	35	70	μА
		Stop mode	Main clock off, Topr = 25 °C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = 0	=	0.7	3.0	μА



### REVISION HISTORY

## R8C/18 Group, R8C/19 Group Datasheet

Day	Doto		Description		
Rev.	Date	Page	Summary		
0.10	Nov 15, 2004	-	First Edition issued		
0.20	Jan 11, 2005	5, 6	Tables 1.3 and 1.4: The date updated		
0.21	Apr 04, 2005	2, 3	Tables 1.1 and 1.2: Partly revised		
		4	Figure 1.1: Partly revised		
		5, 6	Tables 1.3 and 1.4: Partly revised		
		5, 6	Figure 1.2 and 1.3: Partly revised		
		7, 8	Figure 1.4 and 1.5: Partly revised		
		10	Table 1.6: Partly revised		
		16	Table 4.1: Partly revised		
		17	Table 4.2: Partly revised		
		18	Table 4.3: Partly revised		
		20	Package Dimensions are revised		
1.00	May 27, 2005	5, 6	Tables 1.3 and 1.4: Partly revised		
		9	Table 1.5: Partly revised		
		25	Table 5.9: Revised		
		26	Table 5.10: Partly revised		
		28	Table 5.13: Partly revised		
		32	Table 5.20: Partly revised		
1.10	Jun 09, 2005	26	Table 5.10: Partly revised		
1.20	Nov 01, 2005	3	Table 1.2 Performance Outline of the R8C/19 Group; Flash Memory: (Data area) → (Data flash) (Program area) → (Program ROM) revised		
		4	Figure 1.1 Block Diagram; "Peripheral Function" added, "System Clock Generation" → "System Clock Generator" revised		
		6	Table 1.4 Product Information of R8C/19 Group; ROM capacity: "Program area" → "Program ROM", "Data area" → "Data flash" revised		
		9	Table 1.5 Pin Description; Power Supply Input: "VCC/AVCC" → "VCC",  "VSS/AVSS" → "VSS" revised  Analog Power Supply Input: added		
		11	Figure 2.1 CPU Register; "Reserved Area" → "Reserved Bit" revised		
		13	2.8.10 Reserved Area; "Reserved Area" → "Reserved Bit" revised		
		15	3.2 R8C/19 Group, Figure 3.2 Memory Map of R8C/19 Group; "Data area" → "Data flash", "Program area" → "Program ROM" revised		

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