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Applications of "<u>Embedded - Microcontrollers</u>"

D-4-9-	
Details	
Product Status	Active
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	SIO, UART/USART
Peripherals	LED, POR, Voltage Detect, WDT
Number of I/O	13
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-LSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21184dsp-u0

Email: info@E-XFL.COM

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1.3 Block Diagram

Figure 1.1 shows a Block Diagram.

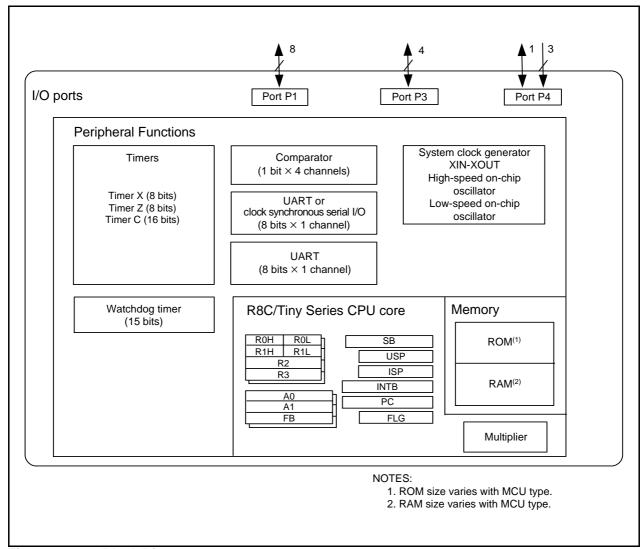


Figure 1.1 Block Diagram

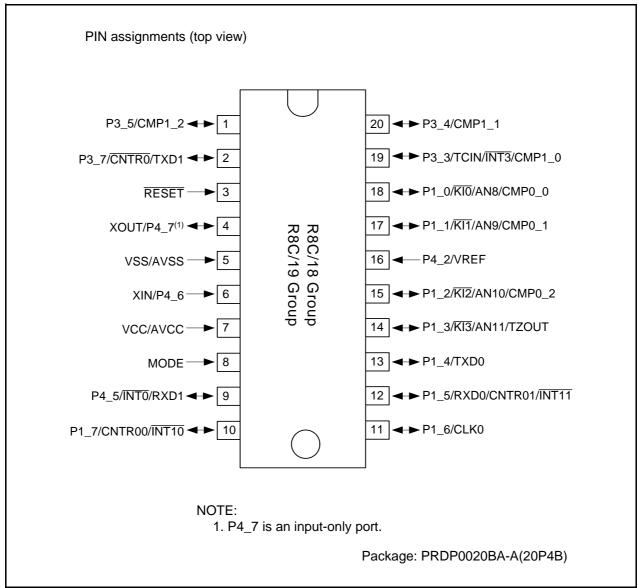


Figure 1.5 Pin Assignments for PRDP0020BA-A Package (Top View)

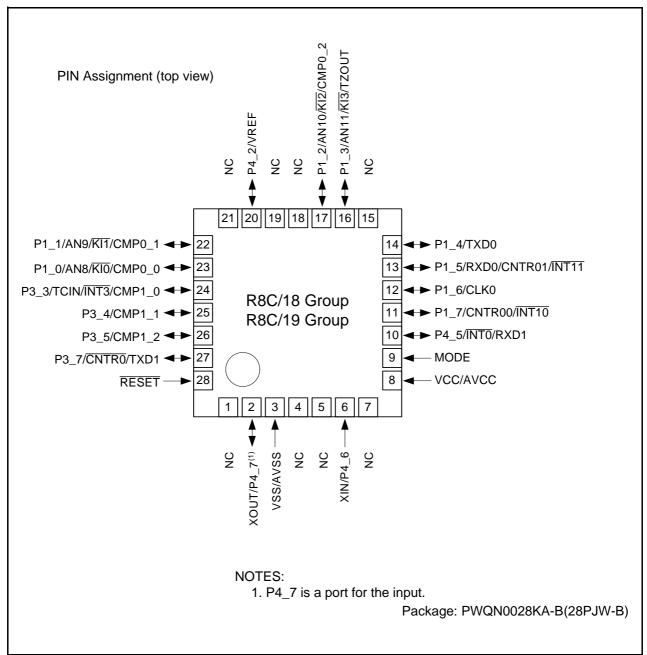


Figure 1.6 Pin Assignments for PWQN0028KA-B Package (Top View)

1.6 Pin Functions

Table 1.5 lists Pin Functions, Table 1.6 lists Pin Name Information by Pin Number of PLSP0020JB-A, PRDP0020BA-A packages, and Table 1.7 lists Pin Name Information by Pin Number of PWQN0028KA-B package.

Table 1.5 Pin Functions

Туре	Symbol	I/O Type	Description
Power supply input	VCC VSS	I	Apply 2.7 V to 5.5 V to the VCC pin. Apply 0 V to the VSS pin.
Analog power supply input	AVCC, AVSS	I	Power supply for the comparator Connect a capacitor between AVCC and AVSS.
Reset input	RESET	I	Input "L" on this pin resets the MCU.
MODE	MODE	I	Connect this pin to VCC via a resistor.
Main clock input	XIN	I	These pins are provided for main clock generation circuit I/O. Connect a ceramic resonator or a crystal oscillator between the XIN and XOUT pins.
Main clock output	XOUT	0	To use an external clock, input it to the XIN pin and leave the XOUT pin open.
INT interrupt	INTO, INT1, INT3	I	INT interrupt input pins
Key input interrupt	KI0 to KI3	I	Key input interrupt input pins
Timer X	CNTR0	I/O	Timer X I/O pin
	CNTR0	0	Timer X output pin
Timer Z	TZOUT	0	Timer Z output pin
Timer C	TCIN	I	Timer C input pin
	CMP0_0 to CMP0_2, CMP1_0 to CMP1_2	0	Timer C output pins
Serial interface	CLK0	I/O	Transfer clock I/O pin
	RXD0, RXD1	I	Serial data input pins
	TXD0, TXD1	0	Serial data output pins
Reference voltage input	VREF	I	Reference voltage input pin to comparator
Comparator	AN8 to AN11	I	Analog input pins to comparator
I/O port	P1_0 to P1_7, P3_3 to P3_5, P3_7, P4_5	I/O	CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually. Any port set to input can be set to use a pull-up resistor or not by a program. P1_0 to P1_3 also function as LED drive ports.
Input port	P4_2, P4_6, P4_7	I	Input-only ports

I: Input O: Output

I/O: Input and output

Pin Name Information by Pin Number of PLSP0020JB-A, PRDP0020BA-A packages Table 1.6

Pin	Control	Port	I/O Pin Functions for Peripheral Modules			
Number	Pin	FUIL	Interrupt	Timer	Serial Interface	Comparator
1		P3_5		CMP1_2		
2		P3_7		CNTR0	TXD1	
3	RESET					
4	XOUT	P4_7				
5	VSS/AVSS					
6	XIN	P4_6				
7	VCC/AVCC					
8	MODE					
9		P4_5	ĪNT0		RXD1	
10		P1_7	ĪNT10	CNTR00		
11		P1_6			CLK0	
12		P1_5	ĪNT11	CNTR01	RXD0	
13		P1_4			TXD0	
14		P1_3	KI3	TZOUT		AN11
15		P1_2	KI2	CMP0_2		AN10
16	VREF	P4_2				
17		P1_1	KI1	CMP0_1		AN9
18		P1_0	KI0	CMP0_0		AN8
19		P3_3	ĪNT3	TCIN/CMP1_0		
20		P3_4		CMP1_1		

4. Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 4.1 to 4.4 list the special function registers.

Table 4.1 SFR Information (1)⁽¹⁾

Address	Register	Symbol	After reset
0000h	rvegistei	Syllibol	Alter reset
0000h			
0001h			
0002H			
	Draggagy Mada Dagistor O	PM0	006
	Processor Mode Register 0		00h
	Processor Mode Register 1	PM1	00h
0006h	System Clock Control Register 0	CM0	01101000b
	System Clock Control Register 1	CM1	00100000b
0008h			
	Address Match Interrupt Enable Register	AIER	00h
	Protect Register	PRCR	00h
000Bh			
	Oscillation Stop Detection Register	OCD	00000100b
000Dh	Watchdog Timer Reset Register	WDTR	XXh
000Eh	Watchdog Timer Start Register	WDTS	XXh
000Fh	Watchdog Timer Control Register	WDC	00011111b
0010h	Address Match Interrupt Register 0	RMAD0	00h
0011h			00h
0012h			X0h
0012h			7.0
	Address Match Interrupt Register 1	RMAD1	00h
0014II 0015h	Address mater interrupt register 1	KIVIAD I	00h
0016h			X0h
0017h			
0018h			
0019h			
001Ah			
001Bh			
	Count Source Protection Mode Register	CSPR	00h
001Dh			
001Eh	INT0 Input Filter Select Register	INT0F	00h
001Fh	THE INDICE THE COLOUR PROJECT		
	High-Speed On-Chip Oscillator Control Register 0	HRA0	00h
	High-Speed On-Chip Oscillator Control Register 1	HRA1	
002111 0022h	High-Speed On-Chip Oscillator Control Register 2	HRA2	When shipping 00h
	High-Speed On-Chip Oscillator Control Register 2	HRA2	oon
0023h			
002Ah			
002Bh			
002Ch			
002Dh			
002Eh			
002Fh			
0030h			
	Voltage Detection Register 1 ⁽²⁾	VCA1	00001000b
	Voltage Detection Register 2 ⁽²⁾	VCA2	00h ⁽³⁾
	Takaga Datoolion Rogiotol E. /	1 3.12	01000000b ⁽⁴⁾
00335			01000000000
0033h			
0034h			
0035h			
0036h	Voltage Monitor 1 Circuit Control Register (2)	VW1C	0000X000b ⁽³⁾
			0100X001b ⁽⁴⁾
0037h	Voltage Monitor 2 Circuit Control Register (5)	VW2C	00h
0038h	5 .0		
0039h			
0033H			
003An			
003Ch			
003Dh			
003Eh 003Fh			
			1

X: Undefined

- 1. The blank regions are reserved. Do not access locations in these regions.
- 2. Software reset, watchdog timer reset, and voltage monitor 2 reset do not affect this register.
- 3. After hardware reset.
- 4. After power-on reset or voltage monitor 1 reset.
- 5. Software reset, watchdog timer reset, and voltage monitor 2 reset do not affect b2 and b3.



SFR Information (3)⁽¹⁾ Table 4.3

Address	Register	Symbol	After reset
0080h	Timer Z Mode Register	TZMR	00h
0081h			
0082h			
0083h			
0084h	Timer Z Waveform Output Control Register	PUM	00h
0085h	Prescaler Z Register	PREZ	FFh
0086h	Timer Z Secondary Register	TZSC	FFh
	Timer Z Primary Register		
0087h	Timer Z Primary Register	TZPR	FFh
0088h			
0089h			
008Ah	Timer Z Output Control Register	TZOC	00h
008Bh	Timer X Mode Register	TXMR	00h
008Ch	Prescaler X Register	PREX	FFh
008Dh	Timer X Register	TX	FFh
008Eh	Timer Count Source Setting Register	TCSS	00h
008Fh	3 - 3 - 1 - 1 - 1 - 1 - 1 - 1 - 1 - 1 -		
0090h	Timer C Register	TC	00h
0090H	Timer & register	10	00h
			0011
0092h			
0093h			
0094h			
0095h			
0096h	External Input Enable Register	INTEN	00h
0097h			
0098h	Key Input Enable Register	KIEN	00h
0099h	, , , ,		
009Ah	Timer C Control Register 0	TCC0	00h
009Bh	Timer C Control Register 1	TCC1	00h
009Bh	Capture, Compare 0 Register	TMO	00h
	Capture, Compare o Register	TIMO	
009Dh			00h ⁽²⁾
009Eh	Compare 1 Register	TM1	FFh
009Fh			FFh
00A0h	UART0 Transmit/Receive Mode Register	U0MR	00h
00A1h	UART0 Bit Rate Register	U0BRG	XXh
00A2h	UART0 Transmit Buffer Register	UOTB	XXh
00A3h			XXh
00A4h	UART0 Transmit/Receive Control Register 0	U0C0	00001000b
00/(4ff	UART0 Transmit/Receive Control Register 1	U0C1	00001000b
00A6h	UART0 Receive Buffer Register	UORB	XXh
00A7h			XXh
00A8h	UART1 Transmit/Receive Mode Register	U1MR	00h
00A9h	UART1 Bit Rate Register	U1BRG	XXh
00AAh	UART1 Transmit Buffer Register	U1TB	XXh
00ABh			XXh
00ACh	UART1 Transmit/Receive Control Register 0	U1C0	00001000b
00ADh	UART1 Transmit/Receive Control Register 1	U1C1	00000010b
00AEh	UART1 Receive Buffer Register	U1RB	XXh
00AEn	- Common Parior Regional	O IND	XXh
	LIART Transmit/Pagaiya Control Pagister 2	LICON	
00B0h	UART Transmit/Receive Control Register 2	UCON	00h
00B1h			
00B2h			
00B3h			
00B4h			
00B5h			
00B6h			
00B7h	<u> </u>	+	
00B8h	<u> </u>	<u> </u>	
00B8h	<u> </u>	<u> </u>	
00BAh			
00BBh			
00BCh			
0.000			
00BDh			
00BDh 00BEh			

X: Undefined

- The blank regions are reserved. Do not access locations in these regions.
 When the output compare mode is selected (the TCC13 bit in the TCC1 register = 1), the value is set to FFFF16.

SFR Information (4)⁽¹⁾ Table 4.4

DOCCOR	Address	Register	Symbol	After reset
0002h 0003h 0003	00C0h			
9003h				
00C4h 00C8h 00C8h 00C8h 00C7h 00C7h 00C7h 00C7h 00C2h 00C7h 00C2h 00C7h 00C7h 00C7h 00C7h 00C7h 00D9h 00D9h 00D9h <td></td> <td></td> <td></td> <td></td>				
0005h				
000C6h	00C4h			
00C7h 00C8h 00C8h 00C8h 00D0h 00D0h 00D1h 00D0h 00D2h AD Control Register 0 00D5h 00D0h 00D7h AD Control Register 0 00D8h 00D0h 00D8h 00D0h 00D8h 00D0h 00D8h 00D0h 00D0h 00D0h 00D0h 00D0h 00E0h 00D0h 00E0h 00C8h 00E3h 00F1 Port P3 Register 00E3h Port P1 Register 00E3h Port P3 Register 00E3h Port P3 Register 00E3h Port P3 Port P3 Register 00E4h 00E5h 00E5h Port P3 Registe				
0005h 0005				
0005h 0006h 0006				
00Cbh 00Cbh 00Cbh 00Cbh 00Cbh 00Cbh 00Cbh 00Cbh 00D0bh 00D0bh 00D2h 00D3h 00D3h AD Control Register 2 00D6h ADCON0 00D8h AD Control Register 0 00D8h ADCON1 00D8h ADCON1 00D8h ADCON1 00D8h ADCON1 00D8h ADCON1 00D8h ADCON1 00D8h ODCh 00Eh Port P1 Register 00Eh Port P2 Register 00Eh Port P3 Direction Register 00Eh Port P3 Direction Register	00C9h			
00CCh 00CEh 00CCh 00CEh 00CCh 00CH 00D0h 00D0h 00D1h 00D1h 00D3h 00D3h 00D3h AD Control Register 2 00D4h AD Control Register 1 00D4h AD Control Register 1 00D7h AD Control Register 1 00D4h AD CON1 00D4h 00D8h 00D4h 00D8h 00D4h 00D8h 00D4h 00D8h 00D4h 00D8h 00D4h 00D8h 00D5h 00D8h 00D6h 00D8h 00E0h 00D8h 00E1h 00E2h 00E2h 00E3h 00E3h Port P1 Direction Register 00E3h Port P2 Direction Register 00E4h Port P3 Brecition Register 00E6h Port P4 Direction Register 00E6h Port P4 Direction Register 00E6h 00E6h 00E6h 00E6h				
000Cbh 00CFh 00Cbh 00CPh 00Cbh 00Ch 00Dlah 00Dlah 00Dlah AD Control Register 2 00Dsh AD Control Register 0 00Dsh AD Control Register 1 00Dbh AD Control Register 1 00Dsh AD Control Register 1 00Dsh ADCON1 00Dsh 00Dsh 00Esh 00Esh 00Esh Port P1 Direction Register 00Esh Port P3 Direction Register 00Esh Port P4 Register 00Esh Port P4 Register 00Esh Port P5 Direction Register 00Esh Port P5 Dir				
00CEh 00Ch 00DOh 00DOh 00D1h 00D3h 00D3h 00D3h 00D3h AD Control Register 2 00D3h AD Control Register 1 00D4h AD COND 00D4h AD COND 00D4h 00DAn 00D4h 00DAn 00D4h 00DAn 00D4h 00DAn 00D5h 00DAn 00D4h 00DAn 00D5h 00DAn 00E3h 00FD 00E3h Pot P3 Register 00E4h 00E3h 00E5h Pot P3 Direction Register P3 00E4h 00E3h 00E4h 00E3h 00E4h 00E3h				
00CPh 00D0h 00D1h 00D1h 00D2h 00D0h 00D3h AD Control Register 2 00h 00D3h AD Control Register 0 00000h 00D3h AD Control Register 1 00h 00D3h AD Control Register 1 00h 00D3h 00D3h 00h 00D4h 00D4h 00h 00D4h 00D4h 00h 00D5h 00D6h 00h 00D6h 00D6h 00h 00D6h 00D6h 00h 00D6h 00D6h 00h 00E3h 00Fh 00h 00E3h Port P1 Register P1 XXh 00E3h Port P3 Register P3 XXh 00E3h Port P3 Register P3 00h 00E3h Port P3 Register P4 XXh 00E3h Port P4 Direction Register P3 00h 00E4h Port P3 Direction Register P4 00h 00E4h Port				
00010h				
00D1h 00D2h 00D2h 0D0h 00D3h AD Control Register 2 ADCON2 00h 00D5h AD Control Register 0 ADCON0 000000XXb 00D7h AD Control Register 1 ADCON1 00h 00D8h 00D0h 00h 00h 00D8h 00D0h 00D0h 00D0h 00D0h 00D0h 00D0h 00D0h 00D0h 00D0h 00D0h 00D0h 00D0h 00D0h 00D0h 00D0h 00D0h 00D0h 00D0h 00D0h 00D2h 00D0h 00D0h 00D0h 00D2h 00D0h 00D0h 00D0h 00E3h Port P1 Register P1 XXh 00E3h Port P3 Register P3 XXh 00E3h Port P3 Register P3 XXh 00E3h Port P4 Direction Register P3 00h 00E3h Port P4 Direction Register P4 00h 00E4h <t< td=""><td></td><td></td><td></td><td></td></t<>				
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00D4h AD Control Register 2 ADCON2 00h 00D5h AD Control Register 0 ADCON0 000000XXXb 00D7h AD Control Register 1 ADCON1 00h 00D8h 00D8h 00DA 00DA 00D8h 00DA 00DA 00DA 00D5h 00DBh 00DBh 00DBh 00D5h 00DBh 00DBh 00DBh 00D5h 00DBh 00DBh 00DBh 00D6h 00DBh 00DBh 00DBh 00E3h Port P1 Register P1 XXh 00E3h Port P3 Register P3 XXh 00E4h P0T P3 Direction Register P03 00h 00E8h Port P4 Register P4 XXh 00E8h P0T P4 Register P0 00h 00E8h P0T P4 Regis				
00D4h AD Control Register 2 ADCON2 00h 00D5h AD Control Register 0 ADCON0 000000XXXb 00D7h AD Control Register 1 ADCON1 00h 00D8h 00D8h 00DA 00DA 00D8h 00DA 00DA 00DA 00D5h 00DBh 00DBh 00DBh 00D5h 00DBh 00DBh 00DBh 00D5h 00DBh 00DBh 00DBh 00D6h 00DBh 00DBh 00DBh 00E3h Port P1 Register P1 XXh 00E3h Port P3 Register P3 XXh 00E4h P0T P3 Direction Register P03 00h 00E8h Port P4 Register P4 XXh 00E8h P0T P4 Register P0 00h 00E8h P0T P4 Regis	00D3h			
00D6h A/D Control Register 0 ADCON0 00000XXXb 00D7h A/D Control Register 1 ADCON1 000h 00D8h 00DAh 00DAh 00DAh 00DBh 00DBh 00DBh 00DBh 00DCh 00DCh 00DCh 00DBh 00DDh 00DBh 00DBh 00DBh 00DFh 00DFh 00DBh 00DBh 00E1h 00E1h 00DBh 00DBh 00E2h 00E3h 00E3h 00DBh 00E3h Port P1 Direction Register PD1 00h 00E4h 00E3h Port P3 Register P3 XXh 00E6h 00E7h 00H 00E8h 00H 00E8h Port P4 Register P4 XXh 00E8h Port P4 Direction Register PD4 00h 00E8h 00E0h 00H 00H 00E8h 00E0h 00H 00H 00E0h 00E0h 00H 00H 00E0h <t< td=""><td>00D4h</td><td>A/D Control Register 2</td><td>ADCON2</td><td>00h</td></t<>	00D4h	A/D Control Register 2	ADCON2	00h
00DRh A/D Control Register 1 00h 00D8h 00D9h 00DAh 00DBh 00DCh 00DCh 00DCh 00DCh 00DEh 00DEh 00Eh 00Eh 00Eh <t< td=""><td></td><td></td><td></td><td></td></t<>				
00D8h 00DAh 00DAh 00DAh 00DBh 00DCh 00DDh 00DDh 00DDh 00DDh 00DFh 00DFh 00DFh 00DFh 00E1h Port P1 Register 00E2h 00E3h 00E3h Port P1 Direction Register 00E3h Port P2 Breston Register 00E6h Port P3 Direction Register 00E8h Port P4 Register 00E8h Port P4 Direction Register 00E8h Port P4 Direction Register 00E8h Port P5 Direction Register 00E8h Port P6 Direction Register 00E8h Port P7 Direction Register 00E8h Port P8 Direction Register 00E2h Oberth 00E2h Oberth 00E2h Oberth 00E2h Oberth 00E2h Oberth 00F3h Oberth 00F4h Oberth 00F5h Oberth 00F6h Oberth <t< td=""><td>00D6h</td><td>A/D Control Register 0</td><td>ADCON0</td><td></td></t<>	00D6h	A/D Control Register 0	ADCON0	
00D9h 00DBh 00DBh 00DBh 00DCh 00DCh 00DEh 00DEh 00DFh 00DFh 00E1h 00E1h 00E2h 00E3h 00E3h Port P1 Direction Register 00E3h Port P2 Direction Register 00E3h Port P3 Register 00E6h Port P4 Register 00E7h Port P4 Register 00E8h Port P4 Register 00E8h Port P4 Register 00E8h Port P4 Direction Register 00E8h Port P4 Direction Register 00E8h Port P4 Direction Register 00E8h Port P5 P4 Direction Register 00E8h Port P6 Register 00E9h Port P6 Register 00E9h Port P7 Register 00E9h Port P8 Register 00E9h Port P8 Register 00F8h Port P8 Register 00F8h Port P8 Register 00F8h Port P8 Register 00F8h Port P8 Register <t< td=""><td></td><td>A/D Control Register 1</td><td>ADCON1</td><td>uun</td></t<>		A/D Control Register 1	ADCON1	uun
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01B5h Flash Memory Control Register 1 FMR1 1000000Xb 01B6h 01B7h Flash Memory Control Register 0 FMR0 00000001b		aaanory control regional 4		0.000000
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01B7h Flash Memory Control Register 0 FMR0 00000001b	01B6h	-		
0FFFFh Optional Function Select Register OFS (Note 2)	01B7h	Flash Memory Control Register 0	FMR0	00000001b
UFFFF Optional Function Select Register OFS (Note 2)				
	0FFFFh	Optional Function Select Register	OFS	(Note 2)

X: Undefined NOTES:

- The blank regions, 0100h to 01B2h and 01B8h to 02FFh are all reserved. Do not access locations in these regions.
 The OFS register cannot be changed by a program. Use a flash programmer to write to it.

Table 5.4 Flash Memory (Program ROM) Electrical Characteristics

Cymahal	Darameter	Conditions		Lloit		
Symbol	Parameter	Conditions	Min.	Тур.	9 97+CPU clock × 6 cycles - 3+CPU clock × 4 cycles 5.5 60	Unit
=	Program/erase endurance ⁽²⁾	R8C/18 Group	100(3)	-	=	times
		R8C/19 Group	1,000(3)	-	-	times
-	Byte program time		ī	50	400	μS
=	Block erase time		-	0.4	9	S
td(SR-SUS)	Time delay from suspend request until suspend		=	=		μS
_	Interval from erase start/restart until following suspend request		650	=	-	μS
_	Interval from program start/restart until following suspend request		0	=	-	ns
=	Time from suspend until program/erase restart		=	=		μS
_	Program, erase voltage		2.7	_	5.5	V
-	Read voltage		2.7	-	5.5	V
=	Program, erase temperature		0	-	60	°C
=	Data hold time ⁽⁸⁾	Ambient temperature = 55 °C	20	-	=	year

- 1. Vcc = 2.7 to 5.5 V at Topr = 0 to 60 °C, unless otherwise specified.
- 2. Definition of programming/erasure endurance
 - The programming and erasure endurance is defined on a per-block basis.
 - If the programming and erasure endurance is n (n = 100 or 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one. However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
- 3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
- 4. If emergency processing is required, a suspend request can be generated independent of this characteristic. In that case the normal time delay to Suspend can be applied to the request. However, we recommend that a suspend request with an interval of less than 650 μs is only used once because, if the suspend state continues, erasure cannot operate and the incidence of erasure error rises.
- 5. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. In addition, averaging the number of erase operations between block A and block B can further reduce the effective number of rewrites. It is also advisable to retain data on the erase count of each block and limit the number of erase operations to a certain number.
- 6. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
- 7. Customers desiring programming/erasure failure rate information should contact their Renesas technical support representative.
- 8. The data hold time includes time that the power supply is off or the clock is not supplied.

Cumbal	Doromotor	Conditions	Standard			Unit
Symbol Parameter - Program/erase endurance(2) - Byte program time (Program/erase endurance ≤ 1,000 times) - Byte program time (Program/erase endurance > 1,000 times) - Block erase time (Program/erase endurance ≤ 1,000 times) - Block erase time (Program/erase endurance > 1,000 times) td(SR-SUS) Time delay from suspend request until suspend - Interval from erase start/restart until following suspend request	Conditions	Min.	Тур.	Max.	Uniii	
=	Program/erase endurance ⁽²⁾		10,000(3)	-	-	times
=	, , ,		_	50	400	μS
_	• • •		_	65	_	μS
=			=	0.2	9	S
=			=	0.3	_	S
td(SR-SUS)			_	=	97+CPU clock × 6 cycles	μS
_			650	_	_	μS
_	Interval from program start/restart until following suspend request		0	_	_	ns
=	Time from suspend until program/erase restart		_	=	3+CPU clock × 4 cycles	μS
_	Program, erase voltage		2.7	_	5.5	V
=	Read voltage		2.7	-	5.5	V
=	Program, erase temperature		-20 ⁽⁸⁾	=	85	°C
_	Data hold time ⁽⁹⁾	Ambient temperature = 55 °C	20	-	_	year

Table 5.5 Flash Memory (Data flash Block A, Block B) Electrical Characteristics

- 1. Vcc = 2.7 to 5.5 V at Topr = -20 to 85 °C / -40 to 85 °C, unless otherwise specified.
- 2. Definition of programming/erasure endurance
 - The programming and erasure endurance is defined on a per-block basis.
 - If the programming and erasure endurance is n (n = 100 or 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one. However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
- 3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
- 4. If emergency processing is required, a suspend request can be generated independent of this characteristic. In that case the normal time delay to suspend can be applied to the request. However, we recommend that a suspend request with an interval of less than 650 μs is only used once because, if the suspend state continues, erasure cannot operate and the incidence of erasure error rises.
- 5. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erase count of each block and limit the number of erase operations to a certain number.
- 6. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
- 7. Customers desiring programming/erasure failure rate information should contact their Renesas technical support representative.
- 8. -40 °C for D version.
- 9. The data hold time includes time that the power supply is off or the clock is not supplied.

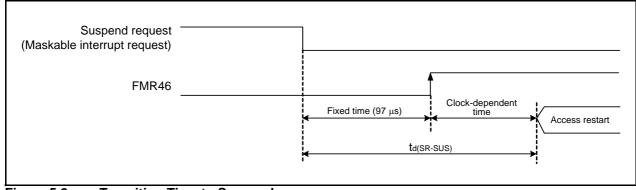


Figure 5.2 Transition Time to Suspend

Table 5.6 **Voltage Detection 1 Circuit Electrical Characteristics**

Symbol	Dorometer	Parameter Condition -		Unit		
Syllibol	Falanetei		Min.	Тур.	Max.	Offic
Vdet1	Voltage detection level ⁽³⁾		2.70	2.85	3.00	V
=	Voltage detection circuit self power consumption	VCA26 = 1, Vcc = 5.0 V	=	600	-	nA
td(E-A)	Waiting time until voltage detection circuit operation starts ⁽²⁾		=	=	100	μS
Vccmin	MCU operating voltage minimum value		2.7	_	_	V

- 1. The measurement condition is Vcc = 2.7 V to 5.5 V and T_{opr} = -40°C to 85 °C.
- 2. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.
- 3. Ensure that Vdet2 > Vdet1.

Table 5.7 **Voltage Detection 2 Circuit Electrical Characteristics**

Symbol	Parameter	Condition		Unit		
Syllibol	Farameter	Condition	Min.	Тур.	Max.	Offic
Vdet2	Voltage detection level ⁽⁴⁾		3.00	3.30	3.60	V
=	Voltage monitor 2 interrupt request generation time(2)		-	40	_	μS
=	Voltage detection circuit self power consumption	VCA27 = 1, Vcc = 5.0 V	=	600	=	nA
td(E-A)	Waiting time until voltage detection circuit operation starts ⁽³⁾		-	-	100	μS

- The measurement condition is Vcc = 2.7 V to 5.5 V and Topr = -40°C to 85 °C.
 Time until the voltage monitor 2 interrupt request is generated after the voltage passes Vdet1.
- 3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.
- 4. Ensure that Vdet2 > Vdet1.

Table 5.8 Reset Circuit Electrical Characteristics (When Using Voltage Monitor 1 Reset)

Symbol	Parameter	Condition	,	Standard		
			Min.	Тур.	Max.	
Vpor2	Power-on reset valid voltage	$-20^{\circ}C \leq Topr \leq 85^{\circ}C$	-	-	Vdet1	V
tw(Vpor2-Vdet1)	Supply voltage rising time when power-on reset is deasserted ⁽¹⁾	$ -20^{\circ}C \leq Topr \leq 85^{\circ}C, \\ t_{w(por2)} \geq 0s^{(3)} $	I	I	100	ms

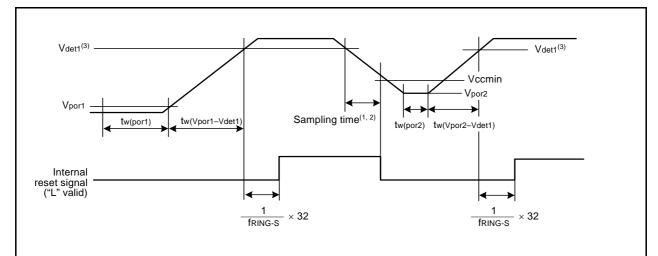
- 1. This condition is not applicable when using with $Vcc \ge 1.0 \text{ V}$.
- 2. When turning power on after the time to hold the external power below effective voltage (Vpor1) exceeds10 s, refer to Table 5.9 Reset Circuit Electrical Characteristics (When Not Using Voltage Monitor 1 Reset).
- 3. tw(por2) is the time to hold the external power below effective voltage (Vpor2).

Reset Circuit Electrical Characteristics (When Not Using Voltage Monitor 1 Reset) Table 5.9

Symbol	Parameter	Condition		Unit		
			Min.	Тур.	Max.	
Vpor1	Power-on reset valid voltage	-20°C ≤ Topr ≤ 85°C	=	=	0.1	V
tw(Vpor1-Vdet1)	Supply voltage rising time when power-on reset is deasserted	$0^{\circ}C \leq Topr \leq 85^{\circ}C,$ $tw(por1) \geq 10 s^{(2)}$	-	-	100	ms
tw(Vpor1-Vdet1)	Supply voltage rising time when power-on reset is deasserted	$ -20^{\circ}C \leq Topr < 0^{\circ}C, \\ tw(por1) \geq 30 \ s^{(2)} $	-	=	100	ms
tw(Vpor1-Vdet1)	Supply voltage rising time when power-on reset is deasserted	$ -20^{\circ}C \leq Topr < 0^{\circ}C, $ $ tw(por1) \geq 10 \ s^{(2)} $	-	=	1	ms
tw(Vpor1-Vdet1)	Supply voltage rising time when power-on reset is deasserted	$0^{\circ}C \leq Topr \leq 85^{\circ}C,$ $tw(por1) \geq 1 s^{(2)}$	-	-	0.5	ms

NOTES:

- 1. When not using voltage monitor 1, use with $Vcc \ge 2.7 \text{ V}$.
- 2. tw(por1) is the time to hold the external power below effective voltage (Vpor1).



- 1. Hold the voltage inside the MCU operation voltage range (Vccmin or above) within the sampling time.
- The sampling clock can be selected. Refer to 7. Voltage Detection Circuit for details.
 Vdet1 indicates the voltage detection level of the voltage detection 1 circuit. Refer to 7. Voltage Detection Circuit for details.

Figure 5.3 **Reset Circuit Electrical Characteristics**

Table 5.12 Electrical Characteristics (1) [Vcc = 5 V]

Symbol	Parameter		Cond	Condition		Standard		
,	Fala	meter	Condition		Min.	Тур.	Max.	Unit
Vон	Output "H" voltage	Except Xout	Iон = -5 mA		Vcc - 2.0	_	Vcc	V
			Ιοн = -200 μΑ		Vcc - 0.3	-	Vcc	V
		Хоит	Drive capacity HIGH	Iон = -1 mA	Vcc - 2.0	=	Vcc	V
			Drive capacity LOW	ΙΟΗ = -500 μΑ	Vcc - 2.0	-	Vcc	V
Vol	Output "L" voltage	Except P1_0 to	IoL = 5 mA	-	_	1	2.0	V
		Р1_3, Хоит	IoL = 200 μA		_	1	0.45	V
		P1_0 to P1_3	Drive capacity HIGH	IOL = 15 mA	=	=	2.0	V
			Drive capacity LOW	IOL = 5 mA	=	1	2.0	V
			Drive capacity LOW	IOL = 200 μA	-	-	0.45	V
		Хоит	Drive capacity HIGH	IOL = 1 mA	=	=	2.0	V
			Drive capacity LOW	IOL = 500 μA	=	=	2.0	V
VT+-VT-	Hysteresis	INTO, INT1, INT2, INT3, KIO, KI1, KI2, KI3, CNTRO, CNTR1, TCIN, RXD0			0.2	-	1.0	V
		RESET			0.2	_	2.2	V
lін	Input "H" current	1	VI = 5 V		_	-	5.0	μА
lı∟	Input "L" current		VI = 0 V		-	_	-5.0	μА
RPULLUP	Pull-up resistance		VI = 0 V		30	50	167	kΩ
RfXIN	Feedback resistance	XIN			-	1.0	-	ΜΩ
fring-s	Low-speed on-chip o	scillator frequency			40	125	250	kHz
VRAM	RAM hold voltage		During stop mode		2.0	-	-	V

^{1.} VCC = 4.2 to 5.5 V at Topr = -20 to 85 °C / -40 to 85 °C, f(XIN) = 20 MHz, unless otherwise specified.

Table 5.13 Electrical Characteristics (2) [Vcc = 5 V] (Topr = -40 to 85 $^{\circ}$ C, unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Тур.	Max.	01110
Icc	Power supply current (Vcc = 3.3 to 5.5 V) Single-chip mode, output pins are open,	High-speed mode	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	I	9	15	mA
	other pins are Vss, comparator is stopped		XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	=	8	14	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	I	5	ı	mA
		Medium- speed mode	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	l	4	ı	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	=	3	_	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	-	2	-	mA
		High-speed on-chip oscillator mode	Main clock off High-speed on-chip oscillator on = 8 MHz Low-speed on-chip oscillator on = 125 kHz No division	_	4	8	mA
			Main clock off High-speed on-chip oscillator on = 8 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	ı	1.5	ı	mA
		Low-speed on-chip oscillator mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8 FMR47 = 1	1	110	300	μΑ
		Wait mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = 0	=	40	80	μА
		Wait mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = 0	-	38	76	μА
		Stop mode	Main clock off, Topr = 25 °C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = 0	=	0.8	3.0	μА

Table 5.17 Senal Interrace	Table	5.17	Serial	Interface
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Symbol	Parameter	Stan	dard	Unit	
	raianielei	Min.	Max.	Offic	
tc(CK)	CLKi input cycle time	200	-	ns	
tW(CKH)	CLKi input "H" width	=	ns		
tW(CKL)	CLKi input "L" width	100	=	ns	
td(C-Q)	TXDi output delay time	-	50	ns	
th(C-Q)	TXDi hold time	-	ns		
tsu(D-C)	RXDi input setup time	=	ns		
th(C-D)	RXDi input hold time 90 -				

i = 0 or 1

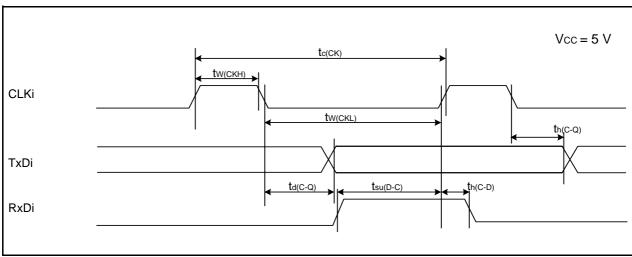


Figure 5.7 Serial Interface Timing Diagram when Vcc = 5 V

Table 5.18 External Interrupt INTO Input

Symbol	Parameter	Standard		Unit
Syllibol	Faidilletei	Min.	Max.	Offic
tW(INH)	INTO input "H" width	250 ⁽¹⁾	-	ns
tW(INL)	INTO input "L" width	250(2)	-	ns

NOTES:

- 1. When selecting the digital filter by the INT0 input filter select bit, use an INT0 input HIGH width of either (1/digital filter clock frequency x 3) or the minimum value of standard, whichever is greater.
- 2. When selecting the digital filter by the INT0 input filter select bit, use an INT0 input LOW width of either (1/digital filter clock frequency x 3) or the minimum value of standard, whichever is greater.

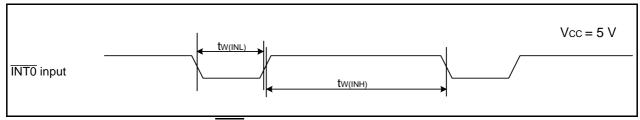


Figure 5.8 External Interrupt INTO Input Timing Diagram when Vcc = 5 V

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Electrical Characteristics (4) [Vcc = 3V] (Topr = -40 to 85 °C, unless otherwise specified.) **Table 5.20**

Symbol	Parameter	Condition		Standard			Unit
			Condition	Min.	Тур.	Max.	01110
Icc	Power supply current (Vcc = 2.7 to 3.3 V) Single-chip mode, output pins are open,	High-speed mode	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	ı	8	13	mA
	other pins are Vss, comparator is stopped		XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	ſ	7	12	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	_	5	ı	mA
	Medium- speed mode XIN = 20 MHz (square wave) High-speed on-chip oscillator on = 125 kHz Divide-by-8 XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8 XIN = 10 MHz (square wave) High-speed on-chip oscillator on = 125 kHz Divide-by-8 XIN = 10 MHz (square wave) High-speed on-chip oscillator on = 125 kHz Divide-by-8 High-speed on-chip oscillator on = 125 kHz Divide-by-8 High-speed on-chip oscillator on = 8 MHz Low-speed on-chip oscillator on = 125 kHz No division Main clock off High-speed on-chip oscillator on = 8 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8 Low-speed On-chip oscillator on = 125 kHz Divide-by-8 Low-speed Divide-by-8 FMR47 = 1	-	3		mA		
		-	2.5	-	mA		
			High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz	I	1.6	İ	mA
		on-chip oscillator	High-speed on-chip oscillator on = 8 MHz Low-speed on-chip oscillator on = 125 kHz	-	3.5	7.5	mA
			High-speed on-chip oscillator on = 8 MHz Low-speed on-chip oscillator on = 125 kHz	-	1.5	-	mA
		on-chip oscillator	High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	-	100	280	μΑ
		Wait mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = 0	-	37	74	μΑ
		Wait mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = 0	=	35	70	μΑ
		Stop mode	Main clock off, Topr = 25 °C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = 0	-	0.7	3.0	μА

Timing requirements

(Unless Otherwise Specified: Vcc = 3 V, Vss = 0 V at Ta = 25 °C) [Vcc = 3 V]

Table 5.21 XIN Input

Symbol	Parameter	Standard		Unit
Symbol	Falanielei		Max.	
tc(XIN)	XIN input cycle time	100	=	ns
twh(xin)	XIN input "H" width	40	=	ns
tWL(XIN)	XIN input "L" width	40	=	ns

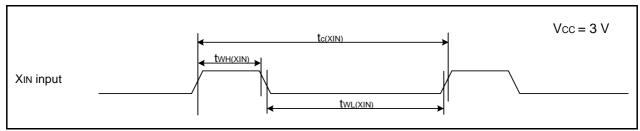


Figure 5.9 XIN Input Timing Diagram when Vcc = 3 V

Table 5.22 CNTR0 Input, CNTR1 Input, INT1 Input

Symbol	Parameter	Standard		Unit
Symbol	Falanielei		Max.	Offic
tc(CNTR0)	CNTR0 input cycle time	300	=	ns
tWH(CNTR0)	CNTR0 input "H" width	120	=	ns
tWL(CNTR0)	CNTR0 input "L" width	120	-	ns

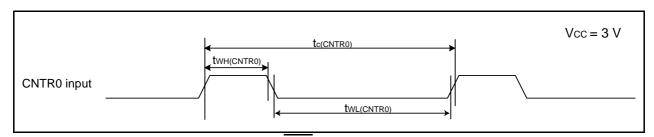


Figure 5.10 CNTR0 Input, CNTR1 Input, INT1 Input Timing Diagram when Vcc = 3 V

Table 5.23 TCIN Input, INT3 Input

Symbol	Parameter	Standard		Unit	
Symbol	Farameter		Max.	Offic	
tc(TCIN)	TCIN input cycle time	1,200(1)	-	ns	
tWH(TCIN)	TCIN input "H" width	600(2)	-	ns	
twl(tcin)	TCIN input "L" width	600(2)	_	ns	

- 1. When using the timer C input capture mode, adjust the cycle time to (1/timer C count source frequency × 3) or above.
- 2. When using the timer C input capture mode, adjust the width to (1/timer C count source frequency x 1.5) or above.

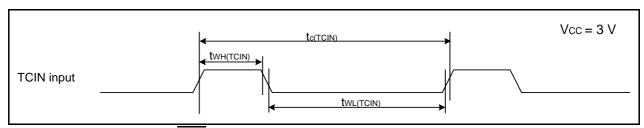


Figure 5.11 TCIN Input, INT3 Input Timing Diagram when Vcc = 3 V

REVISION HISTORY

R8C/18 Group, R8C/19 Group Datasheet

Day	Doto		Description
Rev.	Date	Page	Summary
0.10	Nov 15, 2004	-	First Edition issued
0.20	Jan 11, 2005	5, 6	Tables 1.3 and 1.4: The date updated
0.21	Apr 04, 2005	2, 3	Tables 1.1 and 1.2: Partly revised
		4	Figure 1.1: Partly revised
		5, 6	Tables 1.3 and 1.4: Partly revised
		5, 6	Figure 1.2 and 1.3: Partly revised
		7, 8	Figure 1.4 and 1.5: Partly revised
		10	Table 1.6: Partly revised
		16	Table 4.1: Partly revised
		17	Table 4.2: Partly revised
		18	Table 4.3: Partly revised
		20	Package Dimensions are revised
1.00	May 27, 2005	5, 6	Tables 1.3 and 1.4: Partly revised
		9	Table 1.5: Partly revised
		25	Table 5.9: Revised
		26	Table 5.10: Partly revised
		28	Table 5.13: Partly revised
		32	Table 5.20: Partly revised
1.10	Jun 09, 2005	26	Table 5.10: Partly revised
1.20	Nov 01, 2005	3	Table 1.2 Performance Outline of the R8C/19 Group; Flash Memory: (Data area) → (Data flash) (Program area) → (Program ROM) revised
		4	Figure 1.1 Block Diagram; "Peripheral Function" added, "System Clock Generation" → "System Clock Generator" revised
		6	Table 1.4 Product Information of R8C/19 Group; ROM capacity: "Program area" → "Program ROM", "Data area" → "Data flash" revised
		9	Table 1.5 Pin Description; Power Supply Input: "VCC/AVCC" → "VCC", "VSS/AVSS" → "VSS" revised Analog Power Supply Input: added
		11	Figure 2.1 CPU Register; "Reserved Area" → "Reserved Bit" revised
		13	2.8.10 Reserved Area; "Reserved Area" → "Reserved Bit" revised
		15	3.2 R8C/19 Group, Figure 3.2 Memory Map of R8C/19 Group; "Data area" → "Data flash", "Program area" → "Program ROM" revised

F	REVISION HISTORY		₹Y	R8C/18 Group, R8C/19 Group Datasheet
Rev.	Date			Description
Nev.	Date	Page		Summary
1.20	Nov 01, 2005	16	0009h: 000Ah:	SFR Information(1); "XXXXXX00b" → "00h" "00XXX000b" → "00h" "XXXXX000b" → "00h" revised
		18	0085h: 0086h: 0087h: 008Ch: 008Dh:	SFR Information(3); "Prescaler Z" → "Prescaler Z Register" "Timer Z Secondary" → "Timer Z Secondary Register" "Timer Z Primary" → "Timer Z Primary Register" "Prescaler X" → "Prescaler X Register" "Timer X" → "Timer X Register" 0091h: "Timer C" → "Timer C Register" revised
		22		Flash Memory (Program ROM) Electrical Characteristics; 3 and 5 revised, NOTE8 deleted
		23		Flash Memory (Data flash Block A, Block B) Electrical ristics; NOTES 1 and 3 revised
		25		Reset Circuit Electrical Characteristics (When Using Voltage Reset); NOTE 2 revised
		26	Character "High-S "High-S	O High-speed On-Chip Oscillator Circuit Electrical ristics; peed On-Chip Oscillator" → peed On-Chip Oscillator Frequency" revised 2, 3 added
		28		3 Electrical Characteristics (2) [Vcc = 5V]; deleted
		32		D Electrical Characteristics (4) [Vcc = 3V]; I deleted
1.30	Dec 16, 2005	_	Products	of PWQN0028KA-B package included
		5, 6	Table 1.3,	Table 1.4 revised
		24		Flash Memory (Program ROM) Electrical Characteristics; pient temperature
		25		Flash Memory (Data flash Block A, Block B) Electrical ristics; Ta → Ambient temperature
		30, 34	Table 5.13	3, Table 5.20; The title revised, Condition of Stop Mode added
		32, 36	Table 5.17	7, Table 5.24; td(C-Q) and tsu(D-C) revised
		37, 38	Package	Dimensions revised
1.40	Apr 14, 2006	2, 3	•	Table 1.2; : Internal 8 → 10 sources,
		5, 6	Table 1.3,	Table 1.4; Type No. added, deleted
		16, 17	Figure 3.1	, Figure 3.2; Part Number added, deleted
		24, 25	Table 5.4, Conditions	Table 5.5; s: VCC = 5.0 V at Topr = 25 °C deleted