Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	SIO, UART/USART
Peripherals	LED, POR, Voltage Detect, WDT
Number of I/O	13
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-WFQFN Exposed Pad
Supplier Device Package	28-HWQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21184np-u0

1.4 Product Information

Table 1.3 lists Product Information for R8C/18 Group and Table 1.4 lists Product Information for R8C/19 Group.

Table 1.3   Product Information for R8C/18 Group   **Current of Apr. 2006**

Type No.	ROM Capacity	RAM Capacity	Package Type	Remarks
R5F21181SP	4 Kbytes	384 bytes	PLSP0020JB-A	Flash memory version
R5F21182SP	8 Kbytes	512 bytes	PLSP0020JB-A	
R5F21183SP	12 Kbytes	768 bytes	PLSP0020JB-A	
R5F21184SP	16 Kbytes	1 Kbyte	PLSP0020JB-A	
R5F21181DSP (D)	4 Kbytes	384 bytes	PLSP0020JB-A	D version
R5F21182DSP (D)	8 Kbytes	512 bytes	PLSP0020JB-A	
R5F21183DSP (D)	12 Kbytes	768 bytes	PLSP0020JB-A	
R5F21184DSP (D)	16 Kbytes	1 Kbyte	PLSP0020JB-A	
R5F21181DD	4 Kbytes	384 bytes	PRDP0020BA-A	Flash memory version
R5F21182DD	8 Kbytes	512 bytes	PRDP0020BA-A	
R5F21183DD	12 Kbytes	768 bytes	PRDP0020BA-A	
R5F21184DD	16 Kbytes	1 Kbyte	PRDP0020BA-A	
R5F21182NP	8 Kbytes	512 bytes	PWQN0028KA-B	Flash memory version
R5F21183NP	12 Kbytes	768 bytes	PWQN0028KA-B	
R5F21184NP	16 Kbytes	1 Kbyte	PWQN0028KA-B	

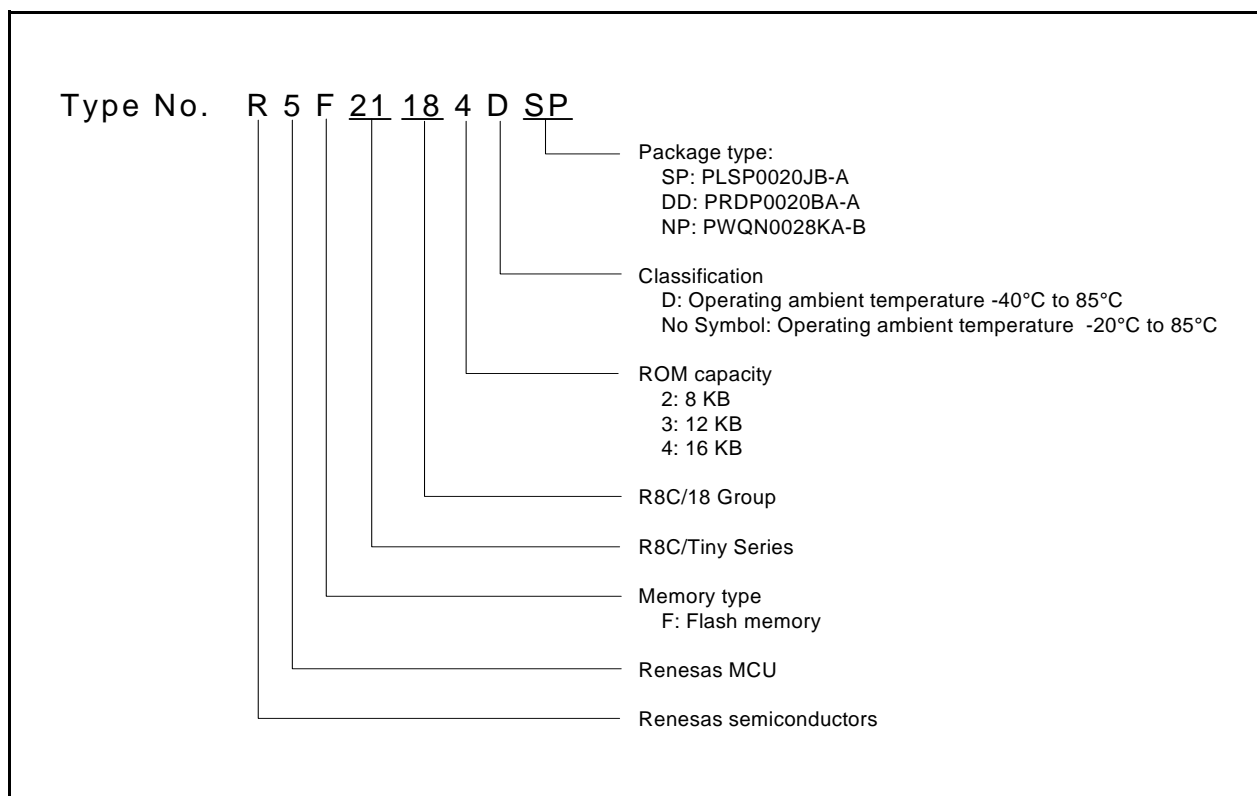(D): Under Development

Figure 1.2   Type Number, Memory Size, and Package of R8C/18 Group

1.5   Pin Assignments

Figure 1.4 shows Pin Assignments for PLSP0020JB-A Package (Top View), Figure 1.5 shows Pin Assignments for PRDP0020BA-A Package (Top View) and Figure 1.6 shows Pin Assignments for PWQN0028KA-B Package (Top View).
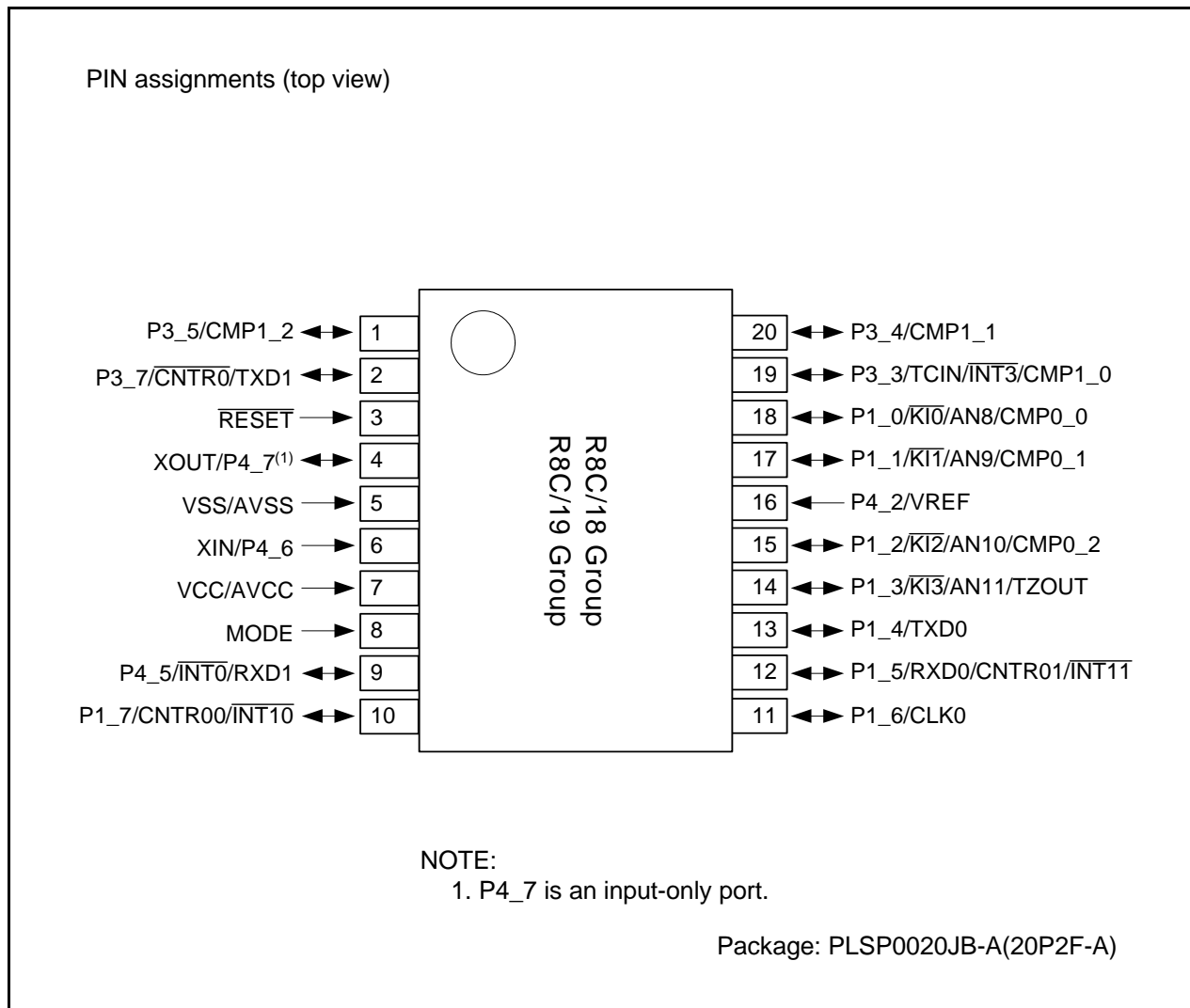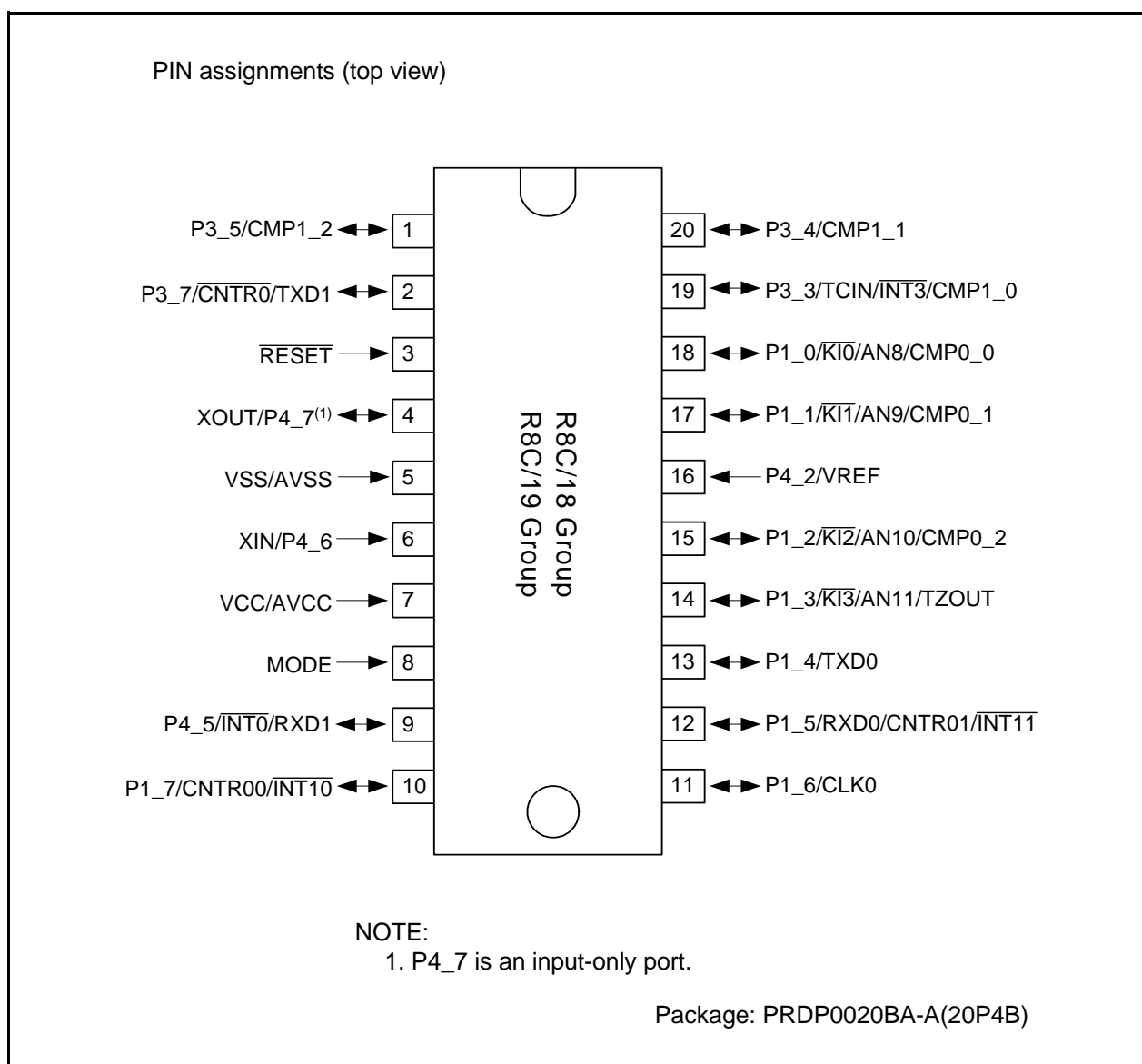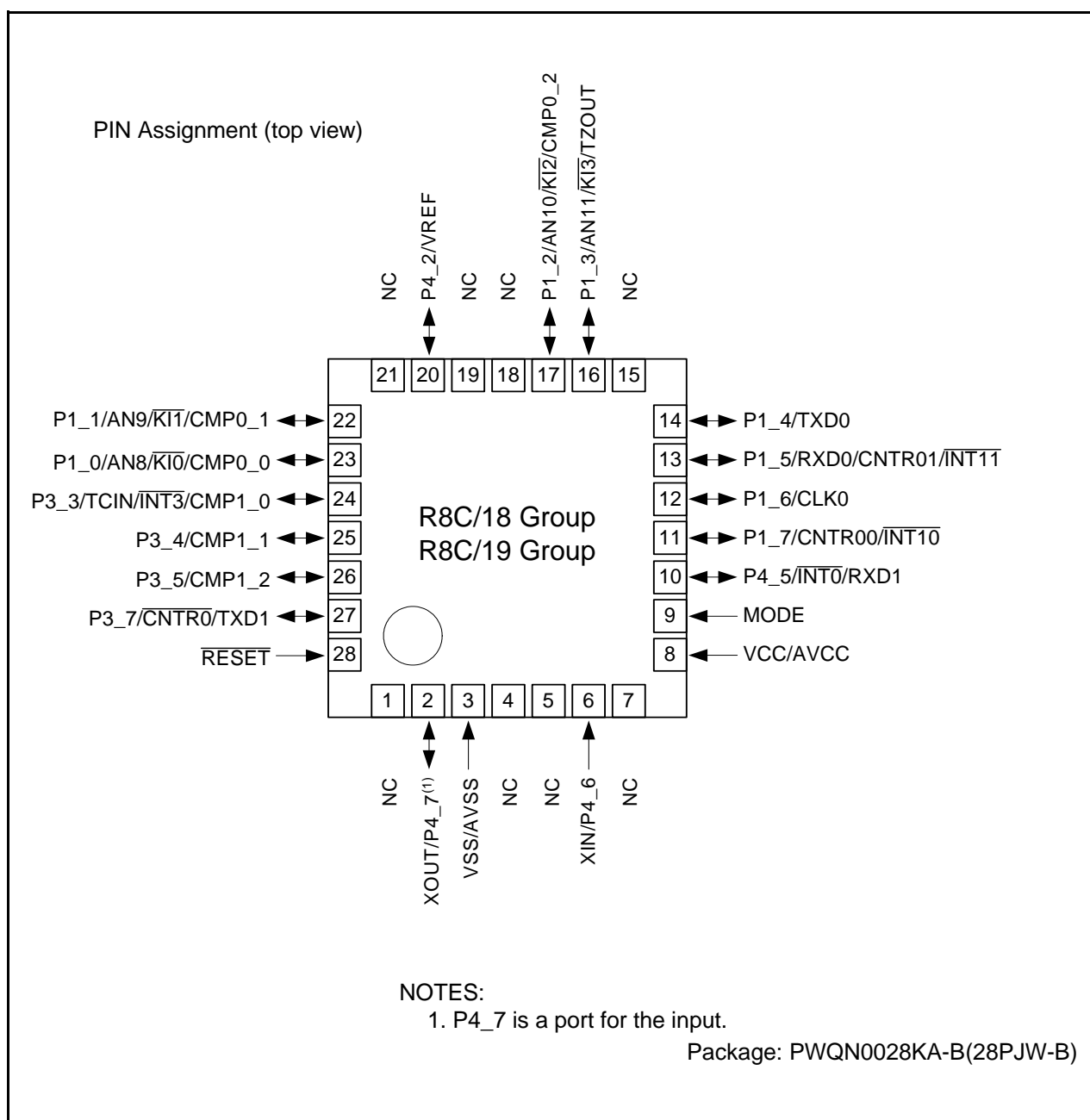
PIN assignments (top view)

Pin	Signal		Pin	Signal
1	P3_5/CMP1_2		20	P3_4/CMP1_1
2	P3_7/$\overline{\text{CNTR0}}$/TXD1		19	P3_3/TCIN/$\overline{\text{INT3}}$/CMP1_0
3	$\overline{\text{RESET}}$		18	P1_0/$\overline{\text{KI0}}$/AN8/CMP0_0
4	XOUT/P4_7[1]		17	P1_1/$\overline{\text{KI1}}$/AN9/CMP0_1
5	VSS/AVSS		16	P4_2/VREF
6	XIN/P4_6		15	P1_2/$\overline{\text{KI2}}$/AN10/CMP0_2
7	VCC/AVCC		14	P1_3/$\overline{\text{KI3}}$/AN11/TZOUT
8	MODE		13	P1_4/TXD0
9	P4_5/$\overline{\text{INT0}}$/RXD1		12	P1_5/RXD0/CNTR01/$\overline{\text{INT11}}$
10	P1_7/CNTR00/$\overline{\text{INT10}}$		11	P1_6/CLK0

R8C/18 Group
R8C/19 Group

NOTE:
1. P4_7 is an input-only port.

Package: PLSP0020JB-A(20P2F-A)

Figure 1.4   Pin Assignments for PLSP0020JB-A Package (Top View)

PIN assignments (top view)

P3_5/CMP1_2	1	20 P3_4/CMP1_1
P3_7/$\overline{\text{CNTR0}}$/TXD1	2	19 P3_3/TCIN/$\overline{\text{INT3}}$/CMP1_0
$\overline{\text{RESET}}$	3	18 P1_0/$\overline{\text{KI0}}$/AN8/CMP0_0
XOUT/P4_7[1]	4	17 P1_1/$\overline{\text{KI1}}$/AN9/CMP0_1
VSS/AVSS	5	16 P4_2/VREF
XIN/P4_6	6	15 P1_2/$\overline{\text{KI2}}$/AN10/CMP0_2
VCC/AVCC	7	14 P1_3/$\overline{\text{KI3}}$/AN11/TZOUT
MODE	8	13 P1_4/TXD0
P4_5/$\overline{\text{INT0}}$/RXD1	9	12 P1_5/RXD0/CNTR01/$\overline{\text{INT11}}$
P1_7/CNTR00/$\overline{\text{INT10}}$	10	11 P1_6/CLK0

R8C/18 Group
R8C/19 Group

NOTE:
1. P4_7 is an input-only port.

Package: PRDP0020BA-A(20P4B)

Figure 1.5   Pin Assignments for PRDP0020BA-A Package (Top View)

PIN Assignment (top view)

21	20	19	18	17	16	15

NC
P4_2/VREF
NC
NC
P1_2/AN10/$\overline{\text{KI2}}$/CMP0_2
P1_3/AN11/$\overline{\text{KI3}}$/TZOUT
NC

P1_1/AN9/$\overline{\text{KI1}}$/CMP0_1 ◄► 22
P1_0/AN8/$\overline{\text{KI0}}$/CMP0_0 ◄► 23
P3_3/TCIN/$\overline{\text{INT3}}$/CMP1_0 ◄► 24
P3_4/CMP1_1 ◄► 25
P3_5/CMP1_2 ◄► 26
P3_7/$\overline{\text{CNTR0}}$/TXD1 ◄► 27
$\overline{\text{RESET}}$ ─► 28

R8C/18 Group
R8C/19 Group

14 ◄► P1_4/TXD0
13 ◄► P1_5/RXD0/CNTR01/$\overline{\text{INT11}}$
12 ◄► P1_6/CLK0
11 ◄► P1_7/CNTR00/$\overline{\text{INT10}}$
10 ◄► P4_5/$\overline{\text{INT0}}$/RXD1
9 ◄─ MODE
8 ◄─ VCC/AVCC

| 1 | 2 | 3 | 4 | 5 | 6 | 7 |

NC
XOUT/P4_7[1]
VSS/AVSS
NC
NC
XIN/P4_6
NC

NOTES:
1. P4_7 is a port for the input.

Package: PWQN0028KA-B(28PJW-B)

Figure 1.6   Pin Assignments for PWQN0028KA-B Package (Top View)

Table 1.6   Pin Name Information by Pin Number of PLSP0020JB-A, PRDP0020BA-A packages

Pin Number	Control Pin	Port	I/O Pin Functions for Peripheral Modules			
			Interrupt	Timer	Serial Interface	Comparator
1		P3_5		CMP1_2		
2		P3_7		$\overline{\text{CNTR0}}$	TXD1	
3	$\overline{\text{RESET}}$					
4	XOUT	P4_7				
5	VSS/AVSS					
6	XIN	P4_6				
7	VCC/AVCC					
8	MODE					
9		P4_5	$\overline{\text{INT0}}$		RXD1	
10		P1_7	$\overline{\text{INT10}}$	CNTR00		
11		P1_6			CLK0	
12		P1_5	$\overline{\text{INT11}}$	CNTR01	RXD0	
13		P1_4			TXD0	
14		P1_3	$\overline{\text{KI3}}$	TZOUT		AN11
15		P1_2	$\overline{\text{KI2}}$	CMP0_2		AN10
16	VREF	P4_2				
17		P1_1	$\overline{\text{KI1}}$	CMP0_1		AN9
18		P1_0	$\overline{\text{KI0}}$	CMP0_0		AN8
19		P3_3	$\overline{\text{INT3}}$	TCIN/CMP1_0		
20		P3_4		CMP1_1		

2.1   Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

2.2   Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic and logic operations. A1 is analogous to A0. A1 can be combined with A0 and used as a 32-bit address register (A1A0).

2.3   Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4   Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the start address of an interrupt vector table.

2.5   Program Counter (PC)

PC is 20 bits wide, indicates the address of the next instruction to be executed.

2.6   User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointer (SP), USP, and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

2.7   Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8   Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

2.8.1   Carry Flag (C)

The C flag retains a carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

2.8.2   Debug Flag (D)

The D flag is for debugging only. Set it to 0.

2.8.3   Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

2.8.4   Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

2.8.5   Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

2.8.6   Overflow Flag (O)

The O flag is set to 1 when the operation results in an overflow; otherwise to 0.

2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts.
Interrupts are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.
The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide, assigns processor interrupt priority levels from level 0 to level 7.
If a requested interrupt has higher priority than IPL, the interrupt is enabled.

2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.

3.   Memory

3.1   R8C/18 Group

Figure 3.1 is a Memory Map of R8C/18 Group. The R8C/18 Group has 1 Mbyte of address space from addresses 00000h to FFFFFh.

The internal ROM area is allocated lower addresses, beginning with address 0FFFFh. For example, a 16-Kbyte internal ROM is allocated addresses 0C000h to 0FFFFh.

The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. They store the starting address of each interrupt routine.

The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 1-Kbyte internal RAM area is allocated addresses 00400h to 007FFh. The internal RAM is used not only for storing data but also for calling subroutines and as stacks when interrupt requests are acknowledged.

Special function registers (SFRs) are allocated addresses 00000h to 002FFh. The peripheral function control registers are allocated here. All addresses within the SFR, which have nothing allocated are reserved for future use and cannot be accessed by users.
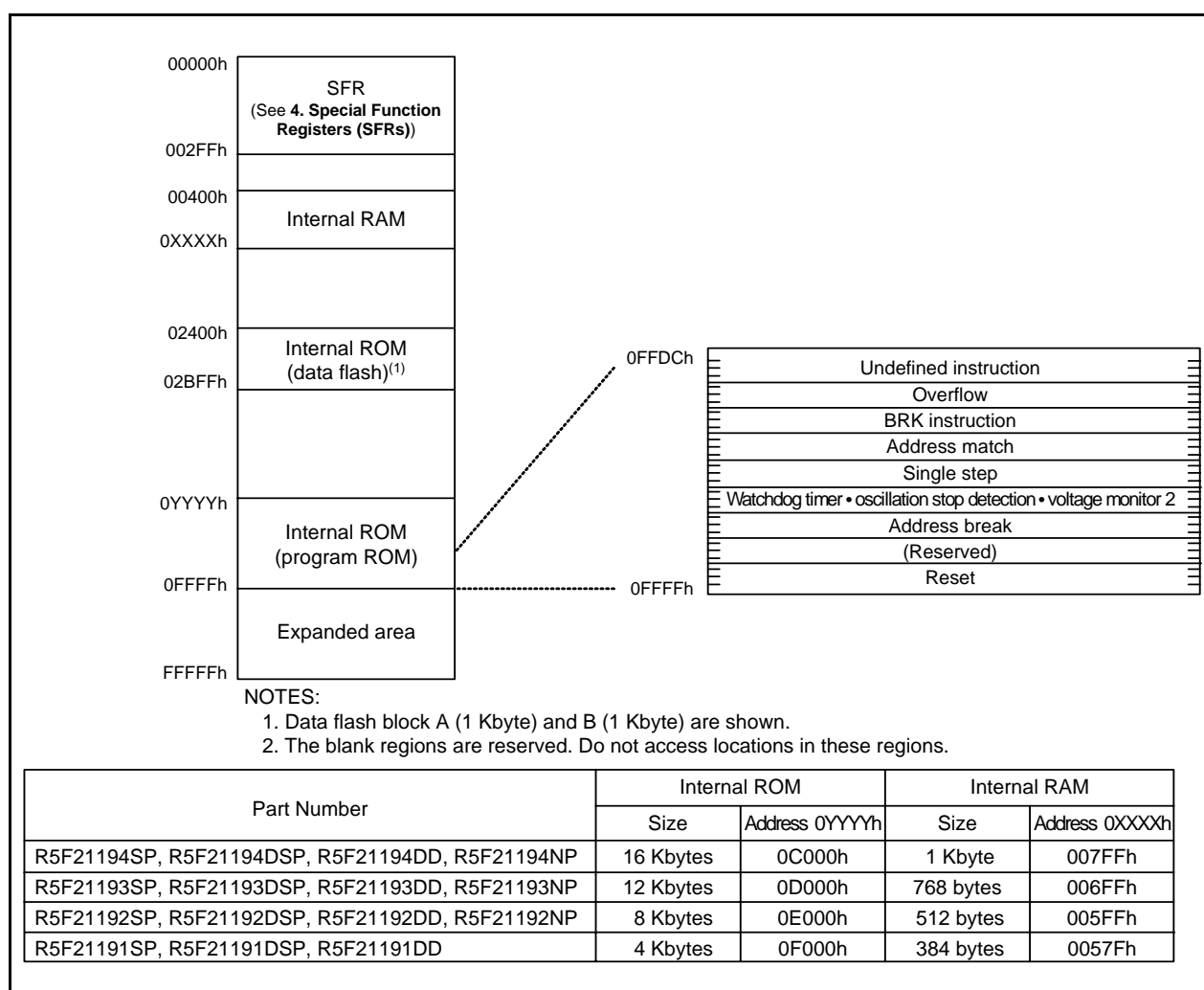

NOTE:
1. The blank regions are reserved. Do not access locations in these regions.

Part Number	Internal ROM		Internal RAM	
	Size	Address 0YYYYh	Size	Address 0XXXXh
R5F21184SP, R5F21184DSP, R5F21184DD, R5F21184NP	16 Kbytes	0C000h	1 Kbyte	007FFh
R5F21183SP, R5F21183DSP, R5F21183DD, R5F21183NP	12 Kbytes	0D000h	768 bytes	006FFh
R5F21182SP, R5F21182DSP, R5F21182DD, R5F21182NP	8 Kbytes	0E000h	512 bytes	005FFh
R5F21181SP, R5F21181DSP, R5F21181DD	4 Kbytes	0F000h	384 bytes	0057Fh

Figure 3.1   Memory Map of R8C/18 Group

3.2   R8C/19 Group

Figure 3.2 is a Memory Map of R8C/19 Group. The R8C/19 group has 1 Mbyte of address space from addresses 00000h to FFFFFh.

The internal ROM (program ROM) is allocated lower addresses, beginning with address 0FFFFh. For example, a 16-Kbyte internal ROM area is allocated addresses 0C000h to 0FFFFh.

The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. They store the starting address of each interrupt routine.

The internal ROM (data flash) is allocated addresses 02400h to 02BFFh.

The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 1-Kbyte internal RAM area is allocated addresses 00400h to 007FFh. The internal RAM is used not only for storing data but also for calling subroutines and as stacks when interrupt requests are acknowledged.

Special function registers (SFRs) are allocated addresses 00000h to 002FFh. The peripheral function control registers are allocated here. All addresses within the SFR, which have nothing allocated are reserved for future use and cannot be accessed by users.

NOTES:
1. Data flash block A (1 Kbyte) and B (1 Kbyte) are shown.
2. The blank regions are reserved. Do not access locations in these regions.

Part Number	Internal ROM		Internal RAM	
	Size	Address 0YYYYh	Size	Address 0XXXXh
R5F21194SP, R5F21194DSP, R5F21194DD, R5F21194NP	16 Kbytes	0C000h	1 Kbyte	007FFh
R5F21193SP, R5F21193DSP, R5F21193DD, R5F21193NP	12 Kbytes	0D000h	768 bytes	006FFh
R5F21192SP, R5F21192DSP, R5F21192DD, R5F21192NP	8 Kbytes	0E000h	512 bytes	005FFh
R5F21191SP, R5F21191DSP, R5F21191DD	4 Kbytes	0F000h	384 bytes	0057Fh

Figure 3.2   Memory Map of R8C/19 Group

Table 4.2 SFR Information (2)[1]

Address	Register	Symbol	After reset
0040h			
0041h			
0042h			
0043h			
0044h			
0045h			
0046h			
0047h			
0048h			
0049h			
004Ah			
004Bh			
004Ch			
004Dh	Key Input Interrupt Control Register	KUPIC	XXXXX000b
004Eh	Comparator Conversion Interrupt Control Register	ADIC	XXXXX000b
004Fh			
0050h	Compare 1 Interrupt Control Register	CMP1IC	XXXXX000b
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXXX000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXXX000b
0053h	UART1 Transmit Interrupt Control Register	S1TIC	XXXXX000b
0054h	UART1 Receive Interrupt Control Register	S1RIC	XXXXX000b
0055h			
0056h	Timer X Interrupt Control Register	TXIC	XXXXX000b
0057h			
0058h	Timer Z Interrupt Control Register	TZIC	XXXXX000b
0059h	$\overline{\text{INT1}}$ Interrupt Control Register	INT1IC	XXXXX000b
005Ah	$\overline{\text{INT3}}$ Interrupt Control Register	INT3IC	XXXXX000b
005Bh	Timer C Interrupt Control Register	TCIC	XXXXX000b
005Ch	Compare 0 Interrupt Control Register	CMP0IC	XXXXX000b
005Dh	$\overline{\text{INT0}}$ Interrupt Control Register	INT0IC	XX00X000b
005Eh			
005Fh			
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h			
006Ah			
006Bh			
006Ch			
006Dh			
006Eh			
006Fh			
0070h			
0071h			
0072h			
0073h			
0074h			
0075h			
0076h			
0077h			
0078h			
0079h			
007Ah			
007Bh			
007Ch			
007Dh			
007Eh			
007Fh			

X: Undefined
NOTE:
 1. The blank regions are reserved. Do not access locations in these regions.

Table 4.4　　　SFR Information (4)[1]

Address	Register	Symbol	After reset
00C0h	A/D Register	AD	XXh
00C1h			
00C2h			
00C3h			
00C4h			
00C5h			
00C6h			
00C7h			
00C8h			
00C9h			
00CAh			
00CBh			
00CCh			
00CDh			
00CEh			
00CFh			
00D0h			
00D1h			
00D2h			
00D3h			
00D4h	A/D Control Register 2	ADCON2	00h
00D5h			
00D6h	A/D Control Register 0	ADCON0	00000XXXb
00D7h	A/D Control Register 1	ADCON1	00h
00D8h			
00D9h			
00DAh			
00DBh			
00DCh			
00DDh			
00DEh			
00DFh			
00E0h			
00E1h	Port P1 Register	P1	XXh
00E2h			
00E3h	Port P1 Direction Register	PD1	00h
00E4h			
00E5h	Port P3 Register	P3	XXh
00E6h			
00E7h	Port P3 Direction Register	PD3	00h
00E8h	Port P4 Register	P4	XXh
00E9h			
00EAh	Port P4 Direction Register	PD4	00h
00EBh			
00ECh			
00EDh			
00EEh			
00EFh			
00F0h			
00F1h			
00F2h			
00F3h			
00F4h			
00F5h			
00F6h			
00F7h			
00F8h			
00F9h			
00FAh			
00FBh			
00FCh	Pull-Up Control Register 0	PUR0	00XX0000b
00FDh	Pull-Up Control Register 1	PUR1	XXXXXX0Xb
00FEh	Port P1 Drive Capacity Control Register	DRR	00h
00FFh	Timer C Output Control Register	TCOUT	00h
01B3h	Flash Memory Control Register 4	FMR4	01000000b
01B4h			
01B5h	Flash Memory Control Register 1	FMR1	1000000Xb
01B6h			
01B7h	Flash Memory Control Register 0	FMR0	00000001b
0FFFFh	Optional Function Select Register	OFS	(Note 2)

X: Undefined
NOTES:
1. The blank regions, 0100h to 01B2h and 01B8h to 02FFh are all reserved. Do not access locations in these regions.
2. The OFS register cannot be changed by a program. Use a flash programmer to write to it.

Table 5.3   Comparator Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
−	Resolution		−	−	1	Bit
−	Absolute accuracy	ϕ_{AD} = 10 MHz[3]	−	−	±20	mV
t_{conv}	Conversion time	ϕ_{AD} = 10 MHz[3]	1	−	−	µs
V_{ref}	Reference voltage		0	−	AV_{CC}	V
V_{IA}	Analog input voltage		0	−	AV_{CC}	V
−	Comparator conversion operating clock frequency[2]		1	−	10	MHz

NOTES:
1. V_{CC} = 2.7 to 5.5 V at T_{opr} = -20 to 85 °C / -40 to 85 °C, unless otherwise specified.
2. If f1 exceeds 10 MHz, divided f1 and ensure the comparator conversion operating clock frequency (ϕ_{AD}) is 10 MHz or below.
3. If AVcc is less than 4.2 V, divided f1 and ensure the comparator conversion operating clock frequency (ϕ_{AD}) is f1/2 or below.
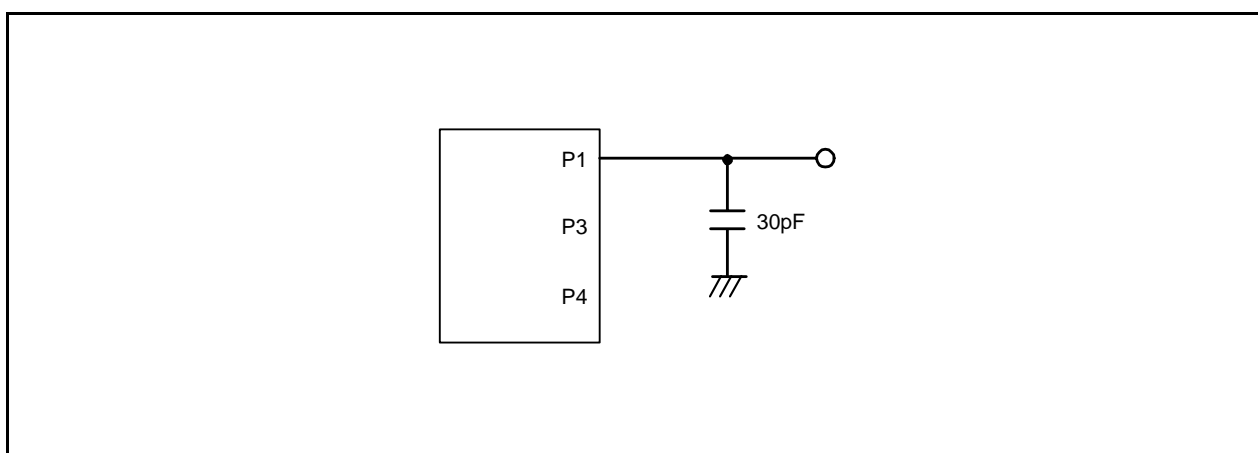
Figure 5.1   Port P1, P3, and P4 Measurement Circuit

Table 5.4   Flash Memory (Program ROM) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
−	Program/erase endurance[2]	R8C/18 Group	100[3]	−	−	times
		R8C/19 Group	1,000[3]	−	−	times
−	Byte program time		−	50	400	μs
−	Block erase time		−	0.4	9	s
td(SR-SUS)	Time delay from suspend request until suspend		−	−	97+CPU clock × 6 cycles	μs
−	Interval from erase start/restart until following suspend request		650	−	−	μs
−	Interval from program start/restart until following suspend request		0	−	−	ns
−	Time from suspend until program/erase restart		−	−	3+CPU clock × 4 cycles	μs
−	Program, erase voltage		2.7	−	5.5	V
−	Read voltage		2.7	−	5.5	V
−	Program, erase temperature		0	−	60	°C
−	Data hold time[8]	Ambient temperature = 55 °C	20	−	−	year

NOTES:
1. V_{CC} = 2.7 to 5.5 V at T_{opr} = 0 to 60 °C, unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 100 or 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one. However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
4. If emergency processing is required, a suspend request can be generated independent of this characteristic. In that case the normal time delay to Suspend can be applied to the request. However, we recommend that a suspend request with an interval of less than 650 μs is only used once because, if the suspend state continues, erasure cannot operate and the incidence of erasure error rises.
5. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. In addition, averaging the number of erase operations between block A and block B can further reduce the effective number of rewrites. It is also advisable to retain data on the erase count of each block and limit the number of erase operations to a certain number.
6. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
7. Customers desiring programming/erasure failure rate information should contact their Renesas technical support representative.
8. The data hold time includes time that the power supply is off or the clock is not supplied.

**Table 5.5   Flash Memory (Data flash Block A, Block B) Electrical Characteristics**

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/erase endurance[2]		10,000[3]	–	–	times
–	Byte program time (Program/erase endurance ≤ 1,000 times)		–	50	400	μs
–	Byte program time (Program/erase endurance > 1,000 times)		–	65	–	μs
–	Block erase time (Program/erase endurance ≤ 1,000 times)		–	0.2	9	s
–	Block erase time (Program/erase endurance > 1,000 times)		–	0.3	–	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend		–	–	97+CPU clock × 6 cycles	μs
–	Interval from erase start/restart until following suspend request		650	–	–	μs
–	Interval from program start/restart until following suspend request		0	–	–	ns
–	Time from suspend until program/erase restart		–	–	3+CPU clock × 4 cycles	μs
–	Program, erase voltage		2.7	–	5.5	V
–	Read voltage		2.7	–	5.5	V
–	Program, erase temperature		-20[8]	–	85	°C
–	Data hold time[9]	Ambient temperature = 55 °C	20	–	–	year

NOTES:
1. V_{CC} = 2.7 to 5.5 V at T_{opr} = -20 to 85 °C / -40 to 85 °C, unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 100 or 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one. However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
4. If emergency processing is required, a suspend request can be generated independent of this characteristic. In that case the normal time delay to suspend can be applied to the request. However, we recommend that a suspend request with an interval of less than 650 μs is only used once because, if the suspend state continues, erasure cannot operate and the incidence of erasure error rises.
5. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erase count of each block and limit the number of erase operations to a certain number.
6. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
7. Customers desiring programming/erasure failure rate information should contact their Renesas technical support representative.
8. -40 °C for D version.
9. The data hold time includes time that the power supply is off or the clock is not supplied.
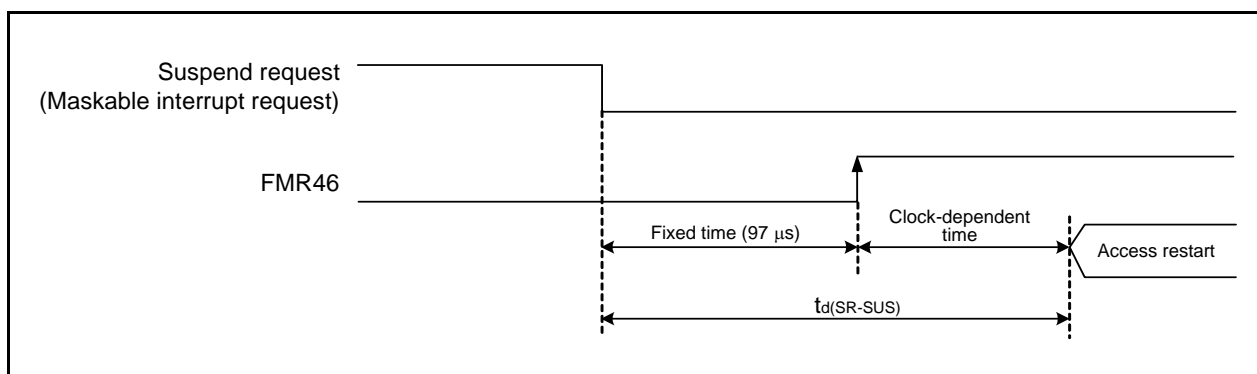
Figure 5.2   Transition Time to Suspend

Table 5.8 Reset Circuit Electrical Characteristics (When Using Voltage Monitor 1 Reset)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{por2}	Power-on reset valid voltage	$-20°C \leq Topr \leq 85°C$	–	–	V_{det1}	V
$t_{w(Vpor2-Vdet1)}$	Supply voltage rising time when power-on reset is deasserted[1]	$-20°C \leq Topr \leq 85°C$, $t_{w(por2)} \geq 0s$[3]	–	–	100	ms

NOTES:
1. This condition is not applicable when using with $Vcc \geq 1.0$ V.
2. When turning power on after the time to hold the external power below effective voltage (V_{por1}) exceeds 10 s, refer to **Table 5.9 Reset Circuit Electrical Characteristics (When Not Using Voltage Monitor 1 Reset)**.
3. $t_{w(por2)}$ is the time to hold the external power below effective voltage (V_{por2}).

Table 5.9 Reset Circuit Electrical Characteristics (When Not Using Voltage Monitor 1 Reset)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{por1}	Power-on reset valid voltage	$-20°C \leq Topr \leq 85°C$	–	–	0.1	V
$t_{w(Vpor1-Vdet1)}$	Supply voltage rising time when power-on reset is deasserted	$0°C \leq Topr \leq 85°C$, $t_{w(por1)} \geq 10$ s[2]	–	–	100	ms
$t_{w(Vpor1-Vdet1)}$	Supply voltage rising time when power-on reset is deasserted	$-20°C \leq Topr < 0°C$, $t_{w(por1)} \geq 30$ s[2]	–	–	100	ms
$t_{w(Vpor1-Vdet1)}$	Supply voltage rising time when power-on reset is deasserted	$-20°C \leq Topr < 0°C$, $t_{w(por1)} \geq 10$ s[2]	–	–	1	ms
$t_{w(Vpor1-Vdet1)}$	Supply voltage rising time when power-on reset is deasserted	$0°C \leq Topr \leq 85°C$, $t_{w(por1)} \geq 1$ s[2]	–	–	0.5	ms

NOTES:
1. When not using voltage monitor 1, use with $Vcc \geq 2.7$ V.
2. $t_{w(por1)}$ is the time to hold the external power below effective voltage (V_{por1}).

NOTES:
1. Hold the voltage inside the MCU operation voltage range (Vccmin or above) within the sampling time.
2. The sampling clock can be selected. Refer to **7. Voltage Detection Circuit** for details.
3. V_{det1} indicates the voltage detection level of the voltage detection 1 circuit. Refer to **7. Voltage Detection Circuit** for details.
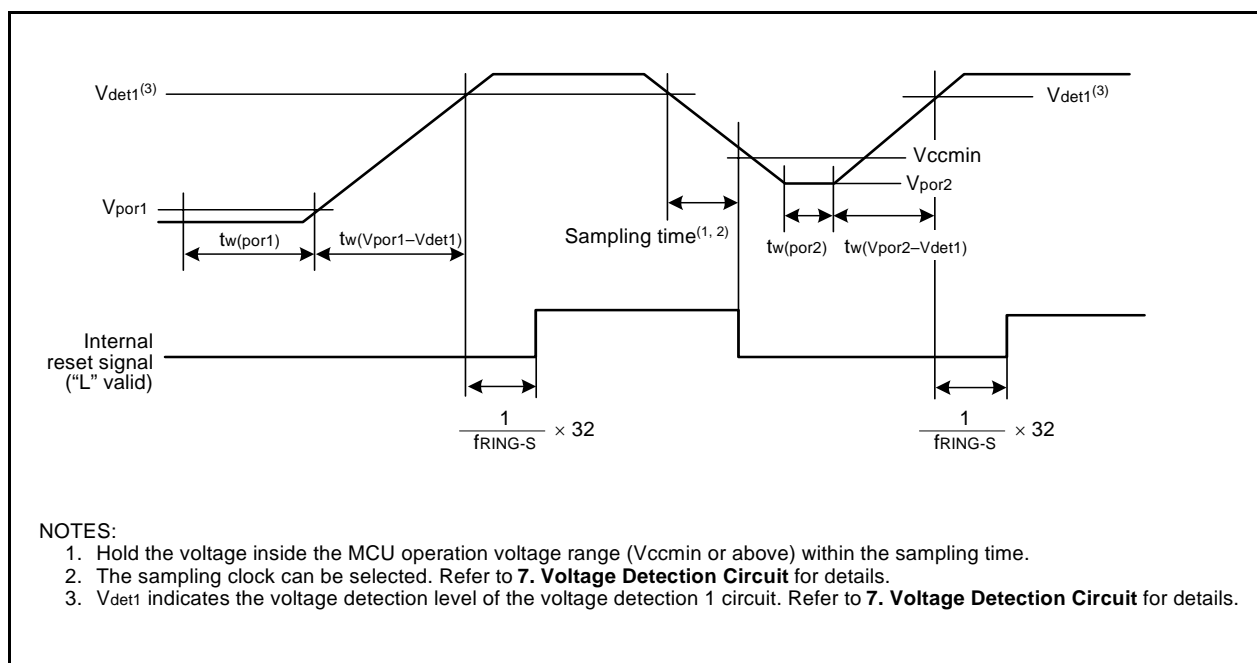
Figure 5.3 Reset Circuit Electrical Characteristics

Timing Requirements
(Unless Otherwise Specified: VCC = 5 V, VSS = 0 V at Ta = 25 °C) [VCC = 5 V]

Table 5.14   XIN Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	50	–	ns
$t_{WH(XIN)}$	XIN input "H" width	25	–	ns
$t_{WL(XIN)}$	XIN input "L" width	25	–	ns
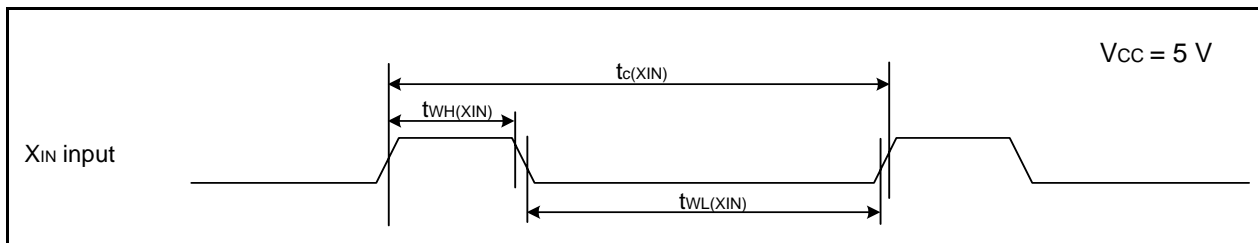
Figure 5.4   XIN Input Timing Diagram when VCC = 5 V

Table 5.15   CNTR0 Input, CNTR1 Input, $\overline{INT1}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CNTR0)}$	CNTR0 input cycle time	100	–	ns
$t_{WH(CNTR0)}$	CNTR0 input "H" width	40	–	ns
$t_{WL(CNTR0)}$	CNTR0 input "L" width	40	–	ns
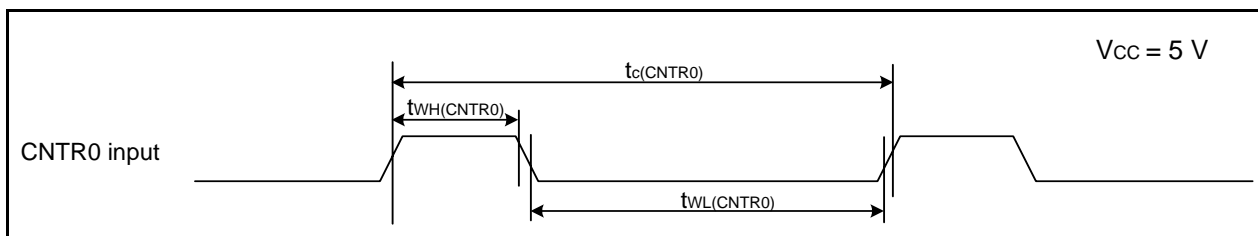
Figure 5.5   CNTR0 Input, CNTR1 Input, $\overline{INT1}$ Input Timing Diagram when VCC = 5 V

Table 5.16   TCIN Input, $\overline{INT3}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TCIN)}$	TCIN input cycle time	400[1]	–	ns
$t_{WH(TCIN)}$	TCIN input "H" width	200[2]	–	ns
$t_{WL(TCIN)}$	TCIN input "L" width	200[2]	–	ns

NOTES:
1. When using timer C input capture mode, adjust the cycle time to (1/timer C count source frequency x 3) or above.
2. When using timer C input capture mode, adjust the pulse width to (1/timer C count source frequency x 1.5) or above.
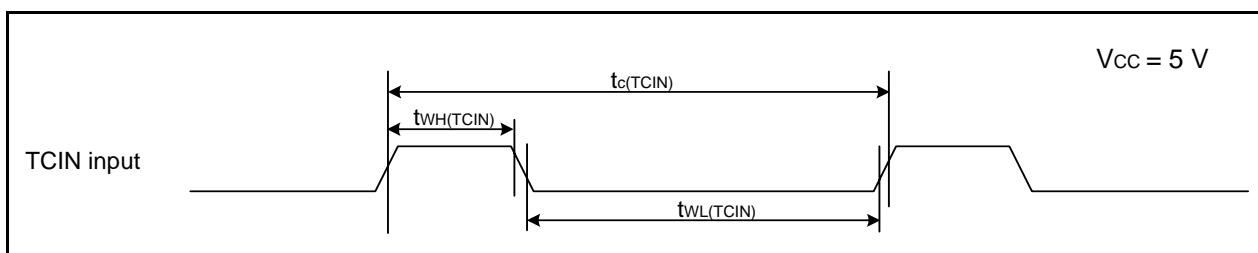
Figure 5.6   TCIN Input, $\overline{INT3}$ Input Timing Diagram when VCC = 5 V

Table 5.17   Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	200	–	ns
$t_{W(CKH)}$	CLKi input "H" width	100	–	ns
$t_{W(CKL)}$	CLKi input "L" width	100	–	ns
$t_{d(C-Q)}$	TXDi output delay time	–	50	ns
$t_{h(C-Q)}$	TXDi hold time	0	–	ns
$t_{su(D-C)}$	RXDi input setup time	50	–	ns
$t_{h(C-D)}$	RXDi input hold time	90	–	ns

i = 0 or 1
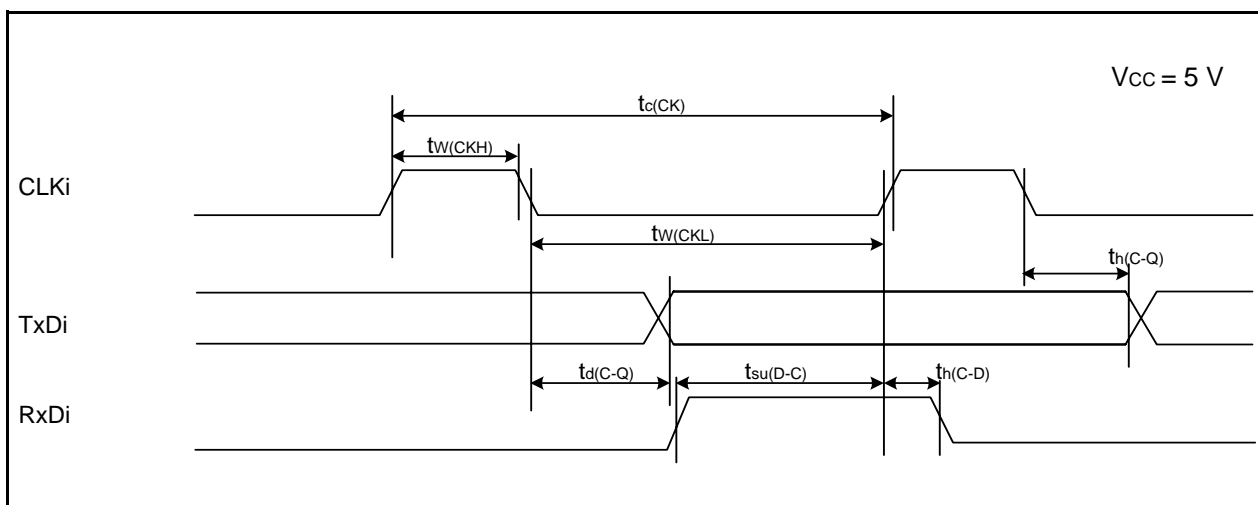
Figure 5.7   Serial Interface Timing Diagram when Vcc = 5 V

Table 5.18   External Interrupt INT0 Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	INT0 input "H" width	250[1]	–	ns
$t_{W(INL)}$	INT0 input "L" width	250[2]	–	ns

NOTES:
1. When selecting the digital filter by the INT0 input filter select bit, use an INT0 input HIGH width of either (1/digital filter clock frequency x 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the INT0 input filter select bit, use an INT0 input LOW width of either (1/digital filter clock frequency x 3) or the minimum value of standard, whichever is greater.
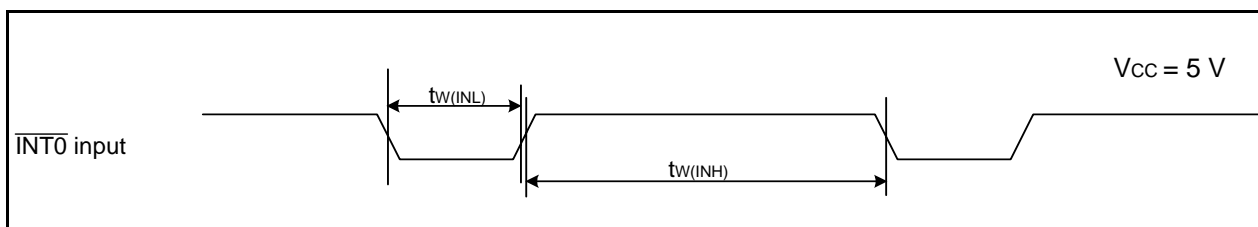
Figure 5.8   External Interrupt INT0 Input Timing Diagram when Vcc = 5 V

Table 5.24   Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t$_{c(CK)}$	CLKi input cycle time	300	–	ns
t$_{W(CKH)}$	CLKi input "H" width	150	–	ns
t$_{W(CKL)}$	CLKi input "L" width	150	–	ns
t$_{d(C-Q)}$	TXDi output delay time	–	80	ns
t$_{h(C-Q)}$	TXDi hold time	0	–	ns
t$_{su(D-C)}$	RXDi input setup time	70	–	ns
t$_{h(C-D)}$	RXDi input hold time	90	–	ns

i = 0 or 1
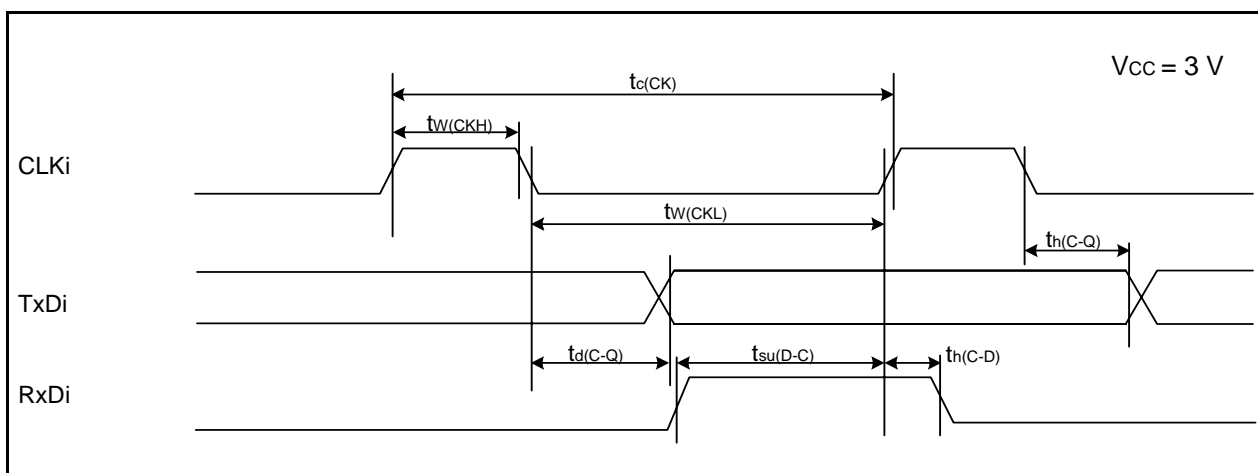
Figure 5.12   Serial Interface Timing Diagram when V$_{CC}$ = 3 V

Table 5.25   External Interrupt $\overline{INT0}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t$_{W(INH)}$	$\overline{INT0}$ input "H" width	380[1]	–	ns
t$_{W(INL)}$	$\overline{INT0}$ input "L" width	380[2]	–	ns

NOTES:
1. When selecting the digital filter by the $\overline{INT0}$ input filter select bit, use an $\overline{INT0}$ input HIGH width of either (1/digital filter clock frequency x 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INT0}$ input filter select bit, use an $\overline{INT0}$ input LOW width of either (1/digital filter clock frequency x 3) or the minimum value of standard, whichever is greater.
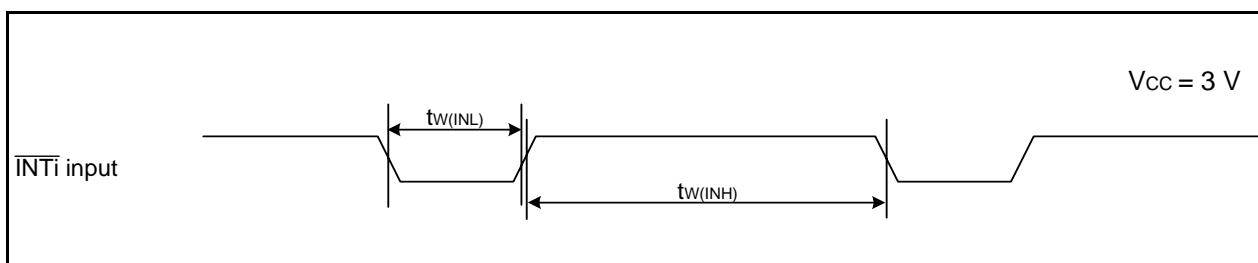
Figure 5.13   External Interrupt $\overline{INT0}$ Input Timing Diagram when V$_{CC}$ = 3 V

Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LSSOP20-4.4x6.5-0.65	PLSP0020JB-A	20P2F-A	0.1g

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Detail F

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.4	6.5	6.6
E	4.3	4.4	4.5
A_2	—	1.15	—
A	—	—	1.45
A_1	0	0.1	0.2
b_p	0.17	0.22	0.32
c	0.13	0.15	0.2
θ	0°	—	10°
H_E	6.2	6.4	6.6
e	0.53	0.65	0.77
y	—	—	0.10
L	0.3	0.5	0.7

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SDIP20-6.3x19-1.78	PRDP0020BA-A	20P4B	1.0g

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
e_1	7.32	7.62	7.92
D	18.8	19.0	19.2
E	6.15	6.3	6.45
A	—	—	4.5
A_1	0.51	—	—
A_2	—	3.3	—
b_p	0.38	0.48	0.58
b_3	0.9	1.0	1.3
c	0.22	0.27	0.34
θ	0°	—	15°
e	1.528	1.778	2.028
L	3.0	—	—

RenesasTechnology Corp. Sales Strategic Planning Div.   Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

RENESAS

RENESAS SALES OFFICES   http://www.renesas.com

Refer to "**http://www.renesas.com/en/network**" for the latest and detailed information.

Renesas Technology America, Inc.
450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

Renesas Technology Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

Renesas Technology (Shanghai) Co., Ltd.
Unit 204, 205, AZIACenter, No.1233 Lujiazui Ring Rd, Pudong District, Shanghai, China 200120
Tel: <86> (21) 5877-1818, Fax: <86> (21) 6887-7898

Renesas Technology Hong Kong Ltd.
7th Floor, North Tower, World Finance Centre, Harbour City, 1 Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2730-6071

Renesas Technology Taiwan Co., Ltd.
10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology Singapore Pte. Ltd.
1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

Renesas Technology Korea Co., Ltd.
Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea
Tel: <82> (2) 796-3115, Fax: <82> (2) 796-2145

Renesas Technology Malaysia Sdn. Bhd
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jalan Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: <603> 7955-9390, Fax: <603> 7955-9510