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Applications of "<u>Embedded - Microcontrollers</u>"

Details	
Product Status	Obsolete
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	SIO, UART/USART
Peripherals	LED, POR, Voltage Detect, WDT
Number of I/O	13
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-WFQFN Exposed Pad
Supplier Device Package	28-HWQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21184np-u0

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Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

## 1.4 Product Information

Table 1.3 lists Product Information for R8C/18 Group and Table 1.4 lists Product Information for R8C/19 Group.

Table 1.3 Product Information for R8C/18 Group

Current of Apr. 2006

Type No.	ROM Capacity	RAM Capacity	Package Type	Remarks
R5F21181SP	4 Kbytes	384 bytes	PLSP0020JB-A	Flash memory version
R5F21182SP	8 Kbytes	512 bytes	PLSP0020JB-A	
R5F21183SP	12 Kbytes	768 bytes	PLSP0020JB-A	
R5F21184SP	16 Kbytes	1 Kbyte	PLSP0020JB-A	
R5F21181DSP (D)	4 Kbytes	384 bytes	PLSP0020JB-A	D version
R5F21182DSP (D)	8 Kbytes	512 bytes	PLSP0020JB-A	
R5F21183DSP (D)	12 Kbytes	768 bytes	PLSP0020JB-A	
R5F21184DSP (D)	16 Kbytes	1 Kbyte	PLSP0020JB-A	
R5F21181DD	4 Kbytes	384 bytes	PRDP0020BA-A	Flash memory version
R5F21182DD	8 Kbytes	512 bytes	PRDP0020BA-A	
R5F21183DD	12 Kbytes	768 bytes	PRDP0020BA-A	
R5F21184DD	16 Kbytes	1 Kbyte	PRDP0020BA-A	
R5F21182NP	8 Kbytes	512 bytes	PWQN0028KA-B	Flash memory version
R5F21183NP	12 Kbytes	768 bytes	PWQN0028KA-B	
R5F21184NP	16 Kbytes	1 Kbyte	PWQN0028KA-B	

(D): Under Development

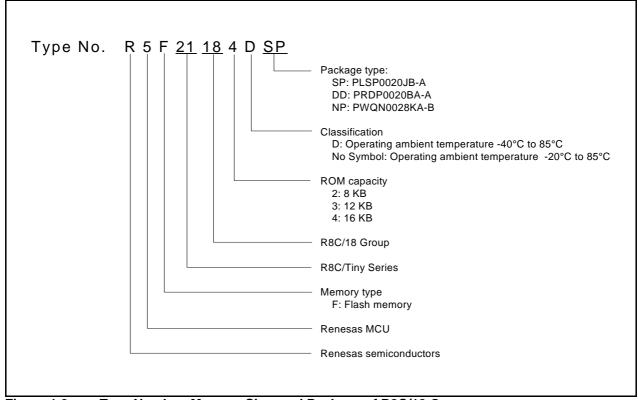


Figure 1.2 Type Number, Memory Size, and Package of R8C/18 Group

# 1.5 Pin Assignments

Figure 1.4 shows Pin Assignments for PLSP0020JB-A Package (Top View), Figure 1.5 shows Pin Assignments for PRDP0020BA-A Package (Top View) and Figure 1.6 shows Pin Assignments for PWQN0028KA-B Package (Top View).

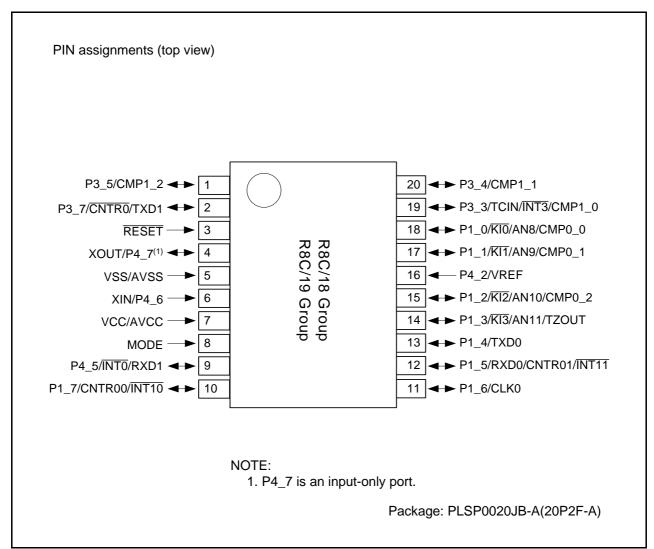


Figure 1.4 Pin Assignments for PLSP0020JB-A Package (Top View)

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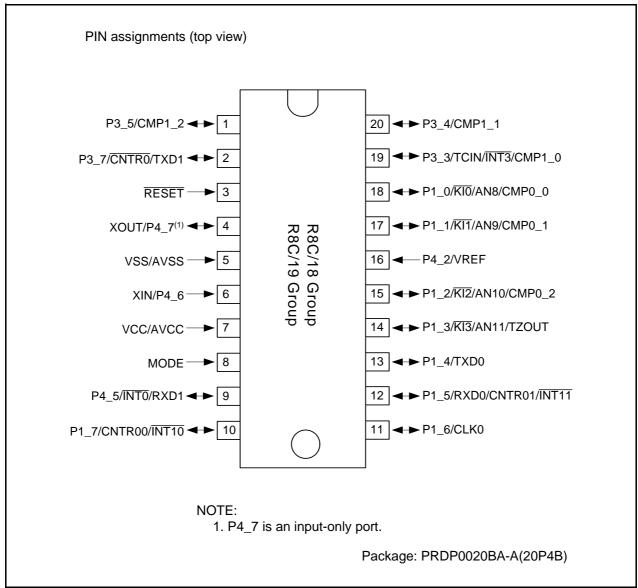


Figure 1.5 Pin Assignments for PRDP0020BA-A Package (Top View)

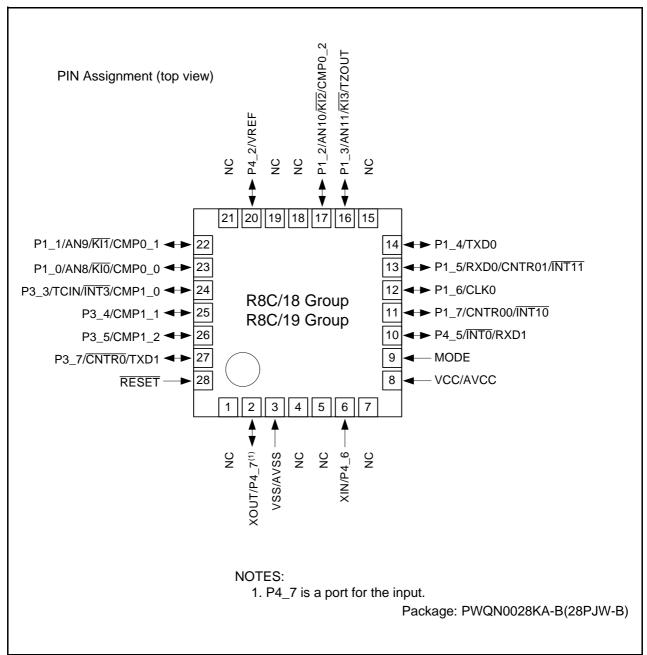


Figure 1.6 Pin Assignments for PWQN0028KA-B Package (Top View)

Pin Name Information by Pin Number of PLSP0020JB-A, PRDP0020BA-A packages Table 1.6

Pin	Control	Port	I/C	I/O Pin Functions for Peripheral Modules				
Number	Pin	FUIL	Interrupt	Timer	Serial Interface	Comparator		
1		P3_5		CMP1_2				
2		P3_7		CNTR0	TXD1			
3	RESET							
4	XOUT	P4_7						
5	VSS/AVSS							
6	XIN	P4_6						
7	VCC/AVCC							
8	MODE							
9		P4_5	ĪNT0		RXD1			
10		P1_7	ĪNT10	CNTR00				
11		P1_6			CLK0			
12		P1_5	ĪNT11	CNTR01	RXD0			
13		P1_4			TXD0			
14		P1_3	KI3	TZOUT		AN11		
15		P1_2	KI2	CMP0_2		AN10		
16	VREF	P4_2						
17		P1_1	KI1	CMP0_1		AN9		
18		P1_0	KI0	CMP0_0		AN8		
19		P3_3	ĪNT3	TCIN/CMP1_0				
20		P3_4		CMP1_1				

# 2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

# 2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic and logic operations. A1 is analogous to A0. A1 can be combined with A0 and used as a 32-bit address register (A1A0).

# 2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

# 2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the start address of an interrupt vector table.

# 2.5 Program Counter (PC)

PC is 20 bits wide, indicates the address of the next instruction to be executed.

# 2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointer (SP), USP, and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

# 2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

# 2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

# 2.8.1 **Carry Flag (C)**

The C flag retains a carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

## 2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

### 2.8.3 **Zero Flag (Z)**

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

# 2.8.4 **Sign Flag (S)**

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

# 2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

# 2.8.6 Overflow Flag (O)

The O flag is set to 1 when the operation results in an overflow; otherwise to 0.



# 2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts.

Interrupts are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

# 2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.

The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

# 2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide, assigns processor interrupt priority levels from level 0 to level 7. If a requested interrupt has higher priority than IPL, the interrupt is enabled.

### 2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.



# 3. Memory

# 3.1 R8C/18 Group

Figure 3.1 is a Memory Map of R8C/18 Group. The R8C/18 Group has 1 Mbyte of address space from addresses 00000h to FFFFFh.

The internal ROM area is allocated lower addresses, beginning with address 0FFFFh. For example, a 16-Kbyte internal ROM is allocated addresses 0C000h to 0FFFFh.

The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. They store the starting address of each interrupt routine.

The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 1-Kbyte internal RAM area is allocated addresses 00400h to 007FFh. The internal RAM is used not only for storing data but also for calling subroutines and as stacks when interrupt requests are acknowledged.

Special function registers (SFRs) are allocated addresses 00000h to 002FFh. The peripheral function control registers are allocated here. All addresses within the SFR, which have nothing allocated are reserved for future use and cannot be accessed by users.

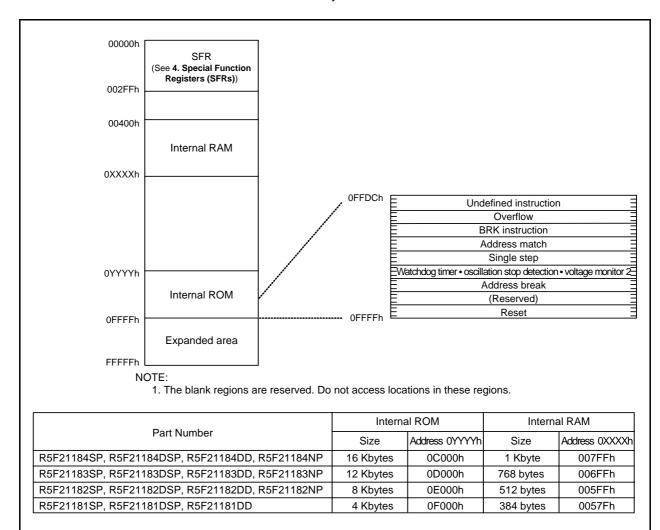


Figure 3.1 Memory Map of R8C/18 Group

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# 3.2 R8C/19 Group

Figure 3.2 is a Memory Map of R8C/19 Group. The R8C/19 group has 1 Mbyte of address space from addresses 00000h to FFFFFh.

The internal ROM (program ROM) is allocated lower addresses, beginning with address 0FFFFh. For example, a 16-Kbyte internal ROM area is allocated addresses 0C000h to 0FFFFh.

The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. They store the starting address of each interrupt routine.

The internal ROM (data flash) is allocated addresses 02400h to 02BFFh.

The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 1-Kbyte internal RAM area is allocated addresses 00400h to 007FFh. The internal RAM is used not only for storing data but also for calling subroutines and as stacks when interrupt requests are acknowledged.

Special function registers (SFRs) are allocated addresses 00000h to 002FFh. The peripheral function control registers are allocated here. All addresses within the SFR, which have nothing allocated are reserved for future use and cannot be accessed by users.

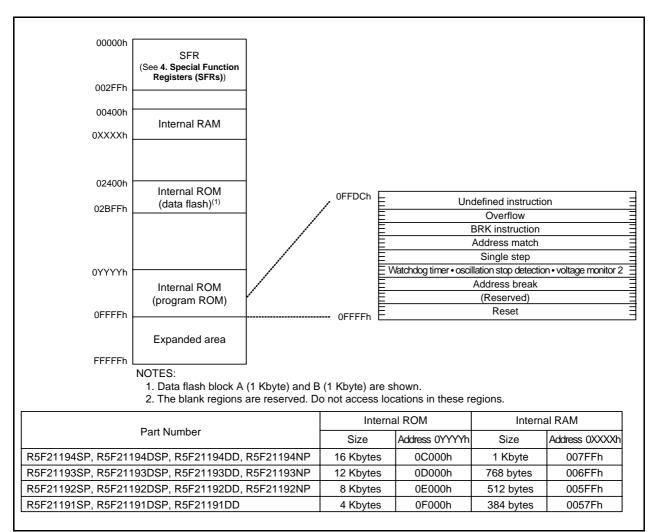


Figure 3.2 Memory Map of R8C/19 Group

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SFR Information (2)<sup>(1)</sup> Table 4.2

Address	Register	Symbol	After reset
0040h	5	,	
0041h			
0042h			
0043h			
0044h			
0045h			
0046h			
0047h			
0048h			
0049h			
004Ah			
004Bh			
004Ch			
004Dh	Key Input Interrupt Control Register	KUPIC	XXXXX000b
004Eh	Comparator Conversion Interrupt Control Register	ADIC	XXXXX000b
004Fh			
0050h	Compare 1 Interrupt Control Register	CMP1IC	XXXXX000b
0051h	UART0 Transmit Interrupt Control Register	SOTIC	XXXXX000b
0052h	UARTO Receive Interrupt Control Register	SORIC	XXXXX000b
0053h	UART1 Transmit Interrupt Control Register	S1TIC	XXXXX000b
0054h	UART1 Receive Interrupt Control Register	S1RIC	XXXXX000b
0055h	Timor V Interrupt Central Pagister	TVIC	VVVVV000h
0056h 0057h	Timer X Interrupt Control Register	TXIC	XXXXX000b
0057h 0058h	Timer Z Interrupt Control Register	TZIC	XXXXX000b
0059h	-	INT1IC	XXXXX000b
	INT1 Interrupt Control Register		
005Ah	INT3 Interrupt Control Register	INT3IC	XXXXX000b
005Bh	Timer C Interrupt Control Register	TCIC	XXXXX000b
005Ch	Compare 0 Interrupt Control Register	CMP0IC	XXXXX000b
005Dh	INTO Interrupt Control Register	INT0IC	XX00X000b
005Eh			
005Fh			
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h 0068h			
0069h			
006Ah			
006Bh			
006Ch			
006Dh			
006Eh			
006Fh			
0070h			
0071h			
0072h			
0073h			
0074h			
0075h			
0076h			
0077h			
0078h			
0079h			
007Ah			
007Bh			
007Ch			
007Dh			
007Eh			
007Fh			

X: Undefined

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

SFR Information (4)<sup>(1)</sup> Table 4.4

DOCCOR	Address	Register	Symbol	After reset
0002h   0003h   0003	00C0h			
9003h				
00C4h         00C8h           00C8h         00C8h           00C7h         00C7h           00C7h         00C7h           00C2h         00C7h           00C2h         00C7h           00C7h         00C7h           00C7h         00C7h           00D9h         00D9h           00D9h <td></td> <td></td> <td></td> <td></td>				
0005h				
000C6h	00C4h			
00C7h         00C8h           00C8h         00C8h           00D0h         00D0h           00D1h         00D0h           00D2h         AD Control Register 0           00D5h         00D0h           00D7h         AD Control Register 0           00D8h         00D0h           00D8h         00D0h           00D8h         00D0h           00D8h         00D0h           00D0h         00D0h           00D0h         00D0h           00E0h         00D0h           00E0h         00C8h           00E3h         00F1 Port P3 Register           00E3h         Port P1 Register           00E3h         Port P3 Register           00E3h         Port P3 Register           00E3h         Port P3 Port P3 Register           00E4h         00E5h           00E5h         Port P3 Registe				
0005h   0005				
0005h   0006h   0006				
00Cbh         00Cbh           00Cbh         00Cbh           00Cbh         00Cbh           00Cbh         00Cbh           00D0bh         00D0bh           00D2h         00D3h           00D3h         AD Control Register 2           00D6h         ADCON0           00D8h         AD Control Register 0           00D8h         ADCON1           00D8h         ADCON1           00D8h         ADCON1           00D8h         ADCON1           00D8h         ADCON1           00D8h         ADCON1           00D8h         ODCh           00Eh         Port P1 Register           00Eh         Port P2 Register           00Eh         Port P3 Direction Register           00Eh         Port P3 Direction Register	00C9h			
00CCh         00CEh           00CCh         00CEh           00CCh         00CH           00D0h         00D0h           00D1h         00D1h           00D3h         00D3h           00D3h         AD Control Register 2           00D4h         AD Control Register 1           00D4h         AD Control Register 1           00D7h         AD Control Register 1           00D4h         AD CON1           00D4h         00D8h           00D4h         00D8h           00D4h         00D8h           00D4h         00D8h           00D4h         00D8h           00D4h         00D8h           00D5h         00D8h           00D6h         00D8h           00E0h         00D8h           00E1h         00E2h           00E2h         00E3h           00E3h         Port P1 Direction Register           00E4h         Port P3 Register         P3           00E4h         Port P4 Register         P4           00E4h         Port P4 Register         P4           00E4h         Port P4 Direction Register         PD3           00E6h         Port P4 Direction Regist				
000Cbh         00CFh           00Cbh         00CPh           00Cbh         00Ch           00Dlah         00Dlah           00Dlah         AD Control Register 2           00Dsh         AD Control Register 0           00Dsh         AD Control Register 1           00Dbh         AD Control Register 1           00Dsh         AD Control Register 1           00Dsh         ADCON1           00Dsh         00Dsh           00Esh         00Esh           00Esh         Port P1 Direction Register           00Esh         Port P3 Direction Register           00Esh         Port P4 Register           00Esh         Port P4 Register           00Esh         Port P5 Direction Register           00Esh         Port P5 Dir				
00CEh         00Ch           00DOh         00DOh           00D1h         00D3h           00D3h         00D3h           00D3h         AD Control Register 2           00D3h         AD Control Register 1           00D4h         AD COND           00D4h         AD COND           00D4h         00DAn           00D4h         00DAn           00D4h         00DAn           00D4h         00DAn           00D5h         00DAn           00D4h         00DAn           00D5h         00DAn           00E3h         00FD           00E3h         Pot P3 Register           00E4h         00E3h           00E5h         Pot P3 Direction Register         P3           00E4h         00E3h           00E4h         00E3h           00E4h         00E3h				
00CPh         00D0h         00D1h           00D1h         00D2h         00D0h           00D3h         AD Control Register 2         00h           00D3h         AD Control Register 0         00000h           00D3h         AD Control Register 1         00h           00D3h         AD Control Register 1         00h           00D3h         00D3h         00h           00D4h         00D4h         00h           00D4h         00D4h         00h           00D5h         00D6h         00h           00D6h         00D6h         00h           00D6h         00D6h         00h           00D6h         00D6h         00h           00E3h         00Fh         00h           00E3h         Port P1 Register         P1         XXh           00E3h         Port P3 Register         P3         XXh           00E3h         Port P3 Register         P3         00h           00E3h         Port P3 Register         P4         XXh           00E3h         Port P4 Direction Register         P3         00h           00E4h         Port P3 Direction Register         P4         00h           00E4h         Port				
00010h				
00D1h         00D2h           00D2h         0D0h           00D3h         AD Control Register 2         ADCON2         00h           00D5h         AD Control Register 0         ADCON0         000000XXb           00D7h         AD Control Register 1         ADCON1         00h           00D8h         00D0h         00h         00h           00D8h         00D0h         00D0h         00D0h           00D0h         00D0h         00D0h         00D0h           00D0h         00D0h         00D0h         00D0h           00D0h         00D0h         00D0h         00D0h           00D0h         00D0h         00D0h         00D0h           00D2h         00D0h         00D0h         00D0h           00D2h         00D0h         00D0h         00D0h           00E3h         Port P1 Register         P1         XXh           00E3h         Port P3 Register         P3         XXh           00E3h         Port P3 Register         P3         XXh           00E3h         Port P4 Direction Register         P3         00h           00E3h         Port P4 Direction Register         P4         00h           00E4h <t< td=""><td></td><td></td><td></td><td></td></t<>				
00D2h         00D4h         AD Control Register 2         ADCON2         00h           00D4h         AD Control Register 0         ADCON0         000000000000000000000000000000000000				
00D4h         AD Control Register 2         ADCON2         00h           00D5h         AD Control Register 0         ADCON0         000000XXXb           00D7h         AD Control Register 1         ADCON1         00h           00D8h         00D8h         00DA         00DA           00D8h         00DA         00DA         00DA           00D5h         00DBh         00DBh         00DBh           00D5h         00DBh         00DBh         00DBh           00D5h         00DBh         00DBh         00DBh           00D6h         00DBh         00DBh         00DBh           00E3h         Port P1 Register         P1         XXh           00E3h         Port P2 Bregister         P3         XXh           00E4h         P0T P3 Register         P3         XXh           00E4h         P0T P4 Register         P4         XXh           00E8h         P0T P4 Register				
00D4h         AD Control Register 2         ADCON2         00h           00D5h         AD Control Register 0         ADCON0         000000XXXb           00D7h         AD Control Register 1         ADCON1         00h           00D8h         00D8h         00DA         00DA           00D8h         00DA         00DA         00DA           00D5h         00DBh         00DBh         00DBh           00D5h         00DBh         00DBh         00DBh           00D5h         00DBh         00DBh         00DBh           00D6h         00DBh         00DBh         00DBh           00E3h         Port P1 Register         P1         XXh           00E3h         Port P2 Bregister         P3         XXh           00E4h         P0T P3 Register         P3         XXh           00E4h         P0T P4 Register         P4         XXh           00E8h         P0T P4 Register	00D3h			
00D6h         A/D Control Register 0         ADCON0         00000XXXb           00D7h         A/D Control Register 1         ADCON1         000h           00D8h         00DAh         00DAh         00DAh           00DBh         00DBh         00DBh         00DBh           00DCh         00DCh         00DCh         00DBh           00DDh         00DBh         00DBh         00DBh           00DFh         00DFh         00DBh         00DBh           00E1h         00E1h         00DBh         00DBh           00E2h         00E3h         00E3h         00DBh           00E3h         Port P1 Direction Register         PD1         00h           00E4h         00E3h         Port P3 Register         P3         XXh           00E6h         00E7h         00H         00E8h         00H           00E8h         Port P4 Register         P4         XXh           00E8h         Port P4 Direction Register         PD4         00h           00E8h         00E0h         00H         00H           00E8h         00E0h         00H         00H           00E0h         00E0h         00H         00H           00E0h <t< td=""><td>00D4h</td><td>A/D Control Register 2</td><td>ADCON2</td><td>00h</td></t<>	00D4h	A/D Control Register 2	ADCON2	00h
00DRh         A/D Control Register 1         00h           00D8h         00D9h           00DAh         00DBh           00DCh         00DCh           00DCh         00DCh           00DEh         00DEh           00Eh         00Eh           00Eh <t< td=""><td></td><td></td><td></td><td></td></t<>				
00D8h         00DAh           00DAh         00DAh           00DBh         00DCh           00DDh         00DDh           00DDh         00DDh           00DFh         00DFh           00DFh         00DFh           00E1h         Port P1 Register           00E2h         00E3h           00E3h         Port P1 Direction Register           00E3h         Port P2 Breston Register           00E6h         Port P3 Direction Register           00E8h         Port P4 Register           00E8h         Port P4 Direction Register           00E8h         Port P4 Direction Register           00E8h         Port P5 Direction Register           00E8h         Port P6 Direction Register           00E8h         Port P7 Direction Register           00E8h         Port P8 Direction Register           00E2h         Oberth           00E2h         Oberth           00E2h         Oberth           00E2h         Oberth           00E2h         Oberth           00F3h         Oberth           00F4h         Oberth           00F5h         Oberth           00F6h         Oberth <t< td=""><td>00D6h</td><td>A/D Control Register 0</td><td>ADCON0</td><td></td></t<>	00D6h	A/D Control Register 0	ADCON0	
00D9h         00DBh           00DBh         00DBh           00DCh         00DCh           00DEh         00DEh           00DFh         00DFh           00E1h         00E1h           00E2h         00E3h           00E3h         Port P1 Direction Register           00E3h         Port P2 Direction Register           00E3h         Port P3 Register           00E6h         Port P4 Register           00E7h         Port P4 Register           00E8h         Port P4 Register           00E8h         Port P4 Register           00E8h         Port P4 Direction Register           00E8h         Port P4 Direction Register           00E8h         Port P4 Direction Register           00E8h         Port P5 P4 Direction Register           00E8h         Port P6 Register           00E9h         Port P6 Register           00E9h         Port P6 Register           00E9h         Port P7 Register           00E9h         Port P8 Register           00F8h         Port P8 Register           00F8h         Port P8 Register           00F8h         Port P8 Register           00F8h         Port P8 Register <t< td=""><td></td><td>A/D Control Register 1</td><td>ADCON1</td><td>uun</td></t<>		A/D Control Register 1	ADCON1	uun
00DAh         00DBh           00DCh         00DCh           00DDh         00DBh           00DFh         00DFh           00E1h         00E1h           00E1h         00E1h           00E1h         00E1h           00E3h         00E3h           00E3h         Port P1 Direction Register           00E3h         Port P2 Register           00E6h         Port P3 Direction Register           00E8h         Port P4 Register           00E8h         Port P4 Register           00E8h         Port P4 Direction Register           00E9h         Ooh           00E1h         Ooh           00E2h         Ooh           00E2h         Ooh           00E2h         Ooh           00E3h         Ooh           00F8h         Ooh           00F8h         Ooh           00F8h         Ooh           00F8h         <				
00DBh         00DCh           00DCh         00DDh           00DFh         00E0h           00E0h         00E1h           00E2h         00E2h           00E2h         00E2h           00E2h         00E2h           00E3h         Port P1 Direction Register           00E3h         Port P3 Register           00E5h         Port P3 Direction Register           00E7h         Port P4 Register           00E8h         Port P4 Register           00E8h         Port P4 Direction Register           00E8h         Port P4 Direction Register           00E8h         Pot P4 Direction Register           00EBh         Do           00ECh         00E0h           00EDh         00E0h           00E7h         00F0h           00E7h         00F3h           00F3h         00F4h           00F3h         00F3h           00F6h         00F6h           00F7h         00F8h           00F8h         00F8h           00F9h         00F9h           00F9h         00F9h           00F9h         00F9h           00F9h         00F9h           00F9	00D9H			
OODCh OODED OODEN O				
OODDh OODEh OODEh OOED OOE1h OOE2h OOE3h OOE3h OOE3h OOE5h OOE5h OOE5h OOE6h OOE7h OOE7h OOE7h OOE7h OOE9h OOF9h OO				
00DFh         00E1h         Port P1 Register         P1         XXh           00E2h         00E3h         Port P1 Direction Register         PD1         00h           00E3h         Port P3 Register         P3         XXh           00E6h         00E7h         Port P3 Direction Register         PD3         00h           00E8h         Port P4 Register         P4         XXh           00E9h         P0         XXh         00E0           00EAh         P0rt P4 Direction Register         PD4         00h           00EBh         P0rt P4 Direction Register         PD4         00h           00EDh         00E0h         00h         00h           00ECh         00EDh         00h         00h           00EFh         00Fh         00Fh         00Fh           00F1h         00Fh         00Fh         00Fh           00F3h         00Fh         00Fh         00Fh           00F3h         00Fh         00Fh         00Fh           00F3h         00Fh         00Fh         00Fh           00F9h         00Fh         00Fh         00Fh         00Fh           00F9h         00Fh         00Fh         00Fh         00Fh	00DDh			
00E1h 00E3h         Port P1 Register         P1         XXh           00E3h 00E3h         Port P1 Direction Register         PD1         00h           00E4h 00E5h         P0T P3 Register         P3         XXh           00E6h 00E7h         Port P3 Direction Register         PD3         00h           00E8h 00E8h 00E8h         P0rt P4 Register         P4         XXh           00E9h 00E9h 00E0h         P0rt P4 Direction Register         PD4         00h           00E8h 00ECh 00E0h         P0rt P4 Direction Register         PD4         00h           00E9h 00E0h 00E0h 00E0h         P0rt P4 Direction Register         PD4         00h           00E1h 00E0h 00E0h 00E0h         P0rt P4 Direction Register         PD4         00h           00E1h 00F2h 00F3h 00F4h         P0rt P4 Direction Register         PD4         00h           00F3h 00F6h 00F6h 00F6h 00F6h         P0rt P4 Direction Register 0         P0rt P4 Direction Register 0         P0rt P4 Direction Register 0           00F8h 00F6h 00F6h         P0rt P4 Direction Register 0         PUR0         00XX0000b 00XX0000b           00F1h 00F6h         P0rt P4 Direction Register 0         PUR0         00XX0000b 00R Direction Register 0           00F1h 00F6h         P0rt P1 Dirive Capacity Control Register 0         PUR0         00XXX000b 00h	00DEh			
00E1h ODE2h         Port PR Register         P1         XXh           00E2h ODE3h         Port P1 Direction Register         PD1         00h           00E4h ODE6h         P0rt P3 Register         P3         XXh           00E6h ODE7h         Port P3 Direction Register         PD3         00h           00E8h P0rt P4 Register         P4         XXh           00E9h ODE8h P0rt P4 Direction Register         PD4         00h           00EAh P0rt P4 Direction Register         PD4         00h           00ED P1         P0F1 P4 Direction Register         PD4         00h           00ED P1         PD4         00h         00h           00ED P2         P0F2         00h				
00E2h         00E3h         Port P1 Direction Register         PD1         00h           00E4h         Port P3 Register         P3         XXh           00E6h         Port P3 Direction Register         PD3         00h           00E8h         Port P4 Register         P4         XXh           00E9h         00E0h         00h         00h           00E8h         Port P4 Direction Register         PD4         00h           00E0h         00E0h         00h         00h           00E0h         00E0h         00h         00h           00E0h         00E0h         00h         00h           00E0h         00E0h         00h         00h           00E1h         00E0h         00H         00H           00E2h         00E0h         00E0h         00E0h           00E1h         00E1h         00E1h         00E1h           00E2h         00E2h         00E2h         00E2h           00E3h         00E3h         00E3h         00E3h           00E4h         00E3h         00E3h         00E3h           00F3h         00F3h         00E3h         00E3h           00F3h         00F3h         00E3h         00E3h				V. 7.
00E3h         Port P1 Direction Register         PD1         00h           00E4h         Port P3 Register         P3         XXh           00E7h         Port P3 Direction Register         PD3         00h           00E8h         Port P4 Register         P4         XXh           00E9h         P0t         P0t         P0t           00EAh         Port P4 Direction Register         PD4         00h           00EBh         00ECh         00ED         00h           00ECh         00EDh         00EDh         00EDh           00EFh         00EFh         00EHh           00Fh         00Fh         00Fh		Port P1 Register	P1	XXh
00E4h         00E6h         Port P3 Register         P3         XXh           00E6h         Port P4 Direction Register         PD3         00h           00E8h         P0T P4 Register         P4         XXh           00E9h         00E0h         00h           00E8h         00h         00h           00EBh         00h         00h           00EDh         00EDh         00h           00EBh         00EDh         00EDh           00EBh         00EDh         00EDh           00EBh         00F0h         00EDh           00EPh         00F0h         00EDh           00F3h         00F3h         00F3h           00F4h         00F3h         00F3h           00F4h         00F3h         00F3h	00E2h	Dort D1 Direction Register	DD4	00h
00E6h         Port P3 Register           00E6h         Port P3 Direction Register           00E7h         Port P4 Register           00E8h         Port P4 Register           00E9h         Port P4 Direction Register           00EAh         Port P4 Direction Register           00EBh         O0           00ECh         O0           00ECh         O0EDh           00ECh         O0EDh           00ECh         O0ERH           00E7h         O0Foh           00F1h         O0Foh           00F2h         O0Foh           00F3h         O0Foh           00F6h         O0Foh           00F6h         O0Foh           00F6h         O0Foh           00F8h         O0Foh           00F8h         O0Foh           00F8h         O0Foh           00F9h         O0Foh           00F0h         Pull-Up Control Register 0           00F0h         Pull-Up Control Register 1           00F0h         Pull P1 Dive Capacity Control Register         Doh           00Feh         O0h           00Feh         O0h         O0h           00FFh         O0h         O0h </td <td></td> <td>  Fort F1 Direction Register</td> <td>וטיו</td> <td>OOT</td>		Fort F1 Direction Register	וטיו	OOT
00E6h         DOETh Port P3 Direction Register         PD3         00h           00E8h         Port P4 Register         P4         XXh           00E8h         00EAh         PD4         00h           00EBh         00         00         00           00EDh         00EBh         00         00           00EDh         00EBh         00         00           00EBh         00Fbh         00         00         00           00Eh         00Eh         00 </td <td></td> <td>L Port P3 Register</td> <td>P3</td> <td>XXh</td>		L Port P3 Register	P3	XXh
00E7h         Port P3 Direction Register         P9         00h           00E8h         Port P4 Register         P4         XXh           00E9h         ODEAh         Port P4 Direction Register         PD4         ODh           00EBh         ODECh         ODH         ODh           00ECh         ODECH         ODECH         ODECH           00EFh         ODECH         ODECH         ODECH           00F1h         ODF3h         ODECH         ODECH           00F3h         ODF3h         ODECH         ODECH           00F6h         ODF6h         ODECH         ODECH           00F8h         ODF8h         ODECH         ODECH           00F8h         ODECH         ODECH         ODECH           00F9h         ODECH         ODECH         ODECH           00F9h         ODECH         ODECH         ODECH           00F0h         DURO         ODXX0000b         DURO           00F0h         DURO         ODXX0000b         DURO           00F0h         DURO         ODXX0000b         DURO           00F0h         DURO         ODXX0000b         DURO           00F0h         DURO         ODXX0000b	00E6h	T or to trog.com	. •	70
00E9h 00E8h 00EBh 00ECh 00ECh 00EDh 00EEh 00EFh 00Fh 00Fh 00Fh 00Fh 00Fh 0			PD3	
00EAh         Port P4 Direction Register         PD4         00h           00EBh         00ECh         00EDh         00EDh <td>00E8h</td> <td>Port P4 Register</td> <td>P4</td> <td>XXh</td>	00E8h	Port P4 Register	P4	XXh
00EBh         00ECh           00EDh         00EFh           00EFh         00Fh           00Fh         00Fh           00Fh         00Fh           00F1h         00Fh           00F3h         00Fh           00F4h         00Fh           00Fh         Pull-Up Control Register 0           00Fh         Pull-Up Control Register 1           00Fh         Port P1 Drive Capacity Control Register           00Fh         Timer C Output Control Register           01B3h         Flash Memory Control Register 4           01B3h         Flash Memory Control Register 1           01B6h         FMR1           01B7h         Flash Memory Control Register 0				
00ECh         00EDh           00EFh         00Fh           00Fh         00Fh           00Fh         00Fh           00Fh         00Fh           00Fh         00Fh           00F3h         00Fh           00F6h         00Fh           00F7h         00Fh           00F9h         00Fh           00Fh         00Fh           00Fh         00Fh           00Fh         00Fh           00Fh         00Fh           00Fh         Pull-Up Control Register 0           00Fh         Pull-Up Control Register 1           00Fh         Port P1 Drive Capacity Control Register           00Fh         Drive Capacity Control Register           00Fh         Timer C Output Control Register           01B3h         Flash Memory Control Register 4         FMR4         01000000b           01B4h         01B5h         Flash Memory Control Register 1         FMR1         1000000xb           01B6h         Flash Memory Control Register 0         FMR0         00000001b		Port P4 Direction Register	PD4	00h
00EDh         00EEh           00EFh	00EBh			
00Eh         00Eh           00F0h	00ECII			
00EFh         00F0h           00F1h         00F1h           00F2h         00F3h           00F4h         00F4h           00F5h         00F6h           00F6h         00F7h           00F8h         00F8h           00F9h         00FAh           00FBh         00FBh           00FDh         Pull-Up Control Register 0           00FDh         Pull-Up Control Register 1           00FFh         Port P1 Drive Capacity Control Register           00FFh         Timer C Output Control Register           01B3h         Flash Memory Control Register 4           01B4h         FMR4           01B5h         Flash Memory Control Register 1           01B6h         FMR1           01B7h         Flash Memory Control Register 0				
00F0h         00F1h           00F2h         00F3h           00F4h         00F4h           00F5h         00F6h           00F7h         00F8h           00F9h         00F9h           00F8h         00F9h           00F0h         Pull-Up Control Register 0           00FDh         PUR0         00XX0000b           00FDh         Pull-Up Control Register 1         PUR1         XXXXXXX0Xb           00FEh         Port P1 Drive Capacity Control Register         DRR         00h           00FFh         Timer C Output Control Register         TCOUT         00h           01B3h         Flash Memory Control Register 4         FMR4         01000000b           01B4h         Flash Memory Control Register 1         FMR1         10000000b           01B6h         Flash Memory Control Register 0         FMR0         00000001b				
00F1h         00F2h           00F3h         00F4h           00F4h         00F5h           00F6h         00F7h           00F8h         00F9h           00F9h         00FAh           00FBh         00FBh           00FDh         Pull-Up Control Register 0           00FDh         Pull-Up Control Register 1           00FEh         Port P1 Drive Capacity Control Register           00FFh         Timer C Output Control Register           01B3h         Flash Memory Control Register 4           01B5h         Flash Memory Control Register 1           01B5h         Flash Memory Control Register 1           01B7h         Flash Memory Control Register 0           01B7h         Flash Memory Control Register 0           01B7h         Flash Memory Control Register 0	00F0h			
00F3h         00F4h           00F5h         00F6h           00F7h         00F8h           00F9h         00F9h           00F8h         00F9h           00F8h         00F9h           00F8h         00F9h           00FCh         Pull-Up Control Register 0         PUR0         00XX0000b           00FDh         Pull-Up Control Register 1         PUR1         XXXXXXXXXb           00FEh         Port P1 Drive Capacity Control Register         DRR         00h           00FFh         Timer C Output Control Register         TCOUT         00h           01B3h         Flash Memory Control Register 4         FMR4         01000000b           01B4h         01B5h         Flash Memory Control Register 1         FMR1         10000000xb           01B6h         01B7h         Flash Memory Control Register 0         FMR0         000000001b	00F1h			
00F4h         00F5h           00F6h         00F7h           00F8h         00F9h           00F9h         00F8h           00FBh         00FCh           00FCh         Pull-Up Control Register 0         PUR0         00XX0000b           00FDh         Pull-Up Control Register 1         PUR1         XXXXXXXXb           00FEh         Port P1 Drive Capacity Control Register         DRR         00h           00FFh         Timer C Output Control Register         TCOUT         00h           01B3h         Flash Memory Control Register 4         FMR4         01000000b           01B4h         01B5h         Flash Memory Control Register 1         FMR1         1000000Xb           01B6h         01B7h         Flash Memory Control Register 0         FMR0         000000001b	00F2h			
00F5h         00F6h           00F7h         00F8h           00F9h         00F9h           00FAh         00FBh           00FCh         Pull-Up Control Register 0         PUR0         00XX0000b           00FDh         Pull-Up Control Register 1         PUR1         XXXXXXXXX           00FEh         Port P1 Drive Capacity Control Register         DRR         00h           00FFh         Timer C Output Control Register         TCOUT         00h           01B3h         Flash Memory Control Register 4         FMR4         01000000b           01B4h         01B5h         Flash Memory Control Register 1         FMR1         1000000Xb           01B7h         Flash Memory Control Register 0         FMR0         00000001b				
00F6h         00F7h           00F8h         00F9h           00F9h         00FAh           00FBh         00FCh           00FCh         Pull-Up Control Register 0         PUR0         00XX0000b           00FDh         Pull-Up Control Register 1         PUR1         XXXXXXXXX           00FEh         Port P1 Drive Capacity Control Register         DRR         00h           00FFh         Timer C Output Control Register         TCOUT         00h           01B3h         Flash Memory Control Register 4         FMR4         01000000b           01B4h         01B5h         Flash Memory Control Register 1         FMR1         1000000Xb           01B6h         01B7h         Flash Memory Control Register 0         FMR0         00000001b	UUF4h			
00F7h         00F8h           00F9h         00F9h           00FAh         00FBh           00FBh         00FCh           00FCh         Pull-Up Control Register 0         PUR0         00XX0000b           00FDh         Pull-Up Control Register 1         PUR1         XXXXXXXXX           00FEh         Port P1 Drive Capacity Control Register         DRR         00h           00FFh         Timer C Output Control Register         TCOUT         00h           01B3h         Flash Memory Control Register 4         FMR4         01000000b           01B4h         01B5h         Flash Memory Control Register 1         FMR1         1000000Xb           01B6h         01B7h         Flash Memory Control Register 0         FMR0         00000001b				
00F8h         00F9h           00F8h         00F8h           00FBh         00FBh           00FCh         Pull-Up Control Register 0         PUR0         00XX0000b           00FDh         Pull-Up Control Register 1         PUR1         XXXXXX0Xb           00FEh         Port P1 Drive Capacity Control Register         DRR         00h           00FFh         Timer C Output Control Register         TCOUT         00h           01B3h         Flash Memory Control Register 4         FMR4         01000000b           01B4h         01B5h         Flash Memory Control Register 1         FMR1         1000000Xb           01B6h         01B7h         Flash Memory Control Register 0         FMR0         00000001b				
00F9h         00FAh           00FAh         00FBh           00FCh         Pull-Up Control Register 0         PUR0         00XX0000b           00FDh         Pull-Up Control Register 1         PUR1         XXXXXX0Xb           00FEh         Port P1 Drive Capacity Control Register         DRR         00h           00FFh         Timer C Output Control Register         TCOUT         00h           01B3h         Flash Memory Control Register 4         FMR4         010000000b           01B4h         01B5h         Flash Memory Control Register 1         FMR1         1000000Xb           01B6h         01B7h         Flash Memory Control Register 0         FMR0         00000001b				
00FAh         00FAh           00FBh         00FCh           00FCh         Pull-Up Control Register 0           00FDh         Pull-Up Control Register 1           00FEh         Port P1 Drive Capacity Control Register           00FFh         Timer C Output Control Register           01B3h         Flash Memory Control Register 4           01B4h         FMR4           01B5h         Flash Memory Control Register 1           01B6h         FMR1           01B7h         Flash Memory Control Register 0           FMR0         00000001b				
00FBh         00FCh         Pull-Up Control Register 0         PUR0         00XX0000b           00FDh         Pull-Up Control Register 1         PUR1         XXXXXX0Xb           00FEh         Port P1 Drive Capacity Control Register         DRR         00h           00FFh         Timer C Output Control Register         TCOUT         00h           01B3h         Flash Memory Control Register 4         FMR4         01000000b           01B4h         Flash Memory Control Register 1         FMR1         1000000Xb           01B6h         Flash Memory Control Register 0         FMR0         00000001b	00FAh			
00FCh         Pull-Up Control Register 0         PUR0         00XX0000b           00FDh         Pull-Up Control Register 1         PUR1         XXXXXX0Xb           00FEh         Port P1 Drive Capacity Control Register         DRR         00h           00FFh         Timer C Output Control Register         TCOUT         00h           01B3h         Flash Memory Control Register 4         FMR4         01000000b           01B4h         01B5h         Flash Memory Control Register 1         FMR1         1000000Xb           01B6h         01B7h         Flash Memory Control Register 0         FMR0         00000001b	00FBh			
00FEh         Port P1 Drive Capacity Control Register         DRR         00h           00FFh         Timer C Output Control Register         TCOUT         00h           01B3h         Flash Memory Control Register 4         FMR4         010000000b           01B4h         01B5h         Flash Memory Control Register 1         FMR1         10000000xb           01B6h         01B7h         Flash Memory Control Register 0         FMR0         00000001b	00FCh	Pull-Up Control Register 0		
00FFh         Timer C Output Control Register         TCOUT         00h           01B3h         Flash Memory Control Register 4         FMR4         01000000b           01B4h         501B5h         Flash Memory Control Register 1         FMR1         1000000Xb           01B6h         701B6h         701B6h         700000001b           01B7h         Flash Memory Control Register 0         FMR0         00000001b	00FDh	Pull-Up Control Register 1		
01B3h         Flash Memory Control Register 4         FMR4         010000000b           01B4h         50         FMR1         1000000Xb           01B5h         Flash Memory Control Register 1         FMR1         1000000Xb           01B6h         01B7h         Flash Memory Control Register 0         FMR0         00000001b	UUFEh	Timer C Output Control Register		
01B4h         01B5h         Flash Memory Control Register 1         FMR1         1000000Xb           01B6h         01B7h         Flash Memory Control Register 0         FMR0         00000001b	UUFFN	Timer C Output Control Register	10001	UUII
01B4h         01B5h         Flash Memory Control Register 1         FMR1         1000000Xb           01B6h         01B7h         Flash Memory Control Register 0         FMR0         00000001b	01B3h	Flash Memory Control Register 4	I FMR4	I 01000000b
01B5h         Flash Memory Control Register 1         FMR1         1000000Xb           01B6h         01B7h         Flash Memory Control Register 0         FMR0         00000001b		aaanory control regional 4		0.000000
01B6h         01B7h         Flash Memory Control Register 0         FMR0         00000001b	01B5h	Flash Memory Control Register 1	FMR1	1000000Xb
01B7h Flash Memory Control Register 0 FMR0 00000001b	01B6h	-		
0FFFFh   Optional Function Select Register   OFS   (Note 2)	01B7h	Flash Memory Control Register 0	FMR0	00000001b
UFFFF   Optional Function Select Register   OFS   (Note 2)				
	0FFFFh	Optional Function Select Register	OFS	(Note 2)

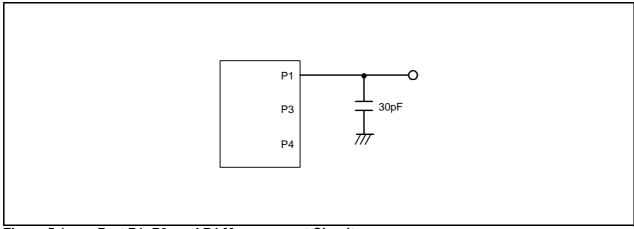
### X: Undefined NOTES:

- The blank regions, 0100h to 01B2h and 01B8h to 02FFh are all reserved. Do not access locations in these regions.
   The OFS register cannot be changed by a program. Use a flash programmer to write to it.

Table 5.3 **Comparator Characteristics** 

Symbol	Parameter	Conditions		Unit		
Symbol	Falametei	Conditions	Min.	Тур.	Max.	Offic
_	Resolution		-	-	1	Bit
-	Absolute accuracy	$\phi AD = 10 \text{ MHz}^{(3)}$	-	-	±20	mV
tconv	Conversion time	φAD = 10 MHz <sup>(3)</sup>	1	=	=	μS
Vref	Reference voltage		0	=	AVcc	V
VIA	Analog input voltage		0	=	AVcc	V
_	Comparator conversion operating clock frequency <sup>(2)</sup>		1	ı	10	MHz

- Vcc = 2.7 to 5.5 V at Topr = -20 to 85 °C / -40 to 85 °C, unless otherwise specified.
   If f1 exceeds 10 MHz, divided f1 and ensure the comparator conversion operating clock frequency (φAD) is 10 MHz or below.
- 3. If AVcc is less than 4.2 V, divided f1 and ensure the comparator conversion operating clock frequency (\$\phiAD\$) is f1/2 or below.



Port P1, P3, and P4 Measurement Circuit Figure 5.1

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Table 5.4 Flash Memory (Program ROM) Electrical Characteristics

Cymahal	Dorometer	Conditions		Linit		
Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
=	Program/erase endurance <sup>(2)</sup>	R8C/18 Group	100(3)	-	=	times
		R8C/19 Group	1,000(3)	-	-	times
-	Byte program time		ī	50	400	μS
=	Block erase time		_	0.4	9	S
td(SR-SUS)	Time delay from suspend request until suspend		=	=	97+CPU clock × 6 cycles	μS
_	Interval from erase start/restart until following suspend request		650	=	-	μS
_	Interval from program start/restart until following suspend request		0	=	-	ns
=	Time from suspend until program/erase restart		=	=	3+CPU clock × 4 cycles	μS
_	Program, erase voltage		2.7	_	5.5	V
-	Read voltage		2.7	-	5.5	V
=	Program, erase temperature		0	-	60	°C
=	Data hold time <sup>(8)</sup>	Ambient temperature = 55 °C	20	-	=	year

- 1. Vcc = 2.7 to 5.5 V at Topr = 0 to 60 °C, unless otherwise specified.
- 2. Definition of programming/erasure endurance
  - The programming and erasure endurance is defined on a per-block basis.
  - If the programming and erasure endurance is n (n = 100 or 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one. However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
- 3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
- 4. If emergency processing is required, a suspend request can be generated independent of this characteristic. In that case the normal time delay to Suspend can be applied to the request. However, we recommend that a suspend request with an interval of less than 650 μs is only used once because, if the suspend state continues, erasure cannot operate and the incidence of erasure error rises.
- 5. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. In addition, averaging the number of erase operations between block A and block B can further reduce the effective number of rewrites. It is also advisable to retain data on the erase count of each block and limit the number of erase operations to a certain number.
- 6. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
- 7. Customers desiring programming/erasure failure rate information should contact their Renesas technical support representative.
- 8. The data hold time includes time that the power supply is off or the clock is not supplied.

Cumbal	Parameter	Conditions		Unit		
Symbol	Parameter	Conditions	Min.	Тур.	Max.	Uniii
=	Program/erase endurance <sup>(2)</sup>		10,000(3)	-	-	times
=	Byte program time (Program/erase endurance ≤ 1,000 times)		_	50	400	μS
_	Byte program time (Program/erase endurance > 1,000 times)		_	65	_	μS
=	Block erase time (Program/erase endurance ≤ 1,000 times)		=	0.2	9	S
=	Block erase time (Program/erase endurance > 1,000 times)		=	0.3	_	S
td(SR-SUS)	Time delay from suspend request until suspend		_	=	97+CPU clock × 6 cycles	μS
_	Interval from erase start/restart until following suspend request		650	_	_	μS
_	Interval from program start/restart until following suspend request		0	_	_	ns
=	Time from suspend until program/erase restart		_	=	3+CPU clock × 4 cycles	μS
_	Program, erase voltage		2.7	_	5.5	V
=	Read voltage		2.7	-	5.5	V
=	Program, erase temperature		-20 <sup>(8)</sup>	=	85	°C
_	Data hold time <sup>(9)</sup>	Ambient temperature = 55 °C	20	-	_	year

Table 5.5 Flash Memory (Data flash Block A, Block B) Electrical Characteristics

- 1. Vcc = 2.7 to 5.5 V at  $T_{opr} = -20$  to 85 °C / -40 to 85 °C, unless otherwise specified.
- 2. Definition of programming/erasure endurance
  - The programming and erasure endurance is defined on a per-block basis.
  - If the programming and erasure endurance is n (n = 100 or 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one. However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
- 3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
- 4. If emergency processing is required, a suspend request can be generated independent of this characteristic. In that case the normal time delay to suspend can be applied to the request. However, we recommend that a suspend request with an interval of less than 650 μs is only used once because, if the suspend state continues, erasure cannot operate and the incidence of erasure error rises.
- 5. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erase count of each block and limit the number of erase operations to a certain number.
- 6. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
- 7. Customers desiring programming/erasure failure rate information should contact their Renesas technical support representative.
- 8. -40 °C for D version.
- 9. The data hold time includes time that the power supply is off or the clock is not supplied.

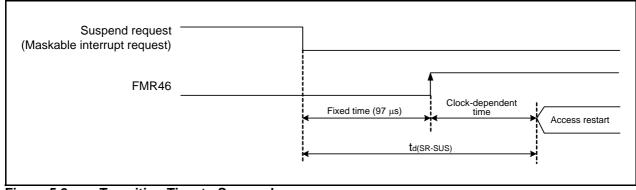


Figure 5.2 Transition Time to Suspend

Table 5.8 Reset Circuit Electrical Characteristics (When Using Voltage Monitor 1 Reset)

Symbol	Parameter	Condition	,	Standard		Unit
			Min.	Тур.	Max.	
Vpor2	Power-on reset valid voltage	$-20^{\circ}C \leq Topr \leq 85^{\circ}C$	-	-	Vdet1	V
tw(Vpor2-Vdet1)	Supply voltage rising time when power-on reset is deasserted <sup>(1)</sup>	$ -20^{\circ}C \leq Topr \leq 85^{\circ}C, \\ t_{w(por2)} \geq 0s^{(3)} $	I	I	100	ms

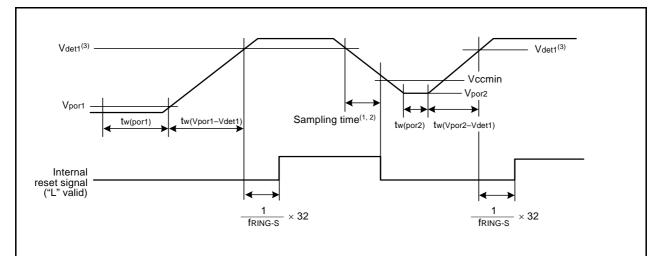
- 1. This condition is not applicable when using with  $Vcc \ge 1.0 \text{ V}$ .
- 2. When turning power on after the time to hold the external power below effective voltage (Vpor1) exceeds10 s, refer to Table 5.9 Reset Circuit Electrical Characteristics (When Not Using Voltage Monitor 1 Reset).
- 3. tw(por2) is the time to hold the external power below effective voltage (Vpor2).

Reset Circuit Electrical Characteristics (When Not Using Voltage Monitor 1 Reset) Table 5.9

Symbol	Parameter	Condition		Standar	d	Unit
			Min.	Тур.	Max.	
Vpor1	Power-on reset valid voltage	-20°C ≤ Topr ≤ 85°C	=	=	0.1	V
tw(Vpor1-Vdet1)	Supply voltage rising time when power-on reset is deasserted	$0^{\circ}C \leq Topr \leq 85^{\circ}C,$ $tw(por1) \geq 10 s^{(2)}$	-	-	100	ms
tw(Vpor1-Vdet1)	Supply voltage rising time when power-on reset is deasserted	$ -20^{\circ}C \leq Topr < 0^{\circ}C, \\ tw(por1) \geq 30 \ s^{(2)} $	-	=	100	ms
tw(Vpor1-Vdet1)	Supply voltage rising time when power-on reset is deasserted	$ -20^{\circ}C \leq Topr < 0^{\circ}C, $ $ tw(por1) \geq 10 \ s^{(2)} $	-	=	1	ms
tw(Vpor1-Vdet1)	Supply voltage rising time when power-on reset is deasserted	$0^{\circ}C \leq Topr \leq 85^{\circ}C,$ $tw(por1) \geq 1 s^{(2)}$	-	-	0.5	ms

### NOTES:

- 1. When not using voltage monitor 1, use with  $Vcc \ge 2.7 \text{ V}$ .
- 2. tw(por1) is the time to hold the external power below effective voltage (Vpor1).



- 1. Hold the voltage inside the MCU operation voltage range (Vccmin or above) within the sampling time.
- The sampling clock can be selected. Refer to 7. Voltage Detection Circuit for details.
   Vdet1 indicates the voltage detection level of the voltage detection 1 circuit. Refer to 7. Voltage Detection Circuit for details.

Figure 5.3 **Reset Circuit Electrical Characteristics** 

## **Timing Requirements**

(Unless Otherwise Specified: Vcc = 5 V, Vss = 0 V at Ta = 25 °C) [Vcc = 5 V]

Table 5.14 XIN Input

Symbol	Parameter		Standard		
			Max.	Unit	
tc(XIN)	XIN input cycle time	50	=	ns	
twh(xin)	XIN input "H" width	25	=	ns	
twl(XIN)	XIN input "L" width	25	-	ns	

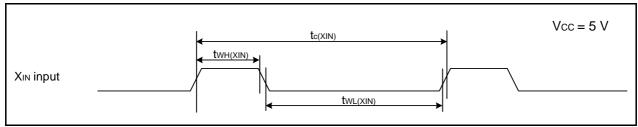


Figure 5.4 XIN Input Timing Diagram when Vcc = 5 V

Table 5.15 CNTR0 Input, CNTR1 Input, INT1 Input

Symbol	Parameter		Standard		
			Max.	Unit	
tc(CNTR0)	CNTR0 input cycle time	100	=	ns	
tWH(CNTR0)	CNTR0 input "H" width	40	=	ns	
tWL(CNTR0)	CNTR0 input "L" width	40		ns	

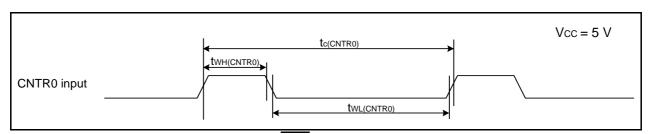


Figure 5.5 CNTR0 Input, CNTR1 Input, INT1 Input Timing Diagram when Vcc = 5 V

Table 5.16 TCIN Input, INT3 Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	Offic
tc(TCIN)	TCIN input cycle time	400 <sup>(1)</sup>	-	ns
tWH(TCIN)	TCIN input "H" width	200(2)	-	ns
tWL(TCIN)	TCIN input "L" width	200(2)	-	ns

- 1. When using timer C input capture mode, adjust the cycle time to (1/timer C count source frequency x 3) or above.
- 2. When using timer C input capture mode, adjust the pulse width to (1/timer C count source frequency x 1.5) or above.

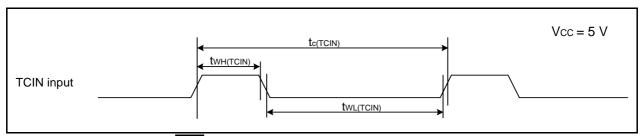


Figure 5.6 TCIN Input, INT3 Input Timing Diagram when Vcc = 5 V

Table 5.17 Senal Interrace	<b>Table</b>	5.17	Serial	Interface
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Symbol	Parameter	Standard		Unit
	Falanteter		Max.	
tc(CK)	CLKi input cycle time	200	-	ns
tW(CKH)	CLKi input "H" width	100	=	ns
tW(CKL)	CLKi input "L" width	100	=	ns
td(C-Q)	TXDi output delay time	-	50	ns
th(C-Q)	TXDi hold time	0	-	ns
tsu(D-C)	RXDi input setup time	50	=	ns
th(C-D)	RXDi input hold time	90	-	ns

i = 0 or 1

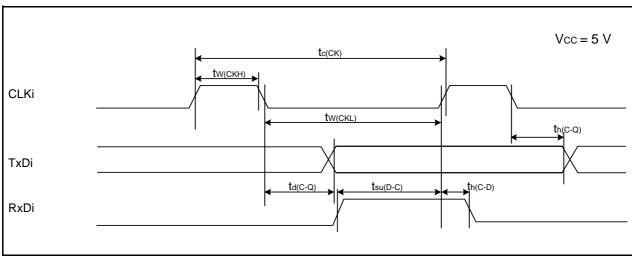


Figure 5.7 Serial Interface Timing Diagram when Vcc = 5 V

Table 5.18 External Interrupt INTO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	Offic
tW(INH)	INTO input "H" width	250 <sup>(1)</sup>	-	ns
tW(INL)	INTO input "L" width	250(2)	-	ns

### NOTES:

- 1. When selecting the digital filter by the INT0 input filter select bit, use an INT0 input HIGH width of either (1/digital filter clock frequency x 3) or the minimum value of standard, whichever is greater.
- 2. When selecting the digital filter by the INT0 input filter select bit, use an INT0 input LOW width of either (1/digital filter clock frequency x 3) or the minimum value of standard, whichever is greater.

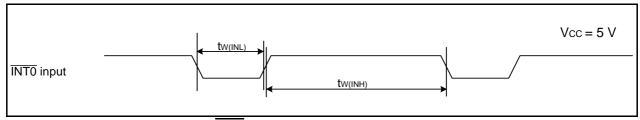


Figure 5.8 External Interrupt INTO Input Timing Diagram when Vcc = 5 V

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Table 5.24 Serial Interface

Symbol	Parameter	Standard		Unit
	Farameter		Max.	
tc(CK)	CLKi input cycle time	300	=	ns
tW(CKH)	CLKi input "H" width	150	=	ns
tW(CKL)	CLKi input "L" width	150	-	ns
td(C-Q)	TXDi output delay time	=	80	ns
th(C-Q)	TXDi hold time	0	-	ns
tsu(D-C)	RXDi input setup time	70	=	ns
th(C-D)	RXDi input hold time	90	-	ns

i = 0 or 1

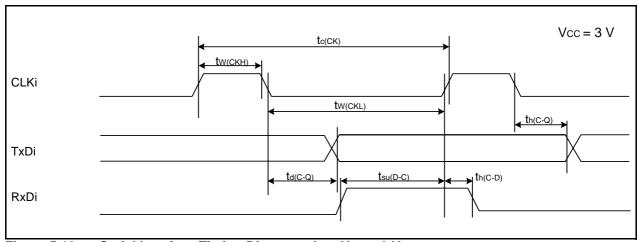


Figure 5.12 Serial Interface Timing Diagram when Vcc = 3 V

Table 5.25 External Interrupt INTO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	Offic
tW(INH)	INTO input "H" width	380 <sup>(1)</sup>	-	ns
tW(INL)	INTO input "L" width	380(2)	-	ns

- 1. When selecting the digital filter by the INT0 input filter select bit, use an INT0 input HIGH width of either (1/digital filter clock frequency x 3) or the minimum value of standard, whichever is greater.
- 2. When selecting the digital filter by the INT0 input filter select bit, use an INT0 input LOW width of either (1/digital filter clock frequency x 3) or the minimum value of standard, whichever is greater.

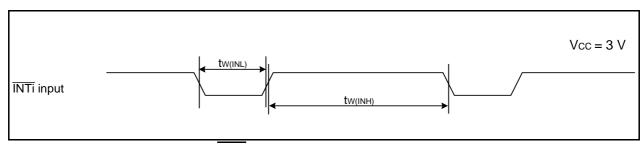
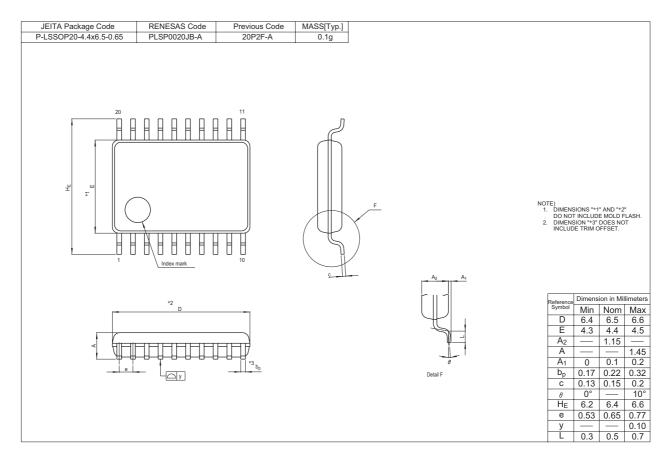
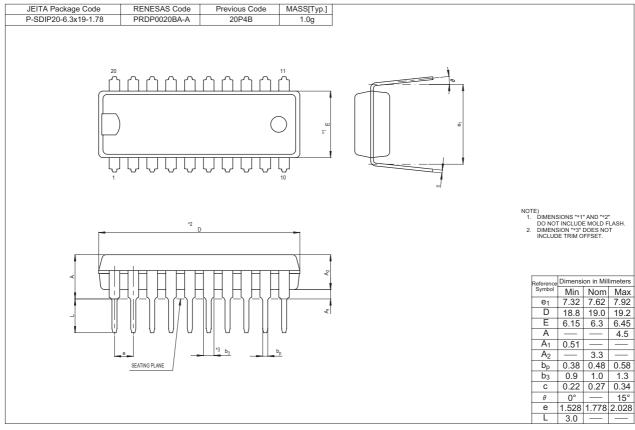


Figure 5.13 External Interrupt INTO Input Timing Diagram when Vcc = 3 V

# **Package Dimensions**





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