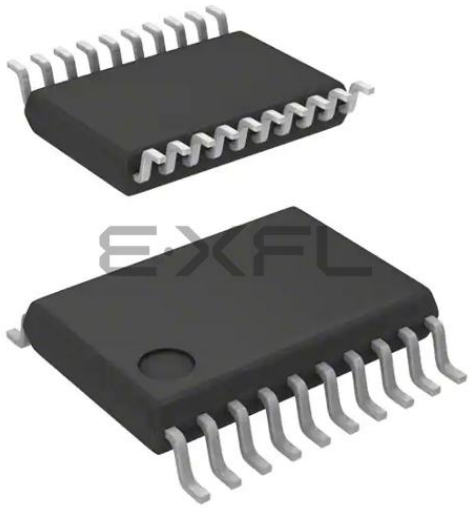

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	SIO, UART/USART
Peripherals	LED, POR, Voltage Detect, WDT
Number of I/O	13
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-LSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21192dsp-u0

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1. Overview

These MCUs are fabricated using a high-performance silicon gate CMOS process, embedding the R8C/Tiny Series CPU core, and is packaged in a 20-pin molded-plastic LSSOP, SDIP or a 28-pin plastic molded-HWQFN. It implements sophisticated instructions for a high level of instruction efficiency. With 1 Mbyte of address space, they are capable of executing instructions at high speed.
Furthermore, the R8C/19 Group has on-chip data flash ROM (1 KB × 2 blocks).
The difference between the R8C/18 Group and R8C/19 Group is only the presence or absence of data flash ROM. Their peripheral functions are the same.

1.1 Applications

Electric household appliances, office equipment, housing equipment (sensors, security systems), general industrial equipment, audio equipment, etc.

1.2 Performance Overview

Table 1.1 outlines the Functions and Specifications for R8C/18 Group and Table 1.2 outlines the Functions and Specifications for R8C/19 Group.

Table 1.1 Functions and Specifications for R8C/18 Group

Item		Specification
CPU	Number of fundamental instructions	89 instructions
	Minimum instruction execution time	50 ns (f(XIN) = 20 MHz, VCC = 3.0 to 5.5 V) 100 ns (f(XIN) = 10 MHz, VCC = 2.7 to 5.5 V)
	Operation mode	Single-chip
	Address space	1 Mbyte
	Memory capacity	Refer to **Table 1.3 Product Information for R8C/18 Group**
Peripheral Functions	Ports	I/O ports: 13 pins (including LED drive port) Input port: 3 pins
	LED drive ports	I/O ports: 4 pins
	Timers	Timer X: 8 bits × 1 channel, timer Z: 8 bits × 1 channel (Each timer equipped with 8-bit prescaler) Timer C: 16 bits × 1 channel (Input capture and output compare circuits)
	Serial interfaces	1 channel Clock synchronous serial I/O, UART 1 channel UART
	Comparator	1-bit comparator: 1 circuit, 4 channels
	Watchdog timer	15 bits × 1 channel (with prescaler) Reset start selectable, count source protection mode
	Interrupts	Internal: 10 sources, External: 4 sources, Software: 4 sources, Priority levels: 7 levels
	Clock generation circuits	2 circuits • Main clock oscillation circuit (with on-chip feedback resistor) • On-chip oscillator (high speed, low speed) High-speed on-chip oscillator has frequency adjustment function
	Oscillation stop detection function	Main clock oscillation stop detection function
	Voltage detection circuit	On-chip
	Power-on reset circuit	On-chip
Electric Characteristics	Supply voltage	VCC = 3.0 to 5.5 V (f(XIN) = 20 MHz) VCC = 2.7 to 5.5 V (f(XIN) = 10 MHz)
	Current consumption	Typ. 9 mA (VCC = 5.0 V, f(XIN) = 20 MHz, comparator stopped) Typ. 5 mA (VCC = 3.0V, f(XIN) = 10 MHz, comparator stopped) Typ. 35 μA (VCC = 3.0 V, wait mode, peripheral clock off) Typ. 0.7 μA (VCC = 3.0 V, stop mode)
Flash Memory	Programming and erasure voltage	VCC = 2.7 to 5.5 V
	Programming and erasure endurance	100 times
Operating Ambient Temperature		-20 to 85°C -40 to 85°C (D version)
Package		20-pin molded-plastic LSSOP
		20-pin molded-plastic SDIP
		28-pin molded-plastic HWQFN

1.3 Block Diagram

Figure 1.1 shows a Block Diagram.

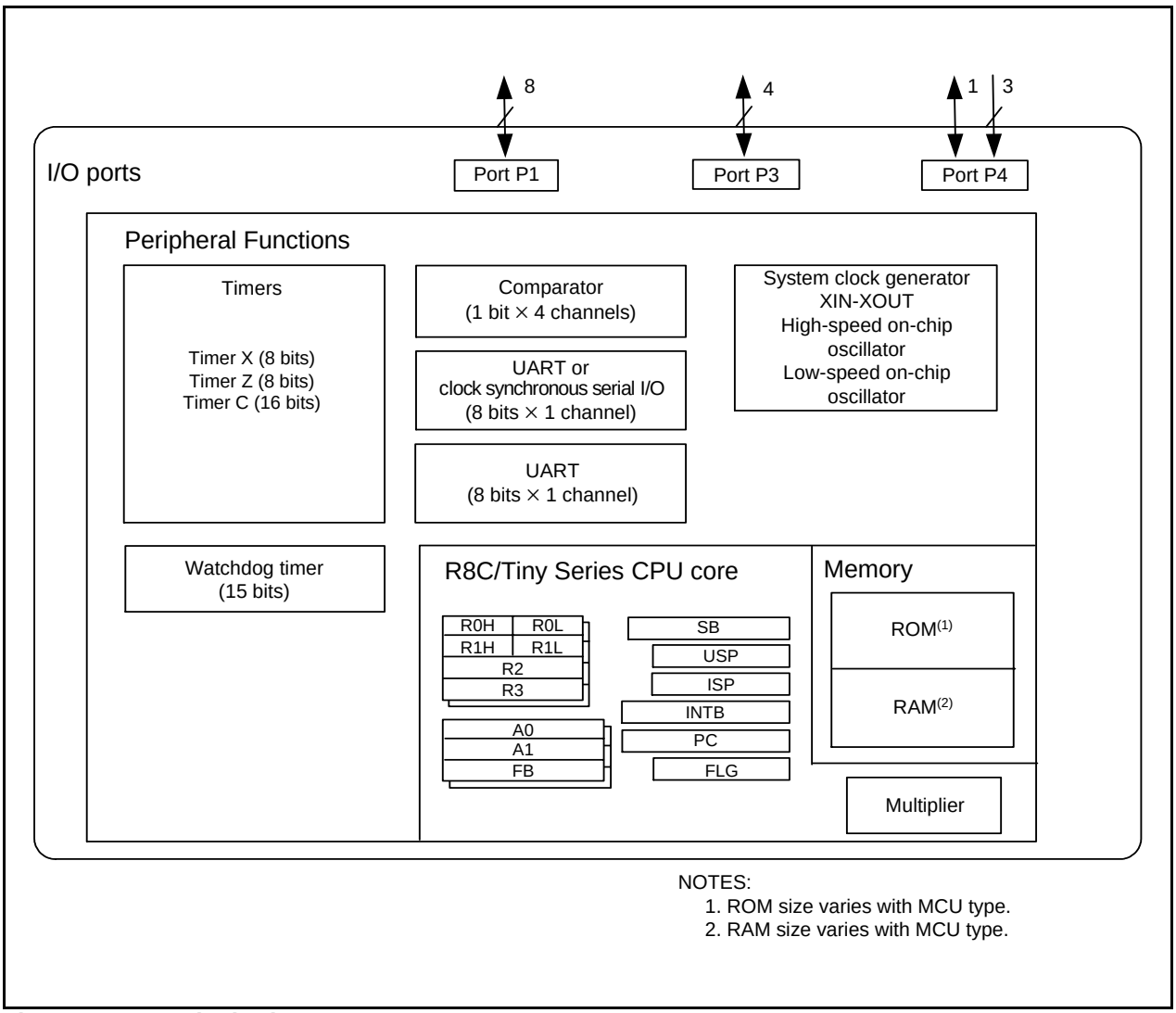


Figure 1.1 Block Diagram

Table 1.4 Product Information for R8C/19 Group Current of Apr. 2006

Type No.	ROM Capacity		RAM Capacity	Package Type	Remarks
	Program ROM	Data flash			
R5F21191SP	4 Kbytes	1 Kbyte × 2	384 bytes	PLSP0020JB-A	Flash memory version
R5F21192SP	8 Kbytes	1 Kbyte × 2	512 bytes	PLSP0020JB-A	
R5F21193SP	12 Kbytes	1 Kbyte × 2	768 bytes	PLSP0020JB-A	
R5F21194SP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLSP0020JB-A	
R5F21191DSP (D)	4 Kbytes	1 Kbyte × 2	384 bytes	PLSP0020JB-A	D version
R5F21192DSP (D)	8 Kbytes	1 Kbyte × 2	512 bytes	PLSP0020JB-A	
R5F21193DSP (D)	12 Kbytes	1 Kbyte × 2	768 bytes	PLSP0020JB-A	
R5F21194DSP (D)	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLSP0020JB-A	
R5F21191DD	4 Kbytes	1 Kbyte × 2	384 bytes	PRDP0020BA-A	Flash memory version
R5F21192DD	8 Kbytes	1 Kbyte × 2	512 bytes	PRDP0020BA-A	
R5F21193DD	12 Kbytes	1 Kbyte × 2	768 bytes	PRDP0020BA-A	
R5F21194DD	16 Kbytes	1 Kbyte × 2	1 Kbyte	PRDP0020BA-A	
R5F21192NP	8 Kbytes	1 Kbyte × 2	512 bytes	PWQN0028KA-B	Flash memory version
R5F21193NP	12 Kbytes	1 Kbyte × 2	768 bytes	PWQN0028KA-B	
R5F21194NP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PWQN0028KA-B	

(D): Under Development

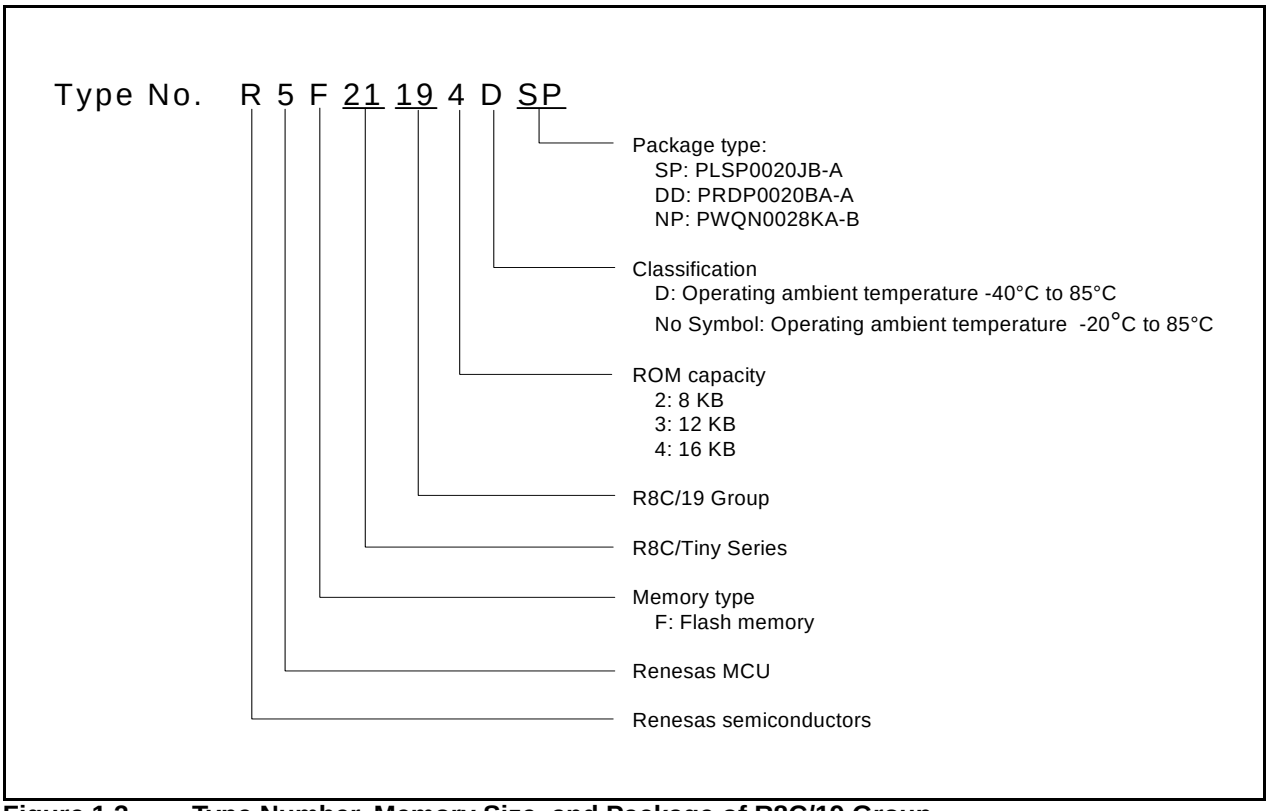


Figure 1.3 Type Number, Memory Size, and Package of R8C/19 Group

1.5 Pin Assignments

Figure 1.4 shows Pin Assignments for PLSP0020JB-A Package (Top View), Figure 1.5 shows Pin Assignments for PRDP0020BA-A Package (Top View) and Figure 1.6 shows Pin Assignments for PWQN0028KA-B Package (Top View).

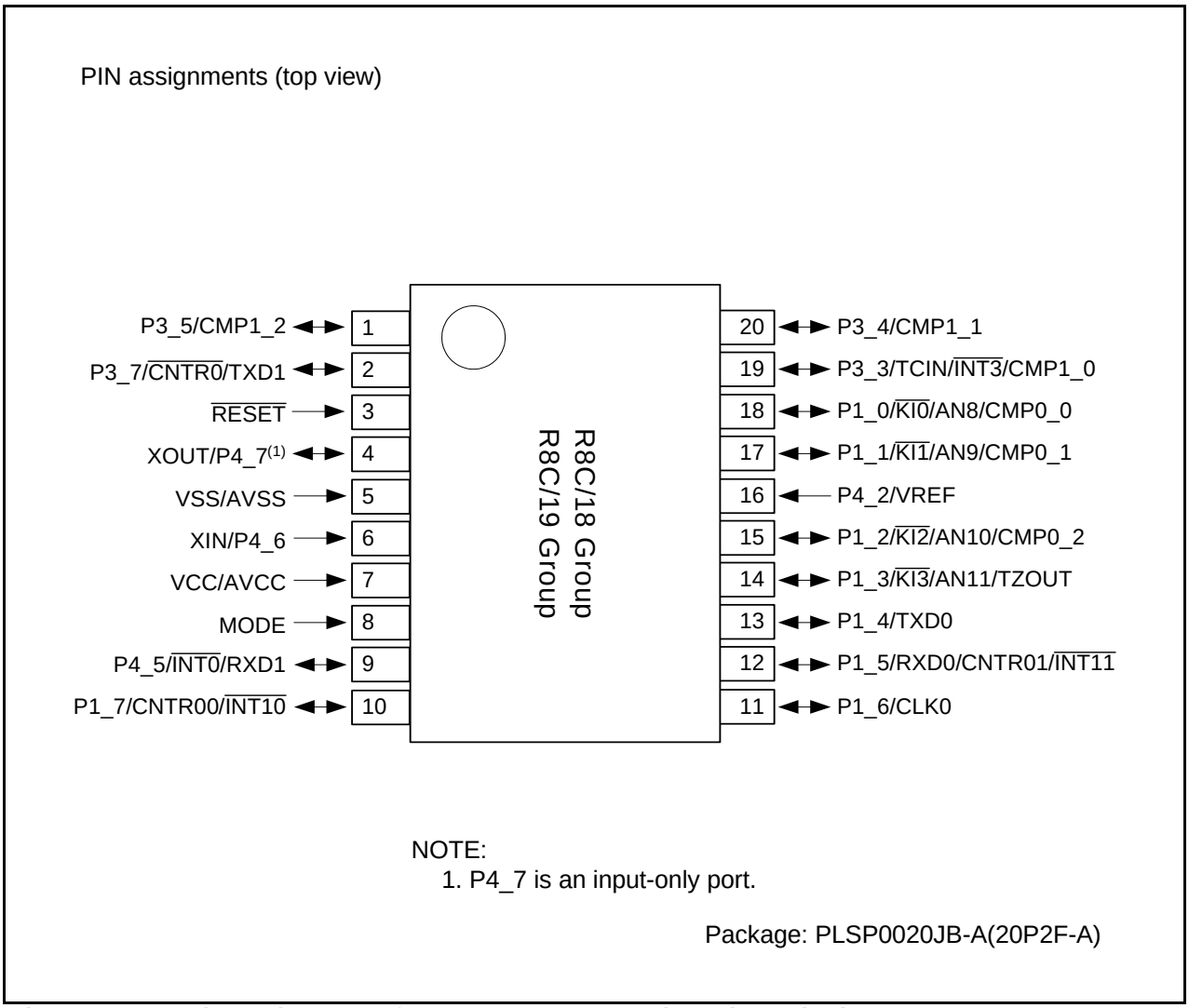


Figure 1.4 Pin Assignments for PLSP0020JB-A Package (Top View)

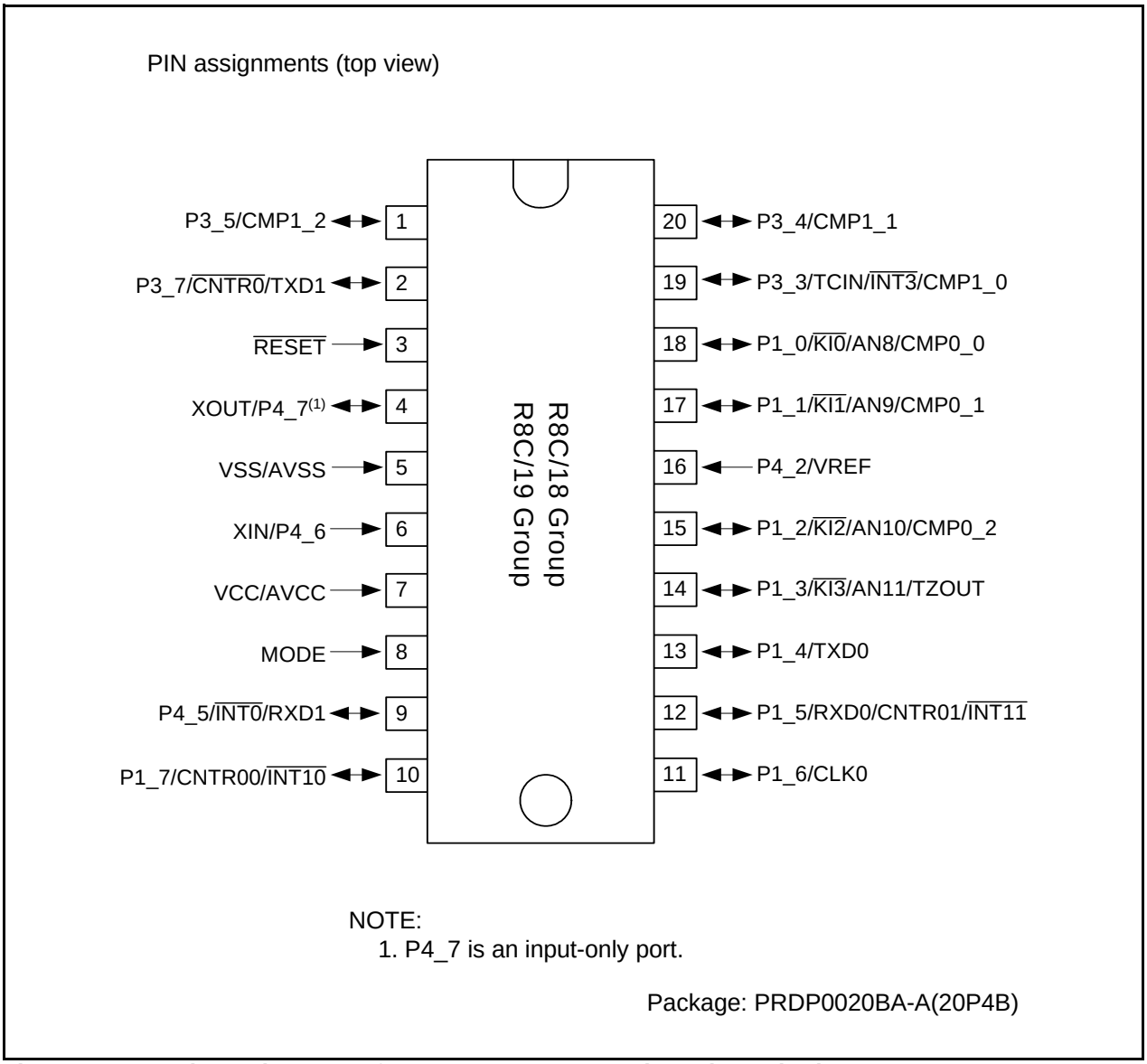
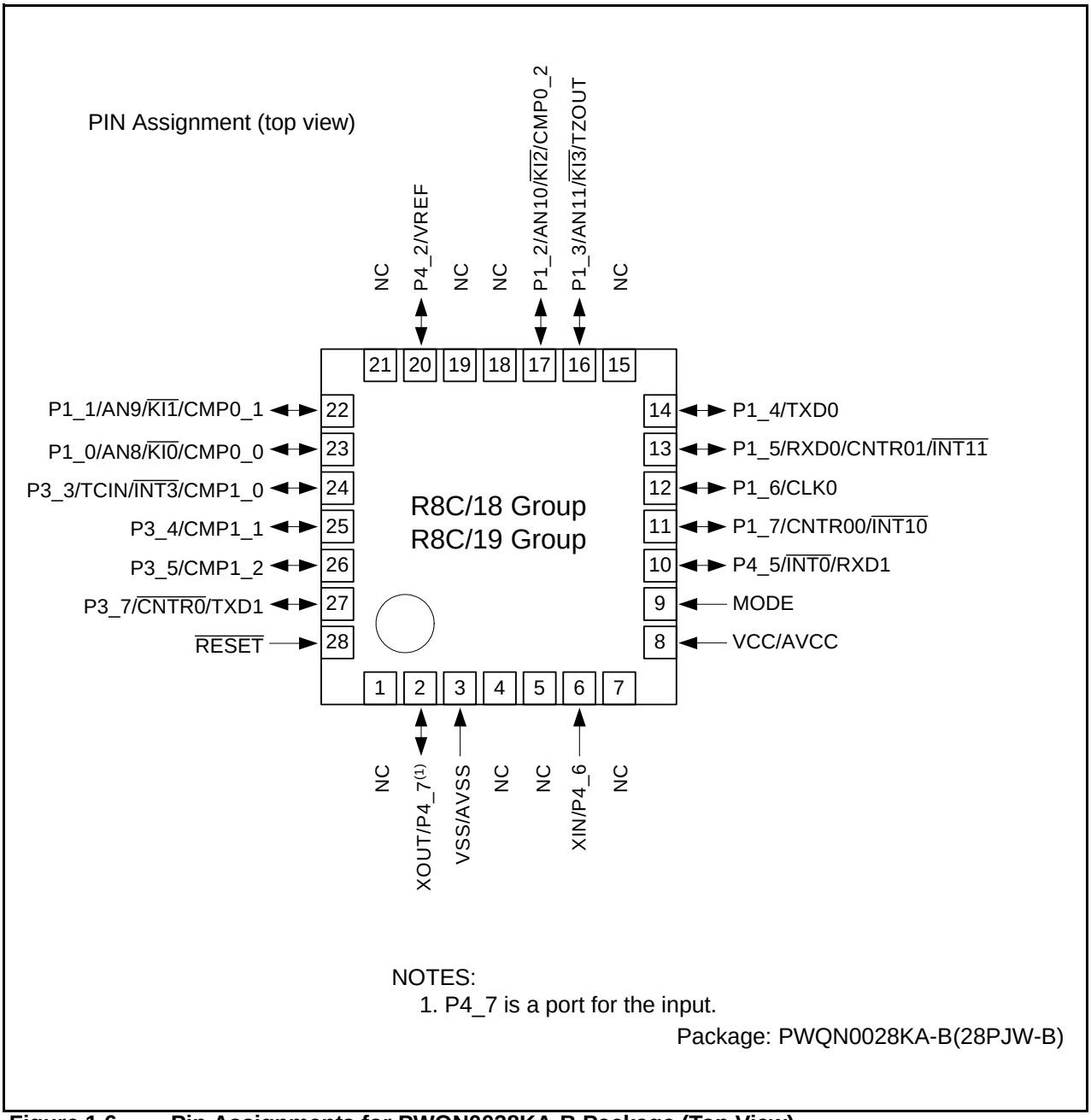


Figure 1.5 Pin Assignments for PRDP0020BA-A Package (Top View)



NOTES:
1. P4_7 is a port for the input.

Package: PWQN0028KA-B(28PJW-B)

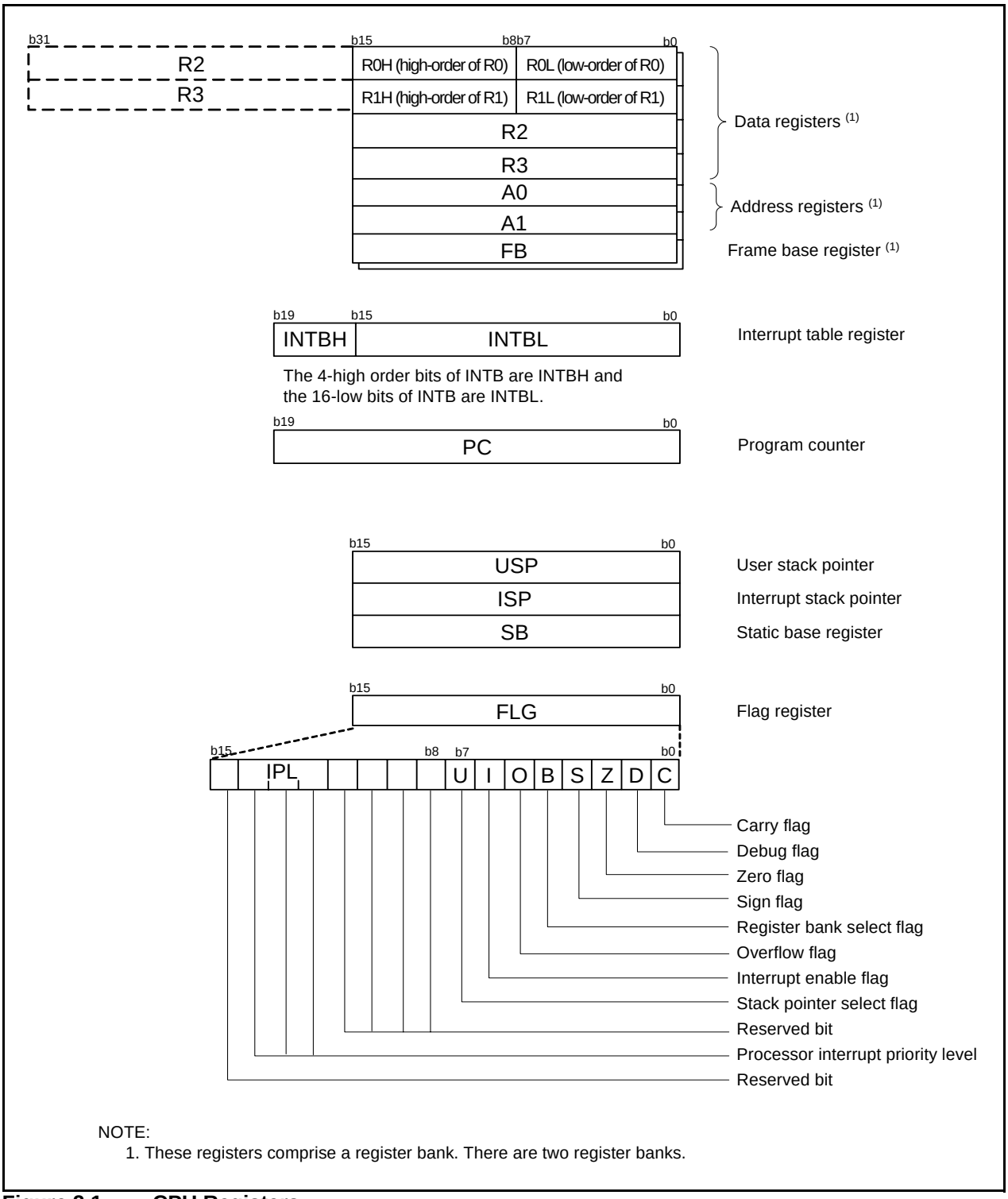
Figure 1.6 Pin Assignments for PWQN0028KA-B Package (Top View)

Table 1.7 Pin Name Information by Pin Number of PWQN0028KA-B package

Pin Number	Control Pin	Port	I/O Pin of Peripheral Function			
			Interrupt	Timer	Serial Interface	Comparator
1	NC					
2	XOUT	P4_7				
3	VSS/AVSS					
4	NC					
5	NC					
6	XIN	P4_6				
7	NC					
8	VCC/AVCC					
9	MODE					
10		P4_5	$\overline{\text{INT0}}$		RXD1	
11		P1_7	$\overline{\text{INT10}}$	CNTR00		
12		P1_6			CLK0	
13		P1_5	$\overline{\text{INT11}}$	CNTR01	RXD0	
14		P1_4			TXD0	
15	NC					
16		P1_3	$\overline{\text{KI3}}$	TZOUT		AN11
17		P1_2	$\overline{\text{KI2}}$	CMP0_2		AN10
18	NC					
19	NC					
20	VREF	P4_2				
21	NC					
22		P1_1	$\overline{\text{KI1}}$	CMP0_1		AN9
23		P1_0	$\overline{\text{KI0}}$	CMP0_0		AN8
24		P3_3	$\overline{\text{INT3}}$	TCIN/CMP1_0		
25		P3_4		CMP1_1		
26		P3_5		CMP1_2		
27		P3_7		$\overline{\text{CNTR0}}$	TXD1	
28	$\overline{\text{RESET}}$					

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. R0, R1, R2, R3, A0, A1, and FB configure a register bank. There are two sets of register bank.



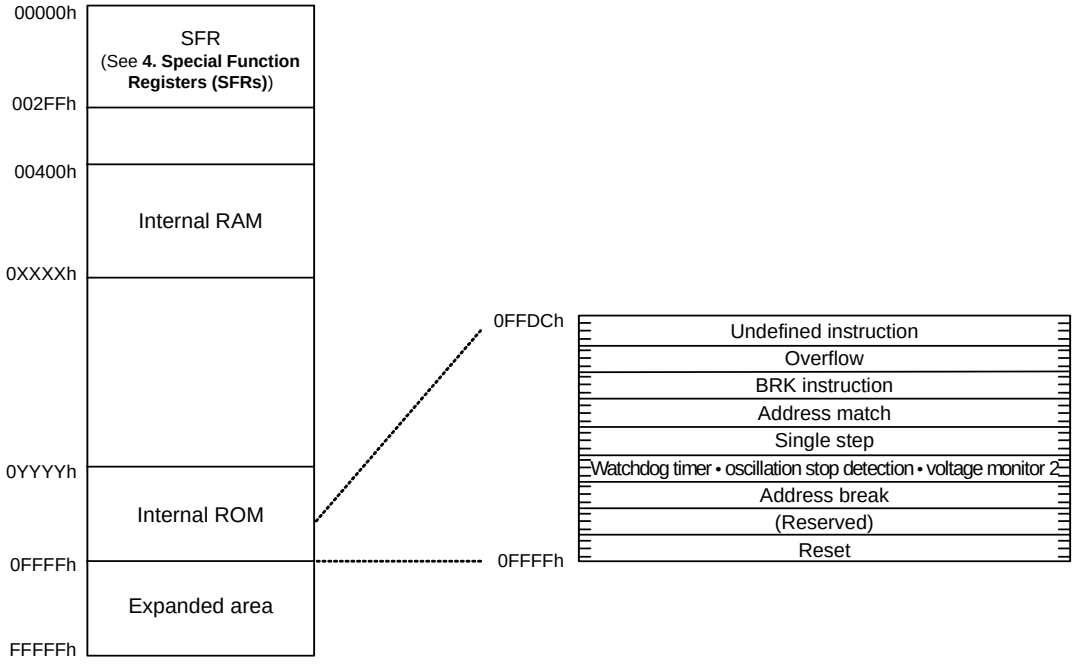
NOTE:
1. These registers comprise a register bank. There are two register banks.

Figure 2.1 CPU Registers

3. Memory

3.1 R8C/18 Group

Figure 3.1 is a Memory Map of R8C/18 Group. The R8C/18 Group has 1 Mbyte of address space from addresses 00000h to FFFFFh.
The internal ROM area is allocated lower addresses, beginning with address 0FFFFh. For example, a 16-Kbyte internal ROM is allocated addresses 0C000h to 0FFFFh.
The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. They store the starting address of each interrupt routine.
The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 1-Kbyte internal RAM area is allocated addresses 00400h to 007FFh. The internal RAM is used not only for storing data but also for calling subroutines and as stacks when interrupt requests are acknowledged.
Special function registers (SFRs) are allocated addresses 00000h to 002FFh. The peripheral function control registers are allocated here. All addresses within the SFR, which have nothing allocated are reserved for future use and cannot be accessed by users.



NOTE:
1. The blank regions are reserved. Do not access locations in these regions.

Part Number	Internal ROM		Internal RAM	
	Size	Address 0YYYYh	Size	Address 0XXXXh
R5F21184SP, R5F21184DSP, R5F21184DD, R5F21184NP	16 Kbytes	0C000h	1 Kbyte	007FFh
R5F21183SP, R5F21183DSP, R5F21183DD, R5F21183NP	12 Kbytes	0D000h	768 bytes	006FFh
R5F21182SP, R5F21182DSP, R5F21182DD, R5F21182NP	8 Kbytes	0E000h	512 bytes	005FFh
R5F21181SP, R5F21181DSP, R5F21181DD	4 Kbytes	0F000h	384 bytes	0057Fh

Figure 3.1 Memory Map of R8C/18 Group

4. Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 4.1 to 4.4 list the special function registers.

Table 4.1 SFR Information (1)[1]

Address	Register	Symbol	After reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	00h
0005h	Processor Mode Register 1	PM1	00h
0006h	System Clock Control Register 0	CM0	01101000b
0007h	System Clock Control Register 1	CM1	00100000b
0008h			
0009h	Address Match Interrupt Enable Register	AIER	00h
000Ah	Protect Register	PRCR	00h
000Bh			
000Ch	Oscillation Stop Detection Register	OCD	00000100b
000Dh	Watchdog Timer Reset Register	WDTR	XXh
000Eh	Watchdog Timer Start Register	WDTS	XXh
000Fh	Watchdog Timer Control Register	WDC	00011111b
0010h	Address Match Interrupt Register 0	RMAD0	00h
0011h			00h
0012h			X0h
0013h			
0014h	Address Match Interrupt Register 1	RMAD1	00h
0015h			00h
0016h			X0h
0017h			
0018h			
0019h			
001Ah			
001Bh			
001Ch	Count Source Protection Mode Register	CSPR	00h
001Dh			
001Eh	$\overline{\text{INT0}}$ Input Filter Select Register	INT0F	00h
001Fh			
0020h	High-Speed On-Chip Oscillator Control Register 0	HRA0	00h
0021h	High-Speed On-Chip Oscillator Control Register 1	HRA1	When shipping
0022h	High-Speed On-Chip Oscillator Control Register 2	HRA2	00h
0023h			
002Ah			
002Bh			
002Ch			
002Dh			
002Eh			
002Fh			
0030h			
0031h	Voltage Detection Register 1[2]	VCA1	00001000b
0032h	Voltage Detection Register 2[2]	VCA2	00h[3] 01000000b[4]
0033h			
0034h			
0035h			
0036h	Voltage Monitor 1 Circuit Control Register [2]	VW1C	0000X000b[3] 0100X001b[4]
0037h	Voltage Monitor 2 Circuit Control Register [5]	VW2C	00h
0038h			
0039h			
003Ah			
003Bh			
003Ch			
003Dh			
003Eh			
003Fh			

X: Undefined

NOTES:

1. The blank regions are reserved. Do not access locations in these regions.
2. Software reset, watchdog timer reset, and voltage monitor 2 reset do not affect this register.
3. After hardware reset.
4. After power-on reset or voltage monitor 1 reset.
5. Software reset, watchdog timer reset, and voltage monitor 2 reset do not affect b2 and b3.

Table 4.2 SFR Information (2)(1)

Address	Register	Symbol	After reset
0040h			
0041h			
0042h			
0043h			
0044h			
0045h			
0046h			
0047h			
0048h			
0049h			
004Ah			
004Bh			
004Ch			
004Dh	Key Input Interrupt Control Register	KUPIC	XXXXX000b
004Eh	Comparator Conversion Interrupt Control Register	ADIC	XXXXX000b
004Fh			
0050h	Compare 1 Interrupt Control Register	CMP1IC	XXXXX000b
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXXX000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXXX000b
0053h	UART1 Transmit Interrupt Control Register	S1TIC	XXXXX000b
0054h	UART1 Receive Interrupt Control Register	S1RIC	XXXXX000b
0055h			
0056h	Timer X Interrupt Control Register	TXIC	XXXXX000b
0057h			
0058h	Timer Z Interrupt Control Register	TZIC	XXXXX000b
0059h	$\overline{\text{INT1}}$ Interrupt Control Register	INT1IC	XXXXX000b
005Ah	$\overline{\text{INT3}}$ Interrupt Control Register	INT3IC	XXXXX000b
005Bh	Timer C Interrupt Control Register	TCIC	XXXXX000b
005Ch	Compare 0 Interrupt Control Register	CMP0IC	XXXXX000b
005Dh	$\overline{\text{INT0}}$ Interrupt Control Register	INT0IC	XX00X000b
005Eh			
005Fh			
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h			
006Ah			
006Bh			
006Ch			
006Dh			
006Eh			
006Fh			
0070h			
0071h			
0072h			
0073h			
0074h			
0075h			
0076h			
0077h			
0078h			
0079h			
007Ah			
007Bh			
007Ch			
007Dh			
007Eh			
007Fh			

X: Undefined

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

Table 5.3 Comparator Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Resolution		–	–	1	Bit
–	Absolute accuracy	ϕ_{AD} = 10 MHz(3)	–	–	±20	mV
t_{conv}	Conversion time	ϕ_{AD} = 10 MHz(3)	1	–	–	µs
V_{ref}	Reference voltage		0	–	AV_{CC}	V
V_{IA}	Analog input voltage		0	–	AV_{CC}	V
–	Comparator conversion operating clock frequency(2)		1	–	10	MHz

NOTES:
1. V_{CC} = 2.7 to 5.5 V at T_{opr} = -20 to 85 °C / -40 to 85 °C, unless otherwise specified.
2. If f1 exceeds 10 MHz, divided f1 and ensure the comparator conversion operating clock frequency (ϕ_{AD}) is 10 MHz or below.
3. If AVcc is less than 4.2 V, divided f1 and ensure the comparator conversion operating clock frequency (ϕ_{AD}) is f1/2 or below.

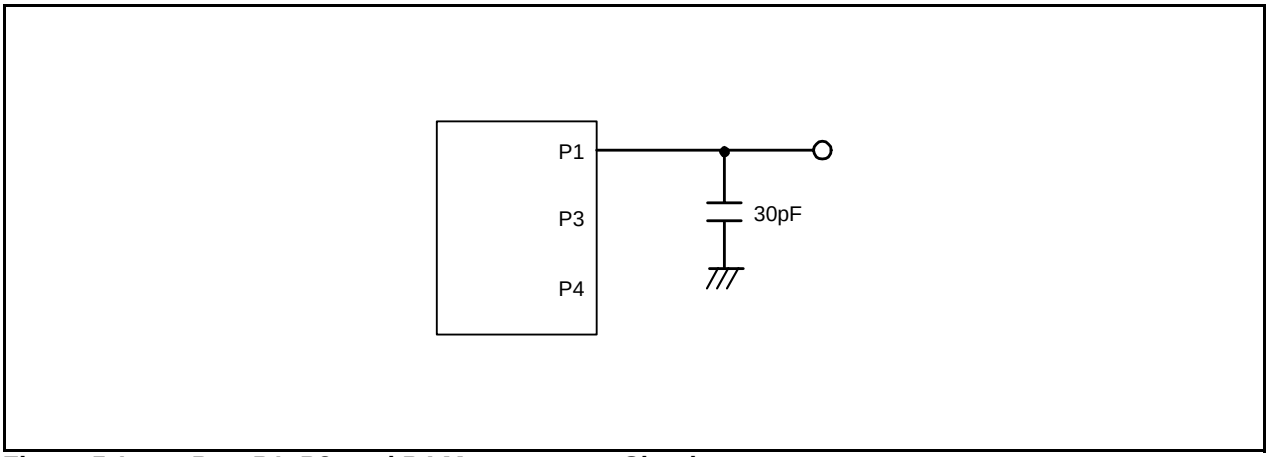


Figure 5.1 Port P1, P3, and P4 Measurement Circuit

Table 5.4 Flash Memory (Program ROM) Electrical Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
–	Program/erase endurance(2)	R8C/18 Group	100(3)	–	–	times
		R8C/19 Group	1,000(3)	–	–	times
–	Byte program time		–	50	400	µs
–	Block erase time		–	0.4	9	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend		–	–	97+CPU clock × 6 cycles	µs
–	Interval from erase start/restart until following suspend request		650	–	–	µs
–	Interval from program start/restart until following suspend request		0	–	–	ns
–	Time from suspend until program/erase restart		–	–	3+CPU clock × 4 cycles	µs
–	Program, erase voltage		2.7	–	5.5	V
–	Read voltage		2.7	–	5.5	V
–	Program, erase temperature		0	–	60	°C
–	Data hold time(8)	Ambient temperature = 55 °C	20	–	–	year

NOTES:
1. V_{CC} = 2.7 to 5.5 V at T_{opr} = 0 to 60 °C, unless otherwise specified.
2. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 100 or 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one. However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
4. If emergency processing is required, a suspend request can be generated independent of this characteristic. In that case the normal time delay to Suspend can be applied to the request.However, we recommend that a suspend request with an interval of less than 650 µs is only used once because, if the suspend state continues, erasure cannot operate and the incidence of erasure error rises.
5. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. In addition, averaging the number of erase operations between block A and block B can further reduce the effective number of rewrites. It is also advisable to retain data on the erase count of each block and limit the number of erase operations to a certain number.
6. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
7. Customers desiring programming/erasure failure rate information should contact their Renesas technical support representative.
8. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 5.8 Reset Circuit Electrical Characteristics (When Using Voltage Monitor 1 Reset)

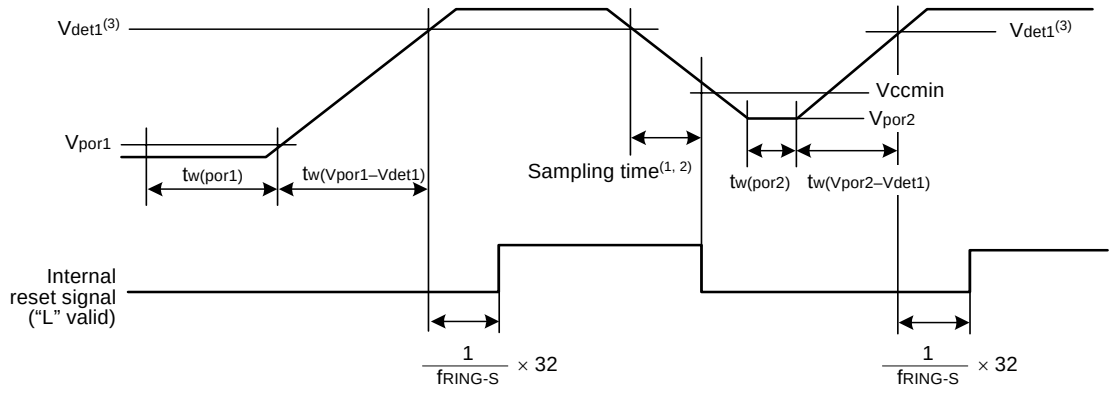
Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{por2}	Power-on reset valid voltage	-20°C ≤ Topr ≤ 85°C	–	–	V_{det1}	V
$t_{w(Vpor2-Vdet1)}$	Supply voltage rising time when power-on reset is deasserted(1)	-20°C ≤ Topr ≤ 85°C, $t_{w(por2)}$ ≥ 0s(3)	–	–	100	ms

NOTES:
1. This condition is not applicable when using with Vcc ≥ 1.0 V.
2. When turning power on after the time to hold the external power below effective voltage (V_{por1}) exceeds10 s, refer to **Table 5.9 Reset Circuit Electrical Characteristics (When Not Using Voltage Monitor 1 Reset)**.
3. $t_{w(por2)}$ is the time to hold the external power below effective voltage (V_{por2}).

Table 5.9 Reset Circuit Electrical Characteristics (When Not Using Voltage Monitor 1 Reset)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{por1}	Power-on reset valid voltage	-20°C ≤ Topr ≤ 85°C	–	–	0.1	V
$t_{w(Vpor1-Vdet1)}$	Supply voltage rising time when power-on reset is deasserted	0°C ≤ Topr ≤ 85°C, $t_{w(por1)}$ ≥ 10 s(2)	–	–	100	ms
$t_{w(Vpor1-Vdet1)}$	Supply voltage rising time when power-on reset is deasserted	-20°C ≤ Topr < 0°C, $t_{w(por1)}$ ≥ 30 s(2)	–	–	100	ms
$t_{w(Vpor1-Vdet1)}$	Supply voltage rising time when power-on reset is deasserted	-20°C ≤ Topr < 0°C, $t_{w(por1)}$ ≥ 10 s(2)	–	–	1	ms
$t_{w(Vpor1-Vdet1)}$	Supply voltage rising time when power-on reset is deasserted	0°C ≤ Topr ≤ 85°C, $t_{w(por1)}$ ≥ 1 s(2)	–	–	0.5	ms

NOTES:
1. When not using voltage monitor 1, use with Vcc ≥ 2.7 V.
2. $t_{w(por1)}$ is the time to hold the external power below effective voltage (V_{por1}).



NOTES:
1. Hold the voltage inside the MCU operation voltage range (Vccmin or above) within the sampling time.
2. The sampling clock can be selected. Refer to **7. Voltage Detection Circuit** for details.
3. V_{det1} indicates the voltage detection level of the voltage detection 1 circuit. Refer to **7. Voltage Detection Circuit** for details.

Figure 5.3 Reset Circuit Electrical Characteristics

Table 5.12 Electrical Characteristics (1) [Vcc = 5 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
VOH	Output “H” voltage	Except XOUT	IOH = -5 mA		Vcc – 2.0	–	Vcc	V
			IOH = -200 µA		Vcc – 0.3	–	Vcc	V
		XOUT	Drive capacity HIGH	IOH = -1 mA	Vcc – 2.0	–	Vcc	V
			Drive capacity LOW	IOH = -500 µA	Vcc – 2.0	–	Vcc	V
VOL	Output “L” voltage	Except P1_0 to P1_3, XOUT	IOL = 5 mA		–	–	2.0	V
			IOL = 200 µA		–	–	0.45	V
		P1_0 to P1_3	Drive capacity HIGH	IOL = 15 mA	–	–	2.0	V
			Drive capacity LOW	IOL = 5 mA	–	–	2.0	V
			Drive capacity LOW	IOL = 200 µA	–	–	0.45	V
		XOUT	Drive capacity HIGH	IOL = 1 mA	–	–	2.0	V
			Drive capacity LOW	IOL = 500 µA	–	–	2.0	V
VT+-VT-	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, CNTR0, CNTR1, TCIN, RXD0			0.2	–	1.0	V
		$\overline{RESET}$			0.2	–	2.2	V
IIH	Input “H” current		VI = 5 V		–	–	5.0	µA
IIL	Input “L” current		VI = 0 V		–	–	-5.0	µA
RPULLUP	Pull-up resistance		VI = 0 V		30	50	167	kΩ
RfXIN	Feedback resistance	XIN			–	1.0	–	MΩ
fRING-S	Low-speed on-chip oscillator frequency				40	125	250	kHz
VRAM	RAM hold voltage		During stop mode		2.0	–	–	V

NOTE:
1. Vcc = 4.2 to 5.5 V at Topr = -20 to 85 °C / -40 to 85 °C, f(XIN) = 20 MHz, unless otherwise specified.

Table 5.19 Electrical Characteristics (3) [Vcc = 3V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output “H” voltage	Except X_{OUT}	I_{OH} = -1 mA		V_{CC} – 0.5	–	V_{CC}	V
		X_{OUT}	Drive capacity HIGH	I_{OH} = -0.1 mA	V_{CC} – 0.5	–	V_{CC}	V
			Drive capacity LOW	I_{OH} = -50 µA	V_{CC} – 0.5	–	V_{CC}	V
V_{OL}	Output “L” voltage	Except P1_0 to P1_3, X_{OUT}	I_{OL} = 1mA		–	–	0.5	V
		P1_0 to P1_3	Drive capacity HIGH	I_{OL} = 2 mA	–	–	0.5	V
			Drive capacity LOW	I_{OL} = 1 mA	–	–	0.5	V
		X_{OUT}	Drive capacity HIGH	I_{OL} = 0.1 mA	–	–	0.5	V
			Drive capacity LOW	I_{OL} = 50 µA	–	–	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, CNTR0, CNTR1, TCIN, RXD0			0.2	–	0.8	V
		$\overline{RESET}$			0.2	–	1.8	V
I_{IH}	Input “H” current		VI = 3 V		–	–	4.0	µA
I_{IL}	Input “L” current		VI = 0 V		–	–	-4.0	µA
R_{PULLUP}	Pull-up resistance		VI = 0 V		66	160	500	kΩ
R_{fXIN}	Feedback resistance	XIN			–	3.0	–	MΩ
f_{RING-S}	Low-speed on-chip oscillator frequency				40	125	250	kHz
V_{RAM}	RAM hold voltage		During stop mode		2.0	–	–	V

NOTE:
1. V_{CC} = 2.7 to 3.3 V at T_{opr} = -20 to 85 °C / -40 to 85 °C, f(XIN) = 10 MHz, unless otherwise specified.

Table 5.24 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	300	–	ns
$t_{W(CKH)}$	CLKi input “H” width	150	–	ns
$t_{W(CKL)}$	CLKi input “L” width	150	–	ns
$t_{d(C-Q)}$	TXDi output delay time	–	80	ns
$t_{h(C-Q)}$	TXDi hold time	0	–	ns
$t_{su(D-C)}$	RXDi input setup time	70	–	ns
$t_{h(C-D)}$	RXDi input hold time	90	–	ns

i = 0 or 1

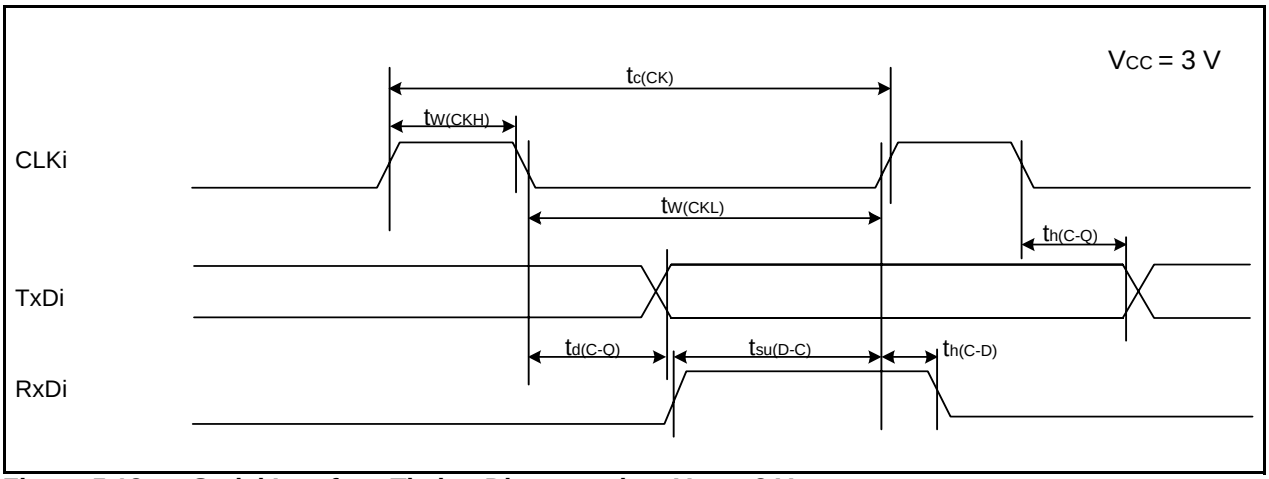


Figure 5.12 Serial Interface Timing Diagram when Vcc = 3 V

Table 5.25 External Interrupt $\overline{INT0}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INT0}$ input “H” width	380(1)	–	ns
$t_{W(INL)}$	$\overline{INT0}$ input “L” width	380(2)	–	ns

NOTES:
1. When selecting the digital filter by the $\overline{INT0}$ input filter select bit, use an $\overline{INT0}$ input HIGH width of either (1/digital filter clock frequency x 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INT0}$ input filter select bit, use an $\overline{INT0}$ input LOW width of either (1/digital filter clock frequency x 3) or the minimum value of standard, whichever is greater.

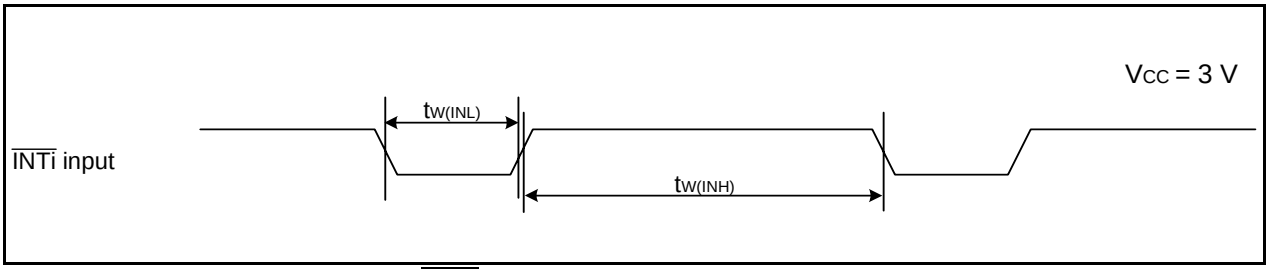


Figure 5.13 External Interrupt $\overline{INT0}$ Input Timing Diagram when Vcc = 3 V

REVISION HISTORY	R8C/18 Group, R8C/19 Group Datasheet

Rev.	Date	Description	
		Page	Summary
1.20	Nov 01, 2005	16	Table 4.1 SFR Information(1); 0009h: "XXXXXX00b" → "00h" 000Ah: "00XXX000b" → "00h" 001Eh: "XXXXX000b" → "00h" revised
		18	Table 4.3 SFR Information(3); 0085h: "Prescaler Z" → "Prescaler Z Register" 0086h: "Timer Z Secondary" → "Timer Z Secondary Register" 0087h: "Timer Z Primary" → "Timer Z Primary Register" 008Ch: "Prescaler X" → "Prescaler X Register" 008Dh: "Timer X" → "Timer X Register" 0090h, 0091h: "Timer C" → "Timer C Register" revised
		22	Table 5.4 Flash Memory (Program ROM) Electrical Characteristics; NOTES 3 and 5 revised, NOTE8 deleted
		23	Table 5.5 Flash Memory (Data flash Block A, Block B) Electrical Characteristics; NOTES 1 and 3 revised
		25	Table 5.8 Reset Circuit Electrical Characteristics (When Using Voltage Monitor 1 Reset); NOTE 2 revised
		26	Table 5.10 High-speed On-Chip Oscillator Circuit Electrical Characteristics; "High-Speed On-Chip Oscillator ..." → "High-Speed On-Chip Oscillator Frequency ..." revised NOTE 2, 3 added
		28	Table 5.13 Electrical Characteristics (2) [Vcc = 5V]; NOTE 1 deleted
		32	Table 5.20 Electrical Characteristics (4) [Vcc = 3V]; NOTE 1 deleted
1.30	Dec 16, 2005	–	Products of PWQN0028KA-B package included
		5, 6	Table 1.3, Table 1.4 revised
		24	Table 5.4 Flash Memory (Program ROM) Electrical Characteristics; Ta → Ambient temperature
		25	Table 5.5 Flash Memory (Data flash Block A, Block B) Electrical Characteristics; Ta → Ambient temperature
		30, 34	Table 5.13, Table 5.20; The title revised, Condition of Stop Mode added
		32, 36	Table 5.17, Table 5.24; td(C-Q) and tsu(D-C) revised
		37, 38	Package Dimensions revised
1.40	Apr 14, 2006	2, 3	Table 1.1, Table 1.2; Interrupts: Internal 8 → 10 sources,
		5, 6	Table 1.3, Table 1.4; Type No. added, deleted
		16, 17	Figure 3.1, Figure 3.2; Part Number added, deleted
		24, 25	Table 5.4, Table 5.5; Conditions: VCC = 5.0 V at Topr = 25 °C deleted