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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	SIO, UART/USART
Peripherals	LED, POR, Voltage Detect, WDT
Number of I/O	13
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-WFQFN Exposed Pad
Supplier Device Package	28-HWQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21194np-u0

1. Overview

These MCUs are fabricated using a high-performance silicon gate CMOS process, embedding the R8C/Tiny Series CPU core, and is packaged in a 20-pin molded-plastic LSSOP, SDIP or a 28-pin plastic molded-HWQFN. It implements sophisticated instructions for a high level of instruction efficiency. With 1 Mbyte of address space, they are capable of executing instructions at high speed.
Furthermore, the R8C/19 Group has on-chip data flash ROM (1 KB × 2 blocks).
The difference between the R8C/18 Group and R8C/19 Group is only the presence or absence of data flash ROM. Their peripheral functions are the same.

1.1 Applications

Electric household appliances, office equipment, housing equipment (sensors, security systems), general industrial equipment, audio equipment, etc.

1.2 Performance Overview

Table 1.1 outlines the Functions and Specifications for R8C/18 Group and Table 1.2 outlines the Functions and Specifications for R8C/19 Group.

Table 1.1 Functions and Specifications for R8C/18 Group

Item		Specification
CPU	Number of fundamental instructions	89 instructions
	Minimum instruction execution time	50 ns (f(XIN) = 20 MHz, VCC = 3.0 to 5.5 V) 100 ns (f(XIN) = 10 MHz, VCC = 2.7 to 5.5 V)
	Operation mode	Single-chip
	Address space	1 Mbyte
	Memory capacity	Refer to **Table 1.3 Product Information for R8C/18 Group**
Peripheral Functions	Ports	I/O ports: 13 pins (including LED drive port) Input port: 3 pins
	LED drive ports	I/O ports: 4 pins
	Timers	Timer X: 8 bits × 1 channel, timer Z: 8 bits × 1 channel (Each timer equipped with 8-bit prescaler) Timer C: 16 bits × 1 channel (Input capture and output compare circuits)
	Serial interfaces	1 channel Clock synchronous serial I/O, UART 1 channel UART
	Comparator	1-bit comparator: 1 circuit, 4 channels
	Watchdog timer	15 bits × 1 channel (with prescaler) Reset start selectable, count source protection mode
	Interrupts	Internal: 10 sources, External: 4 sources, Software: 4 sources, Priority levels: 7 levels
	Clock generation circuits	2 circuits • Main clock oscillation circuit (with on-chip feedback resistor) • On-chip oscillator (high speed, low speed) High-speed on-chip oscillator has frequency adjustment function
	Oscillation stop detection function	Main clock oscillation stop detection function
	Voltage detection circuit	On-chip
	Power-on reset circuit	On-chip
Electric Characteristics	Supply voltage	VCC = 3.0 to 5.5 V (f(XIN) = 20 MHz) VCC = 2.7 to 5.5 V (f(XIN) = 10 MHz)
	Current consumption	Typ. 9 mA (VCC = 5.0 V, f(XIN) = 20 MHz, comparator stopped) Typ. 5 mA (VCC = 3.0V, f(XIN) = 10 MHz, comparator stopped) Typ. 35 μA (VCC = 3.0 V, wait mode, peripheral clock off) Typ. 0.7 μA (VCC = 3.0 V, stop mode)
Flash Memory	Programming and erasure voltage	VCC = 2.7 to 5.5 V
	Programming and erasure endurance	100 times
Operating Ambient Temperature		-20 to 85°C -40 to 85°C (D version)
Package		20-pin molded-plastic LSSOP
		20-pin molded-plastic SDIP
		28-pin molded-plastic HWQFN

1.3 Block Diagram

Figure 1.1 shows a Block Diagram.

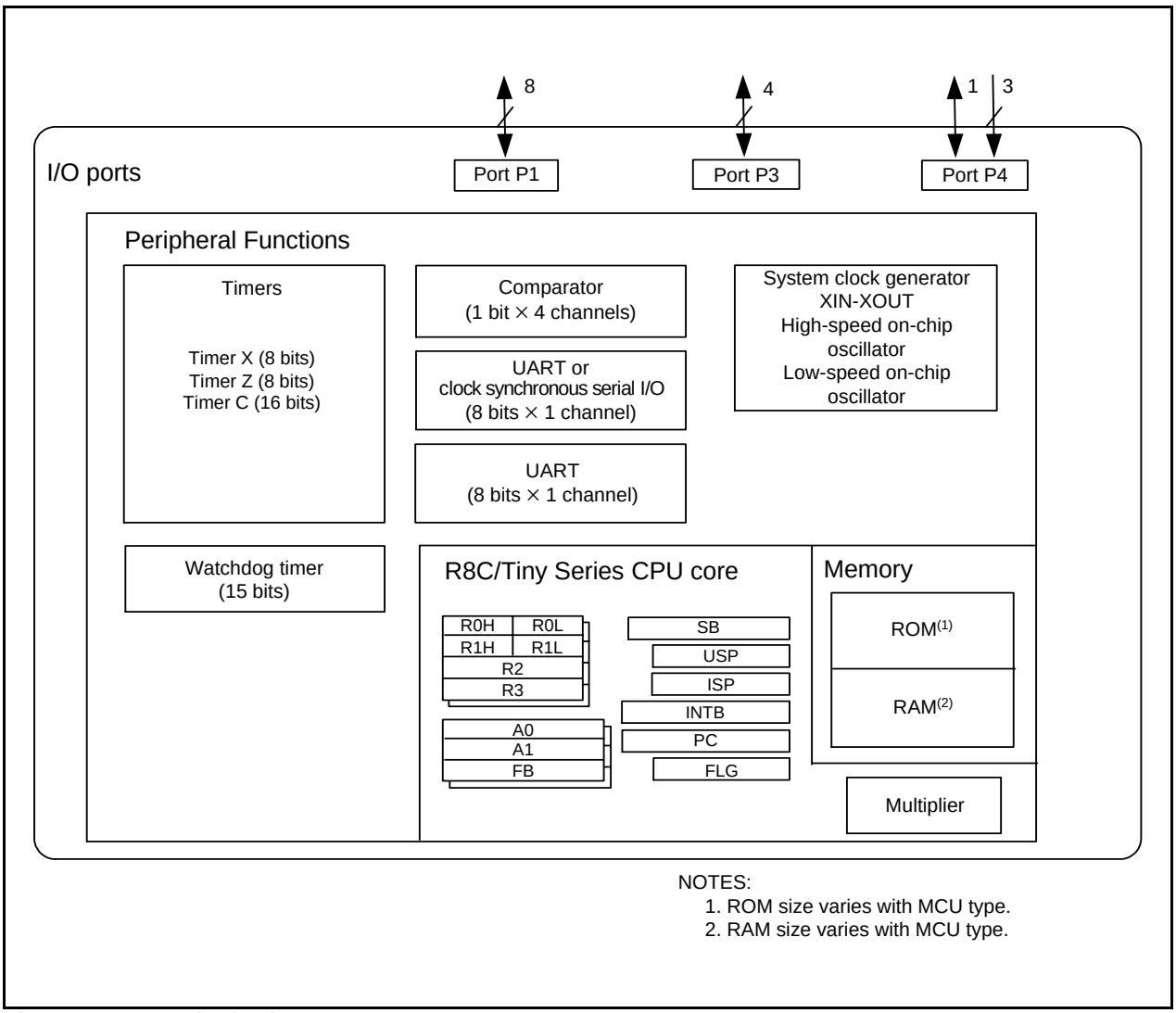


Figure 1.1 Block Diagram

1.4 Product Information

Table 1.3 lists Product Information for R8C/18 Group and Table 1.4 lists Product Information for R8C/19 Group.

Table 1.3 Product Information for R8C/18 Group **Current of Apr. 2006**

Type No.	ROM Capacity	RAM Capacity	Package Type	Remarks
R5F21181SP	4 Kbytes	384 bytes	PLSP0020JB-A	Flash memory version
R5F21182SP	8 Kbytes	512 bytes	PLSP0020JB-A	
R5F21183SP	12 Kbytes	768 bytes	PLSP0020JB-A	
R5F21184SP	16 Kbytes	1 Kbyte	PLSP0020JB-A	
R5F21181DSP (D)	4 Kbytes	384 bytes	PLSP0020JB-A	D version
R5F21182DSP (D)	8 Kbytes	512 bytes	PLSP0020JB-A	
R5F21183DSP (D)	12 Kbytes	768 bytes	PLSP0020JB-A	
R5F21184DSP (D)	16 Kbytes	1 Kbyte	PLSP0020JB-A	
R5F21181DD	4 Kbytes	384 bytes	PRDP0020BA-A	Flash memory version
R5F21182DD	8 Kbytes	512 bytes	PRDP0020BA-A	
R5F21183DD	12 Kbytes	768 bytes	PRDP0020BA-A	
R5F21184DD	16 Kbytes	1 Kbyte	PRDP0020BA-A	
R5F21182NP	8 Kbytes	512 bytes	PWQN0028KA-B	Flash memory version
R5F21183NP	12 Kbytes	768 bytes	PWQN0028KA-B	
R5F21184NP	16 Kbytes	1 Kbyte	PWQN0028KA-B	

(D): Under Development

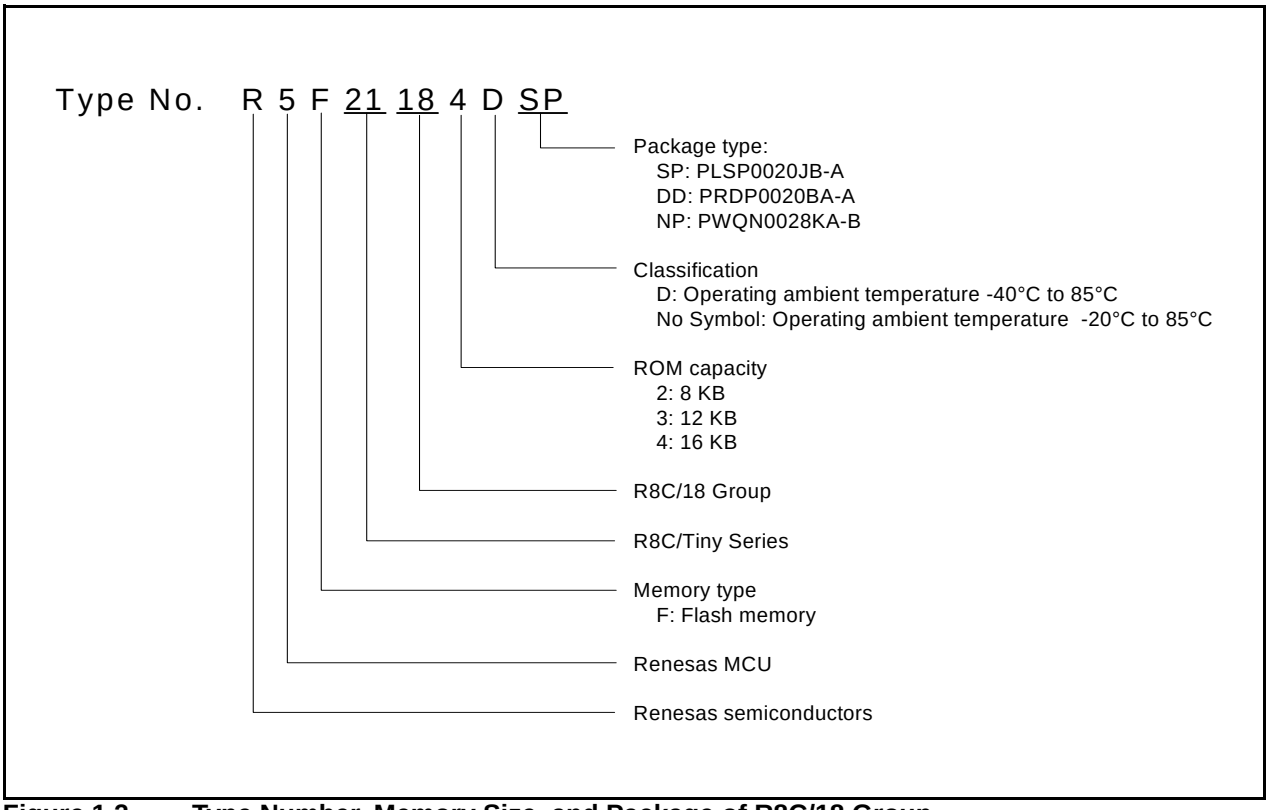


Figure 1.2 Type Number, Memory Size, and Package of R8C/18 Group

Table 1.4 Product Information for R8C/19 Group Current of Apr. 2006

Type No.	ROM Capacity		RAM Capacity	Package Type	Remarks
	Program ROM	Data flash			
R5F21191SP	4 Kbytes	1 Kbyte × 2	384 bytes	PLSP0020JB-A	Flash memory version
R5F21192SP	8 Kbytes	1 Kbyte × 2	512 bytes	PLSP0020JB-A	
R5F21193SP	12 Kbytes	1 Kbyte × 2	768 bytes	PLSP0020JB-A	
R5F21194SP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLSP0020JB-A	
R5F21191DSP (D)	4 Kbytes	1 Kbyte × 2	384 bytes	PLSP0020JB-A	D version
R5F21192DSP (D)	8 Kbytes	1 Kbyte × 2	512 bytes	PLSP0020JB-A	
R5F21193DSP (D)	12 Kbytes	1 Kbyte × 2	768 bytes	PLSP0020JB-A	
R5F21194DSP (D)	16 Kbytes	1 Kbyte × 2	1 Kbyte	PLSP0020JB-A	
R5F21191DD	4 Kbytes	1 Kbyte × 2	384 bytes	PRDP0020BA-A	Flash memory version
R5F21192DD	8 Kbytes	1 Kbyte × 2	512 bytes	PRDP0020BA-A	
R5F21193DD	12 Kbytes	1 Kbyte × 2	768 bytes	PRDP0020BA-A	
R5F21194DD	16 Kbytes	1 Kbyte × 2	1 Kbyte	PRDP0020BA-A	
R5F21192NP	8 Kbytes	1 Kbyte × 2	512 bytes	PWQN0028KA-B	Flash memory version
R5F21193NP	12 Kbytes	1 Kbyte × 2	768 bytes	PWQN0028KA-B	
R5F21194NP	16 Kbytes	1 Kbyte × 2	1 Kbyte	PWQN0028KA-B	

(D): Under Development

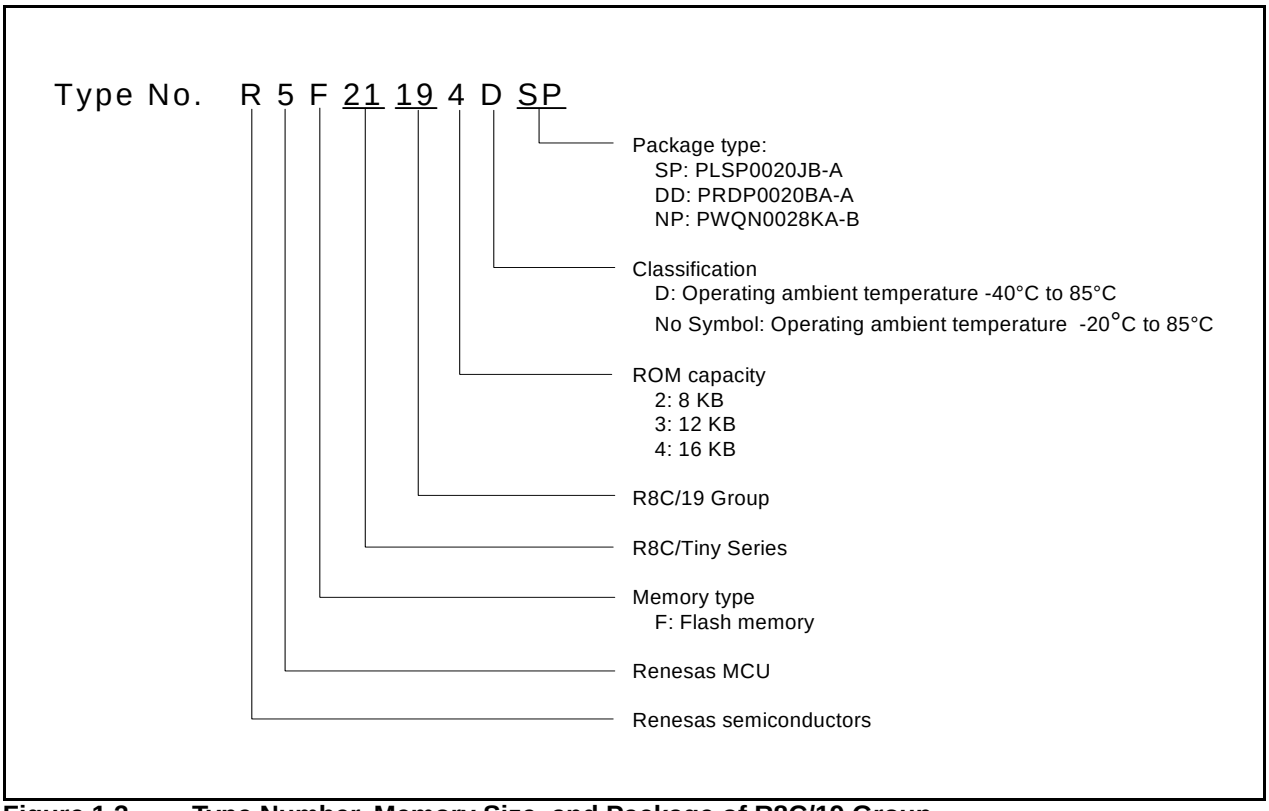
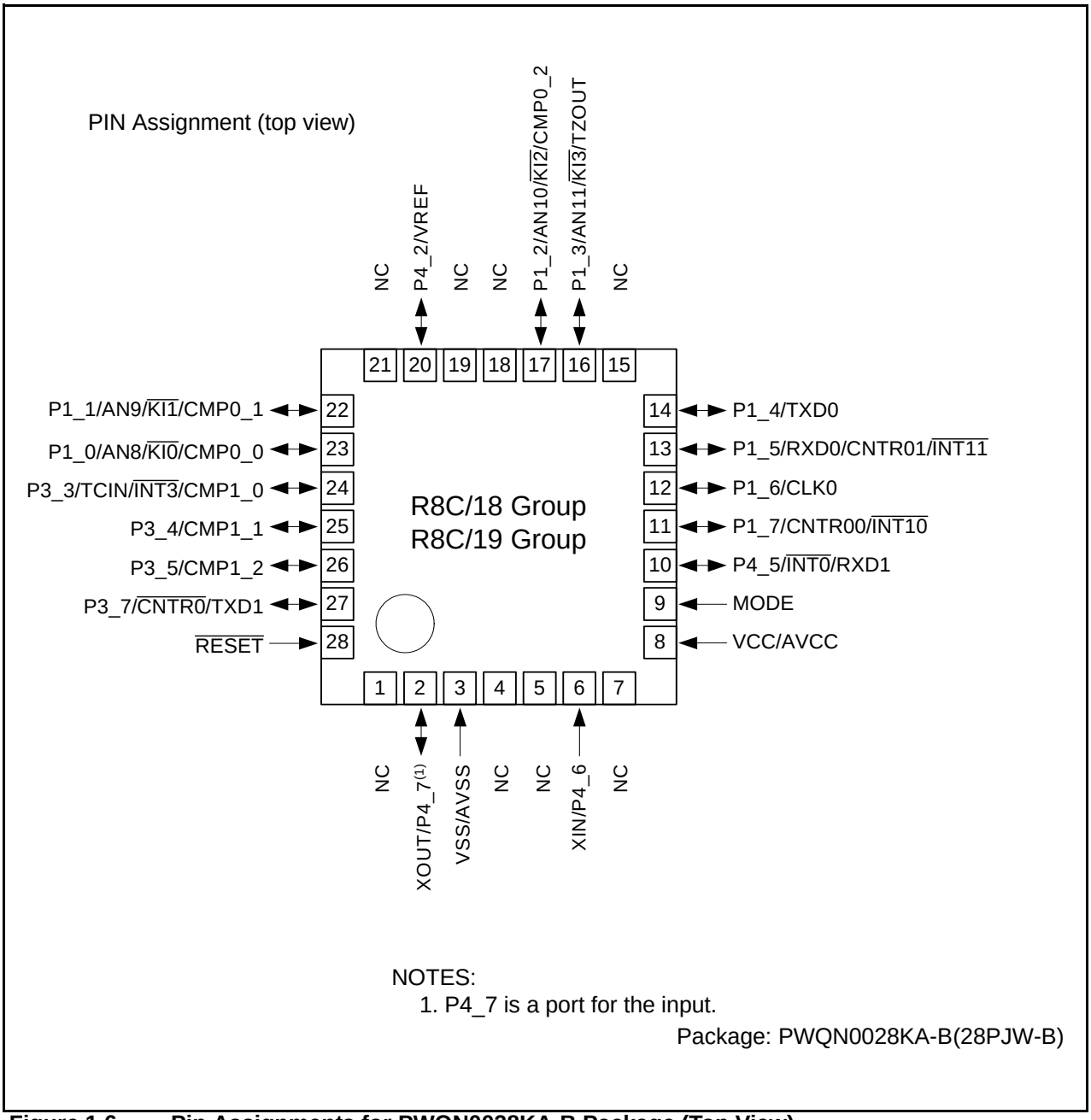


Figure 1.3 Type Number, Memory Size, and Package of R8C/19 Group



NOTES:
1. P4_7 is a port for the input.

Package: PWQN0028KA-B(28PJW-B)

Figure 1.6 Pin Assignments for PWQN0028KA-B Package (Top View)

1.6 Pin Functions

Table 1.5 lists Pin Functions, Table 1.6 lists Pin Name Information by Pin Number of PLSP0020JB-A, PRDP0020BA-A packages, and Table 1.7 lists Pin Name Information by Pin Number of PWQN0028KA-B package.

Table 1.5 Pin Functions

Type	Symbol	I/O Type	Description
Power supply input	VCC VSS	I	Apply 2.7 V to 5.5 V to the VCC pin. Apply 0 V to the VSS pin.
Analog power supply input	AVCC, AVSS	I	Power supply for the comparator Connect a capacitor between AVCC and AVSS.
Reset input	$\overline{\text{RESET}}$	I	Input “L” on this pin resets the MCU.
MODE	MODE	I	Connect this pin to VCC via a resistor.
Main clock input	XIN	I	These pins are provided for main clock generation circuit I/O. Connect a ceramic resonator or a crystal oscillator between the XIN and XOUT pins. To use an external clock, input it to the XIN pin and leave the XOUT pin open.
Main clock output	XOUT	O	
$\overline{\text{INT}}$ interrupt	$\overline{\text{INT0}}$, $\overline{\text{INT1}}$, $\overline{\text{INT3}}$	I	$\overline{\text{INT}}$ interrupt input pins
Key input interrupt	$\overline{\text{KI0}}$ to $\overline{\text{KI3}}$	I	Key input interrupt input pins
Timer X	CNTR0	I/O	Timer X I/O pin
	$\overline{\text{CNTR0}}$	O	Timer X output pin
Timer Z	TZOUT	O	Timer Z output pin
Timer C	TCIN	I	Timer C input pin
	CMP0_0 to CMP0_2, CMP1_0 to CMP1_2	O	Timer C output pins
Serial interface	CLK0	I/O	Transfer clock I/O pin
	RXD0, RXD1	I	Serial data input pins
	TXD0, TXD1	O	Serial data output pins
Reference voltage input	VREF	I	Reference voltage input pin to comparator
Comparator	AN8 to AN11	I	Analog input pins to comparator
I/O port	P1_0 to P1_7, P3_3 to P3_5, P3_7, P4_5	I/O	CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually. Any port set to input can be set to use a pull-up resistor or not by a program. P1_0 to P1_3 also function as LED drive ports.
Input port	P4_2, P4_6, P4_7	I	Input-only ports

I: Input O: Output I/O: Input and output

Table 1.6 Pin Name Information by Pin Number of PLSP0020JB-A, PRDP0020BA-A packages

Pin Number	Control Pin	Port	I/O Pin Functions for Peripheral Modules			
			Interrupt	Timer	Serial Interface	Comparator
1		P3_5		CMP1_2		
2		P3_7		$\overline{\text{CNTR0}}$	TXD1	
3	$\overline{\text{RESET}}$					
4	XOUT	P4_7				
5	VSS/AVSS					
6	XIN	P4_6				
7	VCC/AVCC					
8	MODE					
9		P4_5	$\overline{\text{INT0}}$		RXD1	
10		P1_7	$\overline{\text{INT10}}$	CNTR00		
11		P1_6			CLK0	
12		P1_5	$\overline{\text{INT11}}$	CNTR01	RXD0	
13		P1_4			TXD0	
14		P1_3	$\overline{\text{KI3}}$	TZOUT		AN11
15		P1_2	$\overline{\text{KI2}}$	CMP0_2		AN10
16	VREF	P4_2				
17		P1_1	$\overline{\text{KI1}}$	CMP0_1		AN9
18		P1_0	$\overline{\text{KI0}}$	CMP0_0		AN8
19		P3_3	$\overline{\text{INT3}}$	TCIN/CMP1_0		
20		P3_4		CMP1_1		

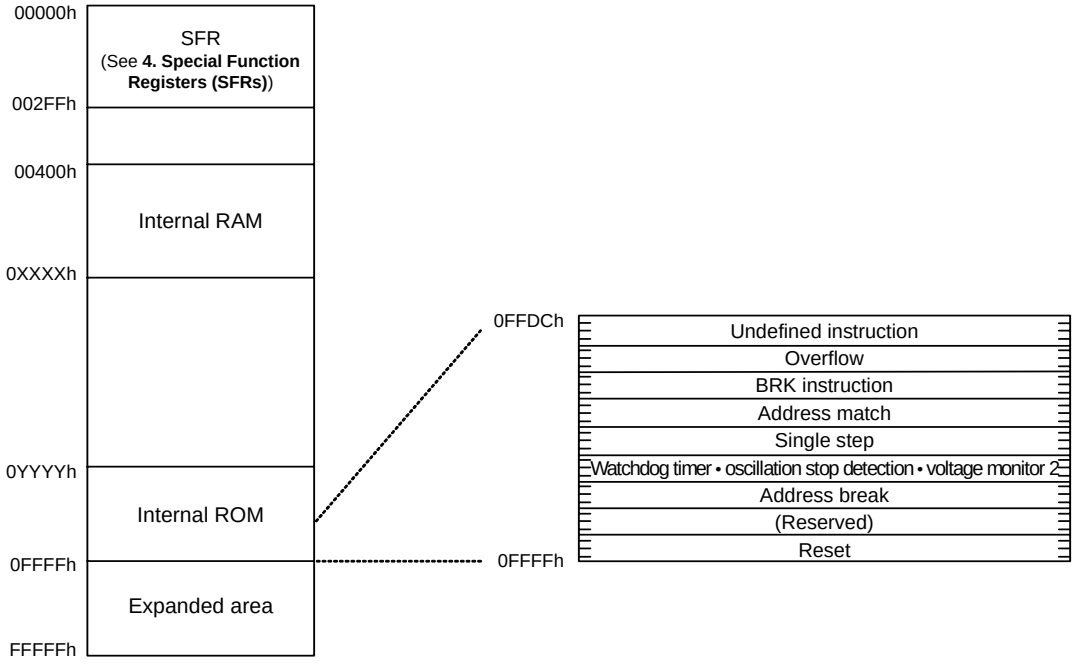
Table 1.7 Pin Name Information by Pin Number of PWQN0028KA-B package

Pin Number	Control Pin	Port	I/O Pin of Peripheral Function			
			Interrupt	Timer	Serial Interface	Comparator
1	NC					
2	XOUT	P4_7				
3	VSS/AVSS					
4	NC					
5	NC					
6	XIN	P4_6				
7	NC					
8	VCC/AVCC					
9	MODE					
10		P4_5	$\overline{\text{INT0}}$		RXD1	
11		P1_7	$\overline{\text{INT10}}$	CNTR00		
12		P1_6			CLK0	
13		P1_5	$\overline{\text{INT11}}$	CNTR01	RXD0	
14		P1_4			TXD0	
15	NC					
16		P1_3	$\overline{\text{KI3}}$	TZOUT		AN11
17		P1_2	$\overline{\text{KI2}}$	CMP0_2		AN10
18	NC					
19	NC					
20	VREF	P4_2				
21	NC					
22		P1_1	$\overline{\text{KI1}}$	CMP0_1		AN9
23		P1_0	$\overline{\text{KI0}}$	CMP0_0		AN8
24		P3_3	$\overline{\text{INT3}}$	TCIN/CMP1_0		
25		P3_4		CMP1_1		
26		P3_5		CMP1_2		
27		P3_7		$\overline{\text{CNTR0}}$	TXD1	
28	$\overline{\text{RESET}}$					

3. Memory

3.1 R8C/18 Group

Figure 3.1 is a Memory Map of R8C/18 Group. The R8C/18 Group has 1 Mbyte of address space from addresses 00000h to FFFFFh.
The internal ROM area is allocated lower addresses, beginning with address 0FFFFh. For example, a 16-Kbyte internal ROM is allocated addresses 0C000h to 0FFFFh.
The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. They store the starting address of each interrupt routine.
The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 1-Kbyte internal RAM area is allocated addresses 00400h to 007FFh. The internal RAM is used not only for storing data but also for calling subroutines and as stacks when interrupt requests are acknowledged.
Special function registers (SFRs) are allocated addresses 00000h to 002FFh. The peripheral function control registers are allocated here. All addresses within the SFR, which have nothing allocated are reserved for future use and cannot be accessed by users.



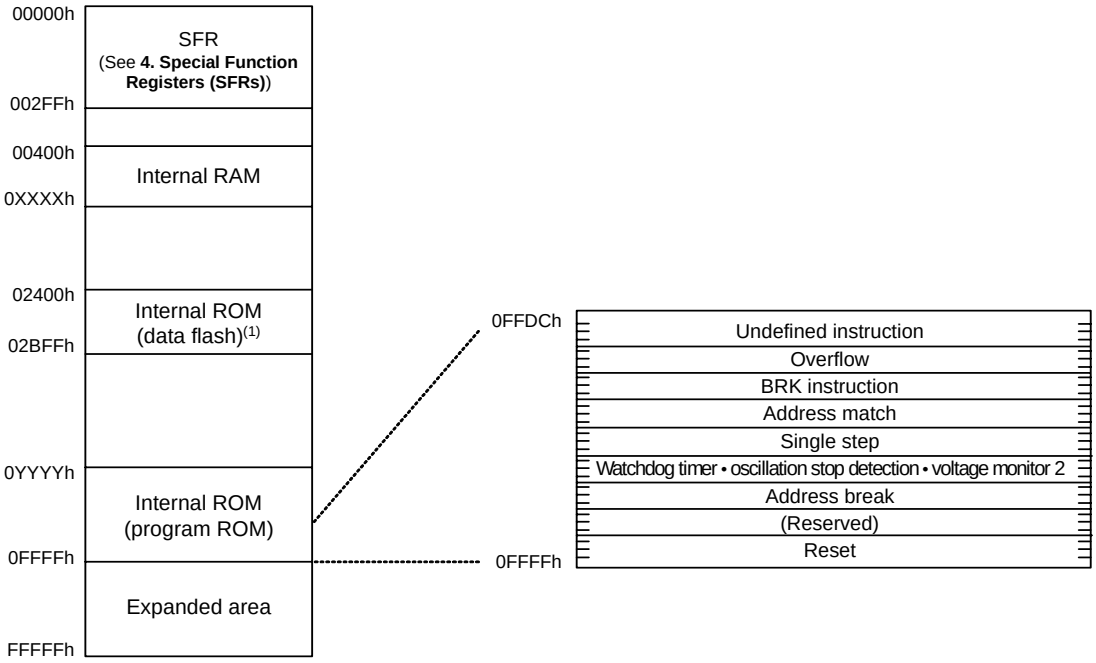
NOTE:
1. The blank regions are reserved. Do not access locations in these regions.

Part Number	Internal ROM		Internal RAM	
	Size	Address 0YYYYh	Size	Address 0XXXXh
R5F21184SP, R5F21184DSP, R5F21184DD, R5F21184NP	16 Kbytes	0C000h	1 Kbyte	007FFh
R5F21183SP, R5F21183DSP, R5F21183DD, R5F21183NP	12 Kbytes	0D000h	768 bytes	006FFh
R5F21182SP, R5F21182DSP, R5F21182DD, R5F21182NP	8 Kbytes	0E000h	512 bytes	005FFh
R5F21181SP, R5F21181DSP, R5F21181DD	4 Kbytes	0F000h	384 bytes	0057Fh

Figure 3.1 Memory Map of R8C/18 Group

3.2 R8C/19 Group

Figure 3.2 is a Memory Map of R8C/19 Group. The R8C/19 group has 1 Mbyte of address space from addresses 00000h to FFFFFh.
The internal ROM (program ROM) is allocated lower addresses, beginning with address 0FFFFh. For example, a 16-Kbyte internal ROM area is allocated addresses 0C000h to 0FFFFh.
The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. They store the starting address of each interrupt routine.
The internal ROM (data flash) is allocated addresses 02400h to 02BFFh.
The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 1-Kbyte internal RAM area is allocated addresses 00400h to 007FFh. The internal RAM is used not only for storing data but also for calling subroutines and as stacks when interrupt requests are acknowledged.
Special function registers (SFRs) are allocated addresses 00000h to 002FFh. The peripheral function control registers are allocated here. All addresses within the SFR, which have nothing allocated are reserved for future use and cannot be accessed by users.



NOTES:
1. Data flash block A (1 Kbyte) and B (1 Kbyte) are shown.
2. The blank regions are reserved. Do not access locations in these regions.

Part Number	Internal ROM		Internal RAM	
	Size	Address 0YYYYh	Size	Address 0XXXXh
R5F21194SP, R5F21194DSP, R5F21194DD, R5F21194NP	16 Kbytes	0C000h	1 Kbyte	007FFh
R5F21193SP, R5F21193DSP, R5F21193DD, R5F21193NP	12 Kbytes	0D000h	768 bytes	006FFh
R5F21192SP, R5F21192DSP, R5F21192DD, R5F21192NP	8 Kbytes	0E000h	512 bytes	005FFh
R5F21191SP, R5F21191DSP, R5F21191DD	4 Kbytes	0F000h	384 bytes	0057Fh

Figure 3.2 Memory Map of R8C/19 Group

5. Electrical Characteristics

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter	Condition	Rated Value	Unit
V_{CC}	Supply voltage	V_{CC} = AV_{CC}	-0.3 to 6.5	V
AV_{CC}	Analog supply voltage	V_{CC} = AV_{CC}	-0.3 to 6.5	V
V_I	Input voltage		-0.3 to V_{CC}+0.3	V
V_O	Output voltage		-0.3 to V_{CC}+0.3	V
P_d	Power dissipation	T_{opr} = 25°C	300	mW
T_{opr}	Operating ambient temperature		-20 to 85 / -40 to 85 (D version)	°C
T_{stg}	Storage temperature		-65 to 150	°C

Table 5.2 Recommended Operating Conditions

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
V_{CC}	Supply voltage			2.7	–	5.5	V
AV_{CC}	Analog supply voltage			–	V_{CC}	–	V
V_{SS}	Supply voltage			–	0	–	V
AV_{SS}	Analog supply voltage			–	0	–	V
V_{IH}	Input “H” voltage			0.8V_{CC}	–	V_{CC}	V
V_{IL}	Input “L” voltage			0	–	0.2V_{CC}	V
$I_{OH(sum)}$	Peak sum output “H” current	Sum of all pins $I_{OH\ (peak)}$		–	–	-60	mA
$I_{OH(peak)}$	Peak output “H” current			–	–	-10	mA
$I_{OH(avg)}$	Average output “H” current			–	–	-5	mA
$I_{OL(sum)}$	Peak sum output “L” currents	Sum of all pins $I_{OL\ (peak)}$		–	–	60	mA
$I_{OL(peak)}$	Peak output “L” currents	Except P1_0 to P1_3		–	–	10	mA
		P1_0 to P1_3	Drive capacity HIGH	–	–	30	mA
			Drive capacity LOW	–	–	10	mA
$I_{OL(avg)}$	Average output “L” current	Except P1_0 to P1_3		–	–	5	mA
		P1_0 to P1_3	Drive capacity HIGH	–	–	15	mA
			Drive capacity LOW	–	–	5	mA
$f_{(XIN)}$	Main clock input oscillation frequency		3.0 V ≤ V_{CC} ≤ 5.5 V	0	–	20	MHz
			2.7 V ≤ V_{CC} < 3.0 V	0	–	10	MHz

NOTES:
1. V_{CC} = 2.7 to 5.5 V at T_{opr} = -20 to 85 °C / -40 to 85 °C, unless otherwise specified.
2. Typical values when average output current is 100 ms.

Table 5.8 Reset Circuit Electrical Characteristics (When Using Voltage Monitor 1 Reset)

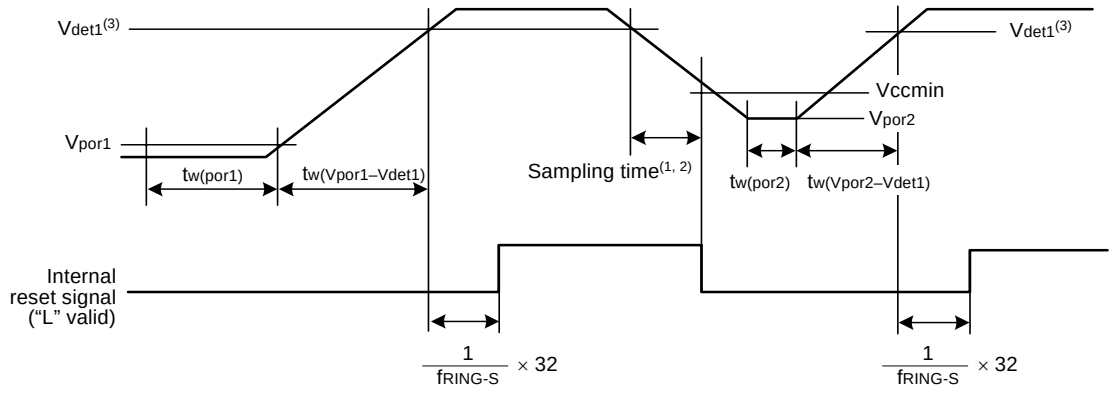
Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{por2}	Power-on reset valid voltage	-20°C ≤ Topr ≤ 85°C	–	–	V_{det1}	V
$t_{w(Vpor2-Vdet1)}$	Supply voltage rising time when power-on reset is deasserted(1)	-20°C ≤ Topr ≤ 85°C, $t_{w(por2)}$ ≥ 0s(3)	–	–	100	ms

NOTES:
1. This condition is not applicable when using with Vcc ≥ 1.0 V.
2. When turning power on after the time to hold the external power below effective voltage (V_{por1}) exceeds10 s, refer to **Table 5.9 Reset Circuit Electrical Characteristics (When Not Using Voltage Monitor 1 Reset)**.
3. $t_{w(por2)}$ is the time to hold the external power below effective voltage (V_{por2}).

Table 5.9 Reset Circuit Electrical Characteristics (When Not Using Voltage Monitor 1 Reset)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{por1}	Power-on reset valid voltage	-20°C ≤ Topr ≤ 85°C	–	–	0.1	V
$t_{w(Vpor1-Vdet1)}$	Supply voltage rising time when power-on reset is deasserted	0°C ≤ Topr ≤ 85°C, $t_{w(por1)}$ ≥ 10 s(2)	–	–	100	ms
$t_{w(Vpor1-Vdet1)}$	Supply voltage rising time when power-on reset is deasserted	-20°C ≤ Topr < 0°C, $t_{w(por1)}$ ≥ 30 s(2)	–	–	100	ms
$t_{w(Vpor1-Vdet1)}$	Supply voltage rising time when power-on reset is deasserted	-20°C ≤ Topr < 0°C, $t_{w(por1)}$ ≥ 10 s(2)	–	–	1	ms
$t_{w(Vpor1-Vdet1)}$	Supply voltage rising time when power-on reset is deasserted	0°C ≤ Topr ≤ 85°C, $t_{w(por1)}$ ≥ 1 s(2)	–	–	0.5	ms

NOTES:
1. When not using voltage monitor 1, use with Vcc ≥ 2.7 V.
2. $t_{w(por1)}$ is the time to hold the external power below effective voltage (V_{por1}).



NOTES:
1. Hold the voltage inside the MCU operation voltage range (Vccmin or above) within the sampling time.
2. The sampling clock can be selected. Refer to **7. Voltage Detection Circuit** for details.
3. V_{det1} indicates the voltage detection level of the voltage detection 1 circuit. Refer to **7. Voltage Detection Circuit** for details.

Figure 5.3 Reset Circuit Electrical Characteristics

Table 5.10 High-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
–	High-speed on-chip oscillator frequency when the reset is deasserted	V_{CC} = 5.0 V, T_{opr} = 25 °C	–	8	–	MHz
–	High-speed on-chip oscillator frequency temperature supply voltage dependence(2)	0 to +60 °C/5 V ± 5 %(3)	7.76	–	8.24	MHz
		-20 to +85 °C/2.7 to 5.5 V(3)	7.68	–	8.32	MHz
		-40 to +85 °C/2.7 to 5.5 V(3)	7.44	–	8.32	MHz

NOTES:
1. The measurement condition is V_{CC} = 5.0 V and T_{opr} = 25 °C.
2. Refer to **10.6.4 High-Speed On-Chip Oscillator Clock** for notes on high-speed on-chip oscillator clock.
3. The standard value shows when the HRA1 register is assumed as the value in shipping and the HRA2 register value is set to 00h.

Table 5.11 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Time for internal power supply stabilization during power-on(2)		1	–	2000	µs
$t_{d(R-S)}$	STOP exit time(3)		–	–	150	µs

NOTES:
1. The measurement condition is V_{CC} = 2.7 to 5.5 V and T_{opr} = 25 °C.
2. Waiting time until the internal power supply generation circuit stabilizes during power-on.
3. Time until CPU clock supply starts after the interrupt is acknowledged to exit stop mode.

Timing Requirements
(Unless Otherwise Specified: Vcc = 5 V, Vss = 0 V at Ta = 25 °C) [Vcc = 5 V]

Table 5.14 XIN Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	50	–	ns
$t_{WH(XIN)}$	XIN input “H” width	25	–	ns
$t_{WL(XIN)}$	XIN input “L” width	25	–	ns

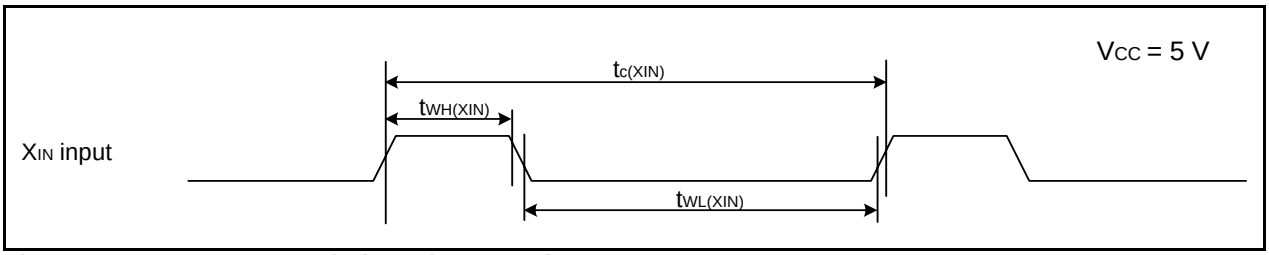


Figure 5.4 XIN Input Timing Diagram when Vcc = 5 V

Table 5.15 CNTR0 Input, CNTR1 Input, $\overline{\text{INT1}}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CNTR0)}$	CNTR0 input cycle time	100	–	ns
$t_{WH(CNTR0)}$	CNTR0 input “H” width	40	–	ns
$t_{WL(CNTR0)}$	CNTR0 input “L” width	40	–	ns

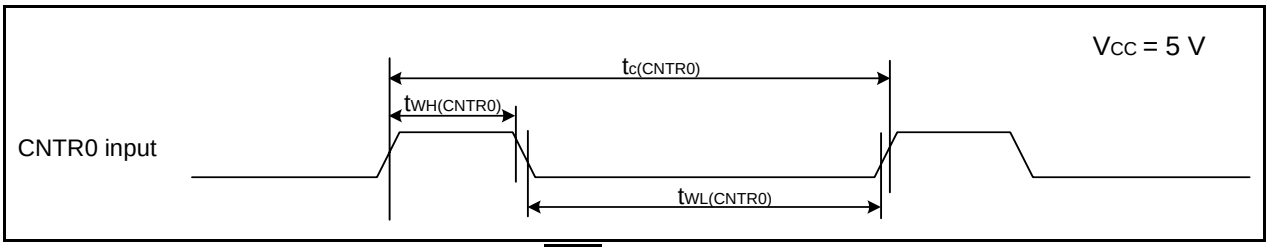


Figure 5.5 CNTR0 Input, CNTR1 Input, $\overline{\text{INT1}}$ Input Timing Diagram when Vcc = 5 V

Table 5.16 TCIN Input, $\overline{\text{INT3}}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TCIN)}$	TCIN input cycle time	400(1)	–	ns
$t_{WH(TCIN)}$	TCIN input “H” width	200(2)	–	ns
$t_{WL(TCIN)}$	TCIN input “L” width	200(2)	–	ns

NOTES:
1. When using timer C input capture mode, adjust the cycle time to (1/timer C count source frequency x 3) or above.
2. When using timer C input capture mode, adjust the pulse width to (1/timer C count source frequency x 1.5) or above.

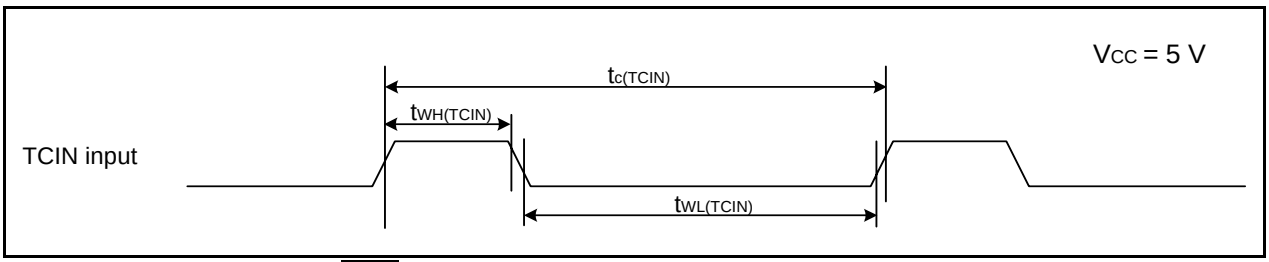


Figure 5.6 TCIN Input, $\overline{\text{INT3}}$ Input Timing Diagram when Vcc = 5 V

Table 5.20 Electrical Characteristics (4) [Vcc = 3V] (Topr = -40 to 85 °C, unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
Icc	Power supply current (Vcc = 2.7 to 3.3 V) Single-chip mode, output pins are open, other pins are Vss, comparator is stopped	High-speed mode	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	8	13	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	7	12	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	5	–	mA
		Medium-speed mode	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	3	–	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	2.5	–	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	1.6	–	mA
		High-speed on-chip oscillator mode	Main clock off High-speed on-chip oscillator on = 8 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	3.5	7.5	mA
			Main clock off High-speed on-chip oscillator on = 8 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	1.5	–	mA
		Low-speed on-chip oscillator mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8 FMR47 = 1	–	100	280	µA
		Wait mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = 0	–	37	74	µA
		Wait mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = 0	–	35	70	µA
		Stop mode	Main clock off, Topr = 25 °C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = 0	–	0.7	3.0	µA

Timing requirements
(Unless Otherwise Specified: Vcc = 3 V, Vss = 0 V at Ta = 25 °C) [Vcc = 3 V]

Table 5.21 XIN Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	100	–	ns
$t_{WH(XIN)}$	XIN input “H” width	40	–	ns
$t_{WL(XIN)}$	XIN input “L” width	40	–	ns

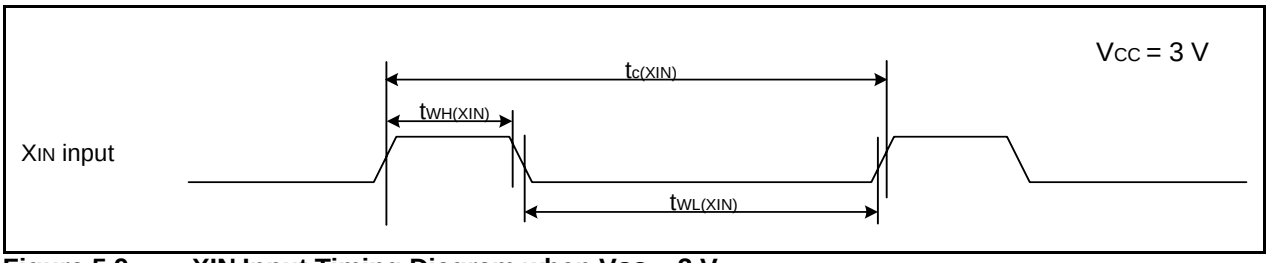


Figure 5.9 XIN Input Timing Diagram when Vcc = 3 V

Table 5.22 CNTR0 Input, CNTR1 Input, $\overline{\text{INT1}}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CNTR0)}$	CNTR0 input cycle time	300	–	ns
$t_{WH(CNTR0)}$	CNTR0 input “H” width	120	–	ns
$t_{WL(CNTR0)}$	CNTR0 input “L” width	120	–	ns

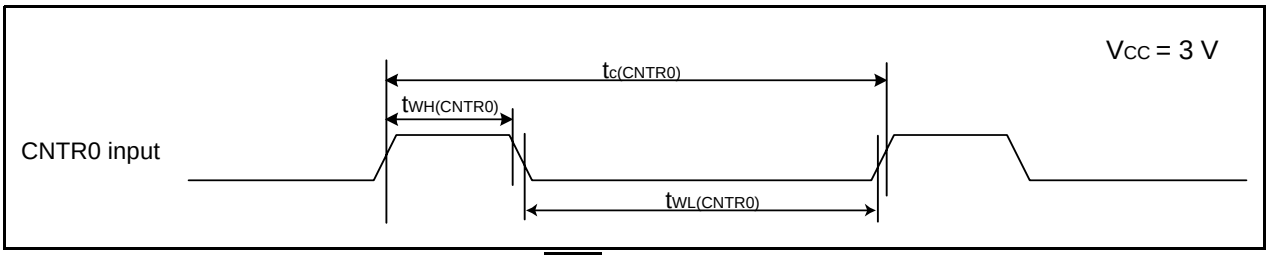


Figure 5.10 CNTR0 Input, CNTR1 Input, $\overline{\text{INT1}}$ Input Timing Diagram when Vcc = 3 V

Table 5.23 TCIN Input, $\overline{\text{INT3}}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TCIN)}$	TCIN input cycle time	1,200(1)	–	ns
$t_{WH(TCIN)}$	TCIN input “H” width	600(2)	–	ns
$t_{WL(TCIN)}$	TCIN input “L” width	600(2)	–	ns

NOTES:
1. When using the timer C input capture mode, adjust the cycle time to (1/timer C count source frequency × 3) or above.
2. When using the timer C input capture mode, adjust the width to (1/timer C count source frequency × 1.5) or above.

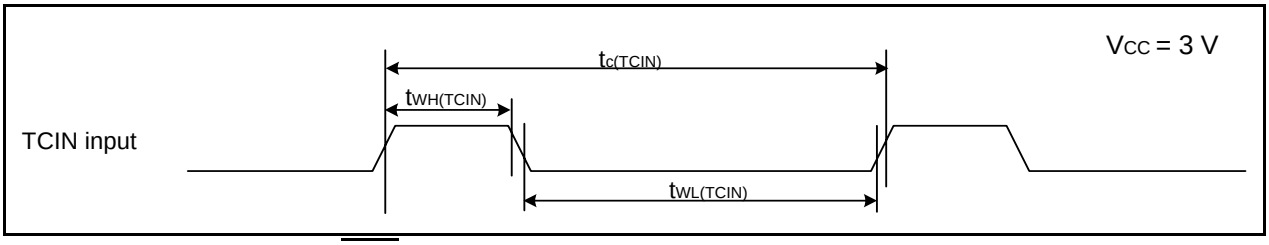
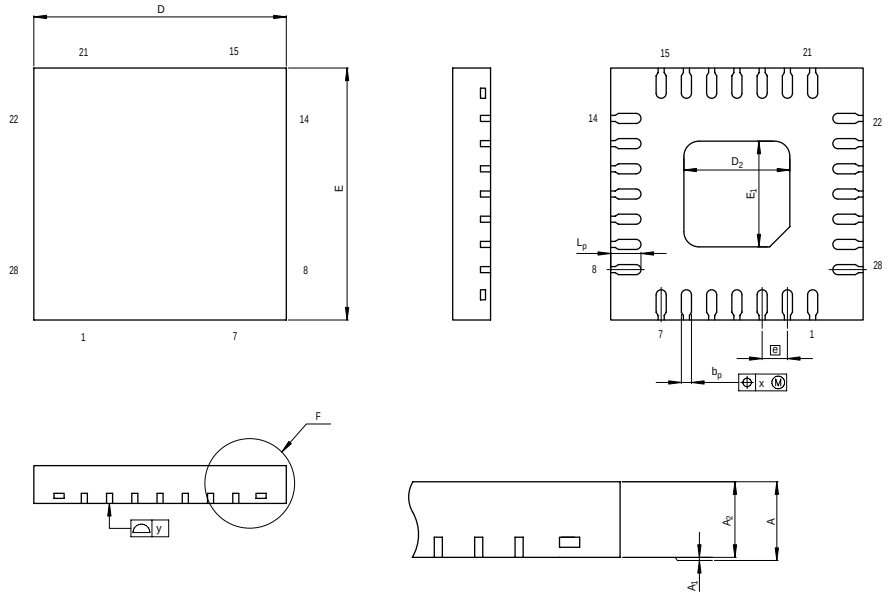


Figure 5.11 TCIN Input, $\overline{\text{INT3}}$ Input Timing Diagram when Vcc = 3 V

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-HWQFN28-5x5-0.50	PWQN0028KA-B	28PJW-B	0.05g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	4.9	5.0	5.1
E	4.9	5.0	5.1
A_2	—	0.75	—
A	—	—	0.8
A_1	0	0	0.05
b_p	0.15	0.2	0.25
e	—	0.5	—
L_p	0.5	0.6	0.7
x	—	—	0.05
y	—	—	0.05
D_2	—	—	2.0
E_1	—	—	2.0

REVISION HISTORY	R8C/18 Group, R8C/19 Group Datasheet

Rev.	Date	Description	
		Page	Summary
0.10	Nov 15, 2004	–	First Edition issued
0.20	Jan 11, 2005	5, 6	Tables 1.3 and 1.4: The date updated
0.21	Apr 04, 2005	2, 3	Tables 1.1 and 1.2: Partly revised
		4	Figure 1.1: Partly revised
		5, 6	Tables 1.3 and 1.4: Partly revised
		5, 6	Figure 1.2 and 1.3: Partly revised
		7, 8	Figure 1.4 and 1.5: Partly revised
		10	Table 1.6: Partly revised
		16	Table 4.1: Partly revised
		17	Table 4.2: Partly revised
		18	Table 4.3: Partly revised
		20	Package Dimensions are revised
1.00	May 27, 2005	5, 6	Tables 1.3 and 1.4: Partly revised
		9	Table 1.5: Partly revised
		25	Table 5.9: Revised
		26	Table 5.10: Partly revised
		28	Table 5.13: Partly revised
		32	Table 5.20: Partly revised
1.10	Jun 09, 2005	26	Table 5.10: Partly revised
1.20	Nov 01, 2005	3	Table 1.2 Performance Outline of the R8C/19 Group; Flash Memory: (Data area) → (Data flash) (Program area) → (Program ROM) revised
		4	Figure 1.1 Block Diagram; “Peripheral Function” added, “System Clock Generation” → “System Clock Generator” revised
		6	Table 1.4 Product Information of R8C/19 Group; ROM capacity: “Program area” → “Program ROM”, “Data area” → “Data flash” revised
		9	Table 1.5 Pin Description; Power Supply Input: “VCC/AVCC” → “VCC”, “VSS/AVSS” → “VSS” revised Analog Power Supply Input: added
		11	Figure 2.1 CPU Register; “Reserved Area” → “Reserved Bit” revised
		13	2.8.10 Reserved Area; “Reserved Area” → “Reserved Bit” revised
		15	3.2 R8C/19 Group, Figure 3.2 Memory Map of R8C/19 Group; “Data area” → “Data flash”, “Program area” → “Program ROM” revised

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