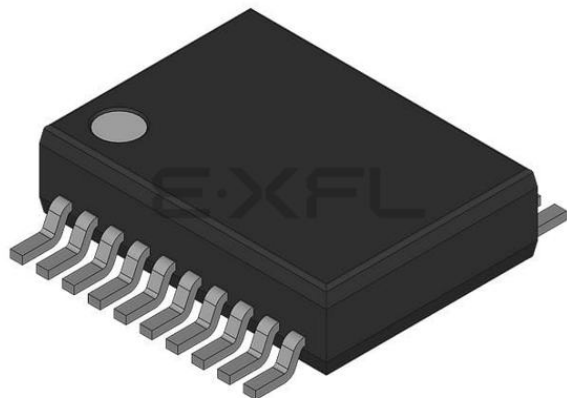




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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	SIO, UART/USART
Peripherals	LED, POR, Voltage Detect, WDT
Number of I/O	13
Program Memory Size	16KB (16K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-LSSOP (0.173", 4.40mm Width)
Supplier Device Package	20-LSSOP
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21194sp-u0

1. Overview

These MCUs are fabricated using a high-performance silicon gate CMOS process, embedding the R8C/Tiny Series CPU core, and is packaged in a 20-pin molded-plastic LSSOP, SDIP or a 28-pin plastic molded-HWQFN. It implements sophisticated instructions for a high level of instruction efficiency. With 1 Mbyte of address space, they are capable of executing instructions at high speed.

Furthermore, the R8C/19 Group has on-chip data flash ROM (1 KB × 2 blocks).

The difference between the R8C/18 Group and R8C/19 Group is only the presence or absence of data flash ROM. Their peripheral functions are the same.

1.1 Applications

Electric household appliances, office equipment, housing equipment (sensors, security systems), general industrial equipment, audio equipment, etc.

1.2 Performance Overview

Table 1.1 outlines the Functions and Specifications for R8C/18 Group and Table 1.2 outlines the Functions and Specifications for R8C/19 Group.

Table 1.1 Functions and Specifications for R8C/18 Group

	Item	Specification
CPU	Number of fundamental instructions	89 instructions
	Minimum instruction execution time	50 ns ($f(XIN) = 20$ MHz, $VCC = 3.0$ to 5.5 V) 100 ns ($f(XIN) = 10$ MHz, $VCC = 2.7$ to 5.5 V)
	Operation mode	Single-chip
	Address space	1 Mbyte
	Memory capacity	Refer to Table 1.3 Product Information for R8C/18 Group
Peripheral Functions	Ports	I/O ports: 13 pins (including LED drive port) Input port: 3 pins
	LED drive ports	I/O ports: 4 pins
	Timers	Timer X: 8 bits $\times$ 1 channel, timer Z: 8 bits $\times$ 1 channel (Each timer equipped with 8-bit prescaler) Timer C: 16 bits $\times$ 1 channel (Input capture and output compare circuits)
	Serial interfaces	1 channel Clock synchronous serial I/O, UART 1 channel UART
	Comparator	1-bit comparator: 1 circuit, 4 channels
	Watchdog timer	15 bits $\times$ 1 channel (with prescaler) Reset start selectable, count source protection mode
	Interrupts	Internal: 10 sources, External: 4 sources, Software: 4 sources, Priority levels: 7 levels
	Clock generation circuits	2 circuits • Main clock oscillation circuit (with on-chip feedback resistor) • On-chip oscillator (high speed, low speed) High-speed on-chip oscillator has frequency adjustment function
	Oscillation stop detection function	Main clock oscillation stop detection function
	Voltage detection circuit	On-chip
	Power-on reset circuit	On-chip
Electric Characteristics	Supply voltage	$VCC = 3.0$ to 5.5 V ($f(XIN) = 20$ MHz) $VCC = 2.7$ to 5.5 V ($f(XIN) = 10$ MHz)
	Current consumption	Typ. 9 mA ($VCC = 5.0$ V, $f(XIN) = 20$ MHz, comparator stopped) Typ. 5 mA ($VCC = 3.0$ V, $f(XIN) = 10$ MHz, comparator stopped) Typ. 35 μ A ($VCC = 3.0$ V, wait mode, peripheral clock off) Typ. 0.7 μ A ($VCC = 3.0$ V, stop mode)
Flash Memory	Programming and erasure voltage	$VCC = 2.7$ to 5.5 V
	Programming and erasure endurance	100 times
Operating Ambient Temperature		-20 to 85°C -40 to 85°C (D version)
Package		20-pin molded-plastic LSSOP
		20-pin molded-plastic SDIP
		28-pin molded-plastic HWQFN

Table 1.2 Functions and Specifications for R8C/19 Group

Item		Specification
CPU	Number of fundamental instructions	89 instructions
	Minimum instruction execution time	50 ns (f(XIN) = 20 MHz, VCC = 3.0 to 5.5 V) 100 ns (f(XIN) = 10 MHz, VCC = 2.7 to 5.5 V)
	Operation mode	Single-chip
	Address space	1 Mbyte
	Memory capacity	Refer to Table 1.4 Product Information for R8C/19 Group
Peripheral Functions	Ports	I/O ports: 13 pins (including LED drive port) Input port: 3 pins
	LED drive ports	I/O ports: 4 pins
	Timers	Timer X: 8 bits × 1 channel, timer Z: 8 bits × 1 channel (Each timer equipped with 8-bit prescaler) Timer C: 16 bits × 1 channel (Input capture and output compare circuits)
	Serial interfaces	1 channel Clock synchronous serial I/O, UART 1 channel UART
	Comparator	1-bit comparator: 1 circuit, 4 channels
	Watchdog timer	15 bits × 1 channel (with prescaler) Reset start selectable, count source protection mode
	Interrupts	Internal: 10 sources, External: 4 sources, Software: 4 sources, Priority levels: 7 levels
	Clock generation circuits	2 circuits • Main clock generation circuit (with on-chip feedback resistor) • On-chip oscillator (high speed, low speed) High-speed on-chip oscillator has frequency adjustment function
	Oscillation stop detection function	Main clock oscillation stop detection function
	Voltage detection circuit	On-chip
Power-on reset circuit	On-chip	
Electric Characteristics	Supply voltage	VCC = 3.0 to 5.5 V (f(XIN) = 20 MHz) VCC = 2.7 to 5.5 V (f(XIN) = 10 MHz)
	Current consumption	Typ. 9 mA (VCC = 5.0 V, f(XIN) = 20 MHz, comparator stopped) Typ. 5 mA (VCC = 3.0 V, f(XIN) = 10MHz, comparator stopped) Typ. 35 μA (VCC = 3.0 V, wait mode, peripheral clock off) Typ. 0.7 μA (VCC = 3.0 V, stop mode)
Flash Memory	Programming and erasure voltage	VCC = 2.7 to 5.5 V
	Programming and erasure endurance	10,000 times (data flash) 1,000 times (program ROM)
Operating Ambient Temperature		-20 to 85°C -40 to 85°C (D version)
Package		20-pin molded-plastic LSSOP
		20-pin molded-plastic SDIP
		28-pin molded-plastic HWQFN

1.4 Product Information

Table 1.3 lists Product Information for R8C/18 Group and Table 1.4 lists Product Information for R8C/19 Group.

Table 1.3 Product Information for R8C/18 Group

Current of Apr. 2006

Type No.	ROM Capacity	RAM Capacity	Package Type	Remarks
R5F21181SP	4 Kbytes	384 bytes	PLSP0020JB-A	Flash memory version D version
R5F21182SP	8 Kbytes	512 bytes	PLSP0020JB-A	
R5F21183SP	12 Kbytes	768 bytes	PLSP0020JB-A	
R5F21184SP	16 Kbytes	1 Kbyte	PLSP0020JB-A	
R5F21181DSP (D)	4 Kbytes	384 bytes	PLSP0020JB-A	
R5F21182DSP (D)	8 Kbytes	512 bytes	PLSP0020JB-A	
R5F21183DSP (D)	12 Kbytes	768 bytes	PLSP0020JB-A	
R5F21184DSP (D)	16 Kbytes	1 Kbyte	PLSP0020JB-A	
R5F21181DD	4 Kbytes	384 bytes	PRDP0020BA-A	Flash memory version
R5F21182DD	8 Kbytes	512 bytes	PRDP0020BA-A	
R5F21183DD	12 Kbytes	768 bytes	PRDP0020BA-A	
R5F21184DD	16 Kbytes	1 Kbyte	PRDP0020BA-A	
R5F21182NP	8 Kbytes	512 bytes	PWQN0028KA-B	Flash memory version
R5F21183NP	12 Kbytes	768 bytes	PWQN0028KA-B	
R5F21184NP	16 Kbytes	1 Kbyte	PWQN0028KA-B	

(D): Under Development

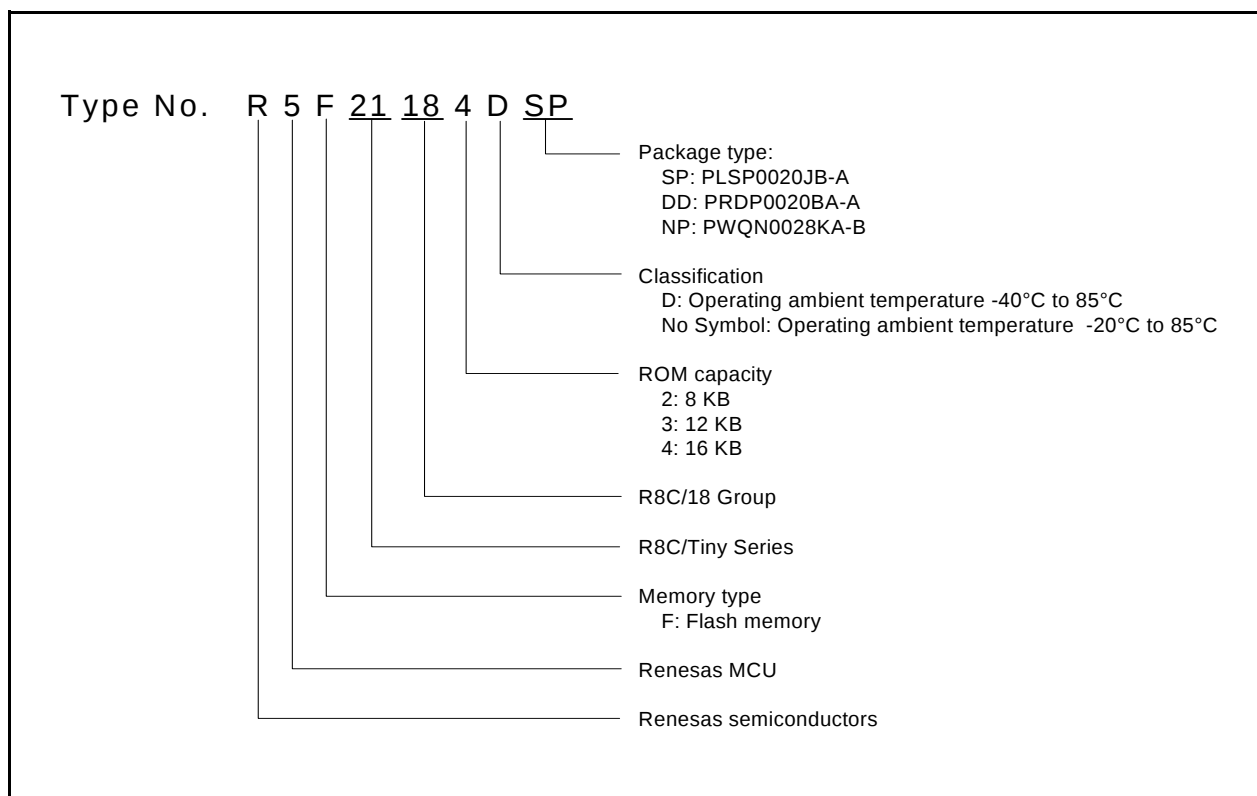


Figure 1.2 Type Number, Memory Size, and Package of R8C/18 Group

1.5 Pin Assignments

Figure 1.4 shows Pin Assignments for PLSP0020JB-A Package (Top View), Figure 1.5 shows Pin Assignments for PRDP0020BA-A Package (Top View) and Figure 1.6 shows Pin Assignments for PWQN0028KA-B Package (Top View).

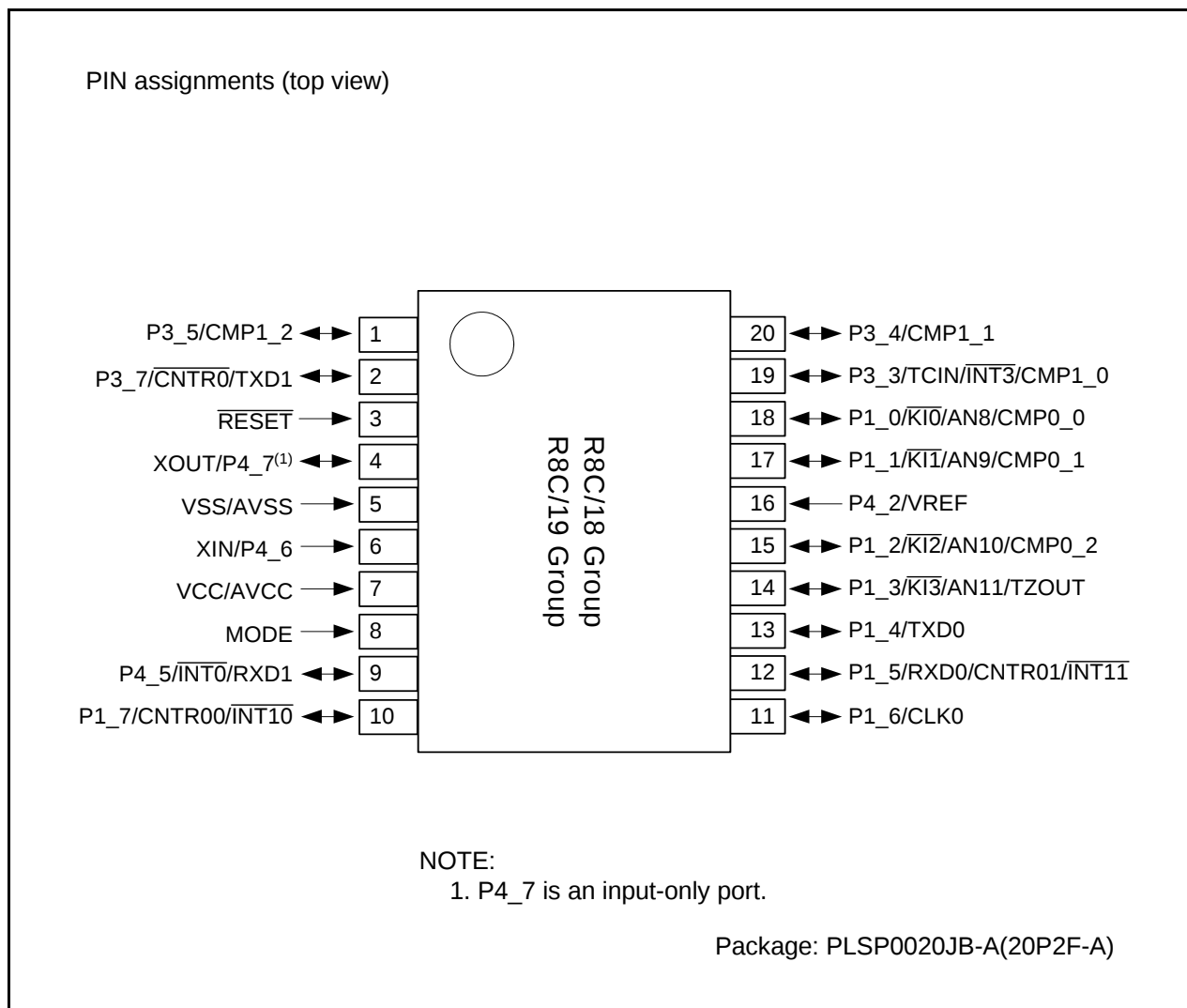


Figure 1.4 Pin Assignments for PLSP0020JB-A Package (Top View)

Table 1.6 Pin Name Information by Pin Number of PLSP0020JB-A, PRDP0020BA-A packages

Pin Number	Control Pin	Port	I/O Pin Functions for Peripheral Modules			
			Interrupt	Timer	Serial Interface	Comparator
1		P3_5		CMP1_2		
2		P3_7		CNTR0	TXD1	
3	RESET					
4	XOUT	P4_7				
5	VSS/AVSS					
6	XIN	P4_6				
7	VCC/AVCC					
8	MODE					
9		P4_5	INT0		RXD1	
10		P1_7	INT10	CNTR00		
11		P1_6			CLK0	
12		P1_5	INT11	CNTR01	RXD0	
13		P1_4			TXD0	
14		P1_3	KI3	TZOUT		AN11
15		P1_2	KI2	CMP0_2		AN10
16	VREF	P4_2				
17		P1_1	KI1	CMP0_1		AN9
18		P1_0	KI0	CMP0_0		AN8
19		P3_3	INT3	TCIN/CMP1_0		
20		P3_4		CMP1_1		

Table 1.7 Pin Name Information by Pin Number of PWQN0028KA-B package

Pin Number	Control Pin	Port	I/O Pin of Peripheral Function			
			Interrupt	Timer	Serial Interface	Comparator
1	NC					
2	XOUT	P4_7				
3	VSS/AVSS					
4	NC					
5	NC					
6	XIN	P4_6				
7	NC					
8	VCC/AVCC					
9	MODE					
10		P4_5	$\overline{\text{INT0}}$		RXD1	
11		P1_7	$\overline{\text{INT10}}$	CNTR00		
12		P1_6			CLK0	
13		P1_5	$\overline{\text{INT11}}$	CNTR01	RXD0	
14		P1_4			TXD0	
15	NC					
16		P1_3	$\overline{\text{KI3}}$	TZOUT		AN11
17		P1_2	$\overline{\text{KI2}}$	CMP0_2		AN10
18	NC					
19	NC					
20	VREF	P4_2				
21	NC					
22		P1_1	$\overline{\text{KI1}}$	CMP0_1		AN9
23		P1_0	$\overline{\text{KI0}}$	CMP0_0		AN8
24		P3_3	$\overline{\text{INT3}}$	TCIN/CMP1_0		
25		P3_4		CMP1_1		
26		P3_5		CMP1_2		
27		P3_7		$\overline{\text{CNTR0}}$	TXD1	
28	$\overline{\text{RESET}}$					

3.2 R8C/19 Group

Figure 3.2 is a Memory Map of R8C/19 Group. The R8C/19 group has 1 Mbyte of address space from addresses 00000h to FFFFFh.

The internal ROM (program ROM) is allocated lower addresses, beginning with address 00000h. For example, a 16-Kbyte internal ROM area is allocated addresses 0C000h to 0FFFFh.

The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. They store the starting address of each interrupt routine.

The internal ROM (data flash) is allocated addresses 02400h to 02BFFh.

The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 1-Kbyte internal RAM area is allocated addresses 00400h to 007FFh. The internal RAM is used not only for storing data but also for calling subroutines and as stacks when interrupt requests are acknowledged.

Special function registers (SFRs) are allocated addresses 00000h to 002FFh. The peripheral function control registers are allocated here. All addresses within the SFR, which have nothing allocated are reserved for future use and cannot be accessed by users.

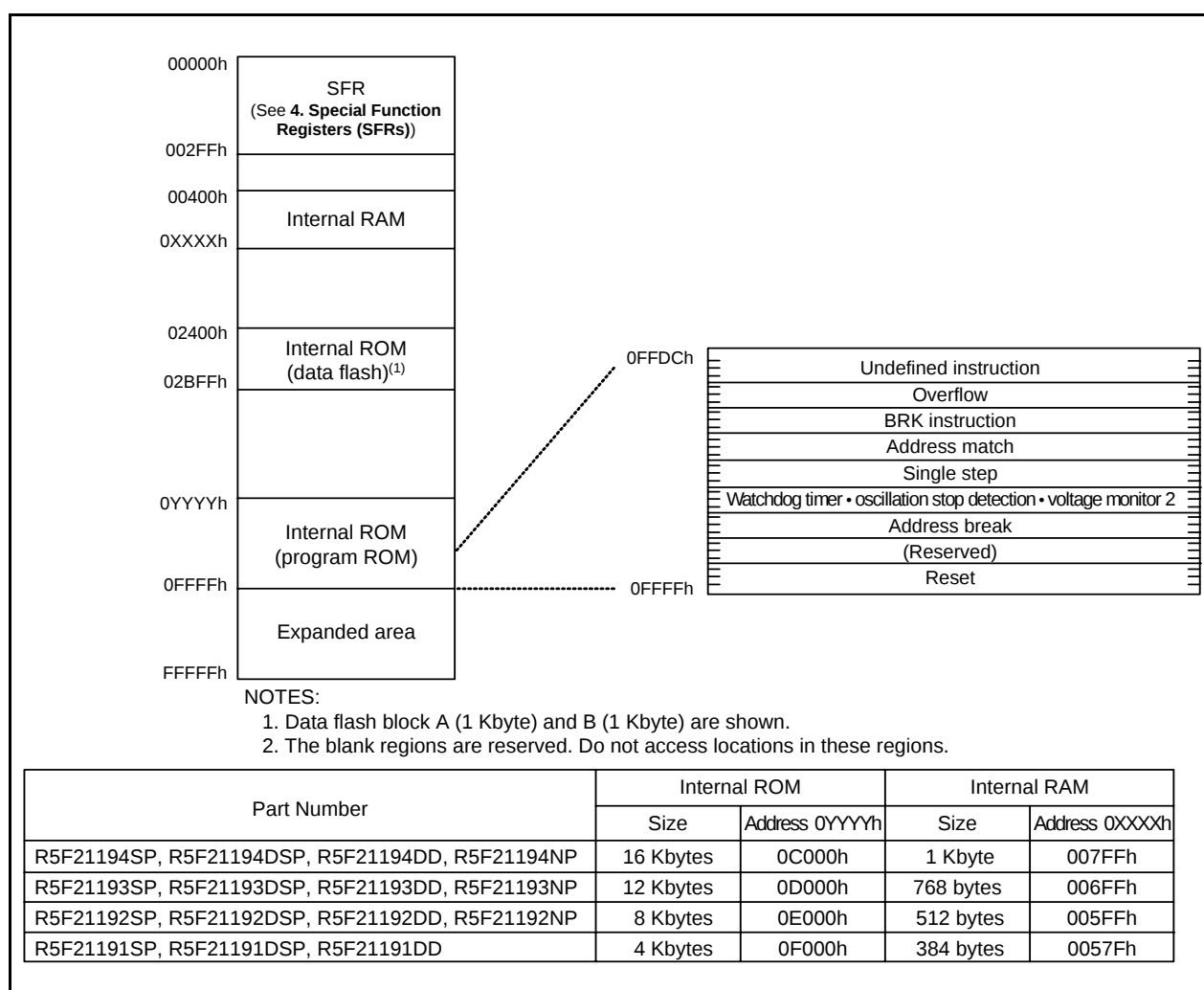


Figure 3.2 Memory Map of R8C/19 Group

4. Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 4.1 to 4.4 list the special function registers.

Table 4.1 SFR Information (1)(1)

Address	Register	Symbol	After reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	00h
0005h	Processor Mode Register 1	PM1	00h
0006h	System Clock Control Register 0	CM0	01101000b
0007h	System Clock Control Register 1	CM1	00100000b
0008h			
0009h	Address Match Interrupt Enable Register	AIER	00h
000Ah	Protect Register	PRCR	00h
000Bh			
000Ch	Oscillation Stop Detection Register	OSD	00000100b
000Dh	Watchdog Timer Reset Register	WDTR	XXh
000Eh	Watchdog Timer Start Register	WDTS	XXh
000Fh	Watchdog Timer Control Register	WDC	00011111b
0010h	Address Match Interrupt Register 0	RMAD0	00h
0011h			00h
0012h			X0h
0013h			
0014h	Address Match Interrupt Register 1	RMAD1	00h
0015h			00h
0016h			X0h
0017h			
0018h			
0019h			
001Ah			
001Bh			
001Ch	Count Source Protection Mode Register	CSPR	00h
001Dh			
001Eh	INT0 Input Filter Select Register	INT0F	00h
001Fh			
0020h	High-Speed On-Chip Oscillator Control Register 0	HRA0	00h
0021h	High-Speed On-Chip Oscillator Control Register 1	HRA1	When shipping
0022h	High-Speed On-Chip Oscillator Control Register 2	HRA2	00h
0023h			
0024h			
0025h			
0026h			
0027h			
0028h			
0029h			
002Ah			
002Bh			
002Ch			
002Dh			
002Eh			
002Fh			
0030h			
0031h	Voltage Detection Register 1 ⁽²⁾	VCA1	00001000b
0032h	Voltage Detection Register 2 ⁽²⁾	VCA2	00h ⁽³⁾ 01000000b ⁽⁴⁾
0033h			
0034h			
0035h			
0036h	Voltage Monitor 1 Circuit Control Register ⁽²⁾	VW1C	0000X000b ⁽³⁾ 0100X001b ⁽⁴⁾
0037h	Voltage Monitor 2 Circuit Control Register ⁽⁵⁾	VW2C	00h
0038h			
0039h			
003Ah			
003Bh			
003Ch			
003Dh			
003Eh			
003Fh			

X: Undefined

NOTES:

1. The blank regions are reserved. Do not access locations in these regions.
2. Software reset, watchdog timer reset, and voltage monitor 2 reset do not affect this register.
3. After hardware reset.
4. After power-on reset or voltage monitor 1 reset.
5. Software reset, watchdog timer reset, and voltage monitor 2 reset do not affect b2 and b3.

Table 4.2 SFR Information (2)⁽¹⁾

Address	Register	Symbol	After reset
0040h			
0041h			
0042h			
0043h			
0044h			
0045h			
0046h			
0047h			
0048h			
0049h			
004Ah			
004Bh			
004Ch			
004Dh	Key Input Interrupt Control Register	KUPIC	XXXXX000b
004Eh	Comparator Conversion Interrupt Control Register	ADIC	XXXXX000b
004Fh			
0050h	Compare 1 Interrupt Control Register	CMP1IC	XXXXX000b
0051h	UART0 Transmit Interrupt Control Register	S0TIC	XXXXX000b
0052h	UART0 Receive Interrupt Control Register	S0RIC	XXXXX000b
0053h	UART1 Transmit Interrupt Control Register	S1TIC	XXXXX000b
0054h	UART1 Receive Interrupt Control Register	S1RIC	XXXXX000b
0055h			
0056h	Timer X Interrupt Control Register	TXIC	XXXXX000b
0057h			
0058h	Timer Z Interrupt Control Register	TZIC	XXXXX000b
0059h	INT1 Interrupt Control Register	INT1IC	XXXXX000b
005Ah	INT3 Interrupt Control Register	INT3IC	XXXXX000b
005Bh	Timer C Interrupt Control Register	TCIC	XXXXX000b
005Ch	Compare 0 Interrupt Control Register	CMP0IC	XXXXX000b
005Dh	INT0 Interrupt Control Register	INT0IC	XX00X000b
005Eh			
005Fh			
0060h			
0061h			
0062h			
0063h			
0064h			
0065h			
0066h			
0067h			
0068h			
0069h			
006Ah			
006Bh			
006Ch			
006Dh			
006Eh			
006Fh			
0070h			
0071h			
0072h			
0073h			
0074h			
0075h			
0076h			
0077h			
0078h			
0079h			
007Ah			
007Bh			
007Ch			
007Dh			
007Eh			
007Fh			

X: Undefined

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

5. Electrical Characteristics

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter	Condition	Rated Value	Unit
V _{CC}	Supply voltage	V _{CC} = AV _{CC}	-0.3 to 6.5	V
AV _{CC}	Analog supply voltage	V _{CC} = AV _{CC}	-0.3 to 6.5	V
V _I	Input voltage		-0.3 to V _{CC} +0.3	V
V _O	Output voltage		-0.3 to V _{CC} +0.3	V
P _d	Power dissipation	T _{opr} = 25°C	300	mW
T _{opr}	Operating ambient temperature		-20 to 85 / -40 to 85 (D version)	°C
T _{stg}	Storage temperature		-65 to 150	°C

Table 5.2 Recommended Operating Conditions

Symbol	Parameter		Conditions	Standard			Unit
				Min.	Typ.	Max.	
V _{CC}	Supply voltage			2.7	—	5.5	V
AV _{CC}	Analog supply voltage			—	V _{CC}	—	V
V _{SS}	Supply voltage			—	0	—	V
AV _{SS}	Analog supply voltage			—	0	—	V
V _{IH}	Input "H" voltage			0.8V _{CC}	—	V _{CC}	V
V _{IL}	Input "L" voltage			0	—	0.2V _{CC}	V
I _{OH} (sum)	Peak sum output "H" current	Sum of all pins I _{OH} (peak)		—	—	-60	mA
I _{OH} (peak)	Peak output "H" current			—	—	-10	mA
I _{OH} (avg)	Average output "H" current			—	—	-5	mA
I _{OL} (sum)	Peak sum output "L" currents	Sum of all pins I _{OL} (peak)		—	—	60	mA
I _{OL} (peak)	Peak output "L" currents	Except P1_0 to P1_3		—	—	10	mA
		P1_0 to P1_3	Drive capacity HIGH	—	—	30	mA
			Drive capacity LOW	—	—	10	mA
I _{OL} (avg)	Average output "L" current	Except P1_0 to P1_3		—	—	5	mA
		P1_0 to P1_3	Drive capacity HIGH	—	—	15	mA
			Drive capacity LOW	—	—	5	mA
f _(XIN)	Main clock input oscillation frequency		3.0 V ≤ V _{CC} ≤ 5.5 V	0	—	20	MHz
			2.7 V ≤ V _{CC} < 3.0 V	0	—	10	MHz

NOTES:

1. V_{CC} = 2.7 to 5.5 V at T_{opr} = -20 to 85 °C / -40 to 85 °C, unless otherwise specified.
2. Typical values when average output current is 100 ms.

Table 5.8 Reset Circuit Electrical Characteristics (When Using Voltage Monitor 1 Reset)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V _{por2}	Power-on reset valid voltage	-20°C ≤ Topr ≤ 85°C	—	—	V _{det1}	V
t _w (V _{por2} -V _{det1})	Supply voltage rising time when power-on reset is deasserted ⁽¹⁾	-20°C ≤ Topr ≤ 85°C, t _w (por2) ≥ 0s ⁽³⁾	—	—	100	ms

NOTES:

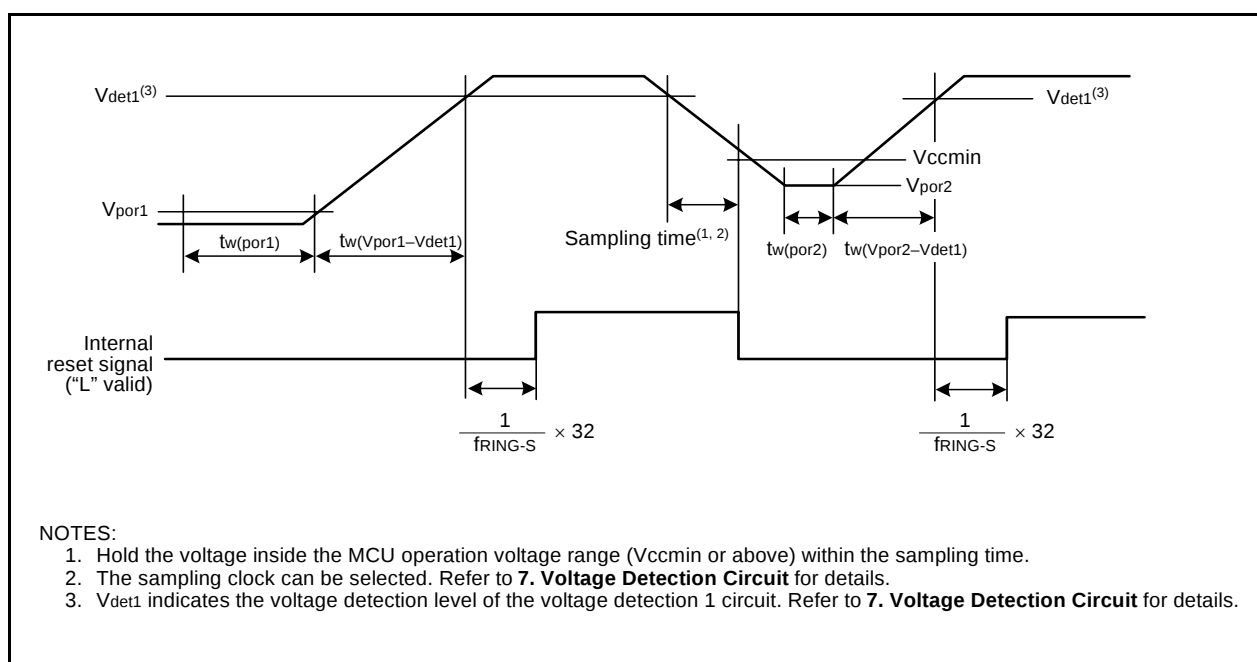
1. This condition is not applicable when using with V_{cc} ≥ 1.0 V.
2. When turning power on after the time to hold the external power below effective voltage (V_{por1}) exceeds 10 s, refer to **Table 5.9 Reset Circuit Electrical Characteristics (When Not Using Voltage Monitor 1 Reset)**.
3. t_w(por2) is the time to hold the external power below effective voltage (V_{por2}).

Table 5.9 Reset Circuit Electrical Characteristics (When Not Using Voltage Monitor 1 Reset)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V _{por1}	Power-on reset valid voltage	-20°C ≤ Topr ≤ 85°C	—	—	0.1	V
t _w (V _{por1} -V _{det1})	Supply voltage rising time when power-on reset is deasserted	0°C ≤ Topr ≤ 85°C, t _w (por1) ≥ 10 s ⁽²⁾	—	—	100	ms
t _w (V _{por1} -V _{det1})	Supply voltage rising time when power-on reset is deasserted	-20°C ≤ Topr < 0°C, t _w (por1) ≥ 30 s ⁽²⁾	—	—	100	ms
t _w (V _{por1} -V _{det1})	Supply voltage rising time when power-on reset is deasserted	-20°C ≤ Topr < 0°C, t _w (por1) ≥ 10 s ⁽²⁾	—	—	1	ms
t _w (V _{por1} -V _{det1})	Supply voltage rising time when power-on reset is deasserted	0°C ≤ Topr ≤ 85°C, t _w (por1) ≥ 1 s ⁽²⁾	—	—	0.5	ms

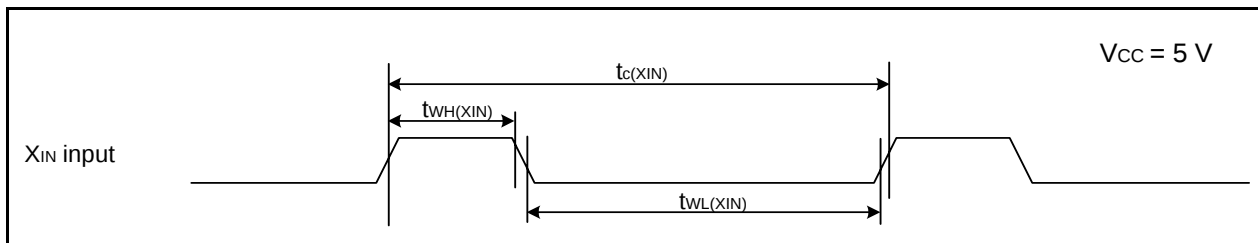
NOTES:

1. When not using voltage monitor 1, use with V_{cc} ≥ 2.7 V.
2. t_w(por1) is the time to hold the external power below effective voltage (V_{por1}).

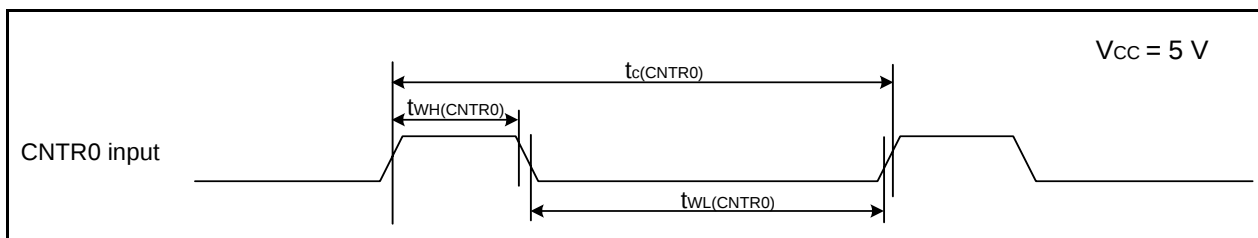
**Figure 5.3 Reset Circuit Electrical Characteristics**

Timing Requirements(Unless Otherwise Specified: $V_{CC} = 5\text{ V}$, $V_{SS} = 0\text{ V}$ at $T_a = 25\text{ }^{\circ}\text{C}$) [$V_{CC} = 5\text{ V}$]**Table 5.14 XIN Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	50	–	ns
$t_{WH(XIN)}$	XIN input “H” width	25	–	ns
$t_{WL(XIN)}$	XIN input “L” width	25	–	ns

**Figure 5.4 XIN Input Timing Diagram when $V_{CC} = 5\text{ V}$** **Table 5.15 CNTR0 Input, CNTR1 Input, $\overline{\text{INT1}}$ Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CNTR0)}$	CNTR0 input cycle time	100	–	ns
$t_{WH(CNTR0)}$	CNTR0 input “H” width	40	–	ns
$t_{WL(CNTR0)}$	CNTR0 input “L” width	40	–	ns

**Figure 5.5 CNTR0 Input, CNTR1 Input, $\overline{\text{INT1}}$ Input Timing Diagram when $V_{CC} = 5\text{ V}$** **Table 5.16 TCIN Input, $\overline{\text{INT3}}$ Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TCIN)}$	TCIN input cycle time	400 ⁽¹⁾	–	ns
$t_{WH(TCIN)}$	TCIN input “H” width	200 ⁽²⁾	–	ns
$t_{WL(TCIN)}$	TCIN input “L” width	200 ⁽²⁾	–	ns

NOTES:

1. When using timer C input capture mode, adjust the cycle time to (1/timer C count source frequency x 3) or above.
2. When using timer C input capture mode, adjust the pulse width to (1/timer C count source frequency x 1.5) or above.

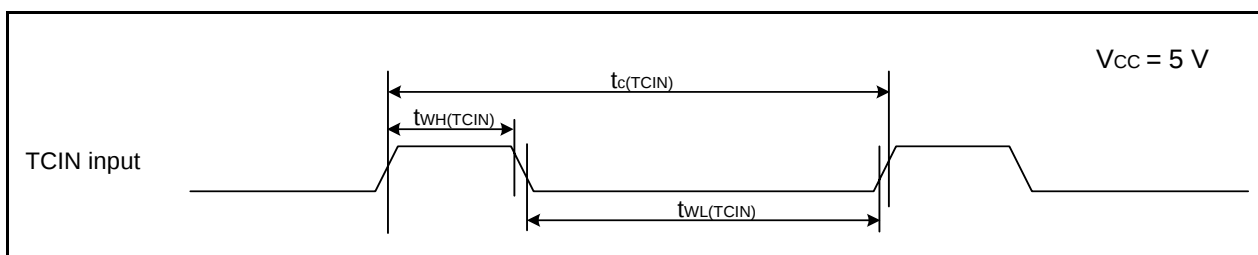
**Figure 5.6 TCIN Input, $\overline{\text{INT3}}$ Input Timing Diagram when $V_{CC} = 5\text{ V}$**

Table 5.19 Electrical Characteristics (3) [V_{CC} = 3V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V _{OH}	Output "H" voltage	Except X _{OUT}	I _{OH} = -1 mA		V _{CC} - 0.5	—	V _{CC}	V
		X _{OUT}	Drive capacity HIGH	I _{OH} = -0.1 mA	V _{CC} - 0.5	—	V _{CC}	V
			Drive capacity LOW	I _{OH} = -50 μA	V _{CC} - 0.5	—	V _{CC}	V
V _{OL}	Output "L" voltage	Except P1_0 to P1_3, X _{OUT}	I _{OL} = 1mA		—	—	0.5	V
		P1_0 to P1_3	Drive capacity HIGH	I _{OL} = 2 mA	—	—	0.5	V
			Drive capacity LOW	I _{OL} = 1 mA	—	—	0.5	V
		X _{OUT}	Drive capacity HIGH	I _{OL} = 0.1 mA	—	—	0.5	V
			Drive capacity LOW	I _{OL} = 50 μA	—	—	0.5	V
V _{T+} -V _{T-}	Hysteresis	INT0, INT1, INT2, INT3, KI0, KI1, KI2, KI3, CNTR0, CNTR1, TCIN, RXD0			0.2	—	0.8	V
		RESET			0.2	—	1.8	V
I _{IH}	Input "H" current		V _I = 3 V		—	—	4.0	μA
I _{IL}	Input "L" current		V _I = 0 V		—	—	-4.0	μA
R _{PULLUP}	Pull-up resistance		V _I = 0 V		66	160	500	kΩ
R _{FXIN}	Feedback resistance	XIN			—	3.0	—	MΩ
f _{RING-S}	Low-speed on-chip oscillator frequency				40	125	250	kHz
V _{RAM}	RAM hold voltage		During stop mode		2.0	—	—	V

NOTE:

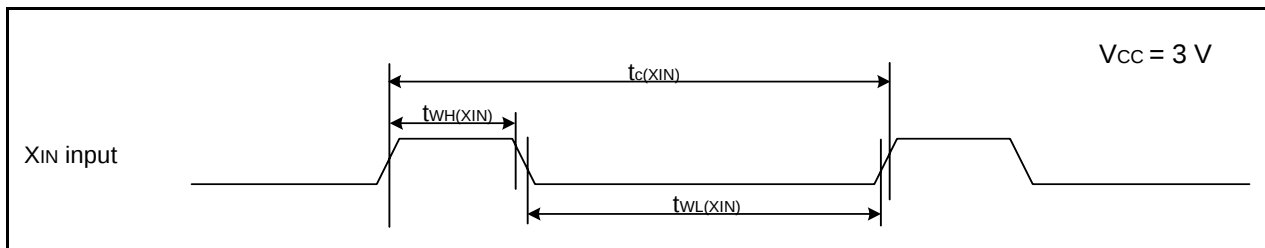
1. V_{CC} = 2.7 to 3.3 V at T_{opr} = -20 to 85 °C / -40 to 85 °C, f(XIN) = 10 MHz, unless otherwise specified.

Table 5.20 Electrical Characteristics (4) [V_{CC} = 3V] (Topr = -40 to 85 °C, unless otherwise specified.)

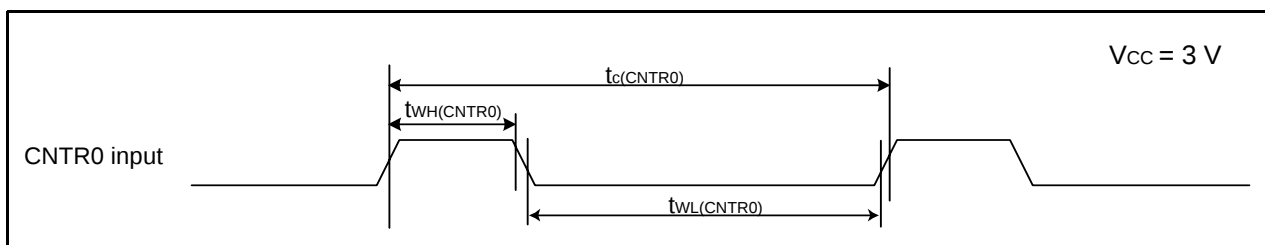
Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
I _{CC}	Power supply current (V _{CC} = 2.7 to 3.3 V) Single-chip mode, output pins are open, other pins are V _{SS} , comparator is stopped	High-speed mode	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	8	13	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	7	12	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	5	–	mA
		Medium- speed mode	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	3	–	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	2.5	–	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	1.6	–	mA
		High-speed on-chip oscillator mode	Main clock off High-speed on-chip oscillator on = 8 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	3.5	7.5	mA
			Main clock off High-speed on-chip oscillator on = 8 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	1.5	–	mA
		Low-speed on-chip oscillator mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8 FMR47 = 1	–	100	280	μA
		Wait mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = 0	–	37	74	μA
		Wait mode	Main clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = 0	–	35	70	μA
		Stop mode	Main clock off, Topr = 25 °C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = 0	–	0.7	3.0	μA

Timing requirements**(Unless Otherwise Specified: $V_{CC} = 3\text{ V}$, $V_{SS} = 0\text{ V}$ at $T_a = 25\text{ }^{\circ}\text{C}$) [$V_{CC} = 3\text{ V}$]****Table 5.21 XIN Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XIN)}$	XIN input cycle time	100	–	ns
$t_{WH(XIN)}$	XIN input “H” width	40	–	ns
$t_{WL(XIN)}$	XIN input “L” width	40	–	ns

**Figure 5.9 XIN Input Timing Diagram when $V_{CC} = 3\text{ V}$** **Table 5.22 CNTR0 Input, CNTR1 Input, $\overline{\text{INT1}}$ Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CNTR0)}$	CNTR0 input cycle time	300	–	ns
$t_{WH(CNTR0)}$	CNTR0 input “H” width	120	–	ns
$t_{WL(CNTR0)}$	CNTR0 input “L” width	120	–	ns

**Figure 5.10 CNTR0 Input, CNTR1 Input, $\overline{\text{INT1}}$ Input Timing Diagram when $V_{CC} = 3\text{ V}$** **Table 5.23 TCIN Input, $\overline{\text{INT3}}$ Input**

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TCIN)}$	TCIN input cycle time	1,200 ⁽¹⁾	–	ns
$t_{WH(TCIN)}$	TCIN input “H” width	600 ⁽²⁾	–	ns
$t_{WL(TCIN)}$	TCIN input “L” width	600 ⁽²⁾	–	ns

NOTES:

1. When using the timer C input capture mode, adjust the cycle time to (1/timer C count source frequency × 3) or above.
2. When using the timer C input capture mode, adjust the width to (1/timer C count source frequency × 1.5) or above.

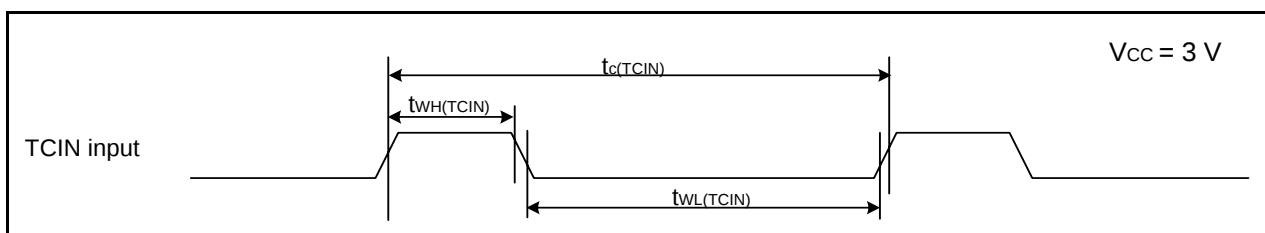
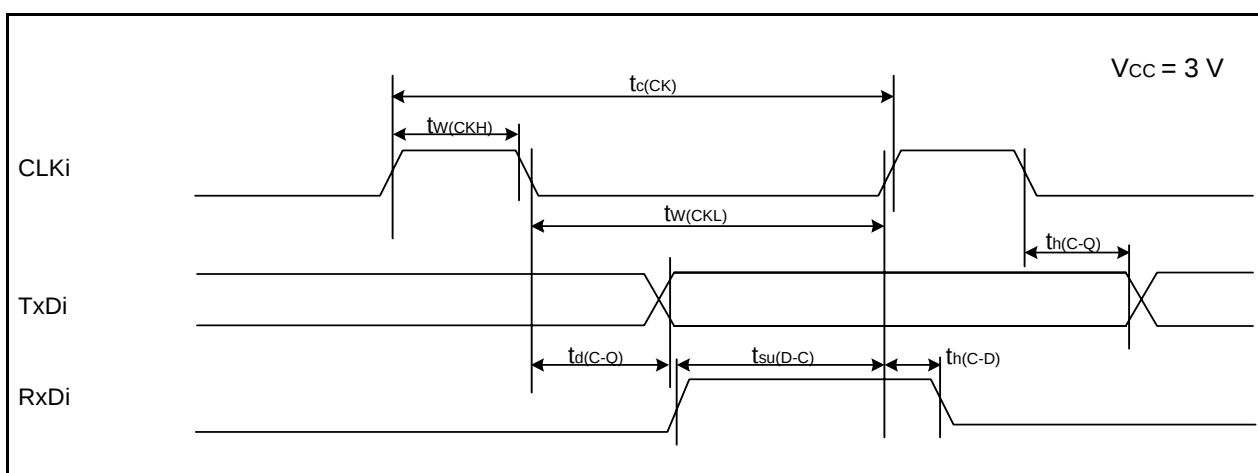
**Figure 5.11 TCIN Input, $\overline{\text{INT3}}$ Input Timing Diagram when $V_{CC} = 3\text{ V}$**

Table 5.24 Serial Interface

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	300	—	ns
$t_{w(CKH)}$	CLKi input "H" width	150	—	ns
$t_{w(CKL)}$	CLKi input "L" width	150	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	80	ns
$t_{h(C-Q)}$	TXDi hold time	0	—	ns
$t_{su(D-C)}$	RXDi input setup time	70	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	ns

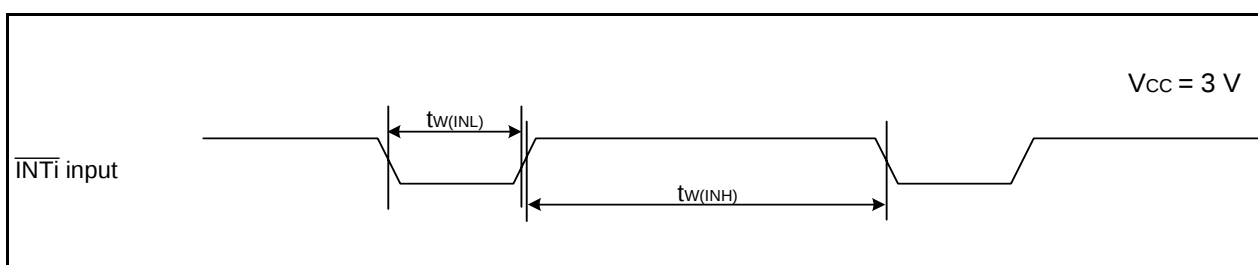
i = 0 or 1

**Figure 5.12 Serial Interface Timing Diagram when Vcc = 3 V****Table 5.25 External Interrupt $\overline{INT0}$ Input**

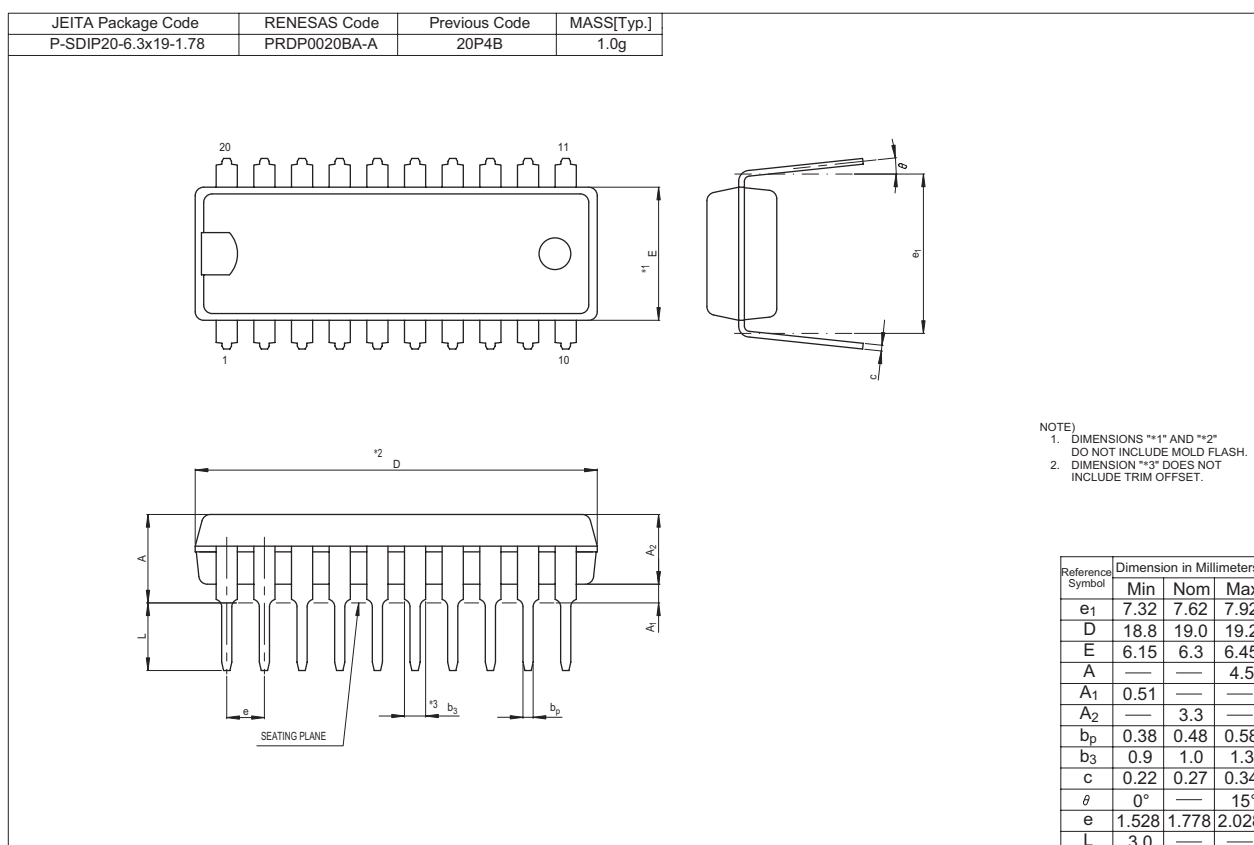
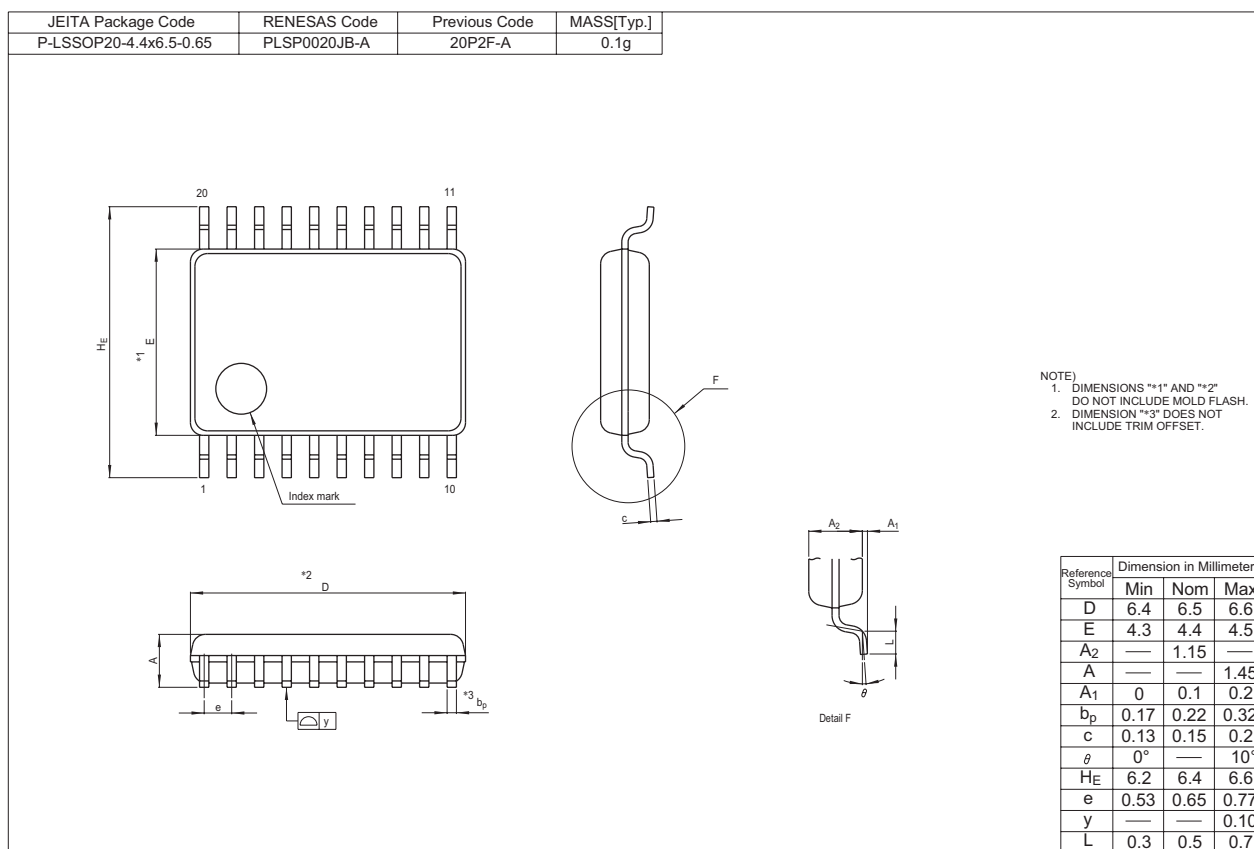
Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INT0}$ input "H" width	380 ⁽¹⁾	—	ns
$t_{w(INL)}$	$\overline{INT0}$ input "L" width	380 ⁽²⁾	—	ns

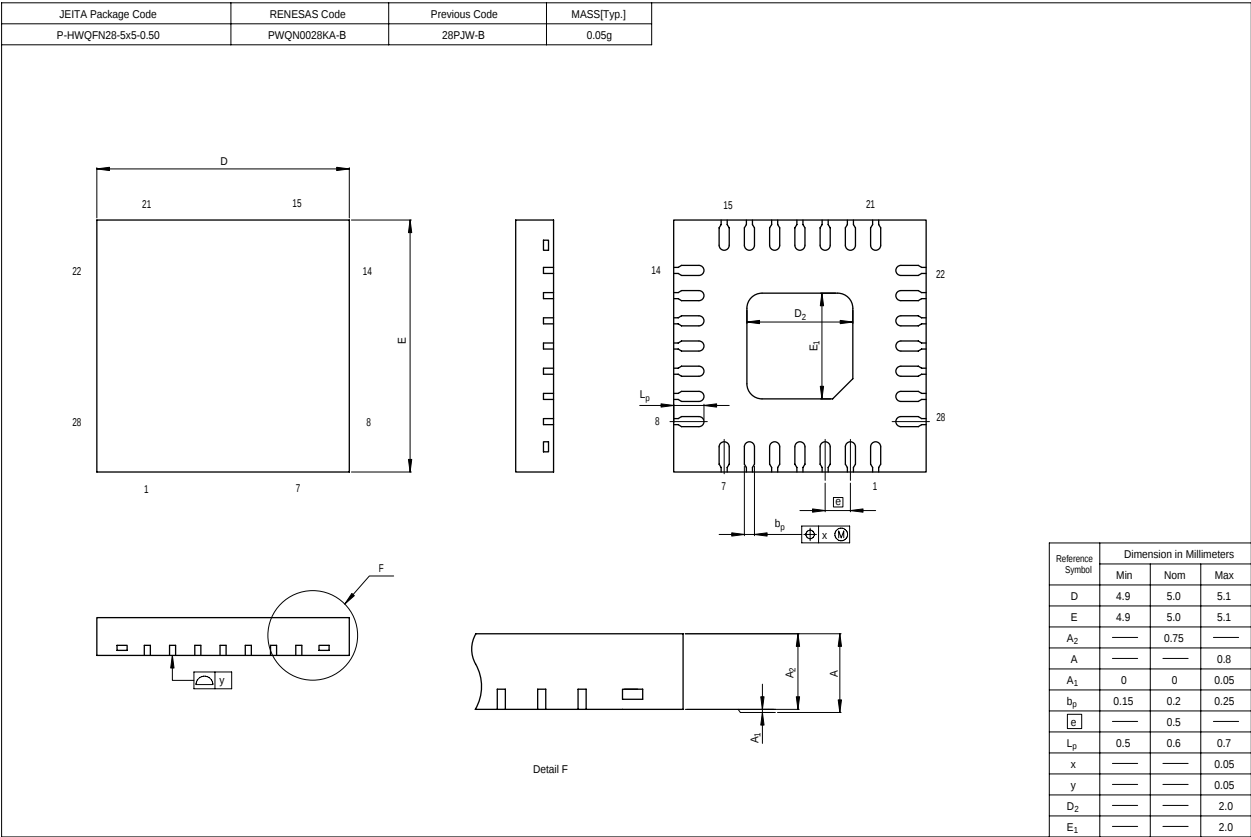
NOTES:

1. When selecting the digital filter by the $\overline{INT0}$ input filter select bit, use an $\overline{INT0}$ input HIGH width of either (1/digital filter clock frequency x 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INT0}$ input filter select bit, use an $\overline{INT0}$ input LOW width of either (1/digital filter clock frequency x 3) or the minimum value of standard, whichever is greater.

**Figure 5.13 External Interrupt $\overline{INT0}$ Input Timing Diagram when Vcc = 3 V**

Package Dimensions





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450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

Renesas Technology Europe Limited

Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
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Renesas Technology (Shanghai) Co., Ltd.

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Tel: <86> (21) 5877-1818, Fax: <86> (21) 6887-7898

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7th Floor, North Tower, World Finance Centre, Harbour City, 1 Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2730-6071

Renesas Technology Taiwan Co., Ltd.

10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology Singapore Pte. Ltd.

1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

Renesas Technology Korea Co., Ltd.

Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea
Tel: <82> (2) 796-3115, Fax: <82> (2) 796-2145

Renesas Technology Malaysia Sdn. Bhd

Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jalan Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: <603> 7955-9390, Fax: <603> 7955-9510