Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8052
Core Size	8-Bit
Speed	40MHz
Connectivity	EBI/EMI, UART/USART
Peripherals	POR, WDT
Number of I/O	32
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/w78e058ddg

9 SPECIAL FUNCTION REGISTERS

The W78E516D/W78E058D series uses Special Function Registers (SFRs) to control and monitor peripherals and their Modes. The SFRs reside in the register locations 80-FFh and are accessed by direct addressing only. Some of the SFRs are bit addressable. This is very useful in cases where users wish to modify a particular bit without changing the others. The SFRs that are bit addressable are those whose addresses end in 0 or 8. The W78E516D/W78E058D series contain all the SFRs present in the standard 8052. However some additional SFRs are added. In some cases the unused bits in the original 8052, have been given new functions. The list of the SFRs is as follows.

W78E516D/W78E058D Special Function Registers (SFRs) and Reset Values

F8									FF
F0	+B						CHPENR		F7
E8									EF
E0	+ACC								E7
D8	+P4								DF
D0	+PSW								D7
C8	+T2CON		RCAP2L	RCAP2H	TL2	TH2			CF
C0	+XICON		P4CONA	P4CONB	**SFRAL**	**SFRAH**	SFRFD	SFRCN	C7
B8	+IP							CHPCON	BF
B0	+P3				**P43AL**	**P43AH**			B7
A8	+IE				**P42AL**	**P42AH**	P2ECON		AF
A0	+P2								A7
98	+SCON	SBUF							9F
90	+P1				**P41AL**	**P41AH**			97
88	+TCON	TMOD	TL0	TL1	TH0	TH1	AUXR	WDTC	8F
80	+P0	SP	DPL	DPH	**P40AL**	**P40AH**	P0UPR	PCON	87

Figure 9-1: Special Function Register Location Table

Note: 1.The SFRs marked with a plus sign(+) are both byte- and bit-addressable.
2. The text of SFR with bold type characters are extension function registers.

GATE	C/$\overline{T}$	M1	M0	GATE	C/$\overline{T}$	M1	M0
TIMER1				TIMER0			

Mnemonic: TMOD Address: 89h

BIT	NAME	FUNCTION
7	GATE	Gating control: When this bit is set, Timer/counter 1 is enabled only while the $\overline{INT1}$ pin is high and the TR1 control bit is set. When cleared, the $\overline{INT1}$ pin has no effect, and Timer 1 is enabled whenever TR1 control bit is set.
6	C/$\overline{T}$	Timer or Counter Select: When clear, Timer 1 is incremented by the internal clock. When set, the timer counts falling edges on the T1 pin.
5	M1	Timer 1 mode select bit 1. See table below.
4	M0	Timer 1 mode select bit 0. See table below.
3	GATE	Gating control: When this bit is set, Timer/counter 0 is enabled only while the $\overline{INT0}$ pin is high and the TR0 control bit is set. When cleared, the $\overline{INT0}$ pin has no effect, and Timer 0 is enabled whenever TR0 control bit is set.
2	C/$\overline{T}$	Timer or Counter Select: When clear, Timer 0 is incremented by the internal clock. When set, the timer counts falling edges on the T0 pin.
1	M1	Timer 0 mode select bit 1. See table below.
0	M0	Timer 0 mode select bit 0. See table below.

M1, M0: Mode Select bits:

M1	M0	MODE
0	0	Mode 0: 8-bit timer/counter TLx serves as 5-bit pre-scale.
0	1	Mode 1: 16-bit timer/counter, no pre-scale.
1	0	Mode 2: 8-bit timer/counter with auto-reload from THx.
1	1	Mode 3: (Timer 0) TL0 is an 8-bit timer/counter controlled by the standard Timer0 control bits. TH0 is an 8-bit timer only controlled by Timer1 control bits. (Timer 1) Timer/Counter 1 is stopped.

Timer 0 LSB

Bit:	7	6	5	4	3	2	1	0
	TL0.7	TL0.6	TL0.5	TL0.4	TL0.3	TL0.2	TL0.1	TL0.0

Mnemonic: TL0 Address: 8Ah

BIT	NAME	FUNCTION
7-0	TL0.[7:0]	Timer 0 LSB.

Timer 1 LSB

Bit:	7	6	5	4	3	2	1	0
	TL1.7	TL1.6	TL1.5	TL1.4	TL1.3	TL1.2	TL1.1	TL1.0

Serial Port Control

Bit:	7	6	5	4	3	2	1	0
	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI

Mnemonic: SCON Address: 98h

BIT	NAME	FUNCTION
7	SM0/FE	Serial port mode select bit 0 or Framing Error Flag: The SMOD0 bit in PCON SFR determines whether this bit acts as SM0 or as FE. The operation of SM0 is described below. When used as FE, this bit will be set to indicate an invalid stop bit. This bit must be manually cleared in software to clear the FE condition.
6	SM1	Serial Port mode select bit 1. See table below.
5	SM2	Multiprocessor communication mode enable. The function of this bit is dependent on the serial port mode. Mode 0: No effect. Mode 1: Checking valid stop bit. 0 = Reception is always valid no matter the logic level of stop bit. 1 = Reception is ignored if the received stop bit is not logic 1. Mode 2 or 3: For multiprocessor communication. 0 = Reception is always valid no matter the logic level of the 9th bit. 1 = Reception is ignored if the received 9th bit is not logic 1.
4	REN	Receive enable: 0: Disable serial reception. 1: Enable serial reception.
3	TB8	This is the 9th bit to be transmitted in modes 2 and 3. This bit is set and cleared by software as desired.
2	RB8	In modes 2 and 3 this is the received 9th data bit. In mode 1, if SM2 = 0, RB8 is the stop bit that was received. In mode 0 it has no function.
1	TI	Transmit interrupt flag: This flag is set by hardware at the end of the 8th bit time in mode 0, or at the beginning of the stop bit in all other modes during serial transmission. This bit must be cleared by software.
0	RI	Receive interrupt flag: This flag is set by hardware at the end of the 8th bit time in mode 0, or halfway through the stop bits time in the other modes during serial reception. However the restrictions of SM2 apply to this bit. This bit can be cleared only by software.

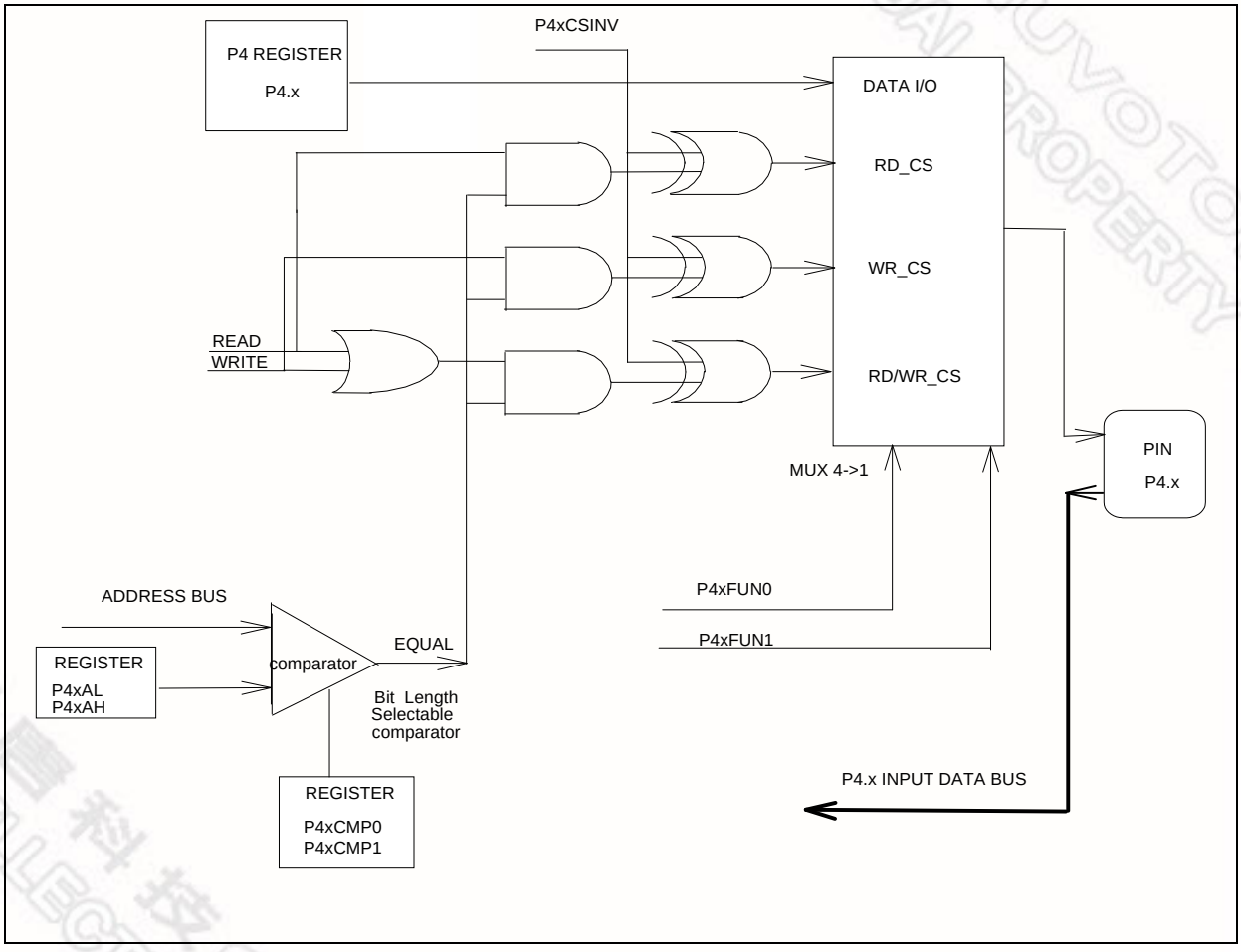
SM1, SM0: Mode Select bits:

Mode	SM0	SM1	Description	Length	Baud Rate
0	0	0	Synchronous	8	Tclk divided by 4 or 12
1	0	1	Asynchronous	10	Variable
2	1	0	Asynchronous	11	Tclk divided by 32 or 64
3	1	1	Asynchronous	11	Variable

Here is an example to program the P4.0 as a write strobe signal at the I/O port address 1234H ~1237H and positive polarity, and P4.1~P4.3 are used as general I/O ports.

```
MOV  P40AH,#12H
MOV  P40AL,#34H              ;Define the base I/O address 1234H for P4.0 as an special function
MOV  P4CONA,#00001010B       ;Define the P4.0 as a write strobe signal pin and the comparator
MOV  P4CONB,#00H             ;P4.1~P4.3 as general I/O port which are the same as PORT1
MOV  P2ECON,#10H             ;Write the P40SINV =1 to inverse the P4.0 write strobe polarity
                             ;default is negative.
```

Then any instruction MOVX @DPTR,A (with DPTR=1234H~1237H) will generate the positive polarity write strobe signal at pin P4.0 . And the instruction MOV P4,#XX will output the bit3 to bit1 of data #XX to pin P4.3~ P4.1.



The Port 4 Structure Diagram

ACCUMULATOR

Bit:	7	6	5	4	3	2	1	0

ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0

Mnemonic: ACC Address: E0h

Bit	Name	Function
7-0	ACC	The A or ACC register is the standard 8052 accumulator.

B Register

Bit:	7	6	5	4	3	2	1	0
	B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0

Mnemonic: B Address: F0h

Bit	Name	Function
7-0	B	The B register is the standard 8052 register that serves as a second accumulator.

Chip Enable Register

Bit:	7	6	5	4	3	2	1	0
	CHPENR.7	CHPENR.6	CHPENR.5	CHPENR.4	CHPENR.3	CHPENR.2	CHPENR.1	CHPENR.0

Mnemonic: CHPENR Address: F6h

The CHPCON is read only by default .You must write #87,#59H sequentially to this special register CHPENR to enable the CHPCON write attribute, and write other value to disable CHPCON write attribute. This register protects from writing to the CHPCON register carelessly.

Op-code	HEX Code	Bytes	W78E516D/W78E058D series Clock cycles
SUBB A, R5	9D	1	12
SUBB A, R6	9E	1	12
SUBB A, R7	9F	1	12
SUBB A, @R0	96	1	12
SUBB A, @R1	97	1	12
SUBB A, direct	95	2	12
SUBB A, #data	94	2	12
INC A	04	1	12
INC R0	08	1	12
INC R1	09	1	12
INC R2	0A	1	12
INC R3	0B	1	12
INC R4	0C	1	12
INC R5	0D	1	12
INC R6	0E	1	12
INC R7	0F	1	12
INC @R0	06	1	12
INC @R1	07	1	12
INC direct	05	2	12
INC DPTR	A3	1	24
DEC A	14	1	12
DEC R0	18	1	12
DEC R1	19	1	12
DEC R2	1A	1	12
DEC R3	1B	1	12
DEC R4	1C	1	12
DEC R5	1D	1	12
DEC R6	1E	1	12
DEC R7	1F	1	12
DEC @R0	16	1	12
DEC @R1	17	1	12
DEC direct	15	2	12
MUL AB	A4	1	48
DIV AB	84	1	48

Op-code	HEX Code	Bytes	W78E516D/W78E058D series Clock cycles
DA A	D4	1	12
ANL A, R0	58	1	12
ANL A, R1	59	1	12
ANL A, R2	5A	1	12
ANL A, R3	5B	1	12
ANL A, R4	5C	1	12
ANL A, R5	5D	1	12
ANL A, R6	5E	1	12
ANL A, R7	5F	1	12
ANL A, @R0	56	1	12
ANL A, @R1	57	1	12
ANL A, direct	55	2	12
ANL A, #data	54	2	12
ANL direct, A	52	2	12
ANL direct, #data	53	3	24
ORL A, R0	48	1	12
ORL A, R1	49	1	12
ORL A, R2	4A	1	12
ORL A, R3	4B	1	12
ORL A, R4	4C	1	12
ORL A, R5	4D	1	12
ORL A, R6	4E	1	12
ORL A, R7	4F	1	12
ORL A, @R0	46	1	12
ORL A, @R1	47	1	12
ORL A, direct	45	2	12
ORL A, #data	44	2	12
ORL direct, A	42	2	12
ORL direct, #data	43	3	24
XRL A, R0	68	1	12
XRL A, R1	69	1	12
XRL A, R2	6A	1	12
XRL A, R3	6B	1	12

Op-code	HEX Code	Bytes	W78E516D/W78E058D series Clock cycles
CJNE R6, #data, rel	BE	3	24
CJNE R7, #data, rel	BF	3	24
DJNZ R0, rel	D8	2	24
DJNZ R1, rel	D9	2	24
DJNZ R5, rel	DD	2	24
DJNZ R2, rel	DA	2	24
DJNZ R3, rel	DB	2	24
DJNZ R4, rel	DC	2	24
DJNZ R6, rel	DE	2	24
DJNZ R7, rel	DF	2	24
DJNZ direct, rel	D5	3	24

Table 10-1: Instruction Set for W78E516D/W78E058D

Interrupts

The W78E516D/W78E058D has a 2 priority level interrupt structure with 8 interrupt sources. Each of the interrupt sources has an individual priority bit, flag, interrupt vector and enable bit. In addition, the interrupts can be globally enabled or disabled.

13.2 Interrupt Sources

The External Interrupts $\overline{INT0}$ and $\overline{INT1}$ can be either edge triggered or level triggered, depending on bits IT0 and IT1. The bits IE0 and IE1 in the TCON register are the flags which are checked to generate the interrupt. In the edge triggered mode, the INTx inputs are sampled in every machine cycle. If the sample is high in one cycle and low in the next, then a high to low transition is detected and the interrupts request flag IEx in TCON is set. The flag bit requests the interrupt. Since the external interrupts are sampled every machine cycle, they have to be held high or low for at least one complete machine cycle. The IEx flag is automatically cleared when the service routine is called. If the level triggered mode is selected, then the requesting source has to hold the pin low till the interrupt is serviced. The IEx flag will not be cleared by the hardware on entering the service routine. If the interrupt continues to be held low even after the service routine is completed, then the processor may acknowledge another interrupt request from the same source. Note that the external interrupts $\overline{INT2}$ and $\overline{INT3}$. By default, the individual interrupt flag corresponding to external interrupt 2 to 3 must be cleared manually by software.

The Timer 0 and 1 Interrupts are generated by the TF0 and TF1 flags. These flags are set by the overflow in the Timer 0 and Timer 1. The TF0 and TF1 flags are automatically cleared by the hardware when the timer interrupt is serviced. The Timer 2 interrupt is generated by a logical OR of the TF2 and the EXF2 flags. These flags are set by overflow or capture/reload events in the timer 2 operation. The hardware does not clear these flags when a timer 2 interrupt is executed. Software has to resolve the cause of the interrupt between TF2 and EXF2 and clear the appropriate flag.

The Serial block can generate interrupts on reception or transmission. There are two interrupt sources from the Serial block, which are obtained by the RI and TI bits in the SCON SFR. These bits are not automatically cleared by the hardware, and the user will have to clear these bits using software.

All the bits that generate interrupts can be set or reset by hardware, and thereby software initiated interrupts can be generated. Each of the individual interrupts can be enabled or disabled by setting or clearing a bit in the IE SFR. IE also has a global enable/disable bit EA, which can be cleared to disable all the interrupts, at once.

Source	Vector Address	Source	Vector Address
External Interrupt 0	0003h	Timer 0 Overflow	000Bh
External Interrupt 1	0013h	Timer 1 Overflow	001Bh
Serial Port	0023h	Timer 2 Overflow	002Bh
External Interrupt 2	0033h	External Interrupt 3	003Bh

Table 13- 1 W78E516D/W78E058D interrupt vector table

13.3 Priority Level Structure

There are two priority levels for the interrupts high, low. The interrupt sources can be individually set to either high or low levels. Naturally, a higher priority interrupt cannot be interrupted by a lower priority interrupt. However there exists a pre-defined hierarchy amongst the interrupts themselves. This hierarchy comes into play when the interrupt controller has to resolve simultaneous requests having the same priority level. This hierarchy is defined as shown on Table.

Table below summarizes the interrupt sources, flag bits, vector addresses, enable bits, priority bits, arbitration ranking, and external interrupt may wake up the CPU from Power Down mode.

Source	Flag	Vector address	Enable bit	Flag cleared by	Arbitration ranking	Power-down wakeup
External Interrupt 0	IE0	0003H	EX0 (IE.0)	Hardware, software	1(highest)	Yes
Timer 0 Overflow	TF0	000BH	ET0 (IE.1)	Hardware, software	2	No
External Interrupt 1	IE1	0013H	EX1 (IE.2)	Hardware, software	3	Yes
Timer 1 Overflow	TF1	001BH	ET1 (IE.3)	Hardware, software	4	No
Serial Port	RI + TI	0023H	ES (IE.4)	Software	5	No
Timer 2 Over-flow/Match	TF2	002BH	ET2 (IE.5)	Software	6	No
External Interrupt 2	XICON	0033H	EX2 (XICON.2)	Hardware, software	7	Yes
External Interrupt 3	XICON	003BH	EX3 (XICON.6)	Hardware, software	8(lowest)	Yes

Table 13- 2 Summary of interrupt sources

13.4 Interrupt Response Time

The response time for each interrupt source depends on several factors, such as the nature of the interrupt and the instruction underway. In the case of external interrupts $\overline{INT0}$ and $\overline{INT1}$, they are sampled at S5P2 of every machine cycle and then their corresponding interrupt flags IEx will be set or reset. The Timer 0 and 1 overflow flags are set at C3 of the machine cycle in which overflow has occurred. These flag values are polled only in the next machine cycle. If a request is active and all three conditions are met, then the hardware generated LCALL is executed. This LCALL itself takes four machine cycles to be completed. Thus there is a minimum time of five machine cycles between the interrupt flag being set and the interrupt service routine being executed.

A longer response time should be anticipated if any of the three conditions are not met. If a higher or equal priority is being serviced, then the interrupt latency time obviously depends on the nature of the service routine currently being executed. If the polling cycle is not the last machine cycle of the instruction being executed, then an additional delay is introduced. The maximum response time (if no other interrupt is in service) occurs if the device is performing a write to IE, IP and then executes a MUL or DIV instruction.

13.5 Interrupt Inputs

Since the external interrupt pins are sampled once each machine cycle, an input high or low should hold for at least 6 CPU Clocks to ensure proper sampling. If the external interrupt is high for at least

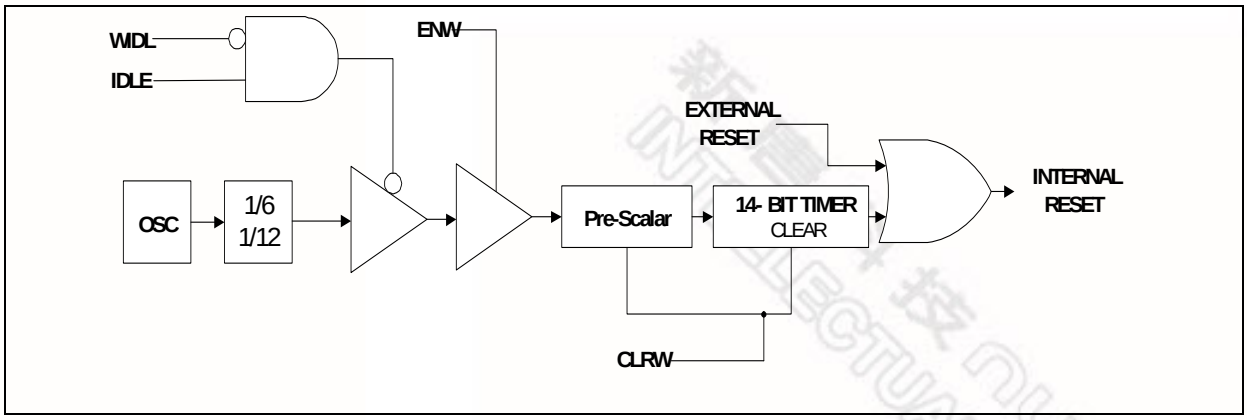


Figure 15- 1 Watchdog Timer Block Diagram

Typical Watch-Dog time-out period when OSC = 20 MHz

PS2	PS1	PS0	Watchdog time-out period
0	0	0	19.66 mS
0	0	1	39.32 mS
0	1	0	78.64 mS
0	1	1	157.28 mS
1	0	0	314.57 mS
1	0	1	629.14 mS
1	1	0	1.25 S
1	1	1	2.50 S

Table 15- 1 Watch-Dog time-out period

The 16 states of the counter effectively divide the bit time into 16 slices. The bit detection is done on a best of three basie. The bit detector samples the RxD pin, at the 8th, 9th and 10th counter states. By using a majority 2 of 3 voting system, the bit value is selected. This is done to improve the noise rejection feature of the serial port. If the first bit detected after the falling edge of RxD pin is not 0, then this indicates an invalid start bit, and the reception is immediately aborted. The serial port again looks for a falling edge in the RxD line. If a valid start bit is detected, then the rest of the bits are also detected and shifted into the SBUF.

After shifting in 8 data bits, there is one more shift to do, after which the SBUF and RB8 are loaded and RI is set. However certain conditions must be met before the loading and setting of RI can be done.

1. RI must be 0 and
2. Either SM2 = 0, or the received stop bit = 1.

If these conditions are met, then the stop bit goes to RB8, the 8 data bits go into SBUF and RI is set. Otherwise the received frame may be lost. After the middle of the stop bit, the receiver goes back to looking for a 1-to-0 transition on the RxD pin.

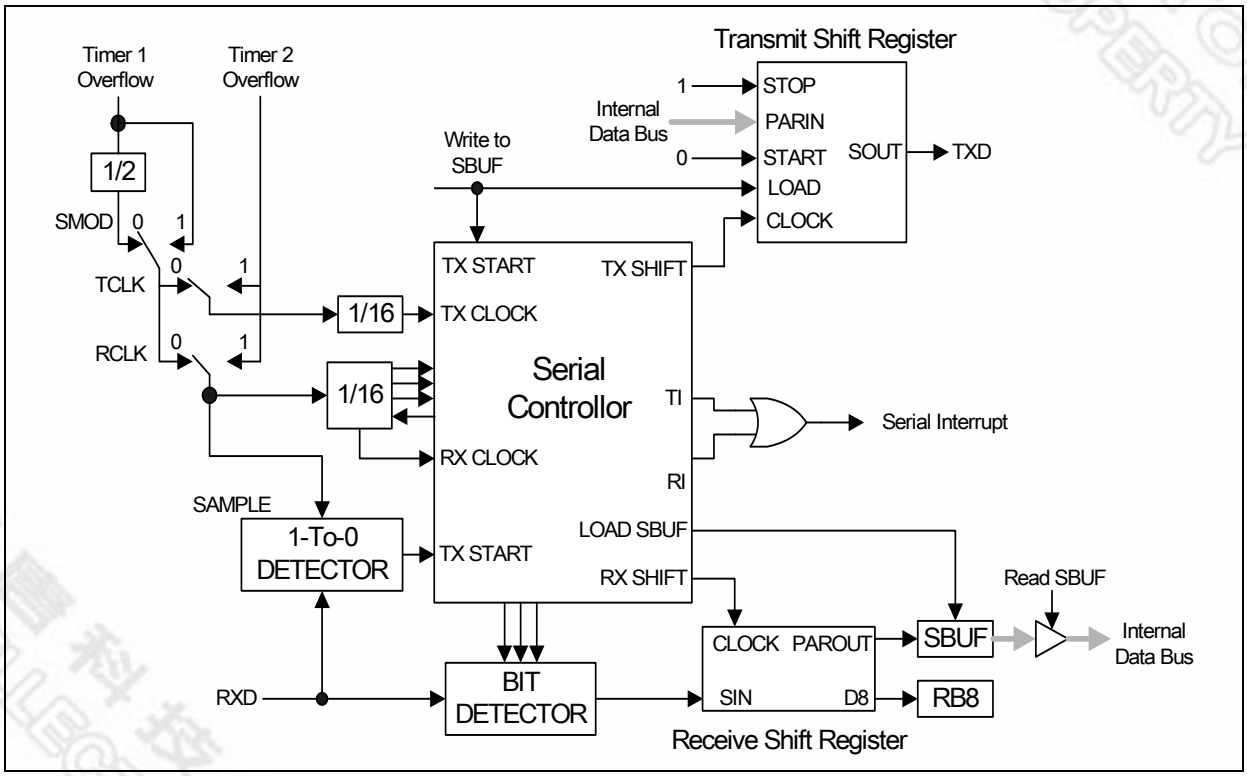


Figure 16- 2 Serial port mode 1

16.3 MODE 2

This mode uses a total of 11 bits in asynchronous full-duplex communication. The functional description is shown in the figure below. The frame consists of one start bit (0), 8 data bits (LSB first), a pro-

1	0	2	Asynch.	32 or 64 TCLKS	11 bits	1	1	0, 1
1	1	3	Asynch.	Timer 1 or 2	11 bits	1	1	0, 1

Table 16- 1 Serial Ports Modes

18 ISP(IN-SYSTEM PROGRAMMING)

ISP is the ability of programmable MCU to be programmed while F/W code in AP-ROM or LD-ROM (ISP work voltage 3.3-5.5V).

The W78E058D/516D equips one 32K byte of main ROM bank for application program (called APROM) and one 4K byte of auxiliary ROM bank for loader program (called LDROM). In the normal operation, the microcontroller executes the code in the APROM. If the content of APROM needs to be modified, the W78E058D/516D allows user to activate the In-System Programming (ISP) mode by setting the CHPCON register. **The CHPCON is read-only by default, software must write two specific values 87H, then 59H sequentially to the CHPENR register to enable the CHPCON write attribute. Writing CHPENR register with the values except 87H and 59H will close CHPCON register write attribute.** The W78E058D/516D achieves all in-system programming operations including enter/exit ISP Mode, program, erase, read ... etc, during device in the idle mode. Setting the bit CHPCON.0 the device will enter in-system programming mode after a wake-up from idle mode. Because device needs proper time to complete the ISP operations before awaken from idle mode, software may use timer interrupt to control the duration for device wake-up from idle mode. To perform ISP operation for revising contents of APROM, software located at APROM setting the CHPCON register then enter idle mode, after awaken from idle mode the device executes the corresponding interrupt service routine in LDROM. Because the device will clear the program counter while switching from APROM to LDROM, the first execution of RETI instruction in interrupt service routine will jump to 00H at LDROM area. The device offers a software reset for switching back to APROM while the content of APROM has been updated completely. **Setting CHPCON register bit 0, 1 and 7 to logic-1 will result a software reset to reset the CPU**. The software reset serves as a external reset. This in-system programming feature makes the job easy and efficient in which the application needs to update firmware frequently. In some applications, the in-system programming feature make it possible to easily update the system firmware without opening the chassis.

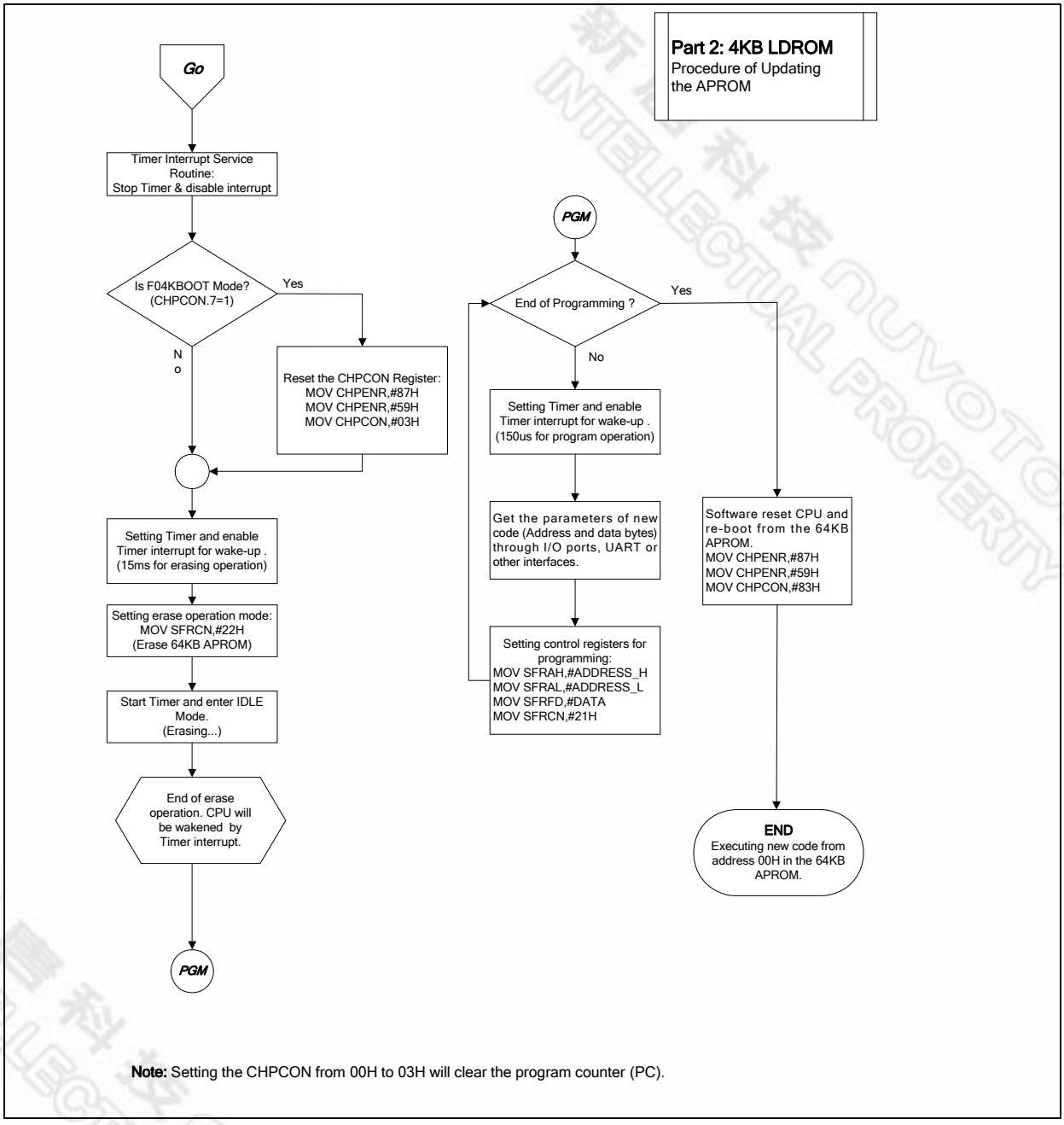
SFRAH, SFRAL: The objective address of on-chip ROM in the in-system programming mode. SFRAH contains the high-order byte of address, SFRAL contains the low-order byte of address.

SFRFD: The programming data for on-chip ROM in programming mode.

SFRCN: The control byte of on-chip ROM programming mode.

SFRCN (C7)

BIT	NAME	FUNCTION
7	-	Reserve.
6	WFWIN	On-chip ROM bank select for in-system programming. 0: 32K/64K bytes ROM bank is selected as destination for re-programming. 1: 4K bytes ROM bank is selected as destination for re-programming.
5	OEN	ROM output enable.
4	CEN	ROM chip enable.
3, 2, 1, 0	CTRL [3:0]	The flash control signals



Note: Setting the CHPCON from 00H to 03H will clear the program counter (PC).

19 CONFIG BITS

During the on-chip Flash EPROM operation mode, the Flash EPROM can be programmed and verified repeatedly. Until the code inside the Flash EPROM is confirmed OK, the code can be protected. The protection of Flash EPROM and those operations on it are described below.

The W78E516D/W78E058D has several Special Setting Registers, including the Security Register and Company/Device ID Registers, which can not be accessed in programming mode. Those bits of the Security Registers can not be changed once they have been programmed from high to low. They

21.2 D.C. ELECTRICAL CHARACTERISTICS

T_A=-40℃~+85℃, V_{DD}=2.4V~5.5V, V_{SS}=0V

Sym	Parameter	Test Condition	Min	Typ[*1]	Max	Unit
V_{IL}	Input Low Voltage (Ports 0~4, /EA, XTAL1, RST)	2.4 < V_{DD} < 5.5V	-0.5		0.2V_{DD}-0.1	V
V_{IH}	Input High Voltage (Ports 0~4, /EA)	2.4 < V_{DD} < 5.5V	0.2V_{DD} +0.9		V_{DD}+ 0.5	V
V_{IH1}	Input High Voltage (XTAL1, RST)	2.4 < V_{DD} < 5.5V	0.7V_{DD}		V_{DD}+ 0.5	V
V_{OL}	Output Low Voltage (Ports 0~4, ALE, /PSEN)	V_{DD}=4.5V, I_{OL}= 12.0mA[*3,*4] V_{DD}=2.4V, I_{OL}= 8.0mA[*3,*4]			0.4	V
V_{OH1}	Output High Voltage (Ports 1~4)	V_{DD}=4.5V, I_{OH}= -300μA[*4] V_{DD}=2.4V, I_{OH}= -20μA[*4]	2.4 2.0			V
V_{OH2}	Output High Voltage (Ports 0 & 2 in external bus mode, ALE, /PSEN)	V_{DD}=4.5V, I_{OH}= -8.0mA[*4] V_{DD}=2.4V, I_{OH}= -2.0mA[*4]	2.4 2.0			V
I_{IL}	Logical 0 Input Current (Ports 1~4)	V_{DD}=5.5V, V_{IN}=0.4V		-45	-50	μA
I_{TL}	Logical 1-to-0 Transition Current (Ports 1~4)	V_{DD}=5.5V, V_{IN}=2.0V[*2]		-510	-650	μA
I_{LI}	Input Leakage Current (Port 0)	0 < V_{IN} < V_{DD}+0.5		±1.0	±10	μA
I_{DD}	Power Supply Current	Active mode[*5] @12MHz, V_{DD}=5.0V @40MHz, V_{DD}=5.0V @12MHz, V_{DD}=3.3V @20MHz, V_{DD}=3.3V		 10.4 18.2 3.6 4.4		mA
		Idle mode @12MHz, V_{DD}=5.0V @40MHz, V_{DD}=5.0V @12MHz, V_{DD}=3.3V @20MHz, V_{DD}=3.3V		 3.4 10.3 1.3 1.9		mA
		Power-down mode		<1	50	μA

```
                MOV         TL0,R6
                MOV         TH0,R7

BLANK_CHECK_LOOP:

                SETB        TR0                     ;ENABLE TIMER 0
                MOV         PCON,#01H               ;ENTER IDLE MODE
                MOV         A,SFRFD                 ;READ ONE BYTE

                CJNE        A,#FFH,BLANK_CHECK_ERROR
                INC         SFRAL                   ;NEXT ADDRESS
                MOV         A,SFRAL
                JNZ         BLANK_CHECK_LOOP
                INC         SFRAH
                MOV         A,SFRAH
                CJNE        A,#C0H,BLANK_CHECK_LOOP   ;END ADDRESS=BFFFH
               JMP          PROGRAM_ROM

BLANK_CHECK_ERROR:

                MOV         P1,#F0H
                MOV         P3,#F0H
                JMP         $

;*******************************************************************************
;* RE-PROGRAMMING APROM BANK
;*******************************************************************************
PROGRAM_ROM:

                MOV         DPTR,#0H                ;THE ADDRESS OF NEW ROM CODE
                MOV         R2,#00H                 ;TARGET LOW BYTE ADDRESS
                MOV         R1,#00H                 ;TARGET HIGH BYTE ADDRESS
                MOV         DPTR,#0H                ;EXTERNAL SRAM BUFFER ADDRESS
                MOV         SFRAH,R1                ;SFRAH, TARGET  HIGH ADDRESS
                 MOV        SFRCN,#21H              ;SFRCN(C7H)=21  (PROGRAM )
                MOV         R6,#0CH                 ;SET TIMER FOR PROGRAMMING, ABOUT 150us.
                MOV         R7,#FEH
                MOV         TL0,R6
                MOV         TH0,R7
PROG_D_:
                MOV         SFRAL,R2                ;SFRAL(C4H)= LOW BYTE ADDRESS
                MOVX        A,@DPTR                 ;READ DATA FROM EXTERNAL SRAM BUFFER
                MOV         SFRFD,A                 ;SFRFD(C6H)=DATA IN
                MOV         TCON,#10H               ;TCON=10H,TR0=1,GO
                MOV         PCON,#01H               ;ENTER IDLE MODE( PRORGAMMING)
                INC         DPTR
                INC         R2
                CJNE        R2,#0H,PROG_D_
                INC         R1
                MOV         SFRAH,R1
                CJNE        R1,#C0H,PROG_D_
;*******************************************************************************
; * VERIFY APROM BANK
;*******************************************************************************
                MOV         R4,#03H                 ;ERROR COUNTER
                MOV         R6,#FBH                 ;SET TIMER FOR READ VERIFY, ABOUT 1.5us.
                MOV         R7,#FFH
```

```
                MOV         TL0,R6
                MOV         TH0,R7
                MOV         DPTR,#0H                ;The start address of sample code
                MOV         R2,#0H                  ;Target  low byte address
                MOV         R1,#0H                  ;Target  high byte address
                MOV         SFRAH,R1                ;SFRAH, Target high address
                MOV         SFRCN,#00H              ;SFRCN=00 (Read ROM CODE)
READ_VERIFY_:
                MOV         SFRAL,R2                ;SFRAL(C4H)= LOW ADDRESS
                MOV         TCON,#10H               ;TCON=10H,TR0=1,GO
                MOV         PCON,#01H
                INC         R2
                MOVX        A,@DPTR
                INC         DPTR
                CJNE        A,SFRFD,ERROR_
                CJNE        R2,#0H,READ_VERIFY_
                INC         R1
                MOV         SFRAH,R1
                CJNE        R1,#C0H,READ_VERIFY_

;*******************************************************************************
;* PROGRAMMING COMPLETLY, SOFTWARE RESET CPU
;*******************************************************************************
                MOV         CHPENR,#87H             ;CHPENR=87H
                MOV         CHPENR,#59H             ;CHPENR=59H
                MOV         CHPCON,#83H             ;CHPCON=83H, SOFTWARE RESET.


ERROR_:
                DJNZ        R4,UPDATE_              ;IF ERROR OCCURS, REPEAT 3 TIMES.
        .                                           ;IN-SYSTEM PROGRAMMING FAIL, USER'S
                                                   ;PROCESS TO DEAL WITH IT.
```

23 REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A01	June 24, 2008	-	Initial Issued
A02	August 21,2008	7,8	Update pin assignment.
A03	September 1,2008	-	Update W78I516D/W78I058D parts
A04	November 3,2008		Update DC table typo error
A05	January 7,2009	74	Update V_{IL} and V_{IH} .
A06	April 2, 2009	- - -	Update DC table Revise some typing errors Rename SFR 86H POR register to P0UPR
A07	April 22,2009	70	Revise the Application Circuit
A08	June 30,2009	6 65 70 71	1. Revise the Table 3-1 2. Add the picture for “F04KBOOT Mode” of P4.3 3. Revise the ISP Flow Chart 4. Revise the CONFIG BITS 5. Remove the “Preliminary” character each page
A09	Feb 15,2011	18 65 70 79	1. Revise the default reset value for CHPCON 2. Add the reset-pin reset can entry the F04KBOOT mode. 3. Revise the flow chart of ISP programming 4. Revise the CONFIG BITS 5. Add the external reset pin timing