Nuvoton Technology Corporation - W78E058DPG Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8052
Core Size	8-Bit
Speed	40MHz
Connectivity	EBI/EMI, UART/USART
Peripherals	POR, WDT
Number of I/O	36
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/w78e058dpg

2 FEATURES

- Fully static design 8-bit CMOS microcontroller
- Optional 12T or 6T mode
  - 12T Mode, 12 clocks per machine cycle operation (default), Speed up to 40 MHz/5V
  - 6T Mode, 6 clocks per machine cycle operation set by the writer, Speed up to 20 MHz/5V
- Wide supply voltage of 2.4 to 5.5V
- Temperature grade is (-40°C~85°C)
- 64K/32K bytes of in-system programmable FLASH EPROM for Application Program (APROM)
- 4K bytes of auxiliary FLASH EPROM for Loader Program (LDROM)
- Low standby current at full supply voltage
- 512 bytes of on-chip RAM. (include 256 bytes of AUX-RAM, software selectable)
- 64K bytes program memory address space and 64K bytes data memory address space
- One 4-bit multipurpose programmable port, additional $\overline{INT2}$ / $\overline{INT3}$
- Support Watch Dog Timer
- Three 16-bit timer/counters
- One full duplex serial port
- 8-sources, 2-level interrupt capability
- Software Reset
- Built-in power management with idle mode and power down mode
- Code protection
- Packages:
  - Lead Free (RoHS) DIP 40: W78E516DDG
  - Lead Free (RoHS) PLCC 44: W78E516DPG
  - Lead Free (RoHS) PQFP 44: W78E516DFG
  - Lead Free (RoHS) LQFP 48: W78E516DLG
  - Lead Free (RoHS) DIP 40: W78E058DDG
  - Lead Free (RoHS) PLCC 44: W78E058DPG
  - Lead Free (RoHS) PQFP 44: W78E058DFG
  - Lead Free (RoHS) LQFP 48: W78E058DLG

8 MEMORY ORGANIZATION

The W78E516D/W78E058D series separate the memory into two separate sections, the Program Memory and the Data Memory. The Program Memory is used to store the instruction op-codes, while the Data Memory is used to store data or for memory mapped devices.

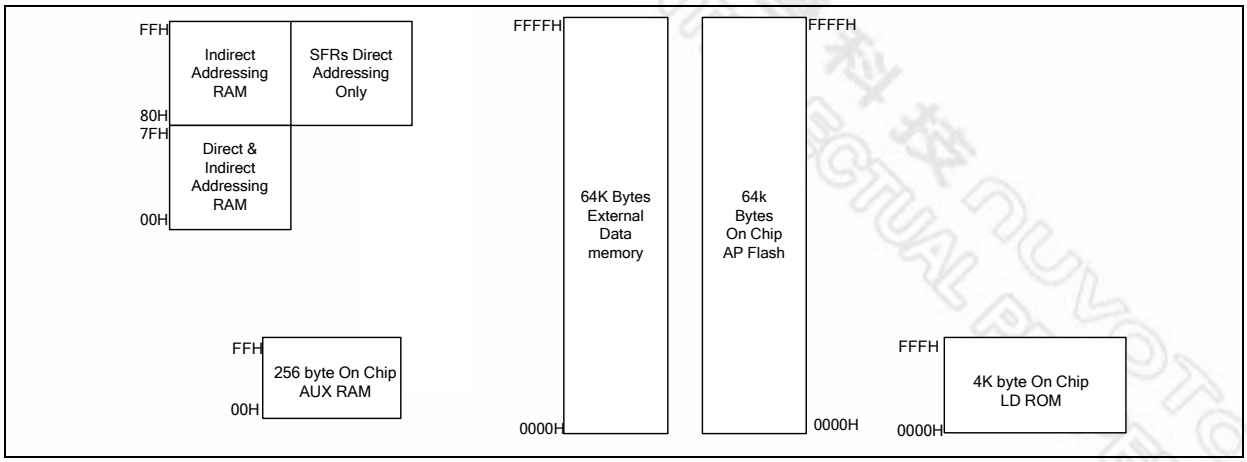


Figure 8- 1 Memory Map

8.1 Program Memory (on-chip Flash)

The Program Memory on the W78E516D/W78E058D series can be up to 64K/32K bytes long. All instructions are fetched for execution from this memory area. The MOVC instruction can also access this memory region.

8.2 Scratch-pad RAM and Register Map

As mentioned before the W78E516D/W78E058D series have separate Program and Data Memory areas. There are also several Special Function Registers (SFRs) which can be accessed by software. The SFRs can be accessed only by direct addressing, while the on-chip RAM can be accessed by either direct or indirect addressing.

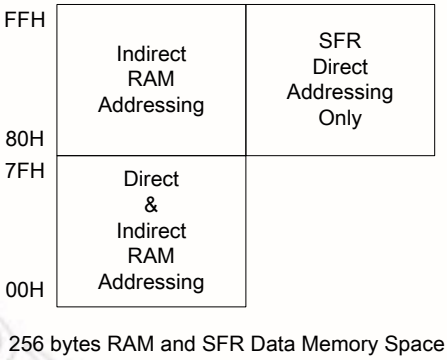


Figure 8- 2 W78E516D/W78E058D RAM and SFR Memory Map

9 SPECIAL FUNCTION REGISTERS

The W78E516D/W78E058D series uses Special Function Registers (SFRs) to control and monitor peripherals and their Modes. The SFRs reside in the register locations 80-FFh and are accessed by direct addressing only. Some of the SFRs are bit addressable. This is very useful in cases where users wish to modify a particular bit without changing the others. The SFRs that are bit addressable are those whose addresses end in 0 or 8. The W78E516D/W78E058D series contain all the SFRs present in the standard 8052. However some additional SFRs are added. In some cases the unused bits in the original 8052, have been given new functions. The list of the SFRs is as follows.

W78E516D/W78E058D Special Function Registers (SFRs) and Reset Values

F8									FF
F0	+B						CHPENR		F7
E8									EF
E0	+ACC								E7
D8	+P4								DF
D0	+PSW								D7
C8	+T2CON		RCAP2L	RCAP2H	TL2	TH2			CF
C0	+XICON		P4CONA	P4CONB	**SFRAL**	**SFRAH**	SFRFD	SFRCN	C7
B8	+IP							CHPCON	BF
B0	+P3				**P43AL**	**P43AH**			B7
A8	+IE				**P42AL**	**P42AH**	P2ECON		AF
A0	+P2								A7
98	+SCON	SBUF							9F
90	+P1				**P41AL**	**P41AH**			97
88	+TCON	TMOD	TL0	TL1	TH0	TH1	AUXR	WDTC	8F
80	+P0	SP	DPL	DPH	**P40AL**	**P40AH**	P0UPR	PCON	87

Figure 9-1: Special Function Register Location Table

Note: 1.The SFRs marked with a plus sign(+) are both byte- and bit-addressable.
2. The text of SFR with bold type characters are extension function registers.

Serial Port Control

Bit:	7	6	5	4	3	2	1	0
	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI

Mnemonic: SCON Address: 98h

BIT	NAME	FUNCTION
7	SM0/FE	Serial port mode select bit 0 or Framing Error Flag: The SMOD0 bit in PCON SFR determines whether this bit acts as SM0 or as FE. The operation of SM0 is described below. When used as FE, this bit will be set to indicate an invalid stop bit. This bit must be manually cleared in software to clear the FE condition.
6	SM1	Serial Port mode select bit 1. See table below.
5	SM2	Multiprocessor communication mode enable. The function of this bit is dependent on the serial port mode. Mode 0: No effect. Mode 1: Checking valid stop bit. 0 = Reception is always valid no matter the logic level of stop bit. 1 = Reception is ignored if the received stop bit is not logic 1. Mode 2 or 3: For multiprocessor communication. 0 = Reception is always valid no matter the logic level of the 9th bit. 1 = Reception is ignored if the received 9th bit is not logic 1.
4	REN	Receive enable: 0: Disable serial reception. 1: Enable serial reception.
3	TB8	This is the 9th bit to be transmitted in modes 2 and 3. This bit is set and cleared by software as desired.
2	RB8	In modes 2 and 3 this is the received 9th data bit. In mode 1, if SM2 = 0, RB8 is the stop bit that was received. In mode 0 it has no function.
1	TI	Transmit interrupt flag: This flag is set by hardware at the end of the 8th bit time in mode 0, or at the beginning of the stop bit in all other modes during serial transmission. This bit must be cleared by software.
0	RI	Receive interrupt flag: This flag is set by hardware at the end of the 8th bit time in mode 0, or halfway through the stop bits time in the other modes during serial reception. However the restrictions of SM2 apply to this bit. This bit can be cleared only by software.

SM1, SM0: Mode Select bits:

Mode	SM0	SM1	Description	Length	Baud Rate
0	0	0	Synchronous	8	Tclk divided by 4 or 12
1	0	1	Asynchronous	10	Variable
2	1	0	Asynchronous	11	Tclk divided by 32 or 64
3	1	1	Asynchronous	11	Variable

BIT	NAME	FUNCTION
7-0	P42AL.[7:0]	The Base address register for comparator of P4.2. P42AL contains the low-order byte of address.

P4.2 Base Address High Byte Register

Bit:	7	6	5	4	3	2	1	0
	P42AH.7	P42AH.6	P42AH.5	P42AH.4	P42AH.3	P42AH.2	P42AH.1	P42AH.0

Mnemonic:P42AH Address: ADh

BIT	NAME	FUNCTION
7-0	P42AH.[7:0]	The Base address register for comparator of P4.2. P42AH contains the High-order byte of address.

Port 2 Expanded Control

Bit:	7	6	5	4	3	2	1	0
	P43CSIN	P42CSIN	P41CSIN	P40CSIN	-	-	-	-

Mnemonic: P2ECON Address:AEh

BIT	NAME	FUNCTION
7	P43CSINV	The active polarity of P4.3 when pin P4.3 is defined as read and/or write strobe signal. 1 : P4.3 is active high when pin P4.3 is defined as read and/or write strobe signal. 0 : P4.3 is active low when pin P4.3 is defined as read and/or write strobe signal.
6	P42CSINV	The similarity definition as P43SINV.
5	P41CSINV	The similarity definition as P43SINV.
4	P40CSINV	The similarity definition as P43SINV.

Port 3

Bit:	7	6	5	4	3	2	1	0
	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0

Mnemonic: P3 Address: B0h

P3.7-0: General purpose Input/Output port. Most instructions will read the port pins in case of a port read access, however in case of read-modify-write instructions, the port latch is read. These alternate functions are described below:

BIT	NAME	FUNCTION
7	P3.7	$\overline{RD}$
6	P3.6	$\overline{WR}$
5	P3.5	T1
4	P3.4	T0

(F04KMODE)				(MUST SET 0)	(MUST SET 0)		

Mnemonic: CHPCON Address: BFh

BIT	NAME	FUNCTION
7	SWRESET(F04KMODE)	When this bit is set to 1, and both FBOOTSL and FPROGEN are set to 1. It will enforce microcontroller reset to initial condition just like power on reset. This action will re-boot the microcontroller and start to normal operation. To read this bit can determine that the F04KBOOT mode is running.
4	ENAUXRAM	1: Enable on-chip AUX-RAM. 0: Disable the on-chip AUX-RAM
1	FBOOTSL	The Loader Program Location Select. 0: The Loader Program locates at the 64K/32K Byte flash memory bank. 1: The Loader Program locates at the 4KB flash memory bank.
0	FPROGEN	Flash EPROM Programming Enable 1: Enable. The microcontroller switches to the programming flash mode after entering the idle mode and waken up from interrupt. The microcontroller will execute the loader program while in on-chip programming mode. 0: Disable. The on-chip flash memory is read-only. In-system programmability is disabled.

External Interrupt Control

Bit:	7	6	5	4	3	2	1	0
	PX3	EX3	IE3	IT3	PX2	EX2	IE2	IT2

Mnemonic: XICON Address: C0h

BIT	NAME	FUNCTION
7	PX3	External interrupt 3 priority high if set
6	EX3	External interrupt 3 enable if set
5	IE3	If IT3 = 1, IE3 is set/cleared automatically by hardware when interrupt is detected/serviced
4	IT3	External interrupt 3 is falling-edge/low-level triggered when this bit is set/cleared by software
3	PX2	External interrupt 2 priority high if set
2	EX2	External interrupt 2 enable if set
1	IE2	If IT2 = 1, IE2 is set/cleared automatically by hardware when interrupt is detected/serviced
0	IT2	External interrupt 2 is falling-edge/low-level triggered when this bit is set/cleared by software

Port 4 control A

10 INSTRUCTION

The W78E516D/W78E058D series execute all the instructions of the standard 8052 family. The operations of these instructions, as well as their effects on flag and status bits, are exactly the same.

Op-code	HEX Code	Bytes	W78E516D/W78E058D series Clock cycles
NOP	00	1	12
ADD A, R0	28	1	12
ADD A, R1	29	1	12
ADD A, R2	2A	1	12
ADD A, R3	2B	1	12
ADD A, R4	2C	1	12
ADD A, R5	2D	1	12
ADD A, R6	2E	1	12
ADD A, R7	2F	1	12
ADD A, @R0	26	1	12
ADD A, @R1	27	1	12
ADD A, direct	25	2	12
ADD A, #data	24	2	12
ADDC A, R0	38	1	12
ADDC A, R1	39	1	12
ADDC A, R2	3A	1	12
ADDC A, R3	3B	1	12
ADDC A, R4	3C	1	12
ADDC A, R5	3D	1	12
ADDC A, R6	3E	1	12
ADDC A, R7	3F	1	12
ADDC A, @R0	36	1	12
ADDC A, @R1	37	1	12
ADDC A, direct	35	2	12
ADDC A, #data	34	2	12
SUBB A, R0	98	1	12
SUBB A, R1	99	1	12
SUBB A, R2	9A	1	12
SUBB A, R3	9B	1	12
SUBB A, R4	9C	1	12

Op-code	HEX Code	Bytes	W78E516D/W78E058D series Clock cycles
MOV R5, A	FD	1	12
MOV R6, A	FE	1	12
MOV R7, A	FF	1	12
MOV R0, direct	A8	2	24
MOV R1, direct	A9	2	24
MOV R2, direct	AA	2	24
MOV R3, direct	AB	2	24
MOV R4, direct	AC	2	24
MOV R5, direct	AD	2	24
MOV R6, direct	AE	2	24
MOV R7, direct	AF	2	24
MOV R0, #data	78	2	12
MOV R1, #data	79	2	12
MOV R2, #data	7A	2	12
MOV R3, #data	7B	2	12
MOV R4, #data	7C	2	12
MOV R5, #data	7D	2	12
MOV R6, #data	7E	2	12
MOV R7, #data	7F	2	12
MOV @R0, A	F6	1	12
MOV @R1, A	F7	1	12
MOV @R0, direct	A6	2	24
MOV @R1, direct	A7	2	24
MOV @R0, #data	76	2	12
MOV @R1, #data	77	2	12
MOV direct, A	F5	2	12
MOV direct, R0	88	2	24
MOV direct, R1	89	2	24
MOV direct, R2	8A	2	24
MOV direct, R3	8B	2	24
MOV direct, R4	8C	2	24
MOV direct, R5	8D	2	24
MOV direct, R6	8E	2	24

Op-code	HEX Code	Bytes	W78E516D/W78E058D series Clock cycles
MOV direct, R7	8F	2	24
MOV direct, @R0	86	2	24
MOV direct, @R1	87	2	24
MOV direct, direct	85	3	24
MOV direct, #data	75	3	24
MOV DPTR, #data 16	90	3	24
MOVC A, @A+DPTR	93	1	24
MOVC A, @A+PC	83	1	24
MOVX A, @R0	E2	1	24
MOVX A, @R1	E3	1	24
MOVX A, @DPTR	E0	1	24
MOVX @R0, A	F2	1	24
MOVX @R1, A	F3	1	24
MOVX @DPTR, A	F0	1	24
PUSH direct	C0	2	24
POP direct	D0	2	24
XCH A, R0	C8	1	12
XCH A, R1	C9	1	12
XCH A, R2	CA	1	12
XCH A, R3	CB	1	12
XCH A, R4	CC	1	12
XCH A, R5	CD	1	12
XCH A, R6	CE	1	12
XCH A, R7	CF	1	12
XCH A, @R0	C6	1	12
XCH A, @R1	C7	1	12
XCHD A, @R0	D6	1	12
XCHD A, @R1	D7	1	12
XCH A, direct	C5	2	24
CLR C	C3	1	12
CLR bit	C2	2	12
SETB C	D3	1	12
SETB bit	D2	2	12
CPL C	B3	1	12

Interrupts

The W78E516D/W78E058D has a 2 priority level interrupt structure with 8 interrupt sources. Each of the interrupt sources has an individual priority bit, flag, interrupt vector and enable bit. In addition, the interrupts can be globally enabled or disabled.

13.2 Interrupt Sources

The External Interrupts $\overline{INT0}$ and $\overline{INT1}$ can be either edge triggered or level triggered, depending on bits IT0 and IT1. The bits IE0 and IE1 in the TCON register are the flags which are checked to generate the interrupt. In the edge triggered mode, the INTx inputs are sampled in every machine cycle. If the sample is high in one cycle and low in the next, then a high to low transition is detected and the interrupts request flag IEx in TCON is set. The flag bit requests the interrupt. Since the external interrupts are sampled every machine cycle, they have to be held high or low for at least one complete machine cycle. The IEx flag is automatically cleared when the service routine is called. If the level triggered mode is selected, then the requesting source has to hold the pin low till the interrupt is serviced. The IEx flag will not be cleared by the hardware on entering the service routine. If the interrupt continues to be held low even after the service routine is completed, then the processor may acknowledge another interrupt request from the same source. Note that the external interrupts $\overline{INT2}$ and $\overline{INT3}$. By default, the individual interrupt flag corresponding to external interrupt 2 to 3 must be cleared manually by software.

The Timer 0 and 1 Interrupts are generated by the TF0 and TF1 flags. These flags are set by the overflow in the Timer 0 and Timer 1. The TF0 and TF1 flags are automatically cleared by the hardware when the timer interrupt is serviced. The Timer 2 interrupt is generated by a logical OR of the TF2 and the EXF2 flags. These flags are set by overflow or capture/reload events in the timer 2 operation. The hardware does not clear these flags when a timer 2 interrupt is executed. Software has to resolve the cause of the interrupt between TF2 and EXF2 and clear the appropriate flag.

The Serial block can generate interrupts on reception or transmission. There are two interrupt sources from the Serial block, which are obtained by the RI and TI bits in the SCON SFR. These bits are not automatically cleared by the hardware, and the user will have to clear these bits using software.

All the bits that generate interrupts can be set or reset by hardware, and thereby software initiated interrupts can be generated. Each of the individual interrupts can be enabled or disabled by setting or clearing a bit in the IE SFR. IE also has a global enable/disable bit EA, which can be cleared to disable all the interrupts, at once.

Source	Vector Address	Source	Vector Address
External Interrupt 0	0003h	Timer 0 Overflow	000Bh
External Interrupt 1	0013h	Timer 1 Overflow	001Bh
Serial Port	0023h	Timer 2 Overflow	002Bh
External Interrupt 2	0033h	External Interrupt 3	003Bh

Table 13- 1 W78E516D/W78E058D interrupt vector table

13.3 Priority Level Structure

There are two priority levels for the interrupts high, low. The interrupt sources can be individually set to either high or low levels. Naturally, a higher priority interrupt cannot be interrupted by a lower priority interrupt. However there exists a pre-defined hierarchy amongst the interrupts themselves. This hierarchy comes into play when the interrupt controller has to resolve simultaneous requests having the same priority level. This hierarchy is defined as shown on Table.

14 PROGRAMMABLE TIMERS/COUNTERS

The W78E516D/W78E058D series have Three 16-bit programmable timer/counters, a machine cycle equals 12 or 6 oscillator periods, and it depends on 12T mode or 6T mode that the user configured this device.

14.1 Timer/Counters 0 & 1

W78E516D/W78E058D has two 16-bit Timer/Counters. Each of these Timer/Counters has two 8 bit registers which form the 16 bit counting register. For Timer/Counter 0 they are TH0, the upper 8 bits register, and TL0, the lower 8 bit register. Similarly Timer/Counter 1 has two 8 bit registers, TH1 and TL1. The two can be configured to operate either as timers, counting machine cycles or as counters counting external inputs.

When configured as a "Timer", the timer counts clock cycles. The timer clock can be programmed to be thought of as 1/12 of the system clock. In the "Counter" mode, the register is incremented on the falling edge of the external input pin, T0 in case of Timer 0, and T1 for Timer 1. The T0 and T1 inputs are sampled in every machine cycle at C4. If the sampled value is high in one machine cycle and low in the next, then a valid high to low transition on the pin is recognized and the count register is incremented. Since it takes two machine cycles to recognize a negative transition on the pin, the maximum rate at which counting will take place is 1/24 of the master clock frequency. In either the "Timer" or "Counter" mode, the count register will be updated at C3. Therefore, in the "Timer" mode, the recognized negative transition on pin T0 and T1 can cause the count register value to be updated only in the machine cycle following the one in which the negative edge was detected.

The "Timer" or "Counter" function is selected by the "$C/\overline{T}$" bit in the TMOD Special Function Register. Each Timer/Counter has one selection bit for its own; bit 2 of TMOD selects the function for Timer/Counter 0 and bit 6 of TMOD selects the function for Timer/Counter 1. In addition each Timer/Counter can be set to operate in any one of four possible modes. The mode selection is done by bits M0 and M1 in the TMOD SFR.

14.2 Time-Base Selection

W78E516D/W78E058D provides users with two modes of operation for the timer. The timers can be programmed to operate like the standard 8051 family, counting at the rate of 1/12 of the clock speed. This will ensure that timing loops on W78E516D/W78E058D and the standard 8051 can be matched. This is the default mode of operation of the W78E516D/W78E058D timers.

14.2.1 Mode 0

In Mode 0, the timer/counter is a 13-bit counter. The 13-bit counter consists of THx (8 MSB) and the five lower bits of TLx (5 LSB). The upper three bits of TLx are ignored. The timer/counter is enabled when TRx is set and either GATE is 0 or $\overline{INTx}$ is 1. When $C/\overline{T}$ is 0, the timer/counter counts clock cycles; when $C/\overline{T}$ is 1, it counts falling edges on T0 (Timer 0) or T1 (Timer 1). For clock cycles, the time base be 1/12 speed, and the falling edge of the clock increments the counter. When the 13-bit value moves from 1FFFh to 0000h, the timer overflow flag TFx is set, and an interrupt occurs if enabled. This is illustrated in next figure below.

14.2.2 Mode 1

Mode 1 is similar to Mode 0 except that the counting register forms a 16-bit counter, rather than a 13-bit counter. This means that all the bits of THx and TLx are used. Roll-over occurs when the timer moves from a count of 0FFFFh to 0000h. The timer overflow flag TFx of the relevant timer is set and if

also generate an interrupt.

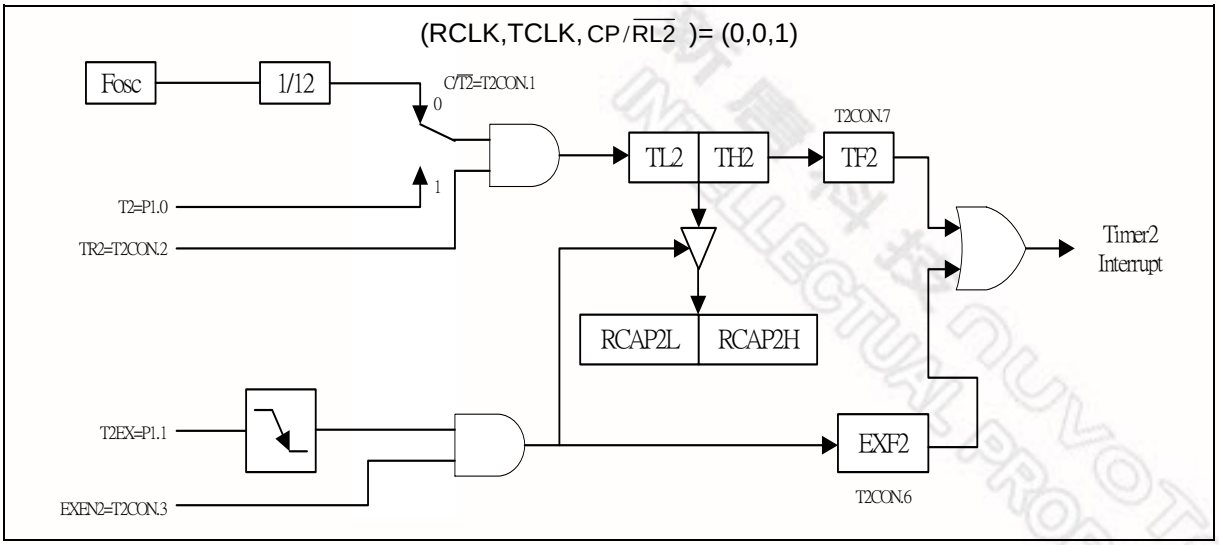


Figure 14-4 16-Bit Capture Mode

14.3.2 Auto-Reload Mode, Counting up

The auto-reload mode as an up counter is enabled by clearing the CP / RL2 bit in the T2CON register. In this mode, Timer/Counter 2 is a 16 bit up counter. When the counter rolls over from 0FFFFh, a reload is generated that causes the contents of the RCAP2L and RCAP2H registers to be reloaded into the TL2 and TH2 registers. The reload action also sets the TF2 bit. If the EXEN2 bit is set, then a negative transition of T2EX pin will also cause a reload. This action also sets the EXF2 bit in T2CON.

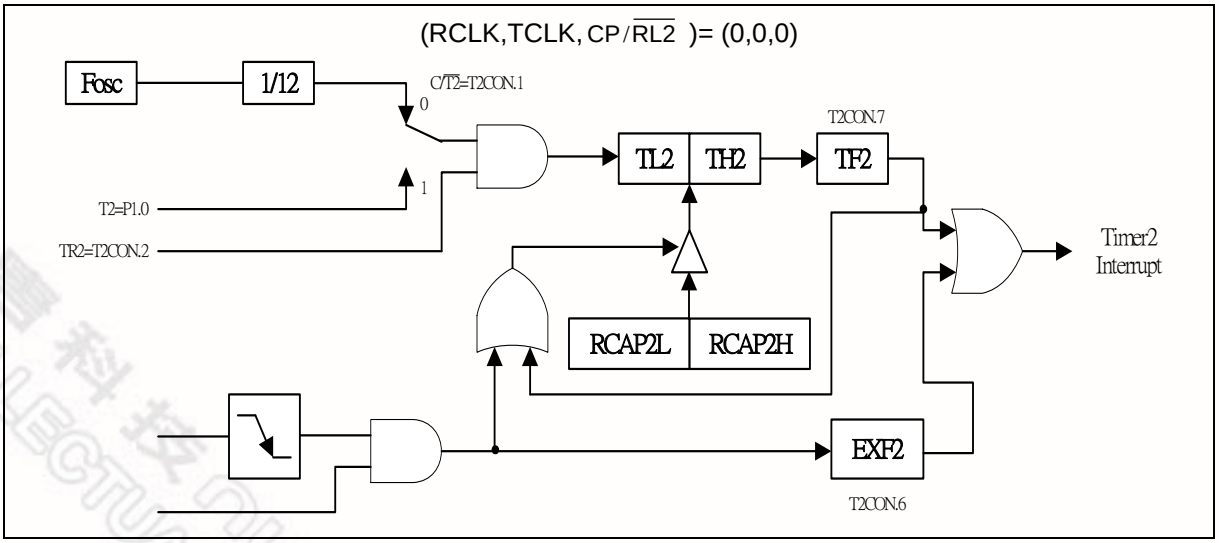


Figure 14- 5 16-Bit Auto-reload Mode, Counting Up

gramming function. Then you can use this F04KBOOT mode to force the W78E516D/W78E058D jump to LDROM and run on chip programming procedure. When you design your system, you can connect the pins P26, P27 to switches or jumpers. For example in a CD ROM system, you can connect the P26 and P27 to PLAY and EJECT buttons on the panel. When the APROM program is fail to execute the normal application program. User can press both two buttons at the same time and then switch on the power of the personal computer to force the W78E516D/W78E058D to enter the F04KBOOT mode. After power on of personal computer, you can release both PLAY and EJECT button.

NOTE2: In application system design, user must take care the P2, P3, ALE, /EA and /PSEN pin value at reset to avoid W78E516D/W78E058D entering the programming mode or F04KBOOT mode in normal operation.

21 ELECTRICAL CHARACTERISTICS

21.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	Min	MAX	UNIT
DC Power Supply	V_{DD}–V_{SS}	2.4	5.5	V
Input Voltage	V_{IN}	V_{SS}-0.3	V_{DD}+0.3	V
Operating Temperature	T_A	-40	+85	°C

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the lift and reliability of the device.

R_{RST}	RST-pin Internal Pull-down Resistor	2.4 < V_{DD} < 5.5V	30		350	KΩ

Note:

*1: Typical values are not guaranteed. The values listed are tested at room temperature and based on a limited number of samples.

*2: Pins of ports 1~4 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} is approximately 2V.

*3: Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
Maximum I_{OL} per port pin: 20mA
Maximum I_{OL} per 8-bit port: 40mA
Maximum total I_{OL} for all outputs: 100mA

*4: If I_{OH} exceeds the test condition, V_{OH} will be lower than the listed specification.
If I_{OL} exceeds the test condition, V_{OL} will be higher than the listed specification.

*5: Tested while CPU is kept in reset state and EA=H, Port0=H.

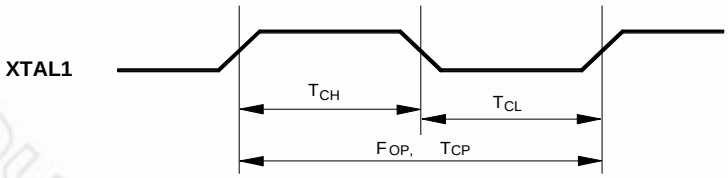
Voltage	**Max.** Frequency	6T/12T mode	Note
4.5-5.5V	40MHz	12T	
4.5-5.5V	20MHz	6T	
2.4V	20MHz	12T	
2.4V	10MHz	6T	

Frequency VS Voltage Table

21.3 AC CHARACTERISTICS

The AC specifications are a function of the particular process used to manufacture the part, the ratings of the I/O buffers, the capacitive load, and the internal routing capacitance. Most of the specifications can be expressed in terms of multiple input clock periods (TCP), and actual parts will usually experience less than a ±20 nS variation. The numbers below represent the performance expected from a 0.6 micron CMOS process when using 2 and 4 mA output buffers.

Clock Input Waveform



PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
Operating Speed	Fop	4	-	40	MHz	1

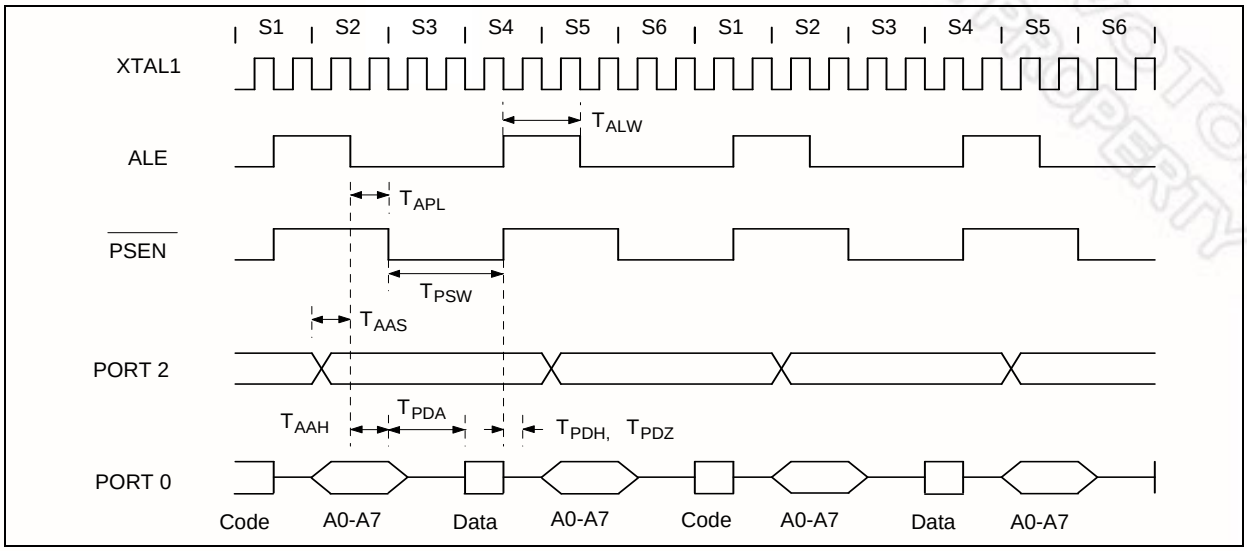
Port Access Cycle

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Port Input Setup to ALE Low	TPDS	1 TCP	-	-	nS
Port Input Hold from ALE Low	TPDH	0	-	-	nS
Port Output to ALE	TPDA	1 TCP	-	-	nS

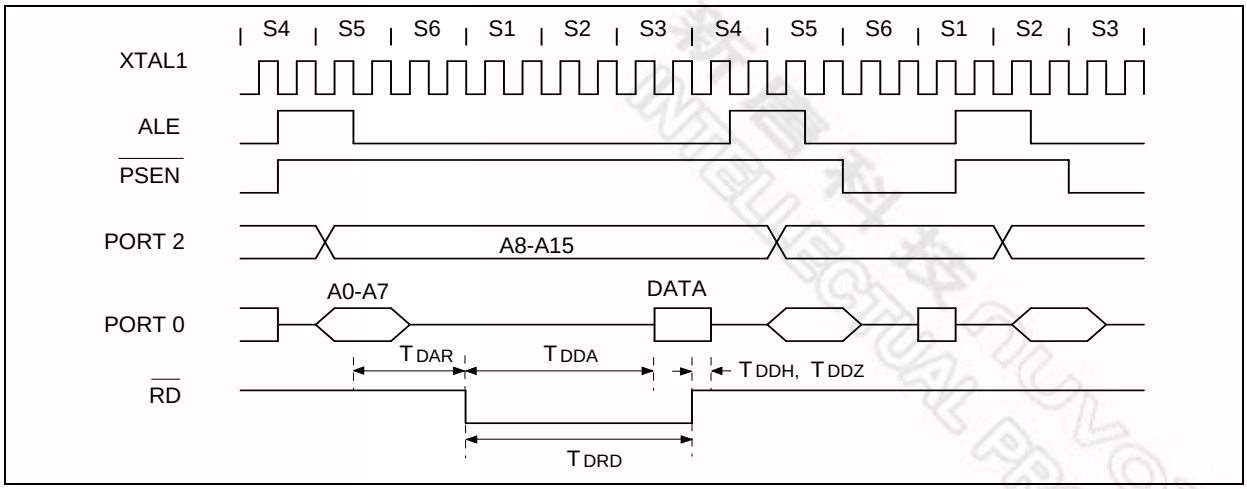
Note: Ports are read during S5P2, and output data becomes available at the end of S6P2. The timing data are referenced to ALE, since it provides a convenient reference.

21.4 TIMING waveforms

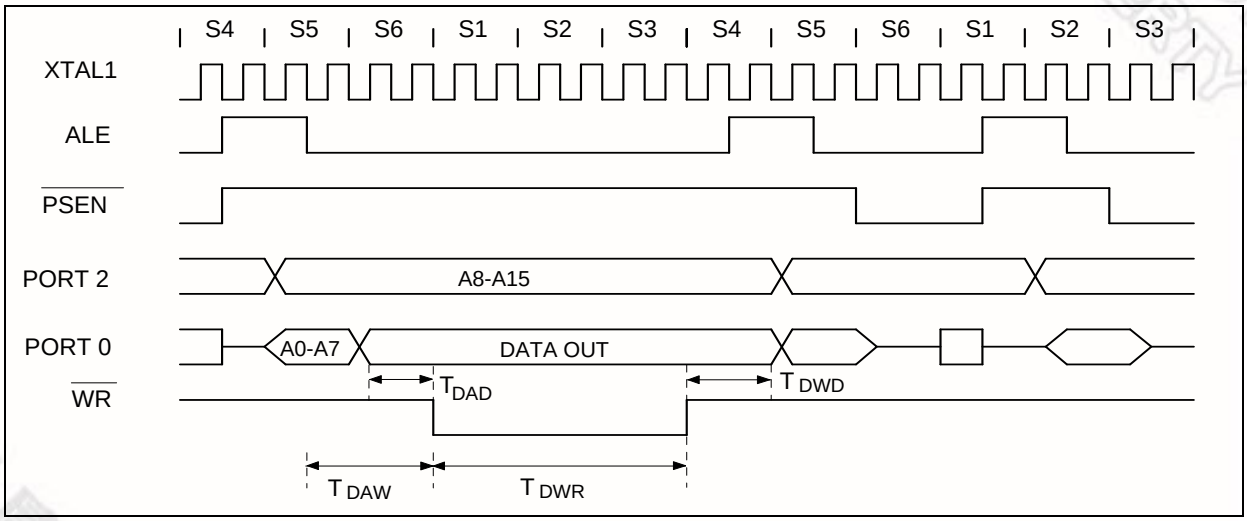
21.4.1 Program Fetch Cycle



21.4.2 Data Read Cycle



21.4.3 Data Write Cycle



```
;*********************************************************************
            ORG 100H

MAIN_4K:

            MOV         CHPENR,#87H             ;CHPENR=87H, CHPCON WRITE ENABLE.
            MOV         CHPENR,#59H             ;CHPENR=59H, CHPCON WRITE ENABLE.
            MOV         7FH,#01H                ;SET F04KBOOT MODE FLAG.

            MOV         A,CHPCON
            ANL         A,#01H
            CJNE        A,#00H,UPDATE_          ;CHECK CHPCON BIT 0
            MOV         7FH,#00H                ;FLAG=0, NOT IN THE F04KBOOT MODE.

            MOV         CHPCON,#01H             ;CHPCON=01H, ENABLE IN-SYSTEM PROGRAMMING.
            MOV         CHPENR,#00H             ;DISABLE CHPCON WRITE ATTRIBUTE

            MOV         TCON,#00H               ;TCON=00H ,TR=0 TIMER0 STOP
            MOV         TMOD,#01H               ;TMOD=01H ,SET TIMER0 A 16BIT TIMER
            MOV         IP,#00H                 ;IP=00H
            MOV         IE,#82H                 ;IE=82H,TIMER0 INTERRUPT ENABLED
            MOV         R6,#FEH
            MOV         R7,#FFH
            MOV         TL0,R6
            MOV         TH0,R7
            MOV         TCON,#10H               ;TCON=10H,TR0=1,GO
            MOV         PCON,#01H               ;ENTER IDLE MODE


UPDATE_:

            MOV         CHPENR,#00H             ;DISABLE CHPCON WRITE-ATTRIBUTE
            MOV         TCON,#00H               ;TCON=00H ,TR=0 TIM0 STOP
            MOV         IP,#00H                 ;IP=00H
            MOV         IE,#82H                 ;IE=82H,TIMER0 INTERRUPT ENABLED
            MOV         TMOD,#01H               ;TMOD=01H ,MODE1

            MOV         R6,#3CH                 ;SET WAKE-UP TIME FOR ERASE OPERATION,
                                                ;ABOUT 15ms.   DEPENDING ON USER'S
                                                ;SYSTEM CLOCK RATE.
            MOV         R7,#B0H
            MOV         TL0,R6
            MOV         TH0,R7

ERASE_P_4K:
            MOV         SFRCN,#22H              ;SFRCN(C7H)=22H  ERASE
            MOV         TCON,#10H               ;TCON=10H,TR0=1,GO
            MOV         PCON,#01H               ;ENTER IDLE MODE( FOR ERASE OPERATION)

;*********************************************************************
;* BLANK CHECK
;*********************************************************************

            MOV         SFRCN,#0H               ;READ APROM MODE
            MOV         SFRAH,#0H               ;START ADDRESS = 0H
            MOV         SFRAL,#0H
            MOV         R6,#FBH                 ;SET TIMER FOR READ OPERATION, ABOUT 1.5us.
            MOV         R7,#FFH
```

23 REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A01	June 24, 2008	-	Initial Issued
A02	August 21,2008	7,8	Update pin assignment.
A03	September 1,2008	-	Update W78I516D/W78I058D parts
A04	November 3,2008		Update DC table typo error
A05	January 7,2009	74	Update V_{IL} and V_{IH} .
A06	April 2, 2009	- - -	Update DC table Revise some typing errors Rename SFR 86H POR register to P0UPR
A07	April 22,2009	70	Revise the Application Circuit
A08	June 30,2009	6 65 70 71	1. Revise the Table 3-1 2. Add the picture for “F04KBOOT Mode” of P4.3 3. Revise the ISP Flow Chart 4. Revise the CONFIG BITS 5. Remove the “Preliminary” character each page
A09	Feb 15,2011	18 65 70 79	1. Revise the default reset value for CHPCON 2. Add the reset-pin reset can entry the F04KBOOT mode. 3. Revise the flow chart of ISP programming 4. Revise the CONFIG BITS 5. Add the external reset pin timing