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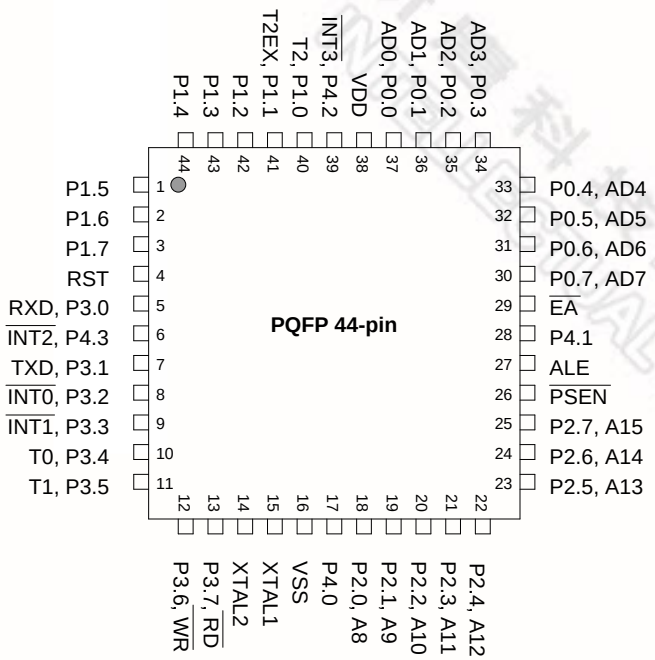
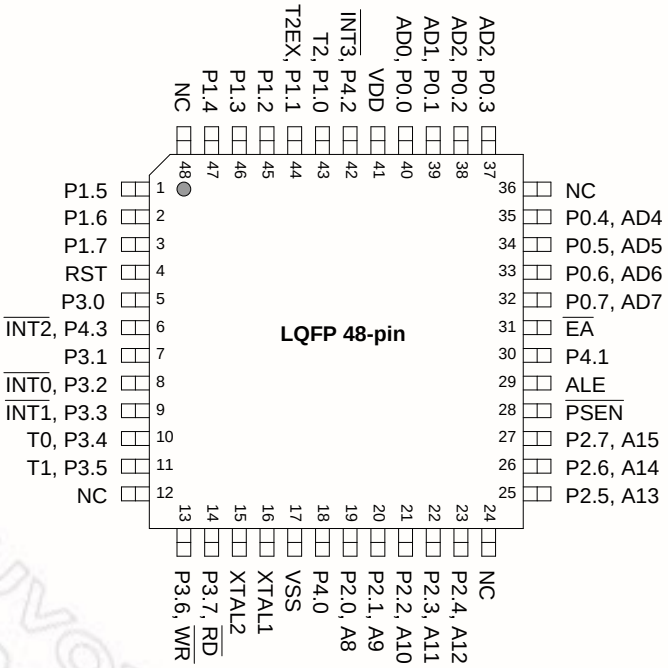
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8052
Core Size	8-Bit
Speed	40MHz
Connectivity	EBI/EMI, UART/USART
Peripherals	POR, WDT
Number of I/O	32
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/w78e516ddg

2 FEATURES

- Fully static design 8-bit CMOS microcontroller
- Optional 12T or 6T mode
  - 12T Mode, 12 clocks per machine cycle operation (default), Speed up to 40 MHz/5V
  - 6T Mode, 6 clocks per machine cycle operation set by the writer, Speed up to 20 MHz/5V
- Wide supply voltage of 2.4 to 5.5V
- Temperature grade is (-40°C~85°C)
- 64K/32K bytes of in-system programmable FLASH EPROM for Application Program (APROM)
- 4K bytes of auxiliary FLASH EPROM for Loader Program (LDROM)
- Low standby current at full supply voltage
- 512 bytes of on-chip RAM. (include 256 bytes of AUX-RAM, software selectable)
- 64K bytes program memory address space and 64K bytes data memory address space
- One 4-bit multipurpose programmable port, additional $\overline{INT2}$ / $\overline{INT3}$
- Support Watch Dog Timer
- Three 16-bit timer/counters
- One full duplex serial port
- 8-sources, 2-level interrupt capability
- Software Reset
- Built-in power management with idle mode and power down mode
- Code protection
- Packages:
  - Lead Free (RoHS) DIP 40: W78E516DDG
  - Lead Free (RoHS) PLCC 44: W78E516DPG
  - Lead Free (RoHS) PQFP 44: W78E516DFG
  - Lead Free (RoHS) LQFP 48: W78E516DLG
  - Lead Free (RoHS) DIP 40: W78E058DDG
  - Lead Free (RoHS) PLCC 44: W78E058DPG
  - Lead Free (RoHS) PQFP 44: W78E058DFG
  - Lead Free (RoHS) LQFP 48: W78E058DLG


P1.4
P1.3
P1.2
T2EX, P1.1
T2, P1.0
INT3, P4.2
VDD
AD0, P0.0
AD1, P0.1
AD2, P0.2
AD3, P0.3
P1.5
P1.6
P1.7
RST
RXD, P3.0
INT2, P4.3
TXD, P3.1
INT0, P3.2
INT1, P3.3
T0, P3.4
T1, P3.5
P0.4, AD4
P0.5, AD5
P0.6, AD6
P0.7, AD7
EA
P4.1
ALE
PSEN
P2.7, A15
P2.6, A14
P2.5, A13
P3.6, WR
P3.7, RD
XTAL2
XTAL1
VSS
P4.0
P2.0, A8
P2.1, A9
P2.2, A10
P2.3, A11
P2.4, A12
PQFP 44-pin


NC
P1.4
P1.3
P1.2
T2EX, P1.1
T2, P1.0
INT3, P4.2
VDD
AD0, P0.0
AD1, P0.1
AD2, P0.2
AD2, P0.3
P1.5
P1.6
P1.7
RST
P3.0
INT2, P4.3
P3.1
INT0, P3.2
INT1, P3.3
T0, P3.4
T1, P3.5
NC
NC
P0.4, AD4
P0.5, AD5
P0.6, AD6
P0.7, AD7
EA
P4.1
ALE
PSEN
P2.7, A15
P2.6, A14
P2.5, A13
P3.6, WR
P3.7, RD
XTAL2
XTAL1
VSS
P4.0
P2.0, A8
P2.1, A9
P2.2, A10
P2.3, A11
P2.4, A12
NC
LQFP 48-pin

6 BLOCK DIAGRAM

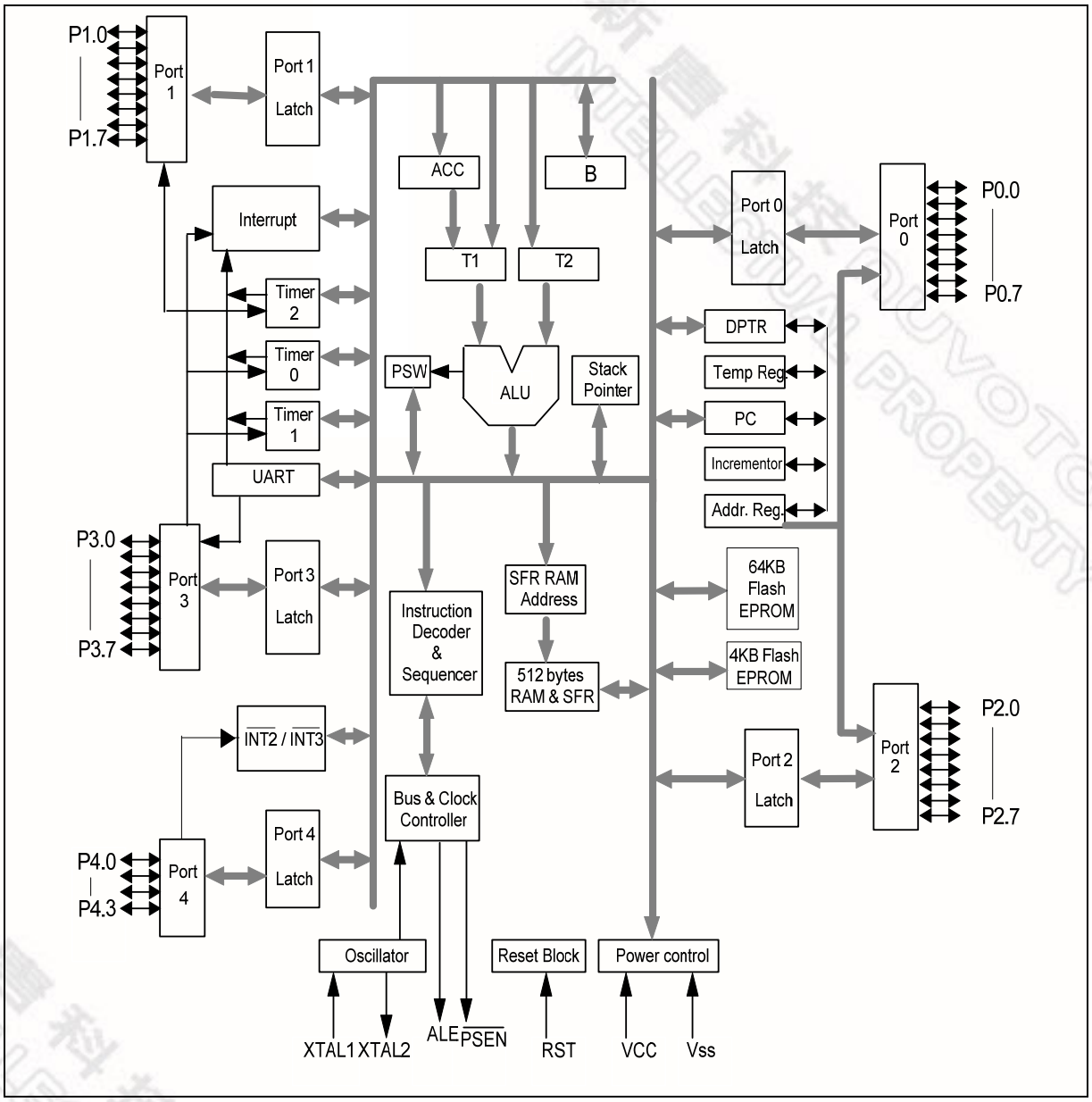


Figure 6- 1 W78E516D/W78E058D Block Diagram

as an internal timer, depending on the setting of bit C/T2 in T2CON. Timer 2 has three operating modes: capture, auto-reload, and baud rate generator. The clock speed at capture or auto-reload mode is the same as that of Timers 0 and 1.

7.4.1 Clock

The W78E516D/W78E058D series are designed to be used with either a crystal oscillator or an external clock. Internally, the clock is divided by two before it is used by default. This makes the W78E516D/W78E058D series relatively insensitive to duty cycle variations in the clock.

7.5 Interrupts

The Interrupt structure in the W78E516D/W78E058D series is slightly different from that of the standard 8052. Due to the presence of additional features and peripherals, the number of interrupt sources and vectors has been increased. The W78E516D/W78E058D series provides 8 interrupt resources with two priority level, including four external interrupt sources, three timer interrupts, serial I/O interrupts.

7.6 Data Pointers

The data pointer of W78E516D/W78E058D series is same as standard 8052 that have one 16-bit Data Pointer (DPTR).

7.7 Architecture

The W78E516D/W78E058D series are based on the standard 8052 device. It is built around an 8-bit ALU that uses internal registers for temporary storage and control of the peripheral devices. It can execute the standard 8052 instruction set.

7.7.1 ALU

The ALU is the heart of the W78E516D/W78E058D series. It is responsible for the arithmetic and logical functions. It is also used in decision making, in case of jump instructions, and is also used in calculating jump addresses. The user cannot directly use the ALU, but the Instruction Decoder reads the op-code, decodes it, and sequences the data through the ALU and its associated registers to generate the required result. The ALU mainly uses the ACC which is a special function register (SFR) on the chip. Another SFR, namely B register is also used Multiply and Divide instructions. The ALU generates several status signals which are stored in the Program Status Word register (PSW).

7.7.2 Accumulator

The Accumulator (ACC) is the primary register used in arithmetic, logical and data transfer operations in the W78E516D/W78E058D series. Since the Accumulator is directly accessible by the CPU, most of the high speed instructions make use of the ACC as one argument.

7.7.3 B Register

This is an 8-bit register that is used as the second argument in the MUL and DIV instructions. For all other instructions it can be used simply as a general purpose register.

7.7.4 Program Status Word

This is an 8-bit SFR that is used to store the status bits of the ALU. It holds the Carry flag, the Auxiliary Carry flag, General purpose flags, the Register Bank Select, the Overflow flag, and the Parity flag.

8.2.1 Working Registers

There are four sets of working registers, each consisting of eight 8-bit registers. These are termed as Banks 0, 1, 2, and 3. Individual registers within these banks can be directly accessed by separate instructions. These individual registers are named as R0, R1, R2, R3, R4, R5, R6 and R7. However, at one time the W78E516D/W78E058D series can work with only one particular bank. The bank selection is done by setting RS1-RS0 bits in the PSW. The R0 and R1 registers are used to store the address for indirect accessing.

8.2.2 Bit addressable Locations

The Scratch-pad RAM area from location 20h to 2Fh is byte as well as bit addressable. This means that a bit in this area can be individually addressed. In addition some of the SFRs are also bit addressable. The instruction decoder is able to distinguish a bit access from a byte access by the type of the instruction itself. In the SFR area, any existing SFR whose address ends in a 0 or 8 is bit addressable.

8.2.3 Stack

The scratch-pad RAM can be used for the stack. This area is selected by the Stack Pointer (SP), which stores the address of the top of the stack. Whenever a jump, call or interrupt is invoked the return address is placed on the stack. There is no restriction as to where the stack can begin in the RAM. By default however, the Stack Pointer contains 07h at reset. The user can then change this to any value desired. The SP will point to the last used value. Therefore, the SP will be incremented and then address saved onto the stack. Conversely, while popping from the stack the contents will be read first, and then the SP is decreased.

8.2.4 AUX-RAM

AUX-RAM 0H~255H is addressed indirectly as the same way to access external data memory with the MOVX instruction. Address pointer are R0 and R1 of the selected register bank and DPTR register. A access to external data memory locations higher than 255 will be performed with the MOVX instruction in the same way as in the 8051. The AUX-RAM is disabled after power-on reset. Setting the bit 4 in CHPCON register will enable the access to AUX-RAM.

Serial Port Control

Bit:	7	6	5	4	3	2	1	0
	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI

Mnemonic: SCON Address: 98h

BIT	NAME	FUNCTION
7	SM0/FE	Serial port mode select bit 0 or Framing Error Flag: The SMOD0 bit in PCON SFR determines whether this bit acts as SM0 or as FE. The operation of SM0 is described below. When used as FE, this bit will be set to indicate an invalid stop bit. This bit must be manually cleared in software to clear the FE condition.
6	SM1	Serial Port mode select bit 1. See table below.
5	SM2	Multiprocessor communication mode enable. The function of this bit is dependent on the serial port mode. Mode 0: No effect. Mode 1: Checking valid stop bit. 0 = Reception is always valid no matter the logic level of stop bit. 1 = Reception is ignored if the received stop bit is not logic 1. Mode 2 or 3: For multiprocessor communication. 0 = Reception is always valid no matter the logic level of the 9th bit. 1 = Reception is ignored if the received 9th bit is not logic 1.
4	REN	Receive enable: 0: Disable serial reception. 1: Enable serial reception.
3	TB8	This is the 9th bit to be transmitted in modes 2 and 3. This bit is set and cleared by software as desired.
2	RB8	In modes 2 and 3 this is the received 9th data bit. In mode 1, if SM2 = 0, RB8 is the stop bit that was received. In mode 0 it has no function.
1	TI	Transmit interrupt flag: This flag is set by hardware at the end of the 8th bit time in mode 0, or at the beginning of the stop bit in all other modes during serial transmission. This bit must be cleared by software.
0	RI	Receive interrupt flag: This flag is set by hardware at the end of the 8th bit time in mode 0, or halfway through the stop bits time in the other modes during serial reception. However the restrictions of SM2 apply to this bit. This bit can be cleared only by software.

SM1, SM0: Mode Select bits:

Mode	SM0	SM1	Description	Length	Baud Rate
0	0	0	Synchronous	8	Tclk divided by 4 or 12
1	0	1	Asynchronous	10	Variable
2	1	0	Asynchronous	11	Tclk divided by 32 or 64
3	1	1	Asynchronous	11	Variable

3	P3.3	$\overline{INT1}$
2	P3.2	$\overline{INT0}$
1	P3.1	TX
0	P3.0	RX

P4.3 Base Address Low Byte Register

Bit:	7	6	5	4	3	2	1	0
	P43AL.7	P43AL.6	P43AL.5	P43AL.4	P43AL.3	P43AL.2	P43AL.1	P43AL.0

Mnemonic: P43AL Address: B4h

BIT	NAME	FUNCTION
7-0	P43AL.[7:0]	The Base address register for comparator of P4.3. P43AL contains the low-order byte of address.

P4.3 Base Address High Byte Register

Bit:	7	6	5	4	3	2	1	0
	P43AH.7	P43AH.6	P43AH.5	P43AH.4	P43AH.3	P43AH.2	P43AH.1	P43AH.0

Mnemonic: P43AH Address: B5h

BIT	NAME	FUNCTION
7-0	P43AH.[7:0]	The Base address register for comparator of P4.3. P43AH contains the High-order byte of address.

Interrupt Priority

Bit:	7	6	5	4	3	2	1	0
	-	-	PT2	PS	PT1	PX1	PT0	PX0

Mnemonic: IP Address: B8h

BIT	NAME	FUNCTION
5	PT2	1: To set interrupt priority of Timer 2 is higher priority level.
4	PS	1: To set interrupt priority of Serial port 0 is higher priority level.
3	PT1	1: To set interrupt priority of Timer 1 is higher priority level.
2	PX1	1: To set interrupt priority of External interrupt 1 is higher priority level.
1	PT0	1: To set interrupt priority of Timer 0 is higher priority level.
0	PX0	1: To set interrupt priority of External interrupt 0 is higher priority level.

Chip Control

Bit:	7	6	5	4	3	2	1	0
	SWRESET	-	-	ENAUXRAM	0	0	FBOOTSL	FPRGEN

Bit:	7	6	5	4	3	2	1	0
	P41FUN1	P41FUN0	P41CMP1	P41CMP0	P40FUN1	P40FUN0	P40CMP1	P40CMP0

Mnemonic: P4CONA Address: C2h

BIT	NAME	FUNCTION
7,6	P41FUN1 P41FUN0	00: Mode 0. P4.1 is a general purpose I/O port which is the same as Port1. 01: Mode 1. P4.1is a Read Strobe signal for chip select purpose. The address range depends on the SFR P41AH, P41AL, P41CMP1 and P41CMP0. 10: Mode 2. P4.1 is a Write Strobe signal for chip select purpose. The address range depends on the SFR P41AH,P41AL,P41CMP1 and P41CMP0. 11: Mode 3. P4.1 is a Read/Write Strobe signal for chip select purpose. The address range depends on the SFR P41AH, P41AL, P41CMP1, and P41CMP0.
5,4	P41CMP1 P41CMP0	Chip-select signals address comparison: 00: Compare the full address (16 bits length) with the base address register P41AH, P41AL. 01: Compare the 15 high bits (A15-A1) of address bus with the base address register P41AH, P41AL. 10: Compare the 14 high bits (A15-A2) of address bus with the base address register P41AH, P41AL. 11: Compare the 8 high bits (A15-A8) of address bus with the base address register P41AH, P41AL.
3,2	P40FUN1 P40FUN0	The P4.0 function control bits which are the similar definition as P40FUN1, P40FUN0. .
1,0	P40CMP1 P40CMP0	The P4.0 address comparator length control bits which are the similar definition as P40CMP, P40CMP0.

Port 4 control B

Bit:	7	6	5	4	3	2	1	0
	P43FUN1	P43FUN0	P43CMP1	P43CMP0	P42FUN1	P42FUN0	P42CMP1	P42CMP0

Mnemonic: P4CONB Address: C3h

BIT	NAME	FUNCTION
7,6	P43FUN1 P43FUN0	The P4.3 function control bits which are the similar definition as P43FUN1, P43FUN0. .
5,4	P43CMP1 P43CMP0	The P4.3 address comparator length control bits which are the similar definition as P43CMP1,P43CMP0.
3,2	P42FUN1 P42FUN0	The P4.2 function control bits which are the similar definition as P42FUN1, P42FUN0. .
1,0	P42CMP1 P42CMP0	The P4.2 address comparator length control bits which are the similar definition as P42CMP1,P42CMP0.

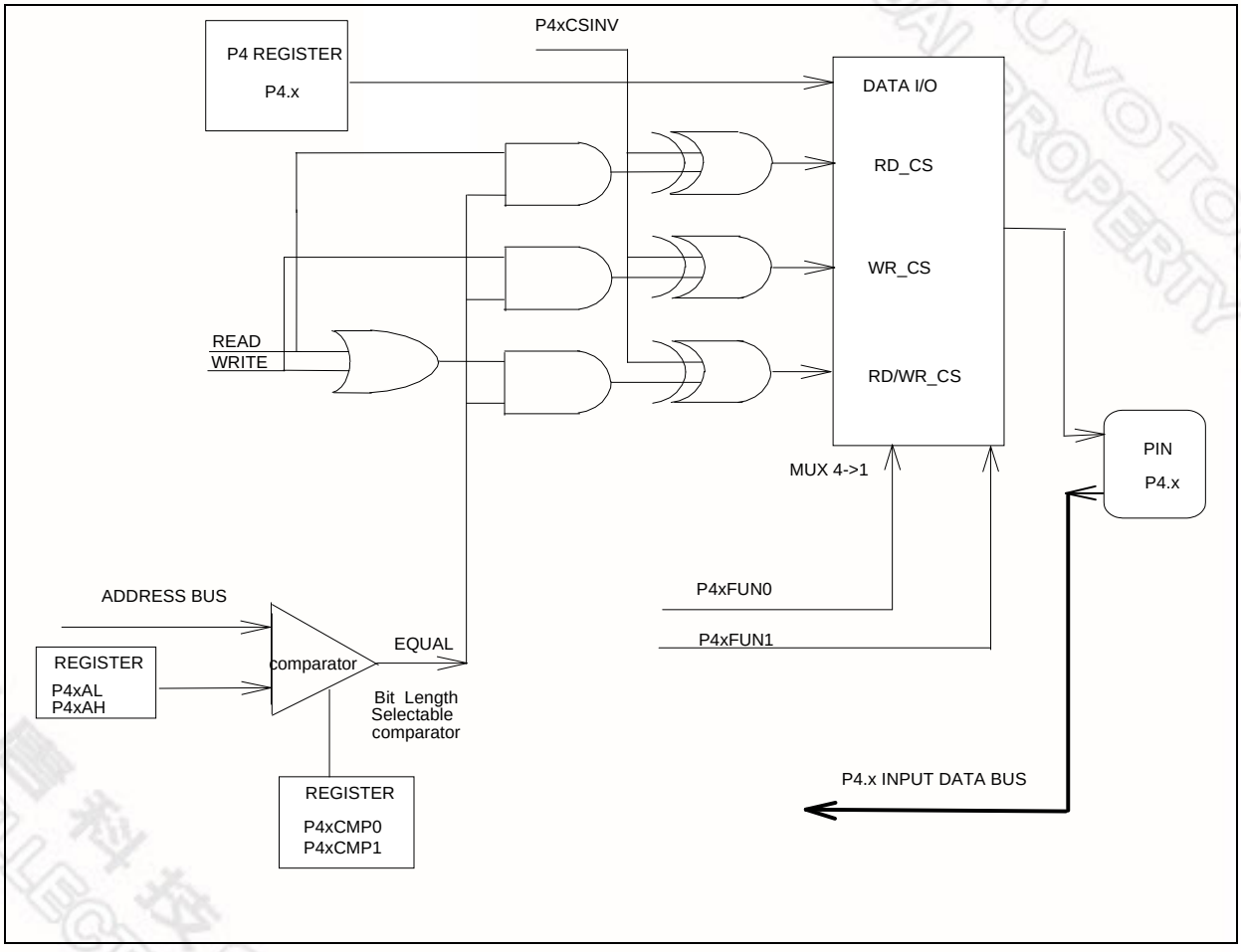
SFR program of address low

Bit:	7	6	5	4	3	2	1	0
	SFRAL.7	SFRAL.6	SFRAL.5	SFRAL.4	SFRAL.3	SFRAL.2	SFRAL.1	SFRAL.0

Here is an example to program the P4.0 as a write strobe signal at the I/O port address 1234H ~1237H and positive polarity, and P4.1~P4.3 are used as general I/O ports.

```
MOV  P40AH,#12H
MOV  P40AL,#34H              ;Define the base I/O address 1234H for P4.0 as an special function
MOV  P4CONA,#00001010B       ;Define the P4.0 as a write strobe signal pin and the comparator
MOV  P4CONB,#00H             ;P4.1~P4.3 as general I/O port which are the same as PORT1
MOV  P2ECON,#10H             ;Write the P40SINV =1 to inverse the P4.0 write strobe polarity
                             ;default is negative.
```

Then any instruction MOVX @DPTR,A (with DPTR=1234H~1237H) will generate the positive polarity write strobe signal at pin P4.0 . And the instruction MOV P4,#XX will output the bit3 to bit1 of data #XX to pin P4.3~ P4.1.



The Port 4 Structure Diagram

ACCUMULATOR

Bit:	7	6	5	4	3	2	1	0

Op-code	HEX Code	Bytes	W78E516D/W78E058D series Clock cycles
DA A	D4	1	12
ANL A, R0	58	1	12
ANL A, R1	59	1	12
ANL A, R2	5A	1	12
ANL A, R3	5B	1	12
ANL A, R4	5C	1	12
ANL A, R5	5D	1	12
ANL A, R6	5E	1	12
ANL A, R7	5F	1	12
ANL A, @R0	56	1	12
ANL A, @R1	57	1	12
ANL A, direct	55	2	12
ANL A, #data	54	2	12
ANL direct, A	52	2	12
ANL direct, #data	53	3	24
ORL A, R0	48	1	12
ORL A, R1	49	1	12
ORL A, R2	4A	1	12
ORL A, R3	4B	1	12
ORL A, R4	4C	1	12
ORL A, R5	4D	1	12
ORL A, R6	4E	1	12
ORL A, R7	4F	1	12
ORL A, @R0	46	1	12
ORL A, @R1	47	1	12
ORL A, direct	45	2	12
ORL A, #data	44	2	12
ORL direct, A	42	2	12
ORL direct, #data	43	3	24
XRL A, R0	68	1	12
XRL A, R1	69	1	12
XRL A, R2	6A	1	12
XRL A, R3	6B	1	12

Op-code	HEX Code	Bytes	W78E516D/W78E058D series Clock cycles
MOV direct, R7	8F	2	24
MOV direct, @R0	86	2	24
MOV direct, @R1	87	2	24
MOV direct, direct	85	3	24
MOV direct, #data	75	3	24
MOV DPTR, #data 16	90	3	24
MOVC A, @A+DPTR	93	1	24
MOVC A, @A+PC	83	1	24
MOVX A, @R0	E2	1	24
MOVX A, @R1	E3	1	24
MOVX A, @DPTR	E0	1	24
MOVX @R0, A	F2	1	24
MOVX @R1, A	F3	1	24
MOVX @DPTR, A	F0	1	24
PUSH direct	C0	2	24
POP direct	D0	2	24
XCH A, R0	C8	1	12
XCH A, R1	C9	1	12
XCH A, R2	CA	1	12
XCH A, R3	CB	1	12
XCH A, R4	CC	1	12
XCH A, R5	CD	1	12
XCH A, R6	CE	1	12
XCH A, R7	CF	1	12
XCH A, @R0	C6	1	12
XCH A, @R1	C7	1	12
XCHD A, @R0	D6	1	12
XCHD A, @R1	D7	1	12
XCH A, direct	C5	2	24
CLR C	C3	1	12
CLR bit	C2	2	12
SETB C	D3	1	12
SETB bit	D2	2	12
CPL C	B3	1	12

Op-code	HEX Code	Bytes	W78E516D/W78E058D series Clock cycles
CPL bit	B2	2	12
ANL C, bit	82	2	24
ANL C, /bit	B0	2	24
ORL C, bit	72	2	24
ORL C, /bit	A0	2	24
MOV C, bit	A2	2	12
MOV bit, C	92	2	24
ACALL addr11	71, 91, B1, 11, 31, 51, D1, F1	2	24
LCALL addr16	12	3	24
RET	22	1	24
RETI	32	1	24
AJMP ADDR11	01, 21, 41, 61, 81, A1, C1, E1	2	24
LJMP addr16	02	3	24
JMP @A+DPTR	73	1	24
SJMP rel	80	2	24
JZ rel	60	2	24
JNZ rel	70	2	24
JC rel	40	2	24
JNC rel	50	2	24
JB bit, rel	20	3	24
JNB bit, rel	30	3	24
JBC bit, rel	10	3	24
CJNE A, direct, rel	B5	3	24
CJNE A, #data, rel	B4	3	24
CJNE @R0, #data, rel	B6	3	24
CJNE @R1, #data, rel	B7	3	24
CJNE R0, #data, rel	B8	3	24
CJNE R1, #data, rel	B9	3	24
CJNE R2, #data, rel	BA	3	24
CJNE R3, #data, rel	BB	3	24
CJNE R4, #data, rel	BC	3	24
CJNE R5, #data, rel	BD	3	24

Interrupts

The W78E516D/W78E058D has a 2 priority level interrupt structure with 8 interrupt sources. Each of the interrupt sources has an individual priority bit, flag, interrupt vector and enable bit. In addition, the interrupts can be globally enabled or disabled.

13.2 Interrupt Sources

The External Interrupts $\overline{INT0}$ and $\overline{INT1}$ can be either edge triggered or level triggered, depending on bits IT0 and IT1. The bits IE0 and IE1 in the TCON register are the flags which are checked to generate the interrupt. In the edge triggered mode, the INTx inputs are sampled in every machine cycle. If the sample is high in one cycle and low in the next, then a high to low transition is detected and the interrupts request flag IEx in TCON is set. The flag bit requests the interrupt. Since the external interrupts are sampled every machine cycle, they have to be held high or low for at least one complete machine cycle. The IEx flag is automatically cleared when the service routine is called. If the level triggered mode is selected, then the requesting source has to hold the pin low till the interrupt is serviced. The IEx flag will not be cleared by the hardware on entering the service routine. If the interrupt continues to be held low even after the service routine is completed, then the processor may acknowledge another interrupt request from the same source. Note that the external interrupts $\overline{INT2}$ and $\overline{INT3}$. By default, the individual interrupt flag corresponding to external interrupt 2 to 3 must be cleared manually by software.

The Timer 0 and 1 Interrupts are generated by the TF0 and TF1 flags. These flags are set by the overflow in the Timer 0 and Timer 1. The TF0 and TF1 flags are automatically cleared by the hardware when the timer interrupt is serviced. The Timer 2 interrupt is generated by a logical OR of the TF2 and the EXF2 flags. These flags are set by overflow or capture/reload events in the timer 2 operation. The hardware does not clear these flags when a timer 2 interrupt is executed. Software has to resolve the cause of the interrupt between TF2 and EXF2 and clear the appropriate flag.

The Serial block can generate interrupts on reception or transmission. There are two interrupt sources from the Serial block, which are obtained by the RI and TI bits in the SCON SFR. These bits are not automatically cleared by the hardware, and the user will have to clear these bits using software.

All the bits that generate interrupts can be set or reset by hardware, and thereby software initiated interrupts can be generated. Each of the individual interrupts can be enabled or disabled by setting or clearing a bit in the IE SFR. IE also has a global enable/disable bit EA, which can be cleared to disable all the interrupts, at once.

Source	Vector Address	Source	Vector Address
External Interrupt 0	0003h	Timer 0 Overflow	000Bh
External Interrupt 1	0013h	Timer 1 Overflow	001Bh
Serial Port	0023h	Timer 2 Overflow	002Bh
External Interrupt 2	0033h	External Interrupt 3	003Bh

Table 13- 1 W78E516D/W78E058D interrupt vector table

13.3 Priority Level Structure

There are two priority levels for the interrupts high, low. The interrupt sources can be individually set to either high or low levels. Naturally, a higher priority interrupt cannot be interrupted by a lower priority interrupt. However there exists a pre-defined hierarchy amongst the interrupts themselves. This hierarchy comes into play when the interrupt controller has to resolve simultaneous requests having the same priority level. This hierarchy is defined as shown on Table.

The 16 states of the counter effectively divide the bit time into 16 slices. The bit detection is done on a best of three basie. The bit detector samples the RxD pin, at the 8th, 9th and 10th counter states. By using a majority 2 of 3 voting system, the bit value is selected. This is done to improve the noise rejection feature of the serial port. If the first bit detected after the falling edge of RxD pin is not 0, then this indicates an invalid start bit, and the reception is immediately aborted. The serial port again looks for a falling edge in the RxD line. If a valid start bit is detected, then the rest of the bits are also detected and shifted into the SBUF.

After shifting in 8 data bits, there is one more shift to do, after which the SBUF and RB8 are loaded and RI is set. However certain conditions must be met before the loading and setting of RI can be done.

1. RI must be 0 and
2. Either SM2 = 0, or the received stop bit = 1.

If these conditions are met, then the stop bit goes to RB8, the 8 data bits go into SBUF and RI is set. Otherwise the received frame may be lost. After the middle of the stop bit, the receiver goes back to looking for a 1-to-0 transition on the RxD pin.

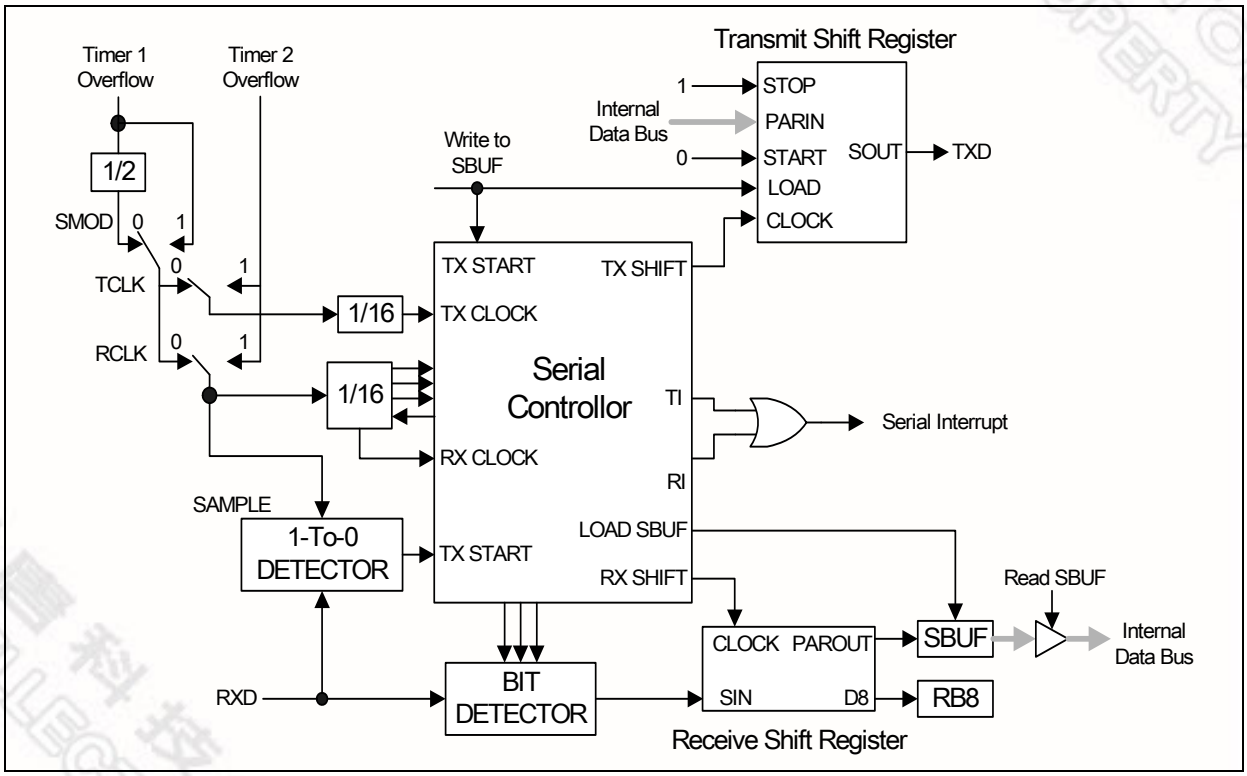


Figure 16- 2 Serial port mode 1

16.3 MODE 2

This mode uses a total of 11 bits in asynchronous full-duplex communication. The functional description is shown in the figure below. The frame consists of one start bit (0), 8 data bits (LSB first), a pro-

grammable 9th bit (TB8) and a stop bit (1). The 9th bit received is put into RB8. The baud rate is programmable to 1/32 or 1/64 of the oscillator frequency, which is determined by the SMOD bit in PCON SFR. Transmission begins with a write to SBUF. The serial data is brought out on to TxD pin at S6P2 following the first roll-over of the divide by 16 counter. The next bit is placed on TxD pin at S6P2 following the next rollover of the divide by 16 counter. Thus the transmission is synchronized to the divide by 16 counters, and not directly to the write to SBUF signal. After all 9 bits of data are transmitted, the stop bit is transmitted. The TI flag is set in the S6P2 state after the stop bit has been put out on TxD pin. This will be at the 11th rollover of the divide by 16 counters after a write to SBUF. Reception is enabled only if REN is high. The serial port actually starts the receiving of serial data, with the detection of a falling edge on the RxD pin. The 1-to-0 detector continuously monitors the RxD line, sampling it at the rate of 16 times the selected baud rate. When a falling edge is detected, the divide by 16 counters is immediately reset. This helps to align the bit boundaries with the rollovers of the divide by 16 counters. The 16 states of the counter effectively divide the bit time into 16 slices. The bit detection is done on a best of three basis. The bit detector samples the RxD pin, at the 8th, 9th and 10th counter states. By using a majority 2 of 3 voting system, the bit value is selected. This is done to improve the noise rejection feature of the serial port.

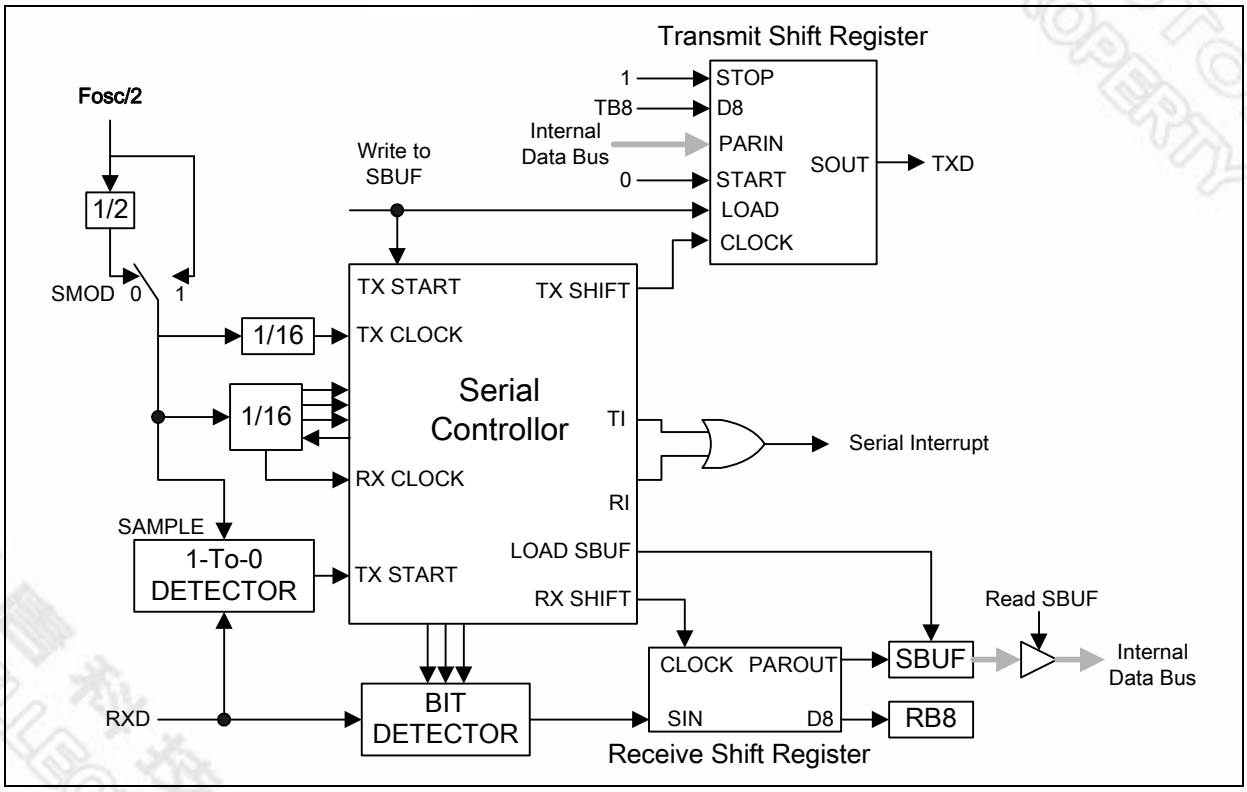


Figure 16- 3 Serial port mode 2

If the first bit detected after the falling edge of RxD pin, is not 0, then this indicates an invalid start bit, and the reception is immediately aborted. The serial port again looks for a falling edge in the RxD line. If a valid start bit is detected, then the rest of the bits are also detected and shifted into the SBUF. After shifting in 9 data bits, there is one more shift to do, after which the SBUF and RB8 are loaded and RI is set. However certain conditions must be met before the loading and setting of RI can be done.

1. RI must be 0 and

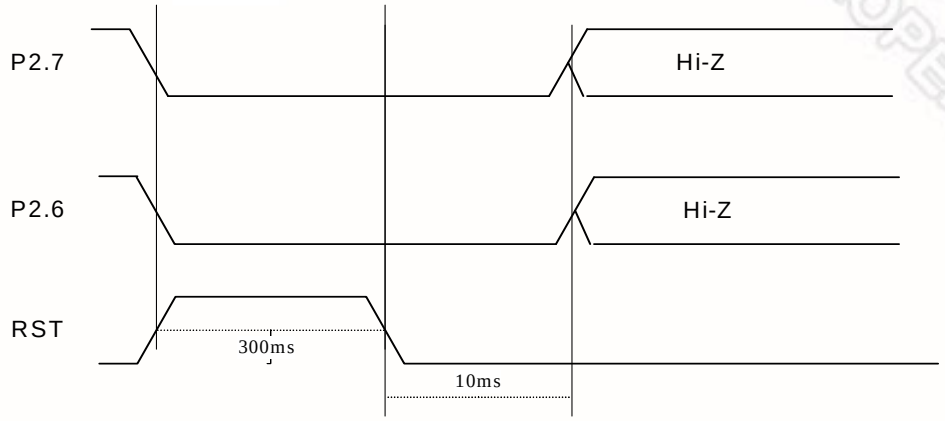
17 F04KBOOT MODE (BOOT FROM 4K BYTES OF LDROM)

The W78E516D/W78E058D boots from APROM program memory(64K/32K bytes) by default at power on reset or reset-pin reset. On some occasions, user can force the W78E516D/W78E058D booting from the LDROM program memory (4K bytes) at power on reset or external reset. The settings for this special mode as follow.

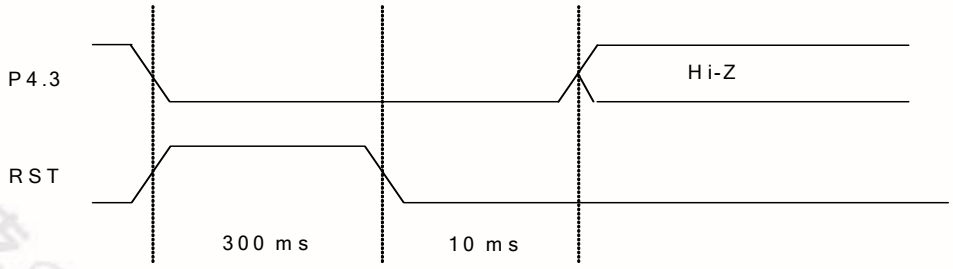
F04KBOOT MODE

P4.3	P2.7	P2.6	Mode
X	L	L	FO4KBOOT
L	X	X	FO4KBOOT

The Reset Timing For Entering F04KBOOT Mode



The Reset Timing For Entering F04KBOOT Mode

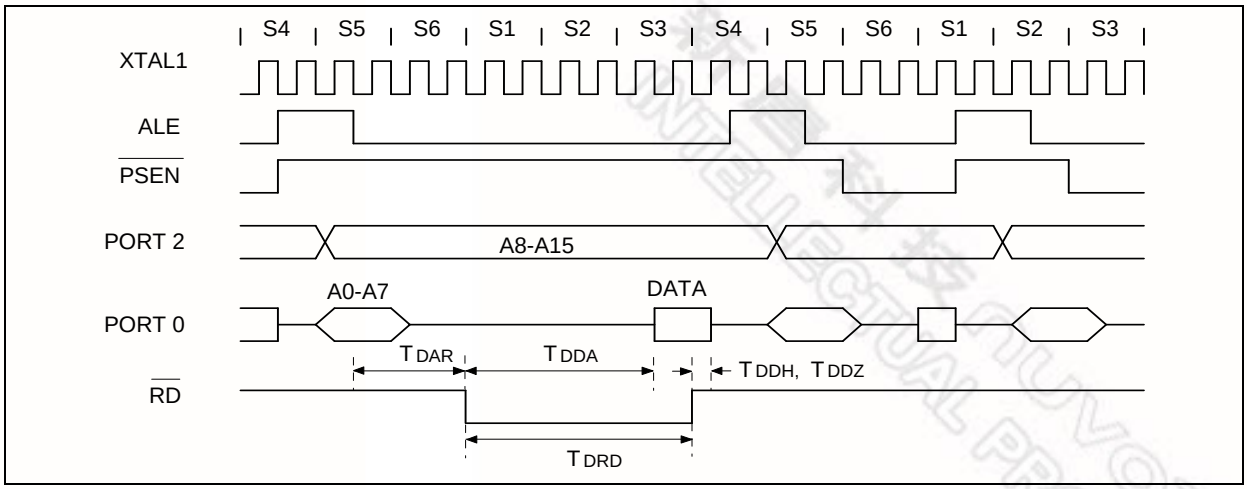


NOTE1: The possible situation that you need to enter F04KBOOT mode is when the APROM program can not run normally and W78E516D/W78E058D can not jump to LDROM to execute on chip pro-

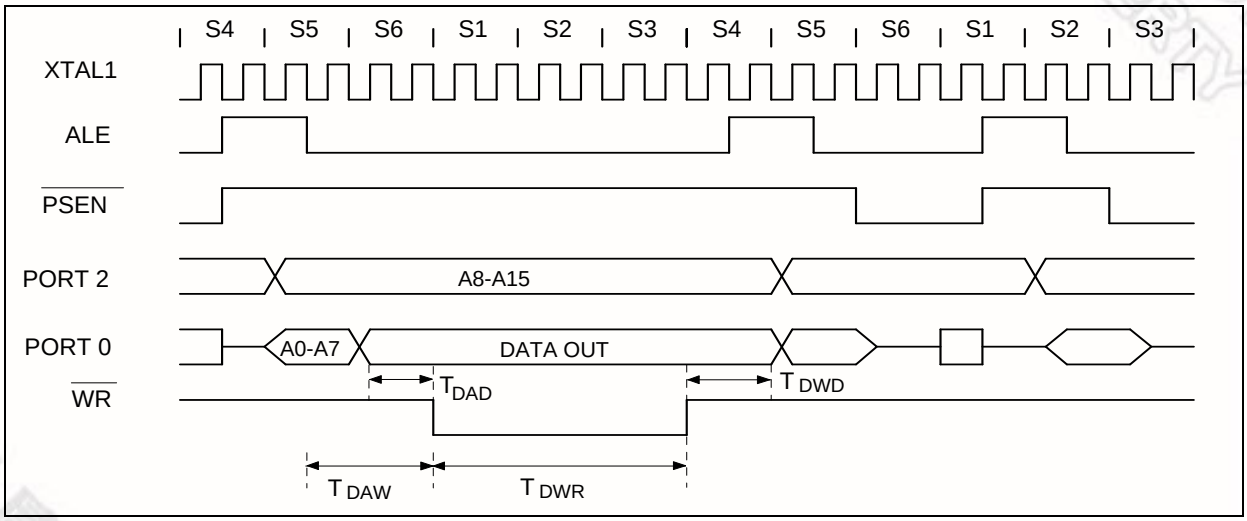
gramming function. Then you can use this F04KBOOT mode to force the W78E516D/W78E058D jump to LDROM and run on chip programming procedure. When you design your system, you can connect the pins P26, P27 to switches or jumpers. For example in a CD ROM system, you can connect the P26 and P27 to PLAY and EJECT buttons on the panel. When the APROM program is fail to execute the normal application program. User can press both two buttons at the same time and then switch on the power of the personal computer to force the W78E516D/W78E058D to enter the F04KBOOT mode. After power on of personal computer, you can release both PLAY and EJECT button.

NOTE2: In application system design, user must take care the P2, P3, ALE, /EA and /PSEN pin value at reset to avoid W78E516D/W78E058D entering the programming mode or F04KBOOT mode in normal operation.

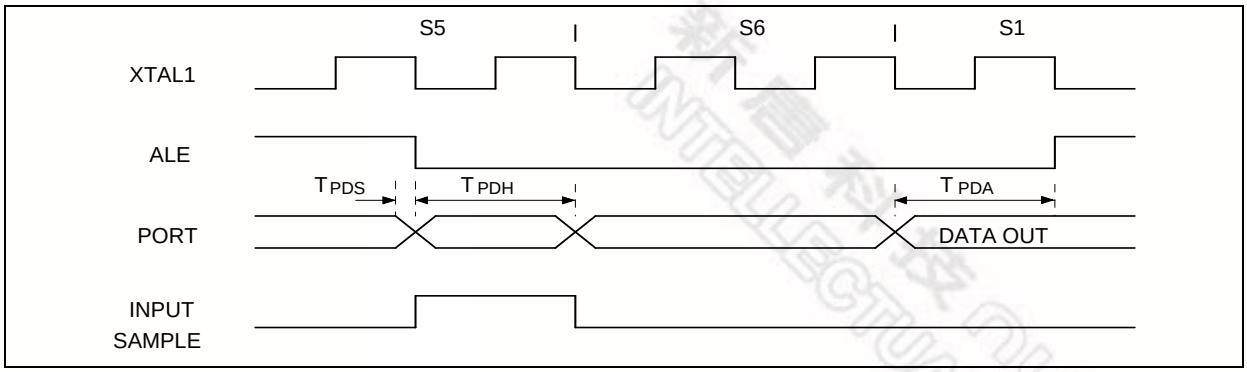
21.4.2 Data Read Cycle



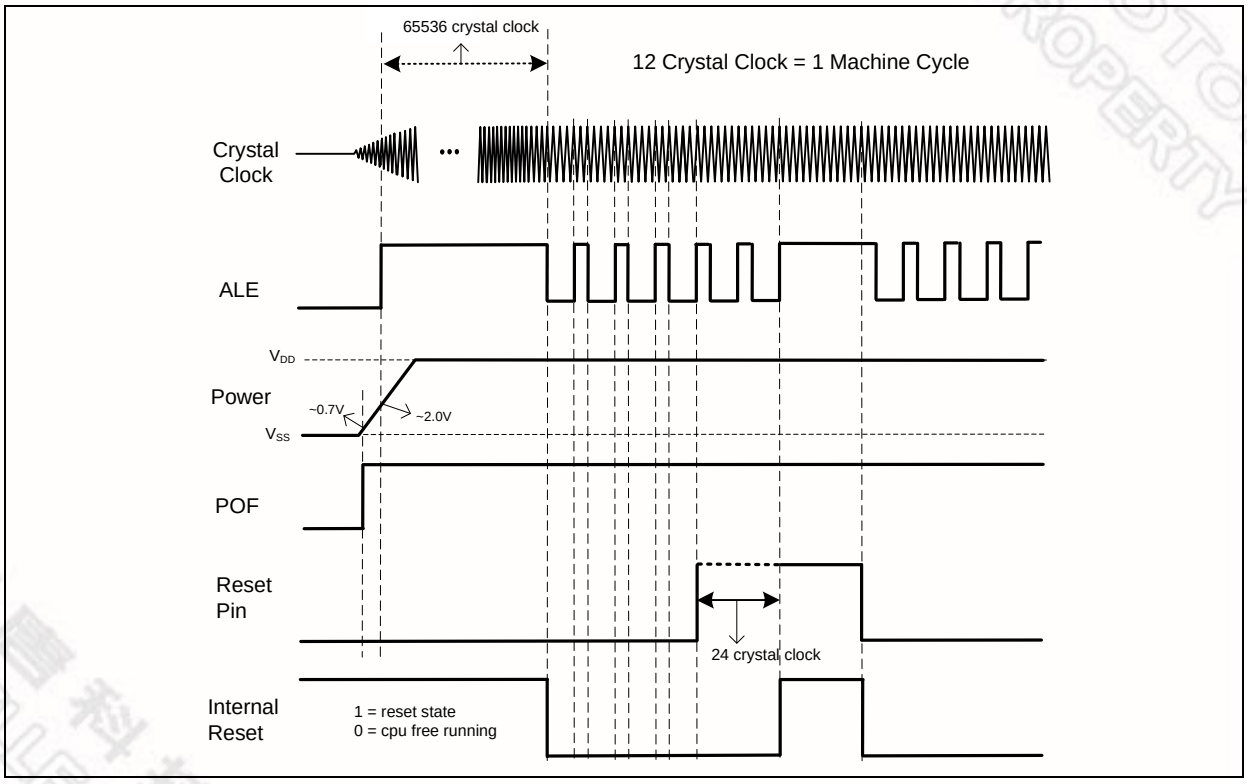
21.4.3 Data Write Cycle



21.4.4 Port Access Cycle



21.4.5 Reset Pin Access Cycle



23 REVISION HISTORY

VERSION	DATE	PAGE	DESCRIPTION
A01	June 24, 2008	-	Initial Issued
A02	August 21,2008	7,8	Update pin assignment.
A03	September 1,2008	-	Update W78I516D/W78I058D parts
A04	November 3,2008		Update DC table typo error
A05	January 7,2009	74	Update V_{IL} and V_{IH} .
A06	April 2, 2009	- - -	Update DC table Revise some typing errors Rename SFR 86H POR register to P0UPR
A07	April 22,2009	70	Revise the Application Circuit
A08	June 30,2009	6 65 70 71	1. Revise the Table 3-1 2. Add the picture for “F04KBOOT Mode” of P4.3 3. Revise the ISP Flow Chart 4. Revise the CONFIG BITS 5. Remove the “Preliminary” character each page
A09	Feb 15,2011	18 65 70 79	1. Revise the default reset value for CHPCON 2. Add the reset-pin reset can entry the F04KBOOT mode. 3. Revise the flow chart of ISP programming 4. Revise the CONFIG BITS 5. Add the external reset pin timing