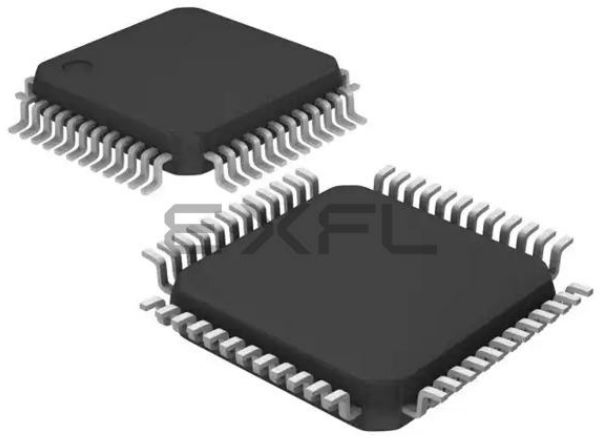

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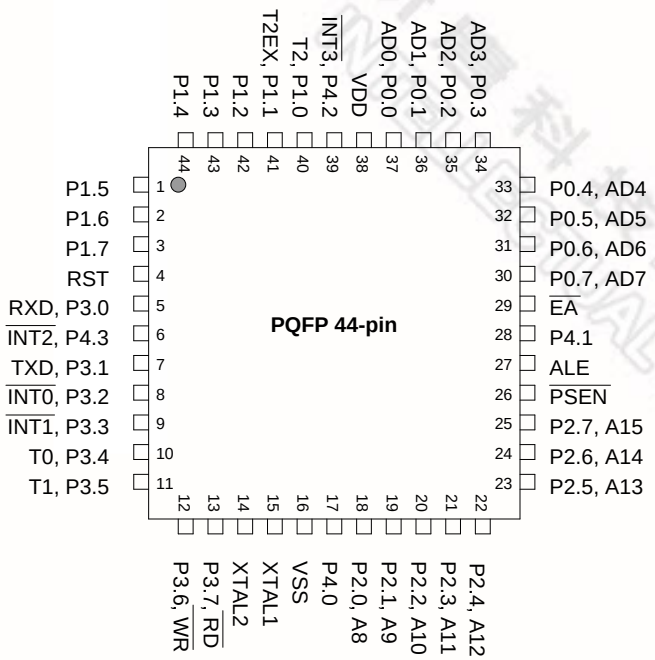
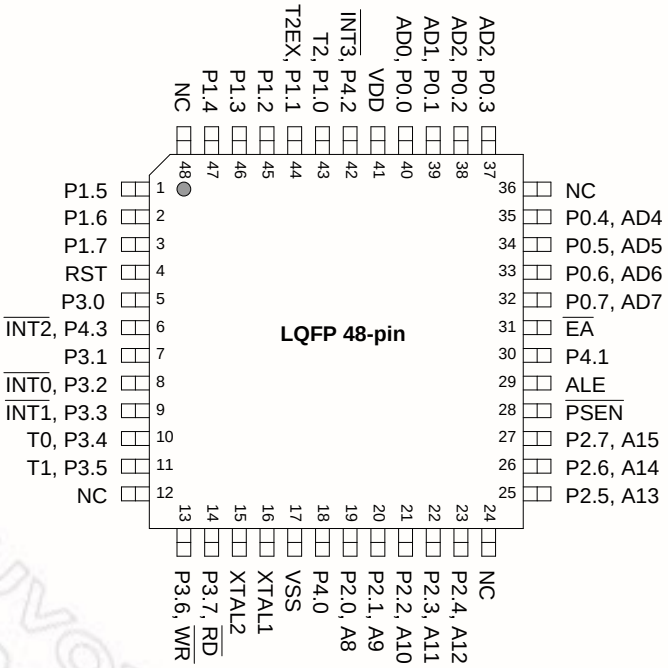
Details	
Product Status	Active
Core Processor	8052
Core Size	8-Bit
Speed	40MHz
Connectivity	EBI/EMI, UART/USART
Peripherals	POR, WDT
Number of I/O	36
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/w78e516dlg

2 FEATURES

- Fully static design 8-bit CMOS microcontroller
- Optional 12T or 6T mode
  - 12T Mode, 12 clocks per machine cycle operation (default), Speed up to 40 MHz/5V
  - 6T Mode, 6 clocks per machine cycle operation set by the writer, Speed up to 20 MHz/5V
- Wide supply voltage of 2.4 to 5.5V
- Temperature grade is (-40°C~85°C)
- 64K/32K bytes of in-system programmable FLASH EPROM for Application Program (APROM)
- 4K bytes of auxiliary FLASH EPROM for Loader Program (LDROM)
- Low standby current at full supply voltage
- 512 bytes of on-chip RAM. (include 256 bytes of AUX-RAM, software selectable)
- 64K bytes program memory address space and 64K bytes data memory address space
- One 4-bit multipurpose programmable port, additional $\overline{INT2}$ / $\overline{INT3}$
- Support Watch Dog Timer
- Three 16-bit timer/counters
- One full duplex serial port
- 8-sources, 2-level interrupt capability
- Software Reset
- Built-in power management with idle mode and power down mode
- Code protection
- Packages:
  - Lead Free (RoHS) DIP 40: W78E516DDG
  - Lead Free (RoHS) PLCC 44: W78E516DPG
  - Lead Free (RoHS) PQFP 44: W78E516DFG
  - Lead Free (RoHS) LQFP 48: W78E516DLG
  - Lead Free (RoHS) DIP 40: W78E058DDG
  - Lead Free (RoHS) PLCC 44: W78E058DPG
  - Lead Free (RoHS) PQFP 44: W78E058DFG
  - Lead Free (RoHS) LQFP 48: W78E058DLG


P1.4
P1.3
P1.2
T2EX, P1.1
T2, P1.0
INT3, P4.2
VDD
AD0, P0.0
AD1, P0.1
AD2, P0.2
AD3, P0.3
P1.5
P1.6
P1.7
RST
RXD, P3.0
INT2, P4.3
TXD, P3.1
INT0, P3.2
INT1, P3.3
T0, P3.4
T1, P3.5
P0.4, AD4
P0.5, AD5
P0.6, AD6
P0.7, AD7
EA
P4.1
ALE
PSEN
P2.7, A15
P2.6, A14
P2.5, A13
P3.6, WR
P3.7, RD
XTAL2
XTAL1
VSS
P4.0
P2.0, A8
P2.1, A9
P2.2, A10
P2.3, A11
P2.4, A12
PQFP 44-pin


NC
P1.4
P1.3
P1.2
T2EX, P1.1
T2, P1.0
INT3, P4.2
VDD
AD0, P0.0
AD1, P0.1
AD2, P0.2
AD2, P0.3
P1.5
P1.6
P1.7
RST
P3.0
INT2, P4.3
P3.1
INT0, P3.2
INT1, P3.3
T0, P3.4
T1, P3.5
NC
NC
P0.4, AD4
P0.5, AD5
P0.6, AD6
P0.7, AD7
EA
P4.1
ALE
PSEN
P2.7, A15
P2.6, A14
P2.5, A13
P3.6, WR
P3.7, RD
XTAL2
XTAL1
VSS
P4.0
P2.0, A8
P2.1, A9
P2.2, A10
P2.3, A11
P2.4, A12
NC
LQFP 48-pin

5 PIN DESCRIPTIONS

SYMBOL	TYPE	DESCRIPTIONS
$\overline{EA}$	I	**EXTERNAL ACCESS ENABLE:** This pin forces the processor to execute the external ROM. The ROM address and data will not be present on the bus if the $\overline{EA}$ pin is high and the program counter is within the internal ROM area. Otherwise they will be present on the bus.
$\overline{PSEN}$	O H	**PROGRAM STORE ENABLE:** $\overline{PSEN}$ enables the external ROM data in the Port 0 address/data bus. When internal ROM access is performed, no $\overline{PSEN}$ strobe signal outputs originate from this pin.
ALE	O H	**ADDRESS LATCH ENABLE:** ALE is used to enable the address latch that separates the address from the data on Port 0. ALE runs at 1/6th of the oscillator frequency. An ALE pulse is omitted during external data memory accesses.
RST	I L	**RESET:** A high on this pin for two machine cycles while the oscillator is running resets the device.
XTAL1	I	**CRYSTAL 1:** This is the crystal oscillator input. This pin may be driven by an external clock.
XTAL2	O	**CRYSTAL 2:** This is the crystal oscillator output. It is the inversion of XTAL1.
VSS	I	**GROUND:** ground potential.
VDD	I	**POWER SUPPLY:** Supply voltage for operation.
P0.0–P0.7	I/O D	**PORT 0:** Port 0 is an **open-drain bi-directional I/O port**. This port also provides a multiplexed low order address/data bus during accesses to external memory.
P1.0–P1.7	I/O H	**PORT 1**: Port 1 is a bi-directional I/O port with internal pull-ups. The bits have alternate functions which are described below: T2(P1.0): Timer/Counter 2 external count input T2EX(P1.1): Timer/Counter 2 Reload/Capture/Direction control
P2.0–P2.7	I/O H	**PORT 2:** Port 2 is a bi-directional I/O port with internal pull-ups. This port also provides the upper address bits for accesses to external memory.
P3.0–P3.7	I/O H	**PORT 3:** Port 3 is a bi-directional I/O port with internal pull-ups. All bits have alternate functions, which are described below: RXD(P3.0): Serial Port 0 input TXD(P3.1): Serial Port 0 output $\overline{INT0}$ (P3.2) : External Interrupt 0 $\overline{INT1}$ (P3.3) : External Interrupt 1 T0(P3.4) : Timer 0 External Input T1(P3.5) : Timer 1 External Input $\overline{WR}$ (P3.6) : External Data Memory Write Strobe $\overline{RD}$ (P3.7) : External Data Memory Read Strobe
P4.0–P4.3	I/O H	**PORT 4:** Another bit-addressable bidirectional I/O port P4. P4.3 and P4.2 are alternative function pins. It can be used as general I/O port or external interrupt input sources ($\overline{INT2}$ / $\overline{INT3}$).

* Note : **TYPE** I: input, O: output, I/O: bi-directional, H: pull-high, L: pull-low, D: open drain

7.7.5 Stack Pointer

The W78E516D/W78E058D series has an 8-bit Stack Pointer which points to the top of the Stack. This stack resides in the Scratch Pad RAM in the W78E516D/W78E058D series. Hence the size of the stack is limited by the size of this RAM.

7.7.6 Scratch-pad RAM

The W78E516D/W78E058D series has a 256 bytes on-chip scratch-pad RAM. This can be used by the user for temporary storage during program execution. A certain section of this RAM is bit address-able, and can be directly addressed for this purpose.

7.7.7 AUX-RAM

AUX-RAM 0H~255H is addressed indirectly as the same way to access external data memory with the MOVX instruction. The data memory region is from 0000H to 00FFH. Memory MAP shows the mem-ory map for this product series. W78E516D/W78E058D series can read/write 256 bytes AUX RAM by the MOVX instruction.

BIT	NAME	FUNCTION
7-0	P42AL.[7:0]	The Base address register for comparator of P4.2. P42AL contains the low-order byte of address.

P4.2 Base Address High Byte Register

Bit:	7	6	5	4	3	2	1	0
	P42AH.7	P42AH.6	P42AH.5	P42AH.4	P42AH.3	P42AH.2	P42AH.1	P42AH.0

Mnemonic:P42AH Address: ADh

BIT	NAME	FUNCTION
7-0	P42AH.[7:0]	The Base address register for comparator of P4.2. P42AH contains the High-order byte of address.

Port 2 Expanded Control

Bit:	7	6	5	4	3	2	1	0
	P43CSIN	P42CSIN	P41CSIN	P40CSIN	-	-	-	-

Mnemonic: P2ECON Address:AEh

BIT	NAME	FUNCTION
7	P43CSINV	The active polarity of P4.3 when pin P4.3 is defined as read and/or write strobe signal. 1 : P4.3 is active high when pin P4.3 is defined as read and/or write strobe signal. 0 : P4.3 is active low when pin P4.3 is defined as read and/or write strobe signal.
6	P42CSINV	The similarity definition as P43SINV.
5	P41CSINV	The similarity definition as P43SINV.
4	P40CSINV	The similarity definition as P43SINV.

Port 3

Bit:	7	6	5	4	3	2	1	0
	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0

Mnemonic: P3 Address: B0h

P3.7-0: General purpose Input/Output port. Most instructions will read the port pins in case of a port read access, however in case of read-modify-write instructions, the port latch is read. These alternate functions are described below:

BIT	NAME	FUNCTION
7	P3.7	$\overline{RD}$
6	P3.6	$\overline{WR}$
5	P3.5	T1
4	P3.4	T0

Op-code	HEX Code	Bytes	W78E516D/W78E058D series Clock cycles
XRL A, R4	6C	1	12
XRL A, R5	6D	1	12
XRL A, R6	6E	1	12
XRL A, R7	6F	1	12
XRL A, @R0	66	1	12
XRL A, @R1	67	1	12
XRL A, direct	65	2	12
XRL A, #data	64	2	12
XRL direct, A	62	2	12
XRL direct, #data	63	3	24
CLR A	E4	1	12
CPL A	F4	1	12
RL A	23	1	12
RLC A	33	1	12
RR A	03	1	12
RRC A	13	1	12
SWAP A	C4	1	12
MOV A, R0	E8	1	12
MOV A, R1	E9	1	12
MOV A, R2	EA	1	12
MOV A, R3	EB	1	12
MOV A, R4	EC	1	12
MOV A, R5	ED	1	12
MOV A, R6	EE	1	12
MOV A, R7	EF	1	12
MOV A, @R0	E6	1	12
MOV A, @R1	E7	1	12
MOV A, direct	E5	2	12
MOV A, #data	74	2	12
MOV R0, A	F8	1	12
MOV R1, A	F9	1	12
MOV R2, A	FA	1	12
MOV R3, A	FB	1	12
MOV R4, A	FC	1	12

13 RESET CONDITIONS

The user has several hardware related options for placing the W78E516D/W78E058D into reset condition. In general, most register bits go to their reset value irrespective of the reset condition, but there are a few flags whose state depends on the source of reset. The user can use these flags to determine the cause of reset using software.

13.1 Sources of reset

13.1.1 External Reset

The device continuously samples the RST pin at state S5P2 of every machine cycle. Therefore the RST pin must be held for at least 2 machine cycles (24 clock cycles) to ensure detection of a valid RST high. The reset circuitry then synchronously applies the internal reset signal. Thus the reset is a synchronous operation and requires the clock to be running to cause an external reset. For more timing descript, please reference the character 21.4.5 (Page 79).

Once the device is in reset condition, it will remain so as long as RST is 1. Even after RST is deactivated, the device will continue to be in reset state for up to two machine cycles, and then begin program execution from 0000h. There is no flag associated with the external reset condition.

13.1.2 Watchdog Timer Reset

The Watchdog timer is a free running timer with programmable time-out intervals. The user can clear the watchdog timer at any time, causing it to restart the count. When the time-out interval is reached an interrupt flag is set. If the Watchdog reset is enabled and the watchdog timer is not cleared, the watchdog timer will generate a reset. This places the device into the reset condition. The reset condition is maintained by hardware for two machine cycles. Once the reset is removed the device will begin execution from 0000h.

13.1.3 Software Reset

The W78E516D/W78E058D offers a software reset to switch back to the AP Flash EPROM. Setting CHPCON bits 0, 1 and 7 to logic-1 creates a software reset to reset the CPU.

13.1.4 RESET STATE

Most of the SFRs and registers on the device will go to the same condition in the reset state. The Program Counter is forced to 0000h and is held there as long as the reset condition is applied. However, the reset state does not affect the on-chip RAM. The data in the RAM will be preserved during the reset. However, the stack pointer is reset to 07h, and therefore the stack contents will be lost. The RAM contents will be lost if the VDD falls below approximately 2V, as this is the minimum voltage level required for the RAM to operate normally. Therefore after a first time power on reset the RAM contents will be indeterminate. During a power fail condition, if the power falls below 2V, the RAM contents are lost.

After a reset most SFRs are cleared. Interrupts and Timers are disabled. The Watchdog timer is disabled if the reset source was a POR. The port SFRs have 0FFh written into them which puts the port pins in a high state.

The interrupt flags are sampled every machine cycle. In the same machine cycle, the sampled interrupts are polled and their priority is resolved. If certain conditions are met then the hardware will execute an internally generated LCALL instruction which will vector the process to the appropriate interrupt vector address. The conditions for generating the LCALL are;

1. An interrupt of equal or higher priority is not currently being serviced.
2. The current polling cycle is the last machine cycle of the instruction currently being executed.
3. The current instruction does not involve a write to IE, IP, XICON registers and is not a RETI.

If any of these conditions are not met, then the LCALL will not be generated. The polling cycle is repeated every machine cycle, with the interrupts sampled in the same machine cycle. If an interrupt flag is active in one cycle but not responded to, and is not active when the above conditions are met, the denied interrupt will not be serviced. This means that active interrupts are not remembered; every polling cycle is new.

The processor responds to a valid interrupt by executing an LCALL instruction to the appropriate service routine. This may or may not clear the flag which caused the interrupt. In case of Timer interrupts, the TF0 or TF1 flags are cleared by hardware whenever the processor vectors to the appropriate timer service routine. In case of external interrupt, /INT0 and /INT1, the flags are cleared only if they are edge triggered. In case of Serial interrupts, the flags are not cleared by hardware. In the case of Timer 2 interrupt, the flags are not cleared by hardware. The hardware LCALL behaves exactly like the software LCALL instruction. This instruction saves the Program Counter contents onto the Stack, but does not save the Program Status Word PSW. The PC is reloaded with the vector address of that interrupt which caused the LCALL. These address of vector for the different sources are as shown on below table. The vector table is not evenly spaced; this is to accommodate future expansions to the device family.

Execution continues from the vectored address till an RETI instruction is executed. On execution of the RETI instruction the processor pops the Stack and loads the PC with the contents at the top of the stack. The user must take care that the status of the stack is restored to what is was after the hardware LCALL, if the execution is to return to the interrupted program. The processor does not notice anything if the stack contents are modified and will proceed with execution from the address put back into PC. Note that a RET instruction would perform exactly the same process as a RETI instruction, but it would not inform the Interrupt Controller that the interrupt service routine is completed, and would leave the controller still thinking that the service routine is underway.

Each interrupt source can be individually enabled or disabled by setting or clearing a bit in registers IE. The IE register also contains a global disable bit, EA, which disables all interrupts at once.

Each interrupt source can be individually programmed to one of 2 priority levels by setting or clearing bits in the IP registers. An interrupt service routine in progress can be interrupted by a higher priority interrupt, but not by another interrupt of the same or lower priority. The highest priority interrupt service cannot be interrupted by any other interrupt source. So, if two requests of different priority levels are received simultaneously, the request of higher priority level is serviced.

If requests of the same priority level are received simultaneously, an internal polling sequence determines which request is serviced. This is called the arbitration ranking. Note that the arbitration ranking is only used to resolve simultaneous requests of the same priority level.

enabled an interrupt will occur. The selection of the time-base in the timer mode is similar to that in Mode 0. The gate function operates similarly to that in Mode 0.

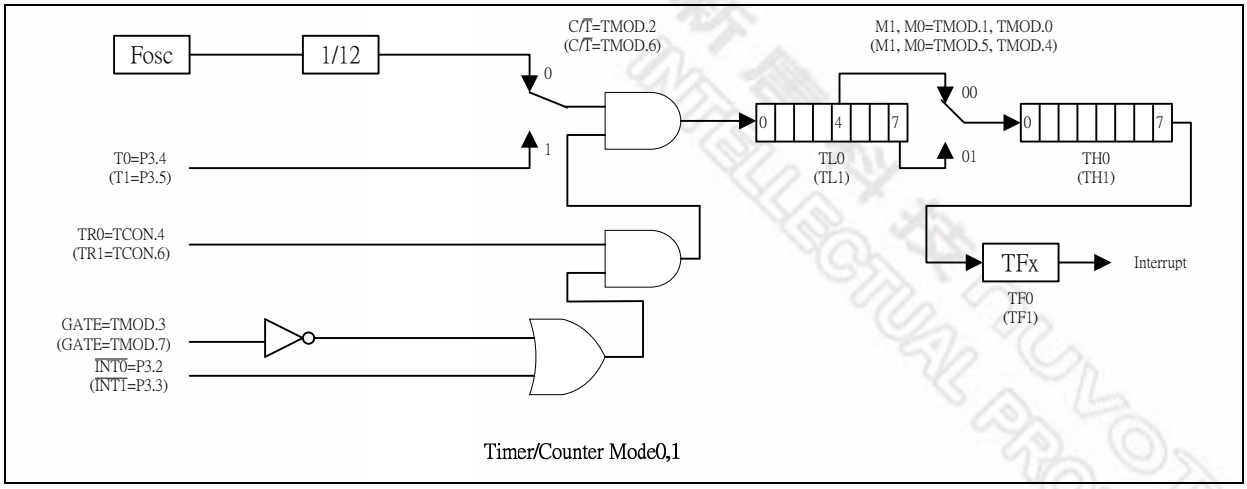


Figure 14- 1 Timer/Counters 0 & 1 in Mode 0,1

14.2.3 Mode 2

In Mode 2, the timer/counter is in the Auto Reload Mode. In this mode, TLx acts as an 8-bit count register, while THx holds the reload value. When the TLx register overflows from FFh to 00h, the TFx bit in TCON is set and TLx is reloaded with the contents of THx, and the counting process continues from here. The reload operation leaves the contents of the THx register unchanged. Counting is enabled by the TRx bit and proper setting of GATE and $\overline{INTx}$. As in the other two modes 0 and 1 mode 2 allows counting of clock/12 or pulses on pin Tn.

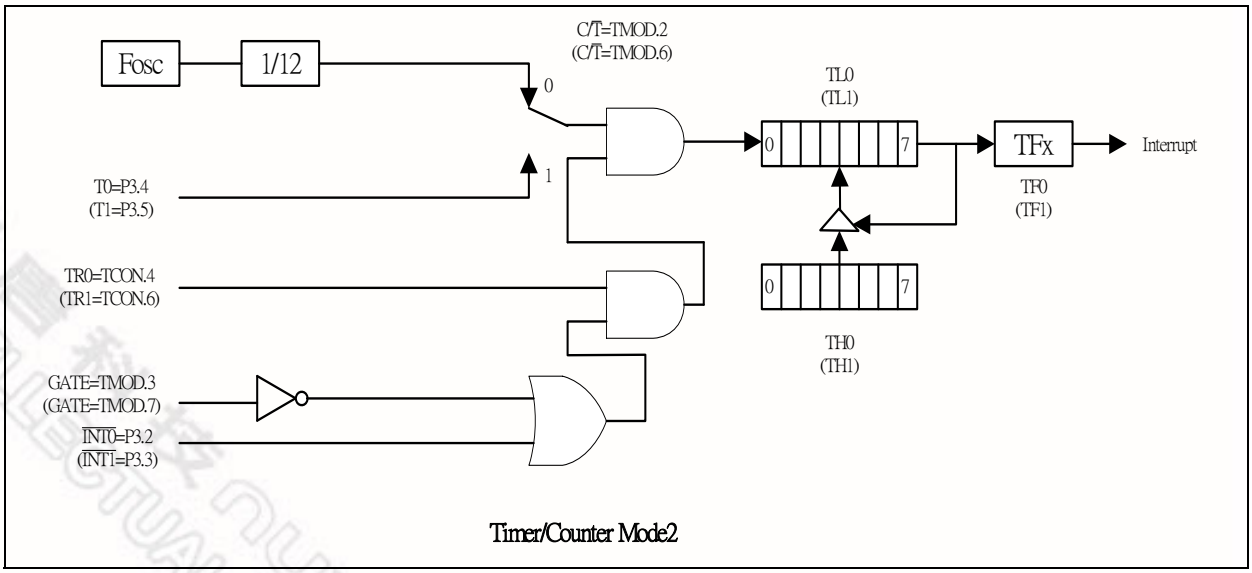


Figure 14- 2 Timer/Counter 0 & 1 in Mode 2

14.2.4 Mode 3

Mode 3 has different operating methods for the two timer/counters. For timer/counter 1, mode 3 simply freezes the counter. Timer/Counter 0, however, configures TL0 and TH0 as two separate 8 bit count registers in this mode. The logic for this mode is shown in the figure. TL0 uses the Timer/Counter 0 control bits $C/\overline{T}$, GATE, TR0, $\overline{INT0}$ and TF0. The TL0 can be used to count clock cycles (clock/12) or 1-to-0 transitions on pin T0 as determined by C/T (TMOD.2). TH0 is forced as a clock cycle counter (clock/12) and takes over the use of TR1 and TF1 from Timer/Counter 1. Mode 3 is used in cases where an extra 8 bit timer is needed. With Timer 0 in Mode 3, Timer 1 can still be used in Modes 0, 1 and 2, but its flexibility is somewhat limited. While its basic functionality is maintained, it no longer has control over its overflow flag TF1 and the enable bit TR1. Timer 1 can still be used as a timer/counter and retains the use of GATE and INT1 pin. In this condition it can be turned on and off by switching it out of and into its own Mode 3. It can also be used as a baud rate generator for the serial port.

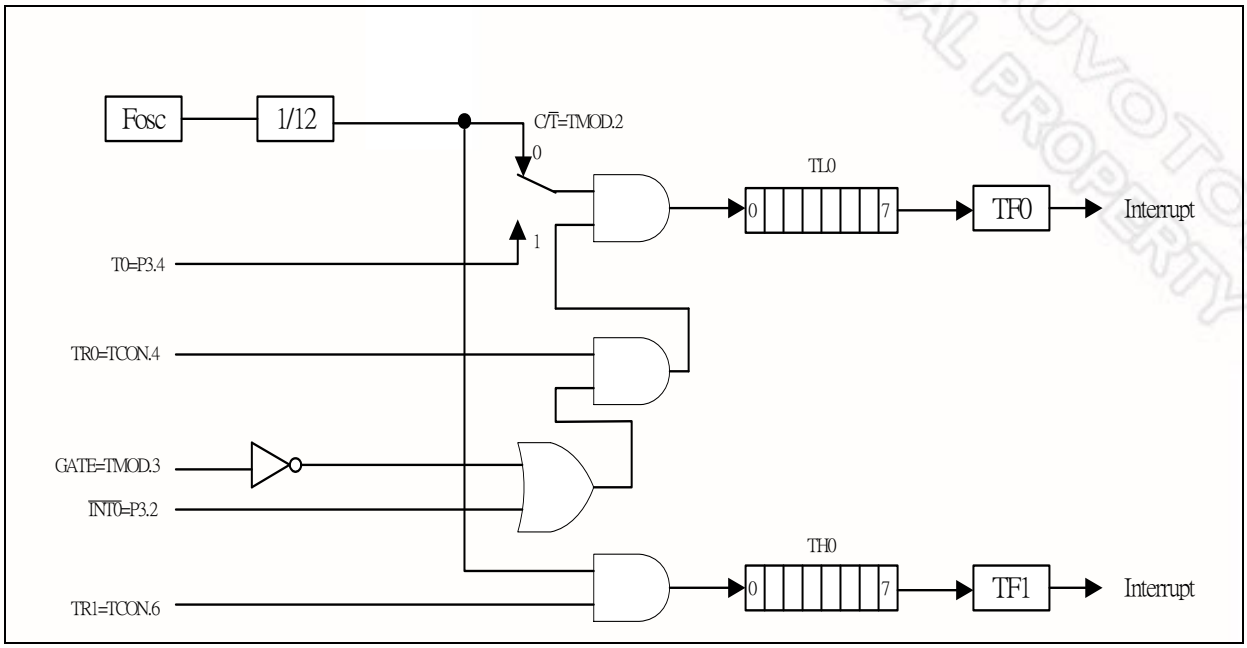


Figure 14-3 Timer/Counter Mode 3

14.3 Timer/Counter 2

Timer/Counter 2 is a 16 bit counter. Timer/Counter 2 is equipped with a capture/reload capability. As with the Timer 0 and Timer 1 counters, there exists considerable flexibility in selecting and controlling the clock, and in defining the operating mode. The clock source for Timer/Counter 2 may be selected for either the external T2 pin (C/T2 = 1) or the crystal oscillator, which is divided by 12 (C/T2 = 0). The clock is then enabled when TR2 is a 1, and disabled when TR2 is a 0.

14.3.1 Capture Mode

The capture mode is enabled by setting the $CP/\overline{RL2}$ bit in the T2CON register to a 1. In the capture mode, Timer/Counter 2 serves as a 16 bit up counter. When the counter rolls over from 0FFFFh to 0000h, the TF2 bit is set, which will generate an interrupt request. If the EXEN2 bit is set, then a negative transition of T2EX pin will cause the value in the TL2 and TH2 register to be captured by the RCAP2L and RCAP2H registers. This action also causes the EXF2 bit in T2CON to be set, which will

14.3.3 Baud Rate Generator Mode

The baud rate generator mode is enabled by setting either the RCLK or TCLK bits in T2CON register. While in the baud rate generator mode, Timer/Counter 2 is a 16 bit counter with auto reload when the count rolls over from 0FFFFh. However, rolling over does not set the TF2 bit. If EXEN2 bit is set, then a negative transition of the T2EX pin will set EXF2 bit in the T2CON register and cause an interrupt request.

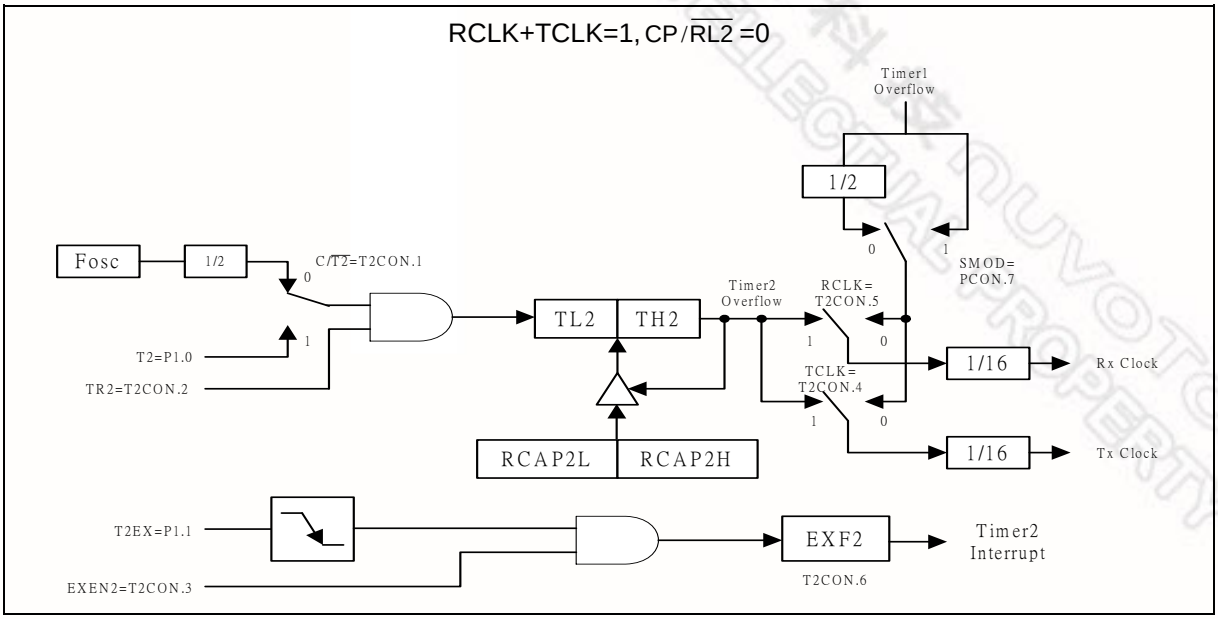


Figure 14- 6 Baud Rate Generator Mode

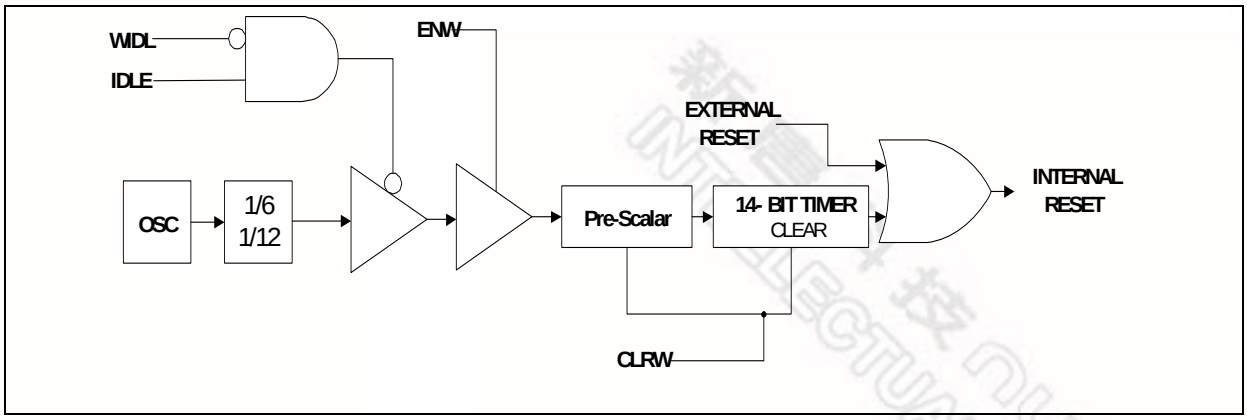


Figure 15- 1 Watchdog Timer Block Diagram

Typical Watch-Dog time-out period when OSC = 20 MHz

PS2	PS1	PS0	Watchdog time-out period
0	0	0	19.66 mS
0	0	1	39.32 mS
0	1	0	78.64 mS
0	1	1	157.28 mS
1	0	0	314.57 mS
1	0	1	629.14 mS
1	1	0	1.25 S
1	1	1	2.50 S

Table 15- 1 Watch-Dog time-out period

The 16 states of the counter effectively divide the bit time into 16 slices. The bit detection is done on a best of three basie. The bit detector samples the RxD pin, at the 8th, 9th and 10th counter states. By using a majority 2 of 3 voting system, the bit value is selected. This is done to improve the noise rejection feature of the serial port. If the first bit detected after the falling edge of RxD pin is not 0, then this indicates an invalid start bit, and the reception is immediately aborted. The serial port again looks for a falling edge in the RxD line. If a valid start bit is detected, then the rest of the bits are also detected and shifted into the SBUF.

After shifting in 8 data bits, there is one more shift to do, after which the SBUF and RB8 are loaded and RI is set. However certain conditions must be met before the loading and setting of RI can be done.

1. RI must be 0 and
2. Either SM2 = 0, or the received stop bit = 1.

If these conditions are met, then the stop bit goes to RB8, the 8 data bits go into SBUF and RI is set. Otherwise the received frame may be lost. After the middle of the stop bit, the receiver goes back to looking for a 1-to-0 transition on the RxD pin.

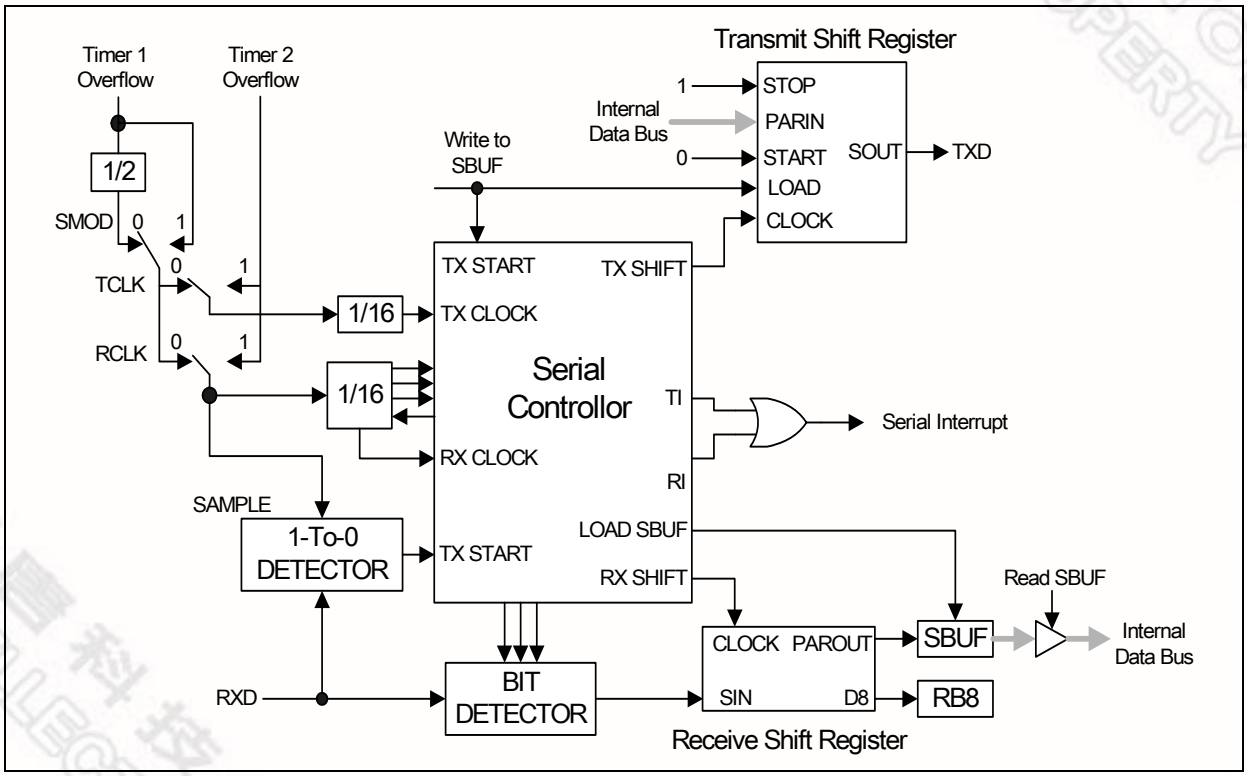


Figure 16- 2 Serial port mode 1

16.3 MODE 2

This mode uses a total of 11 bits in asynchronous full-duplex communication. The functional description is shown in the figure below. The frame consists of one start bit (0), 8 data bits (LSB first), a pro-

gramming function. Then you can use this F04KBOOT mode to force the W78E516D/W78E058D jump to LDROM and run on chip programming procedure. When you design your system, you can connect the pins P26, P27 to switches or jumpers. For example in a CD ROM system, you can connect the P26 and P27 to PLAY and EJECT buttons on the panel. When the APROM program is fail to execute the normal application program. User can press both two buttons at the same time and then switch on the power of the personal computer to force the W78E516D/W78E058D to enter the F04KBOOT mode. After power on of personal computer, you can release both PLAY and EJECT button.

NOTE2: In application system design, user must take care the P2, P3, ALE, /EA and /PSEN pin value at reset to avoid W78E516D/W78E058D entering the programming mode or F04KBOOT mode in normal operation.

18 ISP(IN-SYSTEM PROGRAMMING)

ISP is the ability of programmable MCU to be programmed while F/W code in AP-ROM or LD-ROM (ISP work voltage 3.3-5.5V).

The W78E058D/516D equips one 32K byte of main ROM bank for application program (called APROM) and one 4K byte of auxiliary ROM bank for loader program (called LDROM). In the normal operation, the microcontroller executes the code in the APROM. If the content of APROM needs to be modified, the W78E058D/516D allows user to activate the In-System Programming (ISP) mode by setting the CHPCON register. **The CHPCON is read-only by default, software must write two specific values 87H, then 59H sequentially to the CHPENR register to enable the CHPCON write attribute. Writing CHPENR register with the values except 87H and 59H will close CHPCON register write attribute.** The W78E058D/516D achieves all in-system programming operations including enter/exit ISP Mode, program, erase, read ... etc, during device in the idle mode. Setting the bit CHPCON.0 the device will enter in-system programming mode after a wake-up from idle mode. Because device needs proper time to complete the ISP operations before awaken from idle mode, software may use timer interrupt to control the duration for device wake-up from idle mode. To perform ISP operation for revising contents of APROM, software located at APROM setting the CHPCON register then enter idle mode, after awaken from idle mode the device executes the corresponding interrupt service routine in LDROM. Because the device will clear the program counter while switching from APROM to LDROM, the first execution of RETI instruction in interrupt service routine will jump to 00H at LDROM area. The device offers a software reset for switching back to APROM while the content of APROM has been updated completely. **Setting CHPCON register bit 0, 1 and 7 to logic-1 will result a software reset to reset the CPU**. The software reset serves as a external reset. This in-system programming feature makes the job easy and efficient in which the application needs to update firmware frequently. In some applications, the in-system programming feature make it possible to easily update the system firmware without opening the chassis.

SFRAH, SFRAL: The objective address of on-chip ROM in the in-system programming mode. SFRAH contains the high-order byte of address, SFRAL contains the low-order byte of address.

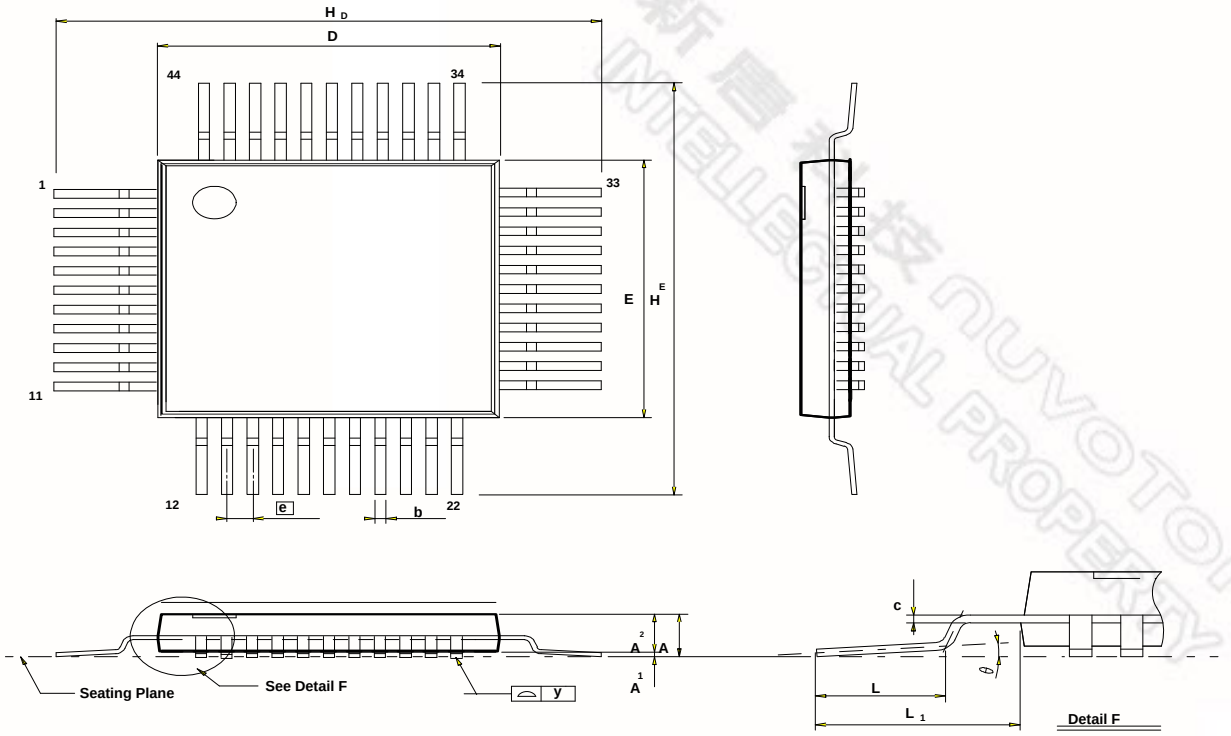
SFRFD: The programming data for on-chip ROM in programming mode.

SFRCN: The control byte of on-chip ROM programming mode.

SFRCN (C7)

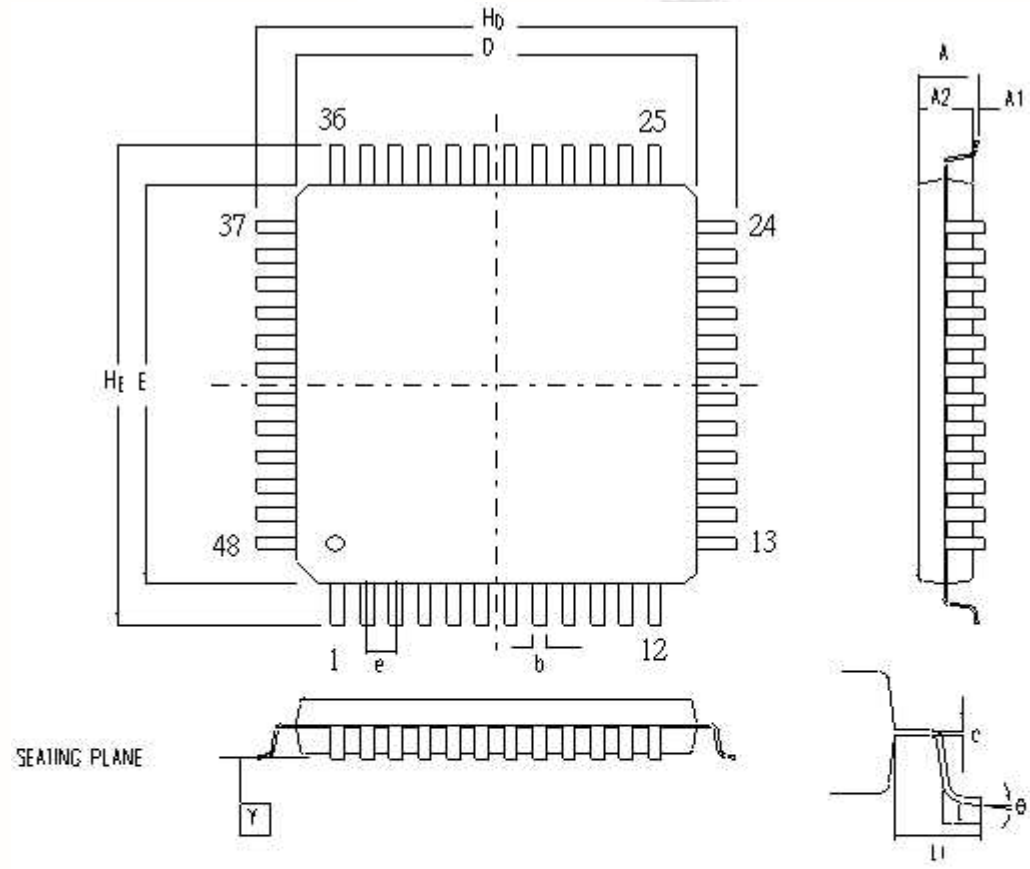
BIT	NAME	FUNCTION
7	-	Reserve.
6	WFWIN	On-chip ROM bank select for in-system programming. 0: 32K/64K bytes ROM bank is selected as destination for re-programming. 1: 4K bytes ROM bank is selected as destination for re-programming.
5	OEN	ROM output enable.
4	CEN	ROM chip enable.
3, 2, 1, 0	CTRL [3:0]	The flash control signals

22.3 44-pin PQFP



Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	-	—	—	-
A_1	0.002	0.01	0.02	0.05	0.25	0.5
A_2	0.075	0.081	0.087	1.90	2.05	2.20
b	0.01	0.014	0.018	0.25	0.35	0.45
c	0.004	0.006	0.010	0.10	0.15	0.25
D	0.390	0.394	0.398	9.9	10.00	10.1
E	0.390	0.394	0.398	9.9	10.00	10.1
e	—	.0315	—	—	0.80	—
H_D	0.510	0.520	0.530	12.95	13.20	13.45
H_E	0.510	0.520	0.530	12.95	13.20	13.45
L	0.025	0.031	0.037	0.65	0.8	0.95
L_1	—	0.063	—	—	1.60	—
y	—	—	0.004	—	—	0.10
θ	0 °	—	10 °	0 °	—	10 °

22.4 48-pin LQFP



Controlling dimension : Millimeters

Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.063	—	—	1.60
A_1	0.002	0.004	0.006	0.05	0.10	0.15
A_2	0.053	0.055	0.057	1.35	1.40	1.45
b	0.006	0.008	0.010	0.15	0.20	0.25
c	0.004	0.006	0.008	0.10	0.15	0.20
D	0.272	0.276	0.280	6.90	7.00	7.10
E	0.272	0.276	0.280	6.90	7.00	7.10
e	0.014	0.020	0.026	0.35	0.50	0.65
H_D	0.350	0.354	0.358	8.90	9.00	9.10
H_E	0.350	0.354	0.358	8.90	9.00	9.10
L	0.018	0.024	0.030	0.45	0.60	0.75
L_1	—	0.039	—	—	1.00	—
Y	—	—	0.004	—	—	0.10
θ	0°	—	7°	0°	—	7°

```
            MOV     TCON,#00H               ;TR=0 TIMER0 STOP
            MOV      IP,#00H                ;IP=00H
            MOV      IE,#82H                ;TIMER0 INTERRUPT ENABLE FOR
                                            ;WAKE-UP FROM IDLE MODE
            MOV     R6,#FEH                 ;TL0=FEH
            MOV     R7,#FFH                 ;TH0=FFH
            MOV     TL0,R6
            MOV     TH0,R7
            MOV     TMOD,#01H               ;TMOD=01H,SET TIMER0 A 16-BIT TIMER
            MOV      TCON,#10H              ;TCON=10H,TR0=1,GO
            MOV      PCON,#01H              ;ENTER IDLE MODE FOR LAUNCHING
                                            ;THE IN-SYSTEM PROGRAMMABILITY
;*****************************************************************************
;* Normal mode APROM program: depending user's application
;*****************************************************************************
NORMAL_MODE:
                                .
                                    ;User's application program
                                .
                                .
                                .
                                .
```

EXAMPLE 2:

```
;*************************************************************************************************************************  ;*
Example of 4KB LDROM program: This lorder program will erase the APROM first, then reads the new ;* code from external SRAM and program them into APROM bank. XTAL = 40 MHz
;*************************************************************************************************************************
    .chip 8052
    .RAMCHK OFF
    .symbols

    CHPCON          EQU         BFH
    CHPENR          EQU         F6H
    SFRAL           EQU         C4H
    SFRAH           EQU         C5H
    SFRFD           EQU         C6H
    SFRCN           EQU         C7H

            ORG     000H
            LJMP    100H                    ;JUMP TO MAIN PROGRAM
  ;*****************************************************************************
  ;* 1. TIMER0 SERVICE VECTOR ORG=0BH
  ;*****************************************************************************
            ORG     000BH
            CLR     TR0                      ;TR0=0,STOP TIMER0
            MOV     TL0,R6
            MOV     TH0,R7
            RETI

  ;*****************************************************************************
  ;*  4KB LDROM MAIN PROGRAM
```

```
                MOV         TL0,R6
                MOV         TH0,R7

BLANK_CHECK_LOOP:

                SETB        TR0                     ;ENABLE TIMER 0
                MOV         PCON,#01H               ;ENTER IDLE MODE
                MOV         A,SFRFD                 ;READ ONE BYTE

                CJNE        A,#FFH,BLANK_CHECK_ERROR
                INC         SFRAL                   ;NEXT ADDRESS
                MOV         A,SFRAL
                JNZ         BLANK_CHECK_LOOP
                INC         SFRAH
                MOV         A,SFRAH
                CJNE        A,#C0H,BLANK_CHECK_LOOP   ;END ADDRESS=BFFFH
               JMP          PROGRAM_ROM

BLANK_CHECK_ERROR:

                MOV         P1,#F0H
                MOV         P3,#F0H
                JMP         $

;*******************************************************************************
;* RE-PROGRAMMING APROM BANK
;*******************************************************************************
PROGRAM_ROM:

                MOV         DPTR,#0H                ;THE ADDRESS OF NEW ROM CODE
                MOV         R2,#00H                 ;TARGET LOW BYTE ADDRESS
                MOV         R1,#00H                 ;TARGET HIGH BYTE ADDRESS
                MOV         DPTR,#0H                ;EXTERNAL SRAM BUFFER ADDRESS
                MOV         SFRAH,R1                ;SFRAH, TARGET  HIGH ADDRESS
                 MOV        SFRCN,#21H              ;SFRCN(C7H)=21  (PROGRAM )
                MOV         R6,#0CH                 ;SET TIMER FOR PROGRAMMING, ABOUT 150us.
                MOV         R7,#FEH
                MOV         TL0,R6
                MOV         TH0,R7
PROG_D_:
                MOV         SFRAL,R2                ;SFRAL(C4H)= LOW BYTE ADDRESS
                MOVX        A,@DPTR                 ;READ DATA FROM EXTERNAL SRAM BUFFER
                MOV         SFRFD,A                 ;SFRFD(C6H)=DATA IN
                MOV         TCON,#10H               ;TCON=10H,TR0=1,GO
                MOV         PCON,#01H               ;ENTER IDLE MODE( PRORGAMMING)
                INC         DPTR
                INC         R2
                CJNE        R2,#0H,PROG_D_
                INC         R1
                MOV         SFRAH,R1
                CJNE        R1,#C0H,PROG_D_
;*******************************************************************************
; * VERIFY APROM BANK
;*******************************************************************************
                MOV         R4,#03H                 ;ERROR COUNTER
                MOV         R6,#FBH                 ;SET TIMER FOR READ VERIFY, ABOUT 1.5us.
                MOV         R7,#FFH
```

```
                MOV         TL0,R6
                MOV         TH0,R7
                MOV         DPTR,#0H                ;The start address of sample code
                MOV         R2,#0H                  ;Target  low byte address
                MOV         R1,#0H                  ;Target  high byte address
                MOV         SFRAH,R1                ;SFRAH, Target high address
                MOV         SFRCN,#00H              ;SFRCN=00 (Read ROM CODE)
READ_VERIFY_:
                MOV         SFRAL,R2                ;SFRAL(C4H)= LOW ADDRESS
                MOV         TCON,#10H               ;TCON=10H,TR0=1,GO
                MOV         PCON,#01H
                INC         R2
                MOVX        A,@DPTR
                INC         DPTR
                CJNE        A,SFRFD,ERROR_
                CJNE        R2,#0H,READ_VERIFY_
                INC         R1
                MOV         SFRAH,R1
                CJNE        R1,#C0H,READ_VERIFY_

;*******************************************************************************
;* PROGRAMMING COMPLETLY, SOFTWARE RESET CPU
;*******************************************************************************
                MOV         CHPENR,#87H             ;CHPENR=87H
                MOV         CHPENR,#59H             ;CHPENR=59H
                MOV         CHPCON,#83H             ;CHPCON=83H, SOFTWARE RESET.


ERROR_:
                DJNZ        R4,UPDATE_              ;IF ERROR OCCURS, REPEAT 3 TIMES.
        .                                           ;IN-SYSTEM PROGRAMMING FAIL, USER'S
                                                   ;PROCESS TO DEAL WITH IT.
```