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Applications of "Embedded - Microcontrollers"

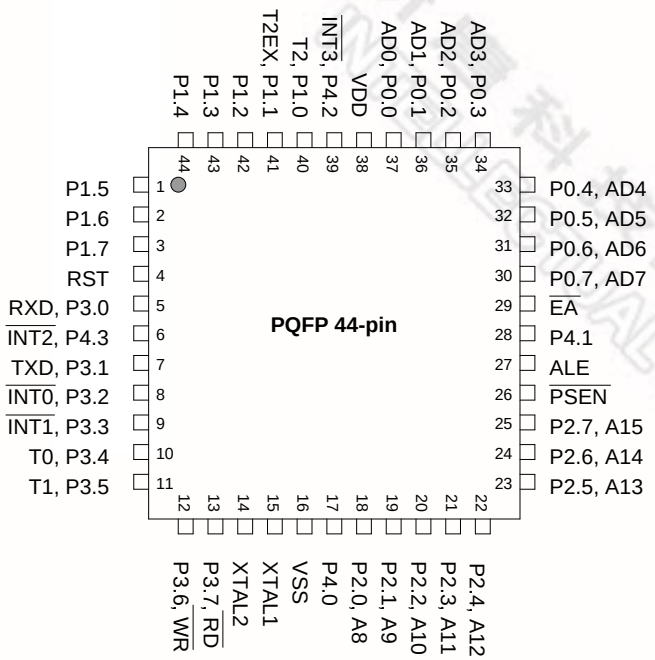
Details	
Product Status	Active
Core Processor	8052
Core Size	8-Bit
Speed	40MHz
Connectivity	EBI/EMI, UART/USART
Peripherals	POR, WDT
Number of I/O	36
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 5.5V
Data Converters	-
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-LCC (J-Lead)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/nuvoton-technology-corporation-america/w78e516dpg

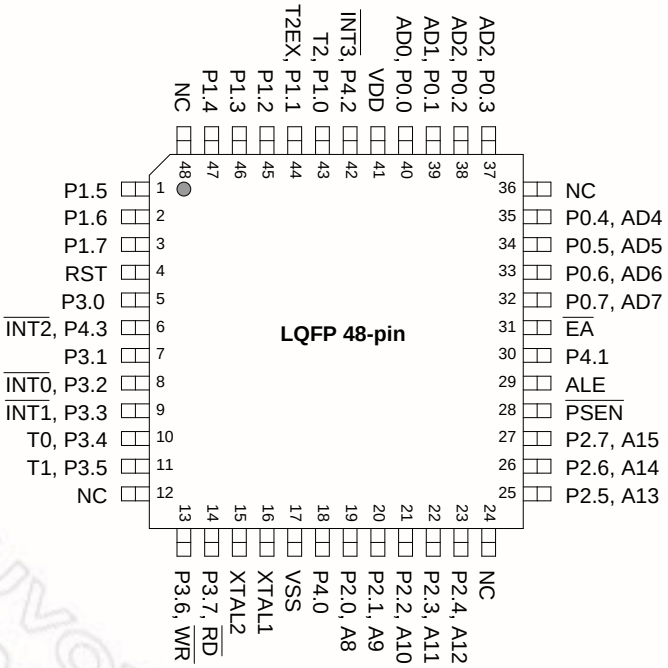
1 GENERAL DESCRIPTION

The W78E516D/W78E058D series is an 8-bit microcontroller which has an in-system programmable Flash EPROM for on-chip firmware updating.

The instruction sets of the W78E516D/W78E058D are fully compatible with the standard 8052. The W78E516D/W78E058D series contains a 64K/32K bytes of main Flash EPROM and a 4K bytes of auxiliary Flash EPROM which allows the contents of the 64K/32K bytes main Flash EPROM to be up-dated by the loader program located in the 4K bytes Flash EPROM; a 256 bytes of SRAM; 256 bytes of AUXRAM; four 8-bit bi-directional and bit-addressable I/O ports; an additional 4-bit port P4; three 16-bit timer/counters; a serial port. These peripherals are supported by an 8 sources 2-level interrupt capability. To facilitate programming and verification, the Flash EPROM inside the W78E516D/W78E058D series allows the program memory to be programmed and read electronically. Once the code is confirmed, the user can protect the code for security.

The W78E516D/W78E058D series microcontroller has two power reduction modes, idle mode and power-down mode, both of which are software selectable. The idle mode turns off the processor clock but allows for continued peripheral operation. The power-down mode stops the crystal oscillator for minimum power consumption. The external clock can be stopped at any time and in any state without affecting the processor.


P1.4
P1.3
P1.2
T2EX, P1.1
T2, P1.0
INT3, P4.2
VDD
AD0, P0.0
AD1, P0.1
AD2, P0.2
AD3, P0.3
P1.5
P1.6
P1.7
RST
RXD, P3.0
INT2, P4.3
TXD, P3.1
INT0, P3.2
INT1, P3.3
T0, P3.4
T1, P3.5
P0.4, AD4
P0.5, AD5
P0.6, AD6
P0.7, AD7
EA
P4.1
ALE
PSEN
P2.7, A15
P2.6, A14
P2.5, A13
P3.6, WR
P3.7, RD
XTAL2
XTAL1
VSS
P4.0
P2.0, A8
P2.1, A9
P2.2, A10
P2.3, A11
P2.4, A12
PQFP 44-pin


NC
P1.4
P1.3
P1.2
T2EX, P1.1
T2, P1.0
INT3, P4.2
VDD
AD0, P0.0
AD1, P0.1
AD2, P0.2
AD2, P0.3
P1.5
P1.6
P1.7
RST
P3.0
INT2, P4.3
P3.1
INT0, P3.2
INT1, P3.3
T0, P3.4
T1, P3.5
NC
NC
P0.4, AD4
P0.5, AD5
P0.6, AD6
P0.7, AD7
EA
P4.1
ALE
PSEN
P2.7, A15
P2.6, A14
P2.5, A13
P3.6, WR
P3.7, RD
XTAL2
XTAL1
VSS
P4.0
P2.0, A8
P2.1, A9
P2.2, A10
P2.3, A11
P2.4, A12
NC
LQFP 48-pin

as an internal timer, depending on the setting of bit C/T2 in T2CON. Timer 2 has three operating modes: capture, auto-reload, and baud rate generator. The clock speed at capture or auto-reload mode is the same as that of Timers 0 and 1.

7.4.1 Clock

The W78E516D/W78E058D series are designed to be used with either a crystal oscillator or an external clock. Internally, the clock is divided by two before it is used by default. This makes the W78E516D/W78E058D series relatively insensitive to duty cycle variations in the clock.

7.5 Interrupts

The Interrupt structure in the W78E516D/W78E058D series is slightly different from that of the standard 8052. Due to the presence of additional features and peripherals, the number of interrupt sources and vectors has been increased. The W78E516D/W78E058D series provides 8 interrupt resources with two priority level, including four external interrupt sources, three timer interrupts, serial I/O interrupts.

7.6 Data Pointers

The data pointer of W78E516D/W78E058D series is same as standard 8052 that have one 16-bit Data Pointer (DPTR).

7.7 Architecture

The W78E516D/W78E058D series are based on the standard 8052 device. It is built around an 8-bit ALU that uses internal registers for temporary storage and control of the peripheral devices. It can execute the standard 8052 instruction set.

7.7.1 ALU

The ALU is the heart of the W78E516D/W78E058D series. It is responsible for the arithmetic and logical functions. It is also used in decision making, in case of jump instructions, and is also used in calculating jump addresses. The user cannot directly use the ALU, but the Instruction Decoder reads the op-code, decodes it, and sequences the data through the ALU and its associated registers to generate the required result. The ALU mainly uses the ACC which is a special function register (SFR) on the chip. Another SFR, namely B register is also used Multiply and Divide instructions. The ALU generates several status signals which are stored in the Program Status Word register (PSW).

7.7.2 Accumulator

The Accumulator (ACC) is the primary register used in arithmetic, logical and data transfer operations in the W78E516D/W78E058D series. Since the Accumulator is directly accessible by the CPU, most of the high speed instructions make use of the ACC as one argument.

7.7.3 B Register

This is an 8-bit register that is used as the second argument in the MUL and DIV instructions. For all other instructions it can be used simply as a general purpose register.

7.7.4 Program Status Word

This is an 8-bit SFR that is used to store the status bits of the ALU. It holds the Carry flag, the Auxiliary Carry flag, General purpose flags, the Register Bank Select, the Overflow flag, and the Parity flag.

7.7.5 Stack Pointer

The W78E516D/W78E058D series has an 8-bit Stack Pointer which points to the top of the Stack. This stack resides in the Scratch Pad RAM in the W78E516D/W78E058D series. Hence the size of the stack is limited by the size of this RAM.

7.7.6 Scratch-pad RAM

The W78E516D/W78E058D series has a 256 bytes on-chip scratch-pad RAM. This can be used by the user for temporary storage during program execution. A certain section of this RAM is bit address-able, and can be directly addressed for this purpose.

7.7.7 AUX-RAM

AUX-RAM 0H~255H is addressed indirectly as the same way to access external data memory with the MOVX instruction. The data memory region is from 0000H to 00FFH. Memory MAP shows the mem-ory map for this product series. W78E516D/W78E058D series can read/write 256 bytes AUX RAM by the MOVX instruction.

Since the scratch-pad RAM is only 256bytes it can be used only when data contents are small. There are several other special purpose areas within the scratch-pad RAM. These are illustrated in next figure.

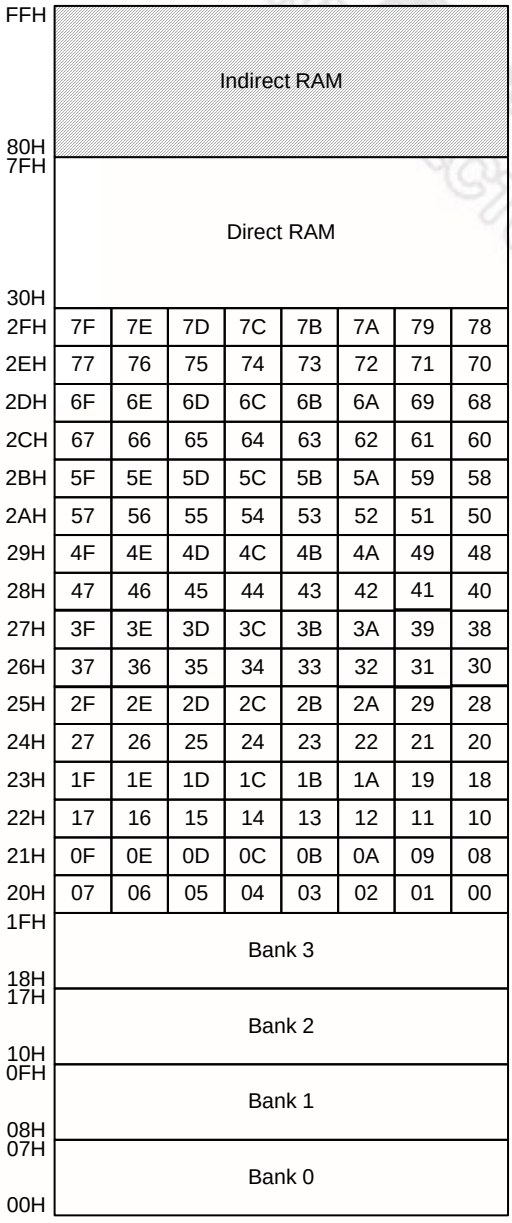


Figure 8- 3 Scratch-pad RAM

DPH.7	DPH.6	DPH.5	DPH.4	DPH.3	DPH.2	DPH.1	DPH.0

Mnemonic: DPH Address: 83h

BIT	NAME	FUNCTION
7-0	DPH.[7:0]	This is the high byte of the standard 8052 16-bit data pointer.

P4.0 Base Address Low Byte Register

Bit:

7	6	5	4	3	2	1	0
P40AL.7	P40AL.6	P40AL.5	P40AL.4	P40AL.3	P40AL.2	P40AL.1	P40AL.0

Mnemonic: P40AL Address: 84h

BIT	NAME	FUNCTION
7-0	P40AL.[7:0]	The Base address register for comparator of P4.0. P40AL contains the low-order byte of address.

P4.0 Base Address High Byte Register

Bit:

7	6	5	4	3	2	1	0
P40AH.7	P40AH.6	P40AH.5	P40AH.4	P40AH.3	P40AH.2	P40AH.1	P40AH.0

Mnemonic:P40AH Address: 85h

BIT	NAME	FUNCTION
7-0	P40AH.[7:0]	The Base address register for comparator of P4.0. P40AH contains the High-order byte of address.

Port 0 Pull up Option Register

Bit:

7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	P0UP

Mnemonic: P0UPR Address: 86h

BIT	NAME	FUNCTION
0	P0UP	0: Port 0 pins are open-drain. 1: Port 0 pins are internally pulled-up. Port 0 is structurally the same as Port 2.

Power Control

Bit:

7	6	5	4	3	2	1	0
SMOD	SMOD0	-	-	GF1	GF0	PD	IDL

Mnemonic: PCON Address: 87h

BIT	NAME	FUNCTION
7	SMOD	1: This bit doubles the serial port baud rate in mode 1, 2, and 3 when set to 1.
6	SMOD 0	0: Framing Error Detection Disable. SCON.7 (SM0/FE) bit is used as SM0 (standard 8052 function). 1: Framing Error Detection Enable. SCON.7 (SM0/FE) bit is used to reflect as

Mnemonic: TL1 Address: 8Bh

BIT	NAME	FUNCTION
7-0	TL1.[7:0]	Timer 1 LSB.

Timer 0 MSB

Bit:	7	6	5	4	3	2	1	0
	TH0.7	TH0.6	TH0.5	TH0.4	TH0.3	TH0.2	TH0.1	TH0.0

Mnemonic: TH0 Address: 8Ch

BIT	NAME	FUNCTION
7-0	TH0.[7:0]	Timer 0 MSB.

Timer 1 MSB

Bit:	7	6	5	4	3	2	1	0
	TH1.7	TH1.6	TH1.5	TH1.4	TH1.3	TH1.2	TH1.1	TH1.0

Mnemonic: TH1 Address: 8Dh

BIT	NAME	FUNCTION
7-0	TH1.[7:0]	Timer 1 MSB.

AUXR

Bit:	7	6	5	4	3	2	1	0
	-	-	-	-	-	-	-	ALE_OFF

Mnemonic: AUXR Address: 8Eh

BIT	NAME	FUNCTION
0	ALE_OFF	1: Disable ALE output 0: Enable ALE output

Watchdog Timer Control Register

Bit:	7	6	5	4	3	2	1	0
	ENW	CLRW	WIDL	-	-	PS2	PS1	PS0

Mnemonic: WDTC Address: 8FH

BIT	NAME	FUNCTION
7	ENW	Enable watch-dog if set.
6	CLRW	Clear watch-dog timer and Pre-scalar if set. This flag will be cleared automatically.
5	WIDL	If this bit is set, watch-dog is enabled under IDLE mode. If cleared, watch-dog is

Serial Port Control

Bit:	7	6	5	4	3	2	1	0
	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI

Mnemonic: SCON Address: 98h

BIT	NAME	FUNCTION
7	SM0/FE	Serial port mode select bit 0 or Framing Error Flag: The SMOD0 bit in PCON SFR determines whether this bit acts as SM0 or as FE. The operation of SM0 is described below. When used as FE, this bit will be set to indicate an invalid stop bit. This bit must be manually cleared in software to clear the FE condition.
6	SM1	Serial Port mode select bit 1. See table below.
5	SM2	Multiprocessor communication mode enable. The function of this bit is dependent on the serial port mode. Mode 0: No effect. Mode 1: Checking valid stop bit. 0 = Reception is always valid no matter the logic level of stop bit. 1 = Reception is ignored if the received stop bit is not logic 1. Mode 2 or 3: For multiprocessor communication. 0 = Reception is always valid no matter the logic level of the 9th bit. 1 = Reception is ignored if the received 9th bit is not logic 1.
4	REN	Receive enable: 0: Disable serial reception. 1: Enable serial reception.
3	TB8	This is the 9th bit to be transmitted in modes 2 and 3. This bit is set and cleared by software as desired.
2	RB8	In modes 2 and 3 this is the received 9th data bit. In mode 1, if SM2 = 0, RB8 is the stop bit that was received. In mode 0 it has no function.
1	TI	Transmit interrupt flag: This flag is set by hardware at the end of the 8th bit time in mode 0, or at the beginning of the stop bit in all other modes during serial transmission. This bit must be cleared by software.
0	RI	Receive interrupt flag: This flag is set by hardware at the end of the 8th bit time in mode 0, or halfway through the stop bits time in the other modes during serial reception. However the restrictions of SM2 apply to this bit. This bit can be cleared only by software.

SM1, SM0: Mode Select bits:

Mode	SM0	SM1	Description	Length	Baud Rate
0	0	0	Synchronous	8	Tclk divided by 4 or 12
1	0	1	Asynchronous	10	Variable
2	1	0	Asynchronous	11	Tclk divided by 32 or 64
3	1	1	Asynchronous	11	Variable

BIT	NAME	FUNCTION
7-0	P42AL.[7:0]	The Base address register for comparator of P4.2. P42AL contains the low-order byte of address.

P4.2 Base Address High Byte Register

Bit:	7	6	5	4	3	2	1	0
	P42AH.7	P42AH.6	P42AH.5	P42AH.4	P42AH.3	P42AH.2	P42AH.1	P42AH.0

Mnemonic:P42AH Address: ADh

BIT	NAME	FUNCTION
7-0	P42AH.[7:0]	The Base address register for comparator of P4.2. P42AH contains the High-order byte of address.

Port 2 Expanded Control

Bit:	7	6	5	4	3	2	1	0
	P43CSIN	P42CSIN	P41CSIN	P40CSIN	-	-	-	-

Mnemonic: P2ECON Address:AEh

BIT	NAME	FUNCTION
7	P43CSINV	The active polarity of P4.3 when pin P4.3 is defined as read and/or write strobe signal. 1 : P4.3 is active high when pin P4.3 is defined as read and/or write strobe signal. 0 : P4.3 is active low when pin P4.3 is defined as read and/or write strobe signal.
6	P42CSINV	The similarity definition as P43SINV.
5	P41CSINV	The similarity definition as P43SINV.
4	P40CSINV	The similarity definition as P43SINV.

Port 3

Bit:	7	6	5	4	3	2	1	0
	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0

Mnemonic: P3 Address: B0h

P3.7-0: General purpose Input/Output port. Most instructions will read the port pins in case of a port read access, however in case of read-modify-write instructions, the port latch is read. These alternate functions are described below:

BIT	NAME	FUNCTION
7	P3.7	$\overline{RD}$
6	P3.6	$\overline{WR}$
5	P3.5	T1
4	P3.4	T0

Mnemonic: SFRAL Address: C4h

BIT	NAME	FUNCTION
7-0	SFRAL.[7:0]	The programming address of on-chip flash memory in programming mode. SFRFAL contains the low-order byte of address.

SFR program of address high

Bit:	7	6	5	4	3	2	1	0
	SFRAH.7	SFRAH.6	SFRAH.5	SFRAH.4	SFRAH.3	SFRAH.2	SFRAH.1	SFRAH.0

Mnemonic: SFRAH Address: C5h

BIT	NAME	FUNCTION
7-0	SFRAH.[7:0]	The programming address of on-chip flash memory in programming mode. SFRFAH contains the high-order byte of address.

SFR program For Data

Bit:	7	6	5	4	3	2	1	0
	SFRFD.7	SFRFD.6	SFRFD.5	SFRFD.4	SFRFD.3	SFRFD.2	SFRFD.1	SFRFD.0

SFRFD Address: C6h

BIT	NAME	FUNCTION
7-0	SFRFD.[7:0]	The programming data for on-chip flash memory in programming mode.

SFR for Program Control

Bit:	7	6	5	4	3	2	1	0
	-	WFWIN	OEN	CEN	CTRL3	CTRL2	CTRL1	CTRL0

SFRCN Address: C7h

BIT	NAME	FUNCTION
6	WFWIN	On-chip FLASH EPROM bank select for in-system programming. 0: 64K bytes FLASH EPROM bank is selected as destination for re-programming. 1: 4K bytes FLASH EPROM bank is selected as destination for re-programming.
5	OEN	FLASH EPROM output enable.
4	CEN	FLASH EPROM chip enable.
3-0	CTRL[3:0]	CTRL[3:0]: The flash control signals

Mode	CTRL<3:0>	WFWIN	OEN	CEN	SFRAH,SFRAL	SFRFD
Erase APROM	0010	0	1	0	X	X
Program APROM	0001	0	1	0	Address in	Data in

Op-code	HEX Code	Bytes	W78E516D/W78E058D series Clock cycles
DA A	D4	1	12
ANL A, R0	58	1	12
ANL A, R1	59	1	12
ANL A, R2	5A	1	12
ANL A, R3	5B	1	12
ANL A, R4	5C	1	12
ANL A, R5	5D	1	12
ANL A, R6	5E	1	12
ANL A, R7	5F	1	12
ANL A, @R0	56	1	12
ANL A, @R1	57	1	12
ANL A, direct	55	2	12
ANL A, #data	54	2	12
ANL direct, A	52	2	12
ANL direct, #data	53	3	24
ORL A, R0	48	1	12
ORL A, R1	49	1	12
ORL A, R2	4A	1	12
ORL A, R3	4B	1	12
ORL A, R4	4C	1	12
ORL A, R5	4D	1	12
ORL A, R6	4E	1	12
ORL A, R7	4F	1	12
ORL A, @R0	46	1	12
ORL A, @R1	47	1	12
ORL A, direct	45	2	12
ORL A, #data	44	2	12
ORL direct, A	42	2	12
ORL direct, #data	43	3	24
XRL A, R0	68	1	12
XRL A, R1	69	1	12
XRL A, R2	6A	1	12
XRL A, R3	6B	1	12

Op-code	HEX Code	Bytes	W78E516D/W78E058D series Clock cycles
MOV direct, R7	8F	2	24
MOV direct, @R0	86	2	24
MOV direct, @R1	87	2	24
MOV direct, direct	85	3	24
MOV direct, #data	75	3	24
MOV DPTR, #data 16	90	3	24
MOVC A, @A+DPTR	93	1	24
MOVC A, @A+PC	83	1	24
MOVX A, @R0	E2	1	24
MOVX A, @R1	E3	1	24
MOVX A, @DPTR	E0	1	24
MOVX @R0, A	F2	1	24
MOVX @R1, A	F3	1	24
MOVX @DPTR, A	F0	1	24
PUSH direct	C0	2	24
POP direct	D0	2	24
XCH A, R0	C8	1	12
XCH A, R1	C9	1	12
XCH A, R2	CA	1	12
XCH A, R3	CB	1	12
XCH A, R4	CC	1	12
XCH A, R5	CD	1	12
XCH A, R6	CE	1	12
XCH A, R7	CF	1	12
XCH A, @R0	C6	1	12
XCH A, @R1	C7	1	12
XCHD A, @R0	D6	1	12
XCHD A, @R1	D7	1	12
XCH A, direct	C5	2	24
CLR C	C3	1	12
CLR bit	C2	2	12
SETB C	D3	1	12
SETB bit	D2	2	12
CPL C	B3	1	12

Op-code	HEX Code	Bytes	W78E516D/W78E058D series Clock cycles
CPL bit	B2	2	12
ANL C, bit	82	2	24
ANL C, /bit	B0	2	24
ORL C, bit	72	2	24
ORL C, /bit	A0	2	24
MOV C, bit	A2	2	12
MOV bit, C	92	2	24
ACALL addr11	71, 91, B1, 11, 31, 51, D1, F1	2	24
LCALL addr16	12	3	24
RET	22	1	24
RETI	32	1	24
AJMP ADDR11	01, 21, 41, 61, 81, A1, C1, E1	2	24
LJMP addr16	02	3	24
JMP @A+DPTR	73	1	24
SJMP rel	80	2	24
JZ rel	60	2	24
JNZ rel	70	2	24
JC rel	40	2	24
JNC rel	50	2	24
JB bit, rel	20	3	24
JNB bit, rel	30	3	24
JBC bit, rel	10	3	24
CJNE A, direct, rel	B5	3	24
CJNE A, #data, rel	B4	3	24
CJNE @R0, #data, rel	B6	3	24
CJNE @R1, #data, rel	B7	3	24
CJNE R0, #data, rel	B8	3	24
CJNE R1, #data, rel	B9	3	24
CJNE R2, #data, rel	BA	3	24
CJNE R3, #data, rel	BB	3	24
CJNE R4, #data, rel	BC	3	24
CJNE R5, #data, rel	BD	3	24

14.3.3 Baud Rate Generator Mode

The baud rate generator mode is enabled by setting either the RCLK or TCLK bits in T2CON register. While in the baud rate generator mode, Timer/Counter 2 is a 16 bit counter with auto reload when the count rolls over from 0FFFFh. However, rolling over does not set the TF2 bit. If EXEN2 bit is set, then a negative transition of the T2EX pin will set EXF2 bit in the T2CON register and cause an interrupt request.

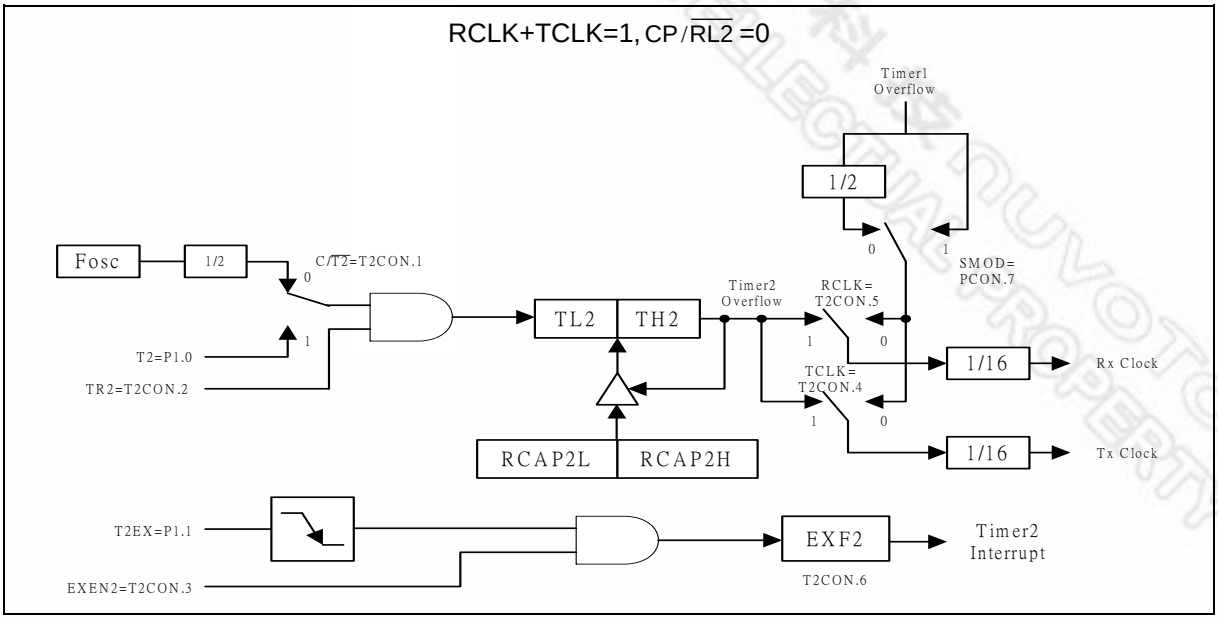


Figure 14- 6 Baud Rate Generator Mode

grammable 9th bit (TB8) and a stop bit (1). The 9th bit received is put into RB8. The baud rate is programmable to 1/32 or 1/64 of the oscillator frequency, which is determined by the SMOD bit in PCON SFR. Transmission begins with a write to SBUF. The serial data is brought out on to TxD pin at S6P2 following the first roll-over of the divide by 16 counter. The next bit is placed on TxD pin at S6P2 following the next rollover of the divide by 16 counter. Thus the transmission is synchronized to the divide by 16 counters, and not directly to the write to SBUF signal. After all 9 bits of data are transmitted, the stop bit is transmitted. The TI flag is set in the S6P2 state after the stop bit has been put out on TxD pin. This will be at the 11th rollover of the divide by 16 counters after a write to SBUF. Reception is enabled only if REN is high. The serial port actually starts the receiving of serial data, with the detection of a falling edge on the RxD pin. The 1-to-0 detector continuously monitors the RxD line, sampling it at the rate of 16 times the selected baud rate. When a falling edge is detected, the divide by 16 counters is immediately reset. This helps to align the bit boundaries with the rollovers of the divide by 16 counters. The 16 states of the counter effectively divide the bit time into 16 slices. The bit detection is done on a best of three basis. The bit detector samples the RxD pin, at the 8th, 9th and 10th counter states. By using a majority 2 of 3 voting system, the bit value is selected. This is done to improve the noise rejection feature of the serial port.

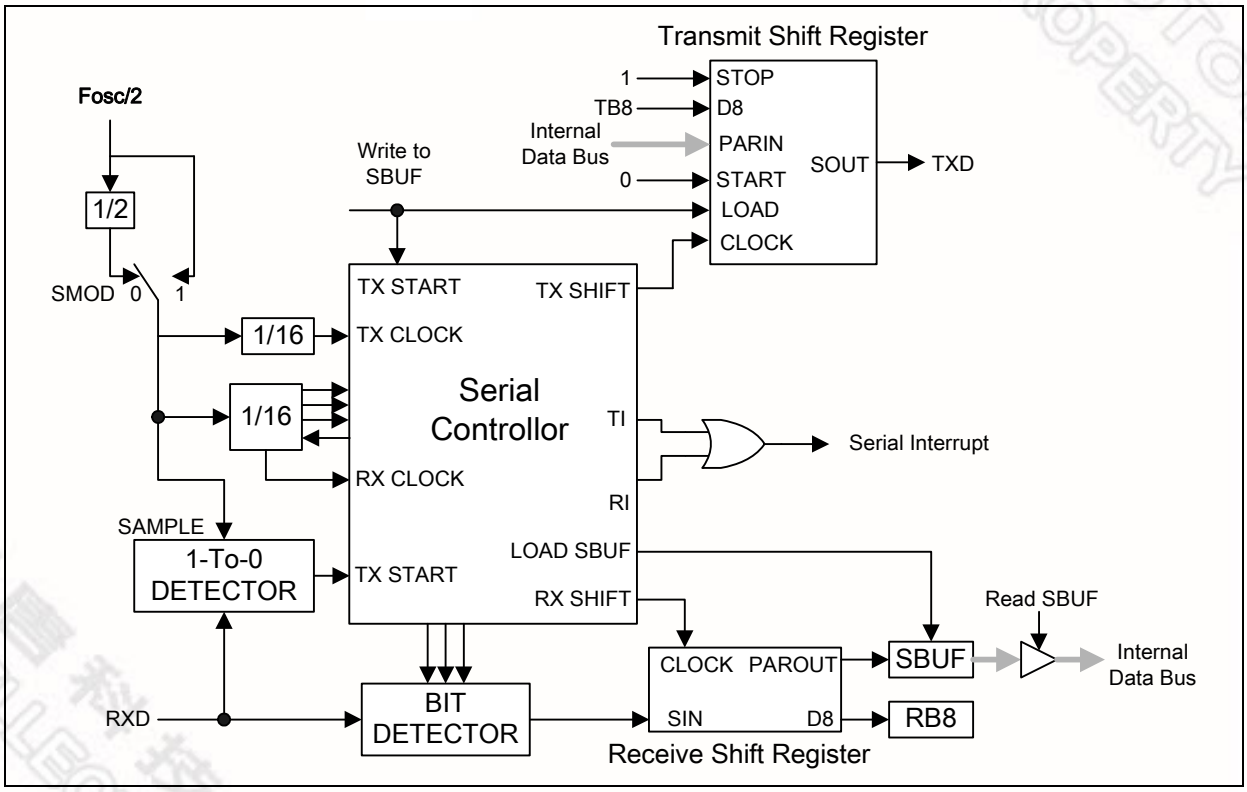


Figure 16- 3 Serial port mode 2

If the first bit detected after the falling edge of RxD pin, is not 0, then this indicates an invalid start bit, and the reception is immediately aborted. The serial port again looks for a falling edge in the RxD line. If a valid start bit is detected, then the rest of the bits are also detected and shifted into the SBUF. After shifting in 9 data bits, there is one more shift to do, after which the SBUF and RB8 are loaded and RI is set. However certain conditions must be met before the loading and setting of RI can be done.

1. RI must be 0 and

18 ISP(IN-SYSTEM PROGRAMMING)

ISP is the ability of programmable MCU to be programmed while F/W code in AP-ROM or LD-ROM (ISP work voltage 3.3-5.5V).

The W78E058D/516D equips one 32K byte of main ROM bank for application program (called APROM) and one 4K byte of auxiliary ROM bank for loader program (called LDROM). In the normal operation, the microcontroller executes the code in the APROM. If the content of APROM needs to be modified, the W78E058D/516D allows user to activate the In-System Programming (ISP) mode by setting the CHPCON register. **The CHPCON is read-only by default, software must write two specific values 87H, then 59H sequentially to the CHPENR register to enable the CHPCON write attribute. Writing CHPENR register with the values except 87H and 59H will close CHPCON register write attribute.** The W78E058D/516D achieves all in-system programming operations including enter/exit ISP Mode, program, erase, read ... etc, during device in the idle mode. Setting the bit CHPCON.0 the device will enter in-system programming mode after a wake-up from idle mode. Because device needs proper time to complete the ISP operations before awaken from idle mode, software may use timer interrupt to control the duration for device wake-up from idle mode. To perform ISP operation for revising contents of APROM, software located at APROM setting the CHPCON register then enter idle mode, after awaken from idle mode the device executes the corresponding interrupt service routine in LDROM. Because the device will clear the program counter while switching from APROM to LDROM, the first execution of RETI instruction in interrupt service routine will jump to 00H at LDROM area. The device offers a software reset for switching back to APROM while the content of APROM has been updated completely. **Setting CHPCON register bit 0, 1 and 7 to logic-1 will result a software reset to reset the CPU**. The software reset serves as a external reset. This in-system programming feature makes the job easy and efficient in which the application needs to update firmware frequently. In some applications, the in-system programming feature make it possible to easily update the system firmware without opening the chassis.

SFRAH, SFRAL: The objective address of on-chip ROM in the in-system programming mode. SFRAH contains the high-order byte of address, SFRAL contains the low-order byte of address.

SFRFD: The programming data for on-chip ROM in programming mode.

SFRCN: The control byte of on-chip ROM programming mode.

SFRCN (C7)

BIT	NAME	FUNCTION
7	-	Reserve.
6	WFWIN	On-chip ROM bank select for in-system programming. 0: 32K/64K bytes ROM bank is selected as destination for re-programming. 1: 4K bytes ROM bank is selected as destination for re-programming.
5	OEN	ROM output enable.
4	CEN	ROM chip enable.
3, 2, 1, 0	CTRL [3:0]	The flash control signals

21 ELECTRICAL CHARACTERISTICS

21.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	Min	MAX	UNIT
DC Power Supply	V_{DD}–V_{SS}	2.4	5.5	V
Input Voltage	V_{IN}	V_{SS}-0.3	V_{DD}+0.3	V
Operating Temperature	T_A	-40	+85	°C

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the lift and reliability of the device.

R_{RST}	RST-pin Internal Pull-down Resistor	2.4 < V_{DD} < 5.5V	30		350	KΩ

Note:

*1: Typical values are not guaranteed. The values listed are tested at room temperature and based on a limited number of samples.

*2: Pins of ports 1~4 source a transition current when they are being externally driven from 1 to 0. The transition current reaches its maximum value when V_{IN} is approximately 2V.

*3: Under steady state (non-transient) conditions, I_{OL} must be externally limited as follows:
Maximum I_{OL} per port pin: 20mA
Maximum I_{OL} per 8-bit port: 40mA
Maximum total I_{OL} for all outputs: 100mA

*4: If I_{OH} exceeds the test condition, V_{OH} will be lower than the listed specification.
If I_{OL} exceeds the test condition, V_{OL} will be higher than the listed specification.

*5: Tested while CPU is kept in reset state and EA=H, Port0=H.

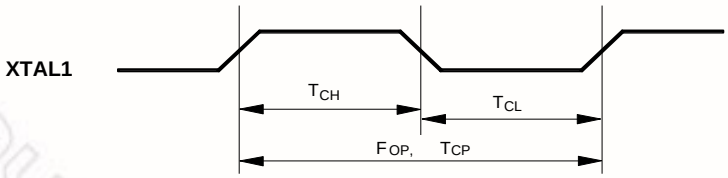
Voltage	**Max.** Frequency	6T/12T mode	Note
4.5-5.5V	40MHz	12T	
4.5-5.5V	20MHz	6T	
2.4V	20MHz	12T	
2.4V	10MHz	6T	

Frequency VS Voltage Table

21.3 AC CHARACTERISTICS

The AC specifications are a function of the particular process used to manufacture the part, the ratings of the I/O buffers, the capacitive load, and the internal routing capacitance. Most of the specifications can be expressed in terms of multiple input clock periods (TCP), and actual parts will usually experience less than a ±20 nS variation. The numbers below represent the performance expected from a 0.6 micron CMOS process when using 2 and 4 mA output buffers.

Clock Input Waveform



PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTES
Operating Speed	Fop	4	-	40	MHz	1

```
            MOV     TCON,#00H               ;TR=0 TIMER0 STOP
            MOV      IP,#00H                ;IP=00H
            MOV      IE,#82H                ;TIMER0 INTERRUPT ENABLE FOR
                                            ;WAKE-UP FROM IDLE MODE
            MOV     R6,#FEH                 ;TL0=FEH
            MOV     R7,#FFH                 ;TH0=FFH
            MOV     TL0,R6
            MOV     TH0,R7
            MOV     TMOD,#01H               ;TMOD=01H,SET TIMER0 A 16-BIT TIMER
            MOV      TCON,#10H              ;TCON=10H,TR0=1,GO
            MOV      PCON,#01H              ;ENTER IDLE MODE FOR LAUNCHING
                                            ;THE IN-SYSTEM PROGRAMMABILITY
;*****************************************************************************
;* Normal mode APROM program: depending user's application
;*****************************************************************************
NORMAL_MODE:
                                .
                                    ;User's application program
                                .
                                .
                                .
                                .
```

EXAMPLE 2:

```
;*************************************************************************************************************************  ;*
Example of 4KB LDROM program: This lorder program will erase the APROM first, then reads the new ;* code from external SRAM and program them into APROM bank. XTAL = 40 MHz
;*************************************************************************************************************************
    .chip 8052
    .RAMCHK OFF
    .symbols

    CHPCON          EQU         BFH
    CHPENR          EQU         F6H
    SFRAL           EQU         C4H
    SFRAH           EQU         C5H
    SFRFD           EQU         C6H
    SFRCN           EQU         C7H

            ORG     000H
            LJMP    100H                    ;JUMP TO MAIN PROGRAM
  ;*****************************************************************************
  ;* 1. TIMER0 SERVICE VECTOR ORG=0BH
  ;*****************************************************************************
            ORG     000BH
            CLR     TR0                      ;TR0=0,STOP TIMER0
            MOV     TL0,R6
            MOV     TH0,R7
            RETI

  ;*****************************************************************************
  ;*  4KB LDROM MAIN PROGRAM
```

```
                MOV         TL0,R6
                MOV         TH0,R7
                MOV         DPTR,#0H                ;The start address of sample code
                MOV         R2,#0H                  ;Target  low byte address
                MOV         R1,#0H                  ;Target  high byte address
                MOV         SFRAH,R1                ;SFRAH, Target high address
                MOV         SFRCN,#00H              ;SFRCN=00 (Read ROM CODE)
READ_VERIFY_:
                MOV         SFRAL,R2                ;SFRAL(C4H)= LOW ADDRESS
                MOV         TCON,#10H               ;TCON=10H,TR0=1,GO
                MOV         PCON,#01H
                INC         R2
                MOVX        A,@DPTR
                INC         DPTR
                CJNE        A,SFRFD,ERROR_
                CJNE        R2,#0H,READ_VERIFY_
                INC         R1
                MOV         SFRAH,R1
                CJNE        R1,#C0H,READ_VERIFY_

;*******************************************************************************
;* PROGRAMMING COMPLETLY, SOFTWARE RESET CPU
;*******************************************************************************
                MOV         CHPENR,#87H             ;CHPENR=87H
                MOV         CHPENR,#59H             ;CHPENR=59H
                MOV         CHPCON,#83H             ;CHPCON=83H, SOFTWARE RESET.


ERROR_:
                DJNZ        R4,UPDATE_              ;IF ERROR OCCURS, REPEAT 3 TIMES.
        .                                           ;IN-SYSTEM PROGRAMMING FAIL, USER'S
                                                   ;PROCESS TO DEAL WITH IT.
```