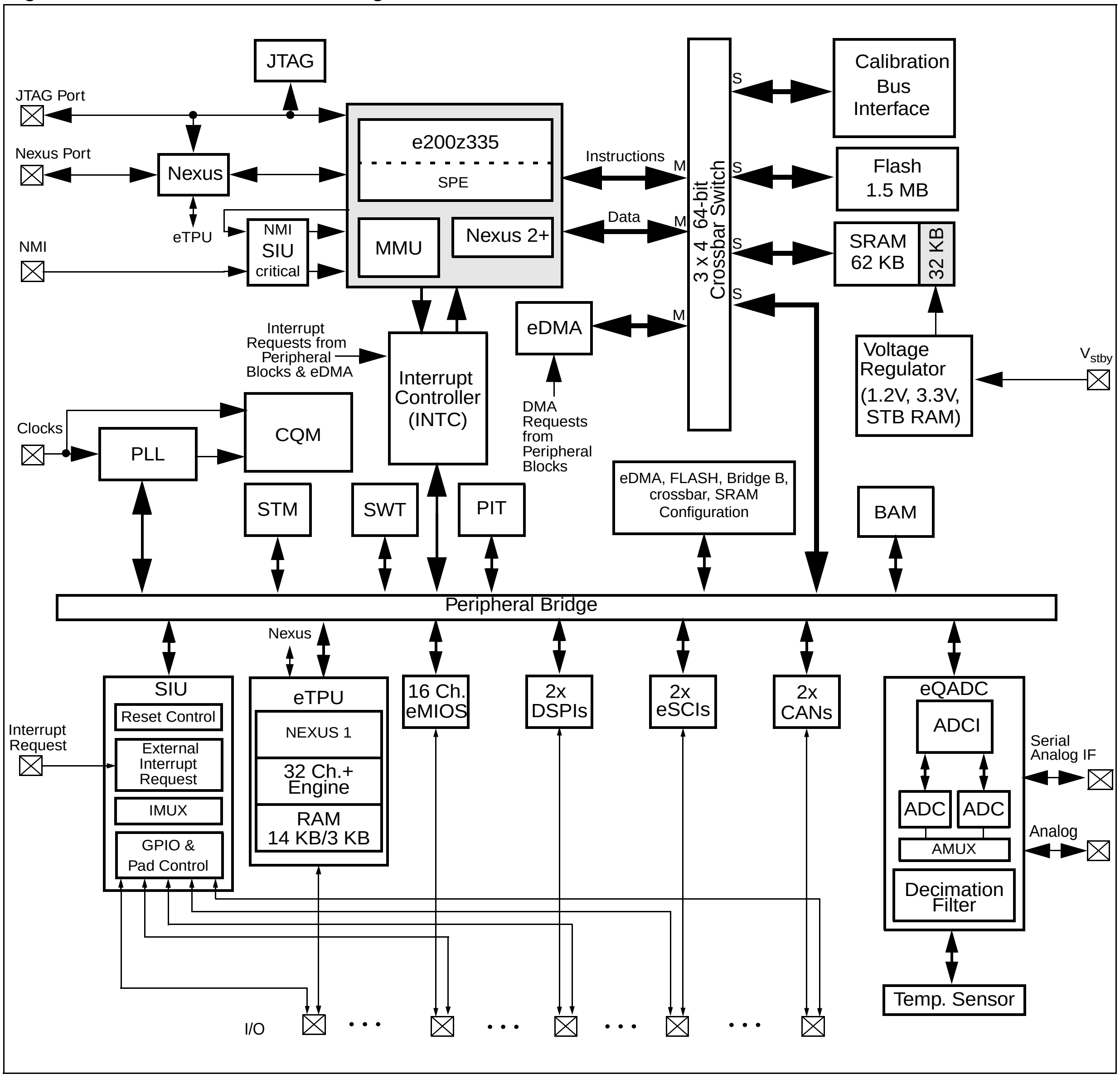
List of tables

List of figures

2 Block diagram

Figure 1 shows a top-level block diagram of the SPC563M64.

Figure 1. SPC563Mxx block diagram



power supply

- Boot assist module (BAM)
  - Enables and manages the transition of MCU from reset to user code execution in the following configurations:
    Execution from internal Flash memory
    Execution from external memory on the calibration bus
    Download and execution of code via FlexCAN or eSCI
- Periodic interrupt timer (PIT)
  - 32-bit wide down counter with automatic reload
  - Four channels clocked by system clock
  - One channel clocked by crystal clock
  - Each channel can produce periodic software interrupt
  - Each channel can produce periodic triggers for eQADC queue triggering
  - One channel out of the five can be used as wake-up timer to wake device from low power stop mode
- System timer module (STM)
  - 32-bit up counter with 8-bit prescaler
  - Clocked from system clock
  - Four-channel timer compare hardware
  - Each channel can generate a unique interrupt request
  - Designed to address AutoSAR task monitor function
- Software watchdog timer (SWT)
  - 32-bit timer
  - Clock by system clock or crystal clock
  - Can generate either system reset or non-maskable interrupt followed by system reset
  - Enabled out of reset
- Enhanced modular I/O system (eMIOS)
  - 16 timer channels (up to 14 channels in LQFP144)
  - 24-bit timer resolution
  - 3 selectable time bases plus shared time or angle counter bus from eTPU2
  - DMA and interrupt request support
  - Motor control capability
- Second-generation enhanced time processor unit (eTPU2)
  - Object-code compatible with eTPU—no changes are required to hardware or software if only eTPU features are used
  - Intelligent co-processor designed for timing control
  - High level tools, assembler and compiler available
  - 32 channels (each channel has dedicated I/O pin in all packages except LQFP100)
  - 24-bit timer resolution
  - 14 KB code memory and 3 KB data memory
  - Double match and capture on all channels

angle.

- Priority Based CFIFOs

  Supports six CFIFOs with fixed priority. The lower the CFIFO number, the higher its priority. When commands of distinct CFIFOs are bound for the same CBuffer, the higher priority CFIFO is always served first.

  Supports software and several hardware trigger modes to arm a particular CFIFO

  Generates interrupt when command coherency is not achieved
- External Hardware Triggers

  Supports rising edge, falling edge, high level and low level triggers

  Supports configurable digital filter
- Supports four external 8-to-1 muxes which can expand the input channel number from 34[d] to 59

● Two deserial serial peripheral interface modules (DSPI)
- SPI

  Full duplex communication ports with interrupt and DMA request support

  Support for queues in RAM

  6 chip selects, expandable to 64 with external demultiplexers

  Programmable frame size, baud rate, clock delay and clock phase on a per frame basis

  Modified SPI mode for interfacing to peripherals with longer setup time requirements

  LVDS option for output clock and data to allow higher speed communication
- Deserial serial interface (DSI)

  Pin reduction by hardware serialization and deserialization of eTPU, eMIOS channels and GPIO

  32 bits per DSPI module

  Triggered transfer control and change in data transfer control (for reduced EMI)

  Compatible with Microsecond Channel Version 1.0 downstream

● Two enhanced serial communication interface (eSCI) modules
- UART mode provides NRZ format and half or full duplex interface
- eSCI bit rate up to 1 Mbps
- Advanced error detection, and optional parity generation and detection
- Word length programmable as 8, 9, 12 or 13 bits
- Separately enabled transmitter and receiver
- LIN support
- DMA support
- Interrupt request support
- Programmable clock source: system clock or oscillator clock
- Support Microsecond Channel (Timed Serial Bus - TSB) upstream Version 1.0

● Two FlexCAN

d. 176-pin and 208-ball packages.

For high priority interrupt requests, the time from the assertion of the interrupt request from the peripheral to when the processor is executing the interrupt service routine (ISR) has been minimized. The INTC provides a unique vector for each interrupt request source for quick determination of which ISR needs to be executed. It also provides an ample number of priorities so that lower priority ISRs do not delay the execution of higher priority ISRs. To allow the appropriate priorities for each source of interrupt request, the priority of each interrupt request is software configurable.

When multiple tasks share a resource, coherent accesses to that resource need to be supported. The INTC supports the priority ceiling protocol for coherent accesses. By providing a modifiable priority mask, the priority can be raised temporarily so that all tasks which share the resource can not preempt each other.

Multiple processors can assert interrupt requests to each other through software setable interrupt requests. These same software setable interrupt requests also can be used to break the work involved in servicing an interrupt request into a high priority portion and a low priority portion. The high priority portion is initiated by a peripheral interrupt request, but then the ISR asserts a software setable interrupt request to finish the servicing in a lower priority ISR. Therefore these software setable interrupt requests can be used instead of the peripheral ISR scheduling a task through the RTOS.

The INTC provides the following features:

- 356 peripheral interrupt request sources
- 8 software setable interrupt request sources
- 9-bit vector addresses
- Unique vector for each interrupt request source
- Hardware connection to processor or read from register
- Each interrupt source can be programmed to one of 16 priorities
- Preemptive prioritized interrupt requests to processor
- ISR at a higher priority preempts executing ISRs or tasks at lower priorities
- Automatic pushing or popping of preempted priority to or from a LIFO
- Ability to modify the ISR or task priority to implement the priority ceiling protocol for accessing shared resources
- Low latency—three clocks from receipt of interrupt request from peripheral to interrupt request to processor

This device also includes a non-maskable interrupt (NMI) pin that bypasses the INTC and multiplexing logic.

3.3.5 FMPLL

The FMPLL allows the user to generate high speed system clocks from a 4 MHz to 20 MHz crystal oscillator or external clock generator. Further, the FMPLL supports programmable frequency modulation of the system clock. The PLL multiplication factor, output clock divider ratio are all software configurable.

drives the $\overline{RSTOUT}$ pin. Communication between the SIU and the e200z335 CPU core is via the crossbar switch. The SIU provides the following features:

- System configuration
  - MCU reset configuration via external pins
  - Pad configuration control for each pad
  - Pad configuration control for virtual I/O via DSPI serialization
- System reset monitoring and generation
  - Power-on reset support
  - Reset status register provides last reset source to software
  - Glitch detection on reset input
  - Software controlled reset assertion
- External interrupt
  - 11 interrupt requests
  - Rising or falling edge event detection
  - Programmable digital filter for glitch rejection
  - Critical Interrupt request
  - Non-Maskable Interrupt request
- GPIO
  - GPIO function on 80 I/O pins
  - Virtual GPIO on 64 I/O pins via DSPI serialization (requires external deserialization device)
  - Dedicated input and output registers for setting each GPIO and Virtual GPIO pin
- Internal multiplexing
  - Allows serial and parallel chaining of DSPIs
  - Allows flexible selection of eQADC trigger inputs
  - Allows selection of interrupt requests between external pins and DSPI

3.3.8 ECSM

The error correction status module provides status information regarding platform memory errors reported by error-correcting codes.

3.3.9 Flash

Devices in the SPC563Mxx family provide up to 1.5 MB of programmable, non-volatile, flash memory. The non-volatile memory (NVM) can be used for instruction and/or data storage. The flash module includes a Fetch Accelerator, that optimizes the performance of the flash array to match the CPU architecture and provides single cycle random access to the flash @ 80 MHz. The flash module interfaces the system bus to a dedicated flash memory array controller. For CPU 'loads', DMA transfers and CPU instruction fetch, it supports a 64-bit data bus width at the system bus port, and a 128-bit read data interface to flash memory. The module contains a four-entry, 128-bit prefetch buffer and a prefetch controller which prefetches sequential lines of data from the flash array into the buffer. Prefetch buffer hits allow no-wait responses. Normal flash array accesses are registered and are forwarded to the system bus on the following cycle, incurring three wait-states. Prefetch operations may be automatically controlled, and are restricted to instruction fetch.

MCU is powered-on or reset in normal mode. The BAM supports different modes of booting. They are:

- Booting from internal Flash memory
- Serial boot loading (A program is downloaded into RAM via eSCI or the FlexCAN and then executed)
- Booting from external memory on calibration bus

The BAM also reads the reset configuration half word (RCHW) from internal flash memory and configures the SPC563Mxx hardware accordingly. The BAM provides the following features:

- Sets up MMU to cover all resources and mapping all physical address to logical addresses with minimum address translation
- Sets up the MMU to allow user boot code to execute as either Power Architecture code (default) or as VLE code
- Detection of user boot code
- Automatic switch to serial boot mode if internal flash is blank or invalid
- Supports user programmable 64-bit password protection for serial boot mode
- Supports serial bootloading via FlexCAN bus and eSCI using fixed baudrate protocol
- Supports serial bootloading via FlexCAN bus and eSCI with auto baud rate sensing
- Supports serial bootloading of either Power Architecture code (default) or VLE code
- Supports booting from calibration bus interface
- Supports censorship protection for internal Flash memory
- Provides an option to enable the core watchdog timer
- Provides an option to disable the system watchdog timer

3.3.12 eMIOS

The eMIOS (Enhanced Modular Input Output System) module provides the functionality to generate or measure time events. The channels on this module provide a range of operating modes including the capability to perform dual input capture or dual output compare as well as PWM output.

The eMIOS provides the following features:

- 16 channels (24-bit timer resolution)
- For compatibility with other family members selected channels and timebases are implemented:
  - Channels 0 to 6, 8 to 15, and 23
  - Timebases A, B and C
- Channels 1, 3, 5 and 6 support modes:
  - General Purpose Input/Output (GPIO)
  - Single Action Input Capture (SAIC)
  - Single Action Output Compare (SAOC)
- Channels 2, 4, 11 and 13 support all the modes above plus:
  - Output Pulse Width Modulation Buffered (OPWMB)
- Channels 0, 8, 9, 10, 12, 14, 15, 23 support all the modes above plus:
  - Input Period Measurement (IPM)
  - Input Pulse Width Measurement (IPWM)
  - Double Action Output Compare (set flag on both matches) (DAOC)
  - Modulus Counter Buffered (MCB)
  - Output Pulse Width and Frequency Modulation Buffered (OPWFMB)
- Three 24-bit wide counter buses
  - Counter bus A can be driven by channel 23 or by the eTPU2 and all channels can use it as a reference
  - Counter bus B is driven by channel 0 and channels 0 to 6 can use it as a reference
  - Counter bus C is driven by channel 8 and channels 8 to 15 can use it as a reference
- Shared time bases with the eTPU2 through the counter buses
- Synchronization among internal and external time bases

3.3.13 eTPU2

The eTPU2 is an enhanced co-processor designed for timing control. Operating in parallel with the host CPU, eTPU2 processes instructions and real-time input events, performs output waveform generation, and accesses shared data without host intervention. Consequently, for each timer event, the host CPU setup and service times are minimized or eliminated. A powerful timer subsystem is formed by combining the eTPU2 with its own instruction and data RAM. High level assembler/compiler and documentation allows customers to develop their own functions on the eTPU2.

The eTPU2 includes these distinctive features:

- The Timer Counter (TCR1), channel logic and digital filters (both channel and the external timer clock input [TCRCLK]) now have an option to run at full system clock speed or system clock / 2.
- Channels support unordered transitions: transition 2 can now be detected before transition 1. Related to this enhancement, the transition detection latches (TDL1 and TDL2) can now be independently negated by microcode.
- A new User Programmable Channel Mode has been added: the blocking, enabling, service request and capture characteristics of this channel mode can be programmed via microcode.
- Microinstructions now provide an option to issue Interrupt and Data Transfer requests selected by channel. They can also be requested simultaneously at the same instruction.
- Channel Flags 0 and 1 can now be tested for branching, in addition to selecting the entry point.
- Channel digital filters can be bypassed.
- The Timer Counter (TCR1), channel logic and digital filters (both channel and the external timer clock input [TCRCLK]) now have an option to run at full system clock speed or system clock / 2.
- Channels support unordered transitions: transition 2 can now be detected before transition 1. Related to this enhancement, the transition detection latches (TDL1 and TDL2) can now be independently negated by microcode.
- A new User Programmable Channel Mode has been added: the blocking, enabling, service request and capture characteristics of this channel mode can be programmed via microcode.
- Microinstructions now provide an option to issue Interrupt and Data Transfer requests selected by channel. They can also be requested simultaneously at the same instruction.
- Channel Flags 0 and 1 can now be tested for branching, in addition to selecting the entry point.
- Channel digital filters can be bypassed.
- 32 channels, each channel is associated with one input and one output signal
  - Enhanced input digital filters on the input pins for improved noise immunity.
  - Identical, orthogonal channels: each channel can perform any time function. Each time function can be assigned to more than one channel at a given time, so each signal can have any functionality.
  - Each channel has an event mechanism which supports single and double action functionality in various combinations. It includes two 24-bit capture registers, two 24-bit match registers, 24-bit greater-equal and equal-only comparators
  - Input and output signal states visible from the host
- 2 independent 24-bit time bases for channel synchronization:
  - First time base clocked by system clock with programmable prescale division from 2 to 512 (in steps of 2), or by output of second time base prescaler
  - Second time base counter can work as a continuous angle counter, enabling angle based applications to match angle instead of time
  - Both time bases can be exported to the eMIOS timer module
  - Both time bases visible from the host

bound for the same ADC, the higher priority Queue is always served first
  - Queue_0 can bypass all prioritization, buffering and abort current conversions to start a Queue_0 conversion a deterministic time after the queue trigger
  - Streaming mode operation of Queue_0 to execute some commands several times
  - Supports software and hardware trigger modes to arm a particular Queue
  - Generates interrupt when command coherency is not achieved
- External hardware triggers
  - Supports rising edge, falling edge, high level and low level triggers
  - Supports configurable digital filter
- Supports four external 8-to-1 muxes which can expand the input channels to 56 channels total

3.3.15 DSPI

The deserial serial peripheral interface (DSPI) block provides a synchronous serial interface for communication between the SPC563Mxx MCU and external devices. The DSPI supports pin count reduction through serialization and deserialization of eTPU and eMIOS channels and memory-mapped registers. The channels and register content are transmitted using a SPI-like protocol. This SPI-like protocol is completely configurable for baud rate, polarity and phase, frame length, chip select assertion, etc. Each bit in the frame may be configured to serialize either eTPU channels, eMIOS channels or GPIO signals. The DSPI can be configured to serialize data to an external device that supports the Microsecond Channel protocol. There are two identical DSPI blocks on the SPC563Mxx MCU. The DSPI ouput pins support 5 V logic levels or Low Voltage Differential Signalling (LVDS) according to the Microsecond Channel specification.

The DSPIs have three configurations:

- Serial Peripheral Interface (SPI) configuration where the DSPI operates as an up to 16-bit SPI with support for queues
- Enhanced Deserial Serial Interface (DSI) configuration where DSPI serializes up to 32 bits with three possible sources per bit
  - eTPU, eMIOS, new virtual GPIO registers as possible bit source
  - Programmable inter-frame gap in continuous mode
  - Bit source selection allows microsecond channel downstream with command or data frames up to 32 bits
  - Microsecond channel dual receiver mode
- Combined Serial Interface (CSI) configuration where the DSPI operates in both SPI and DSI configurations interleaving DSI frames with SPI frames, giving priority to SPI frames

For queued operations, the SPI queues reside in system memory external to the DSPI. Data transfers between the memory and the DSPI FIFOs are accomplished through the use of the eDMA controller or through host software.

The following features are implemented:

- 5-pin JTAG port (JCOMP, TDI, TDO, TMS, and TCK)
  - Always available in production package
  - Supports both JTAG Boundary Scan and debug modes
  - 3.3 V interface
  - Supports Nexus class 1 features
  - Supports Nexus class 3 read/write feature
- 9-pin Reduced Port interface in LQFP144 production package
  - Alternate function as IO
  - 5 V (in GPIO or alternate function mode), 3.3 V (in Nexus mode) interface
  - Auxiliary Output port

    1 MCKO (message clock out) pin

    4 MDO (message data out) pins

    2 $\overline{\text{MSEO}}$ (message start/end out) pins

    1 $\overline{\text{EVTO}}$ (event out) pin
  - Auxiliary input port

    1 $\overline{\text{EVTI}}$ (event in) pin
- 17-pin Full Port interface in calibration package used on calibration tool boards
  - 3.3 V interface
  - Auxiliary Output port

    1 MCKO (message clock out) pin

    4 (reduced port mode) or 12 (full port mode) MDO (message data out) pins; 8 extra full port pins shared with calibration bus

    2 $\overline{\text{MSEO}}$ (message start/end out) pins

    1 $\overline{\text{EVTO}}$ (event out) pin
  - Auxiliary input port

    1 $\overline{\text{EVTI}}$ (event in) pin
- Host processor (e200) development support features
  - IEEE-ISTO 5001-2003 standard class 2 compliant
  - Program trace via branch trace messaging (BTM). Branch trace messaging displays program flow discontinuities (direct branches, indirect branches, exceptions, etc.), allowing the development tool to interpolate what transpires between the discontinuities. Thus, static code may be traced.
  - Watchpoint trigger enable of program trace messaging
  - Data Value Breakpoints (JTAG feature of the e200z335 core): allows CPU to be halted when the CPU writes a specific value to a memory location

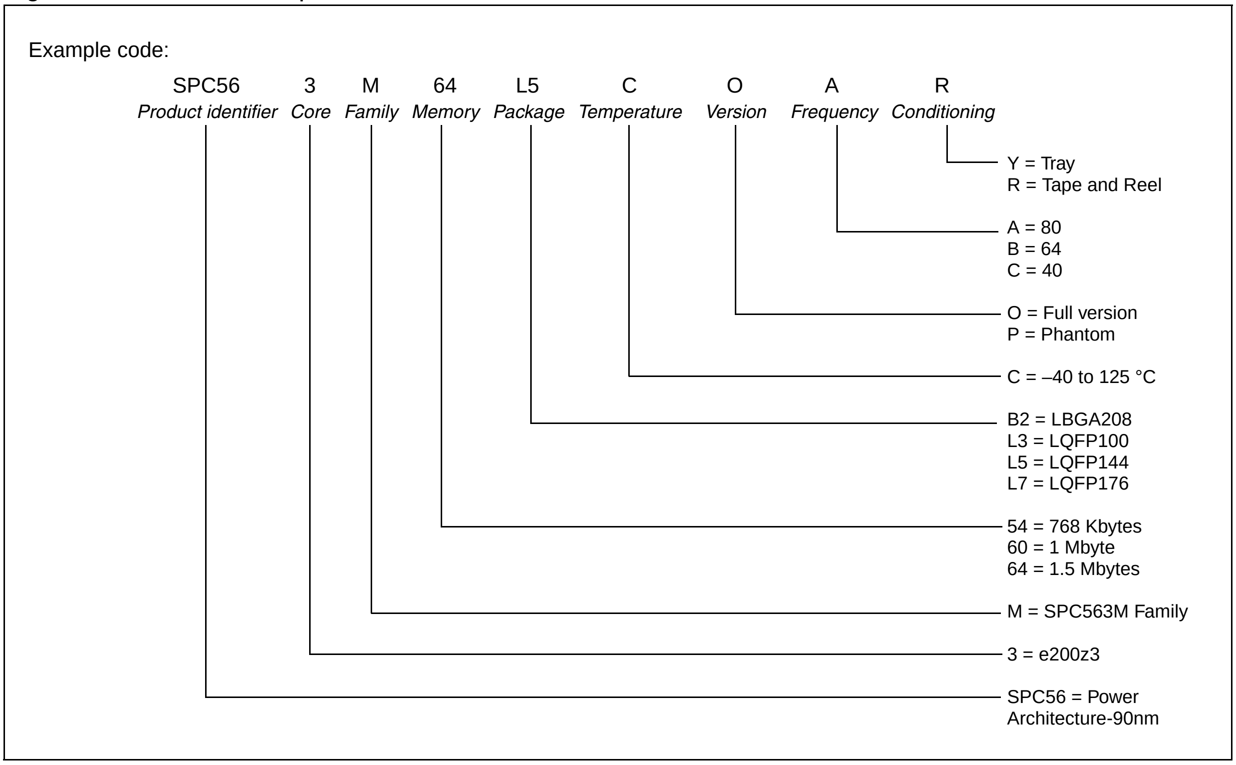
    4 data value breakpoints

    CPU only

    Detects ‘equal’ and ‘not equal’

    Byte, half word, word (naturally aligned)

Figure 2. Commercial product code structure



5 Revision history

Table 4. Revision history

Date	Revision	Description
18-May-2011	4	Internal review. Block diagram updated: – Test Controller removed. Device Summary (device comparison) table updated: – The SPC563M64 will not be offered in an LQFP100 package. – Footnote added clarifying the number of eQADC channels. Feature list: – “Single power supply” applies to all packages. (previously stated 100- and 144-pin packages) – “Nexus pins powered by 3.3 V supply” applies to all packages. (previously stated LBGA208 and LQFP176 packages) – Calibration pin voltages deleted – Details added to eTPU and eQADC features – eMIOS features updated – eTPU renamed to ETPU2; features updated Orderable parts table updated

Table 4. Revision history

Date	Revision	Description
08-Jun-2011	5	Replaced in all document “... Architecture Book E compliant...” with “... Architecture technology compliant...” Updated “Introduction”: Added “Document overview” and “Description” sections. Made the following changes in the “Description” section: – Added “Floating Point Unit (FPU)” bullet under “Single issue, 32-bit Power Architecture technology compliant e200z335 CPU core complex”. – Changed “eTPU” to “eTPU2” in the “32-channel second-generation enhanced time processor unit” sentence. – Changed the “Available in LQFP100, LQFP144, LQFP176 and LBGA208” sentence to “Designed for LQFP100, LQFP144, LQFP176, and LBGA208 packages“. Replaced all instances of “Microsecond Bus” with “Microsecond Channel”. Replaced all instances of “SPC563M54” and “SPC563M60” with “SPC563M54P”and “SPC563M60P”, respectively. Changed the “Standby SRAM size” of the SPC563M60P device from “24” to “32”. Replaced all instances of “downlink” with “downstream” and “uplink” with “upstream”. Made the following changes in the “Flash” section: Changed “Program page size of 128 bits (four words) to accelerate programming” to “Program page size of 64 bits (two words)”. Changed “Erase suspend, program suspend and erase-suspended program” to “Erase suspend”. Made editorial changes in the “BAM” section: Updated the conditional tags in the “Supports serial bootloading...” sentences. Changed “Shared time bases with the eTPU through the counter buses” to “Shared time bases with the eTPU2 through the counter buses” in the “eMIOS” section. Removed the following sentences from the “eTPU2” section: “For Monaco 1.5M, the eTPU2 has been further enhanced with these features:” “Timebases and channels are run at full system clock speed” “Programmable channel mode allows customization of channel function” “More flexibility in requesting DMA and interrupt service” “Channel flags can be tested” Added the following sentence in the “eQADC” section under the “Priority based Queues” bullet: “Streaming mode operation of Queue_0 to execute some commands several times”. Changed the following sentences in the “DSPI” section: “The DSPI can be configured ... that implements ... the Microsecond Bus protocol” to “The DSPI can be configured ... that supports ... the Microsecond Channel protocol”. “The DSPI pins support 5 V logic levels or Low Voltage Differential Signalling (LVDS) to improve high speed operation.” to “The DSPI ouput pins support 5 V logic levels or Low Voltage Differential Signalling (LVDS) according to the Microsecond Channel specification.”

Table 4. Revision history

Date	Revision	Description
08-Jun-2011	5	Made the following changes in the DSPI section: Changed “bus downlink” to “channel downstream”, “Microsecond bus” to “Microsecond channel”, “SIN” to “LVDS pads are for outputs only”, “1 to 16” to “4”, “bus standard” to “channel upstream”, and “17-pin Full Port interface in calibration tool calibration package” to “17-pin Full Port interface in calibration package used on calibration tool boards”. Updated the Order codes table summary table and figures. Changed the “Processor core” information of the SPC563M54P device to: “32-bit e200z335 with SPE and FPU support”. Added the following to the “Available only in the calibration package” sentence in the Features section (496 CSP package).
17-Sep-2013	6	Updated Disclaimer