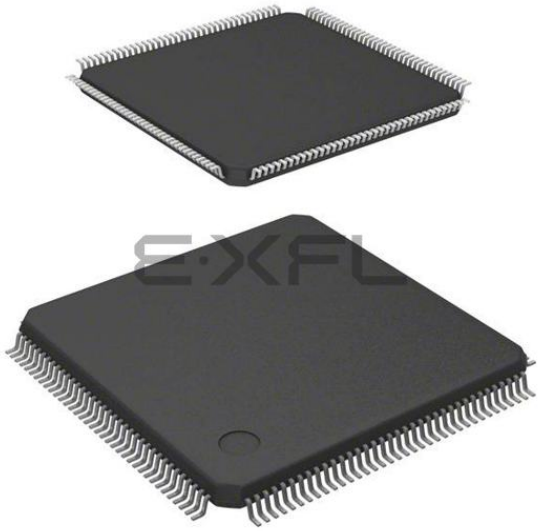

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z3
Core Size	32-Bit Single-Core
Speed	64MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	80
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	94K x 8
Voltage - Supply (Vcc/Vdd)	1.14V ~ 1.32V
Data Converters	A/D 32x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc563m64l5coby

List of figures

1 Introduction

The SPC563Mxx is a family of system-on-chip devices that are built on Power Architecture® technology and:

- Are 100% user-mode compatible with the classic Power Architecture instruction set
- Contain enhancements that improve the architecture's fit in embedded applications
- Include additional instruction support for digital signal processing (DSP)
- Integrate technologies, such as an enhanced time processor unit, enhanced queued analog-to-digital converter, Controller Area Network, and an enhanced modular input-output system, that are important for today's lower-end powertrain applications

This document describes the features of the SPC563Mxx and highlights important electrical and physical characteristics of the device.

1.1 Document overview

This document provides an overview and describes the features of the device series of microcontroller units (MCUs). For functional characteristics, refer to the device reference manual. For electrical specifications and package mechanical drawings, refer to the device data sheet. Pin assignments can be found in both the reference manual and data sheet.

1.2 Description

These 32-bit automotive microcontrollers are a family of system-on-chip (SoC) devices that contain all the features of the SPC563Mxx family and many new features coupled with high performance 90 nm CMOS technology to provide substantial reduction of cost per feature and significant performance improvement.

The advanced and cost-efficient host processor core of this automotive controller family is built on Power Architecture technology. This family contains enhancements that improve the architecture's fit in embedded applications, includes additional instruction support for digital signal processing (DSP), integrates technologies — such as an enhanced time processor unit, enhanced queued analog-to-digital converter, Controller Area Network, and an enhanced modular input-output system — that are important for today's lower-end powertrain applications.

The device has a single level of memory hierarchy consisting of up to 94 KB on-chip SRAM and up to 1.5 MB of internal flash memory. The device also has an external bus interface (EBI) for 'calibration'. This external bus interface has been designed to support most of the standard memories used with the SPC564Axx and SPC563Mxx families.

SPC563Mxx is part of a family of devices that contain many new features coupled with high performance 90 nm CMOS technology to provide substantial reduction of cost per feature and significant performance improvement.

The host processor core of the SPC563Mxx complies with the Power Architecture Book E. It is 100% user mode compatible (with floating point library) with the classic Power Architecture instruction set. The Book E architecture has enhancements that improve the Power Architecture's fit in embedded applications. In addition to the classic Power Architecture instruction set, this core also has additional instruction support for digital signal processing (DSP).

3 Device overview

The following sections provide high level descriptions of the features found on the SPC563Mxx.

3.1 Device comparison

Table 2. SPC563Mxx family device summary

Feature	SPC563M64	SPC563M60P	SPC563M54P
Flash memory size (KB)	1536	1024	768
Total SRAM size (KB)	94	64	48
Standby SRAM size (KB)	32	32	24
Processor core	32-bit e200z335 with SPE and FPU support	32-bit e200z335 with SPE and FPU support	32-bit e200z335 with SPE and FPU support
Core frequency (MHz)	64/80	40/64/80	40/64
Calibration bus width(1)	16 bits	16 bits	—
DMA (direct memory access) channels	32	32	32
eMIOS (enhanced modular input-output system) channels	16	16	8
eQADC (enhanced queued analog-to-digital converter) channels (on-chip)	Up to 34(2)	Up to 34(2)	Up to 32(2)
eSCI (serial communication interface)	2	2	2
DSPI (deserial serial peripheral interface)	2	2	2
Microsecond Channel compatible interface	2	2	2
eTPU (enhanced time processor unit)	Yes	Yes	Yes
Channels	32	32	32
Code memory (KB)	14	14	14
Parameter RAM (KB)	3	3	3
FlexCAN (controller area network)(3)	2	2	2
FMPLL (frequency-modulated phase-locked loop)	Yes	Yes	Yes
INTC (interrupt controller) channels	364(4)	364(4)	364(4)
JTAG controller	Yes	Yes	Yes
NDI (Nexus development interface) level	Class 2+	Class 2+	Class 2+
Non-maskable interrupt and critical interrupt	Yes	Yes	Yes
PIT (peripheral interrupt timers)	5	5	5
Task monitor timer	4 channels	4 channels	4 channels
Temperature sensor	Yes	Yes	Yes

Table 2. SPC563Mxx family device summary (continued)

Feature	SPC563M64	SPC563M60P	SPC563M54P
Windowing software watchdog	Yes	Yes	Yes
Packages	LQFP144 LQFP176	LQFP100 LQFP144 LQFP176	LQFP100 LQFP144

1. Calibration package only.
2. The 176-pin and 208-pin packages have 34 input channels; 144-pin package has 32; 100-pin package has 23.
3. One FlexCAN module has 64 message buffers; the other has 32 message buffers.
4. 165 interrupt channels are reserved for compatibility with future devices. This device has 191 peripheral interrupt sources plus 8 software interrupts available to the user.

3.2 Feature list

- Operating parameters
  - Fully static operation, 0 MHz – 80 MHz (plus 2% frequency modulation - 82 MHz)
  - –40 °C to 150 °C junction temperature operating range
  - Low power design
    - Less than 400 mW power dissipation (nominal)
    - Designed for dynamic power management of core and peripherals
    - Software controlled clock gating of peripherals
    - Low power stop mode, with all clocks stopped
  - Fabricated in 90 nm process
  - 1.2 V internal logic
  - Single power supply with 5.0 V –10% / +5% (4.5 V to 5.25 V) with internal regulator to provide 3.3 V and 1.2 V for the core
  - Input and output pins with 5.0 V –10% / +5% (4.5 V to 5.25 V) range
    - 35%/65% V_{DDE} CMOS switch levels (with hysteresis)
    - Selectable hysteresis
    - Selectable slew rate control
  - Nexus pins powered by 3.3 V supply
  - Designed with EMI reduction techniques
    - Phase-locked loop
    - Frequency modulation of system clock frequency
    - On-chip bypass capacitance
    - Selectable slew rate and drive strength
- High performance e200z335 core processor
  - 32-bit *Power Architecture Book E* programmer's model
  - Variable Length Encoding Enhancements
    - Allows Power Architecture instruction set to be optionally encoded in a mixed 16 and 32-bit instructions
    - Results in smaller code size
  - Single issue, 32-bit *Power Architecture technology* compliant CPU
  - In-order execution and retirement
  - Precise exception handling
  - Branch processing unit
    - Dedicated branch address calculation adder
    - Branch acceleration using Branch Lookahead Instruction Buffer
  - Load/store unit
    - One-cycle load latency
    - Fully pipelined
    - Big and Little Endian support
    - Misaligned access support
    - Zero load-to-use pipeline bubbles
  - Thirty-two 64-bit general purpose registers (GPRs)

  - 9-bit vector
    Unique vector for each interrupt request source
    Provided by hardware connection to processor or read from register
  - Each interrupt source can be programmed to one of 16 priorities
  - Preemption
    Preemptive prioritized interrupt requests to processor
    ISR at a higher priority preempts ISRs or tasks at lower priorities
    Automatic pushing or popping of preempted priority to or from a LIFO
    Ability to modify the ISR or task priority. Modifying the priority can be used to implement the Priority Ceiling Protocol for accessing shared resources.
  - Low latency—three clocks from receipt of interrupt request from peripheral to interrupt request to processor
- Frequency Modulating Phase-locked loop (FMPLL)
  - Reference clock pre-divider (PREDIV) for finer frequency synthesis resolution
  - Reduced frequency divider (RFD) for reducing the FMPLL output clock frequency without forcing the FMPLL to re-lock
  - System clock divider (SYSDIV) for reducing the system clock frequency in normal or bypass mode
  - Input clock frequency range from 4 MHz to 20 MHz before the pre-divider, and from 4 MHz to 16 MHz at the FMPLL input
  - Voltage controlled oscillator (VCO) range from 256 MHz to 512 MHz
  - VCO free-running frequency range from 25 MHz to 125 MHz
  - Four bypass modes: crystal or external reference with PLL on or off
  - Two normal modes: crystal or external reference
  - Programmable frequency modulation
    Triangle wave modulation
    Register programmable modulation frequency and depth
  - Lock detect circuitry reports when the FMPLL has achieved frequency lock and continuously monitors lock status to report loss of lock conditions
    User-selectable ability to generate an interrupt request upon loss of lock
    User-selectable ability to generate a system reset upon loss of lock
  - Clock quality monitor (CQM) module provides loss-of-clock detection for the FMPLL reference and output clocks
    User-selectable ability to generate an interrupt request upon loss of clock
    User-selectable ability to generate a system reset upon loss of clock
    Backup clock (reference clock or FMPLL free-running) can be applied to the system in case of loss of clock
- Calibration bus interface (EBI)
  - Available only in the calibration package (496 CSP package)
  - 1.8 V to 3.3 V ± 10% I/O (1.6 V to 3.6 V)
  - Memory controller with support for various memory types
  - 16-bit data bus, up to 22-bit address bus
  - Selectable drive strength

  - Configurable bus speed modes
  - Bus monitor
  - Configurable wait states
- System integration unit (SIU)
  - Centralized GPIO control of 80 I/O pins
  - Centralized pad control on a per-pin basis
    Pin function selection
    Configurable weak pull-up or pull-down
    Drive strength
    Slew rate
    Hysteresis
  - System reset monitoring and generation
  - External interrupt inputs, filtering and control
  - Critical Interrupt control
  - Non-Maskable Interrupt control
  - Internal multiplexer subblock (IMUX)
    Allows flexible selection of eQADC trigger inputs (eTPU, eMIOS and external signals)
    Allows selection of interrupt requests between external pins and DSPI
- Error correction status module (ECSM)
  - Configurable error-correcting codes (ECC) reporting
  - Single-bit error correction reporting
- On-chip Flash memory
  - Up to 1.5 MB flash memory, accessed via a 64-bit wide bus interface
  - 16 KB shadow block
  - Fetch Accelerator
    Provide single cycle flash access at 80 MHz
    Quadruple 128-bit wide prefetch/burst buffers
    Prefetch buffers can be configured to prefetch code or data or both
  - Censorship protection scheme to prevent flash content visibility
  - Flash divided into two independent arrays, allowing reading from one array while erasing/programming the other array (used for EEPROM emulation)
  - Memory block:
    For SPC563M64: 18 blocks (4×16 KB, 2×32 KB, 2×64 KB, 10×128 KB)
    For SPC563M60P: 14 blocks (4×16 KB, 2×32 KB, 2×64 KB, 6×128 KB)
    For SPC563M54P: 12 blocks (4×16 KB, 2×32 KB, 2×64 KB, 4×128 KB)
  - Hardware programming state machine
- On-chip static RAM
  - For SPC563M64: 94 KB general purpose RAM of which 32 KB are on standby power supply
  - For SPC563M60P: 64 KB general purpose RAM of which 32 KB are on standby power supply
  - For SPC563M54P: 48 KB general purpose RAM of which 24 KB are on standby

- Zero jitter triggering for queue 0. (Queue 0 trigger causes current conversion to be aborted and the queued conversions in the CBUFFER to be bypassed. Delay from Trigger to start of conversion is 13 system clocks + 1 ADC clock.)
- eQADC Result Streaming. Generation of a continuous stream of ADC conversion results from a single eQADC command word. Controlled by two different trigger signals; one to define the rate at which results are generated and the other to define the beginning and ending of the stream. Used to digitize waveforms during specific time/angle windows, e.g., engine knock sensor sampling.
- Angular Decimation. The ability of the eQADC to sample an analog waveform in the time domain, perform Finite Impulse Response (FIR) or Infinite Impulse Response (IIR) filtering also in the time domain, but to down sample the results in the angle domain. Resulting in a time domain filtered result at a given engine

  - One with 32 message buffers; the second with 64 message buffers
  - Full implementation of the CAN protocol specification, Version 2.0B
  - Programmable acceptance filters
  - Short latency time for high priority transmit messages
  - Arbitration scheme according to message ID or message buffer number
  - Listen only mode capabilities
  - Programmable clock source: system clock or oscillator clock
  - Message buffers may be configured as mailboxes or as FIFO
- Nexus port controller (NPC)
  - Per IEEE-ISTO 5001-2003
  - Real time development support for Power Architecture core and eTPU engine through Nexus class 2/1
  - Read and write access (Nexus class 3 feature that is supported on this device)
    Run-time access of entire memory map
    Calibration
  - Support for data value breakpoints / watchpoints
    Run-time access of entire memory map
    Calibration
    Table constants calibrated using MMU and internal and external RAM
    Scalar constants calibrated using cache line locking
  - Configured via the IEEE 1149.1 (JTAG) port
- IEEE 1149.1 JTAG controller (JTAGC)
  - IEEE 1149.1-2001 Test Access Port (TAP) interface
  - 5-bit instruction register that supports IEEE 1149.1-2001 defined instructions
  - 5-bit instruction register that supports additional public instructions
  - Three test data registers: a bypass register, a boundary scan register, and a device identification register
  - Censorship disable register. By writing the 64-bit serial boot password to this register, Censorship may be disabled until the next reset
  - TAP controller state machine that controls the operation of the data registers, instruction register and associated circuitry
- On-chip Voltage Regulator for single 5 V supply operation
  - On-chip regulator 5 V to 3.3 V for internal supplies
  - On-chip regulator controller 5 V to 1.2 V (with external bypass transistor) for core logic
- Low-power modes
  - SLOW Mode. Allows device to be run at very low speed (approximately 1 MHz), with modules (including the PLL) selectively disabled in software
  - STOP Mode. System clock stopped to all modules including the CPU. Wake-up timer used to restart the system clock after a predetermined time

3.3 Feature details

3.3.1 e200z335 core

The e200z335 processor utilizes a four stage pipeline for instruction execution. The Instruction Fetch (stage 1), Instruction Decode/Register file Read/Effective Address Calculation (stage 2), Execute/Memory Access (stage 3), and Register Writeback (stage 4) stages operate in an overlapped fashion, allowing single clock instruction execution for most instructions.

The integer execution unit consists of a 32-bit Arithmetic Unit (AU), a Logic Unit (LU), a 32-bit Barrel shifter (Shifter), a Mask-Insertion Unit (MIU), a Condition Register manipulation Unit (CRU), a Count-Leading-Zeros unit (CLZ), a 32×32 Hardware Multiplier array, result feed-forward hardware, and support hardware for division.

Most arithmetic and logical operations are executed in a single cycle with the exception of the divide instructions. A Count-Leading-Zeros unit operates in a single clock cycle. The Instruction Unit contains a PC incrementer and a dedicated Branch Address adder to minimize delays during change of flow operations. Sequential prefetching is performed to ensure a supply of instructions into the execution pipeline. Branch target prefetching is performed to accelerate taken branches. Prefetched instructions are placed into an instruction buffer capable of holding six instructions.

Branches can also be decoded at the instruction buffer and branch target addresses calculated prior to the branch reaching the instruction decode stage, allowing the branch target to be prefetched early. When a branch is detected at the instruction buffer, a prediction may be made on whether the branch is taken or not. If the branch is predicted to be taken, a target fetch is initiated and its target instructions are placed in the instruction buffer following the branch instruction. Many branches take zero cycle to execute by using branch folding. Branches are folded out from the instruction execution pipe whenever possible. These include unconditional branches and conditional branches with condition codes that can be resolved early.

Conditional branches which are not taken and not folded execute in a single clock. Branches with successful target prefetching which are not folded have an effective execution time of one clock. All other taken branches have an execution time of two clocks. Memory load and store operations are provided for byte, halfword, and word (32-bit) data with automatic zero or sign extension of byte and halfword load data as well as optional byte reversal of data. These instructions can be pipelined to allow effective single cycle throughput. Load and store multiple word instructions allow low overhead context save and restore operations. The load/store unit contains a dedicated effective address adder to allow effective address generation to be optimized. Also, a load-to-use dependency does not incur any pipeline bubbles for most cases.

The Condition Register unit supports the condition register (CR) and condition register operations defined by the Power Architecture. The condition register consists of eight 4-bit fields that reflect the results of certain operations, such as move, integer and floating-point compare, arithmetic, and logical instructions, and provide a mechanism for testing and branching. Vectored and autovectored interrupts are supported by the CPU. Vectored interrupt support is provided to allow multiple interrupt sources to have unique interrupt handlers invoked with no software overhead.

The hardware floating-point unit utilizes the IEEE-754 single-precision floating-point format and supports single-precision floating-point operations in a pipelined fashion. The general purpose register file is used for source and destination operands, thus there is a unified

Note: The calibration EBI must be configured in multiplexed mode when the extended Nexus trace is used on the VertiCal Calibration Systemcalibration tool. This is because Nexus signals and address lines of the calibration bus share the same balls in the calibration package.

- Memory controller with support for various memory types:
  - Asynchronous/legacy flash and SRAM
- Bus monitor
  - User selectable
  - Programmable time-out period (with 8 external bus clock resolution)
- Configurable wait states (via chip selects)
- 3 chip-select (Cal_$\overline{CS}$[0], Cal_$\overline{CS}$[2:3]) signals (Multiplexed with 2 most significant address signals)
- 2 write/byte enable (WE[0:1]/BE[0:1]) signals
- Configurable bus speed modes
  - system frequency
  - 1/2 of system frequency
  - 1/4 of system frequency
- Optional automatic CLKOUT gating to save power and reduce EMI
- Selectable drive strengths; 10 pF, 20 pF, 30 pF, 50 pF

3.3.7 SIU

The SPC563Mxx SIU controls MCU reset configuration, pad configuration, external interrupt, general purpose I/O (GPIO), internal peripheral multiplexing, and the system reset operation. The reset configuration block contains the external pin boot configuration logic. The pad configuration block controls the static electrical characteristics of I/O pins. The GPIO block provides uniform and discrete input/output control of the I/O pins of the MCU. The reset controller performs reset monitoring of internal and external reset sources, and

drives the $\overline{\text{RSTOUT}}$ pin. Communication between the SIU and the e200z335 CPU core is via the crossbar switch. The SIU provides the following features:

- System configuration
  - MCU reset configuration via external pins
  - Pad configuration control for each pad
  - Pad configuration control for virtual I/O via DSPI serialization
- System reset monitoring and generation
  - Power-on reset support
  - Reset status register provides last reset source to software
  - Glitch detection on reset input
  - Software controlled reset assertion
- External interrupt
  - 11 interrupt requests
  - Rising or falling edge event detection
  - Programmable digital filter for glitch rejection
  - Critical Interrupt request
  - Non-Maskable Interrupt request
- GPIO
  - GPIO function on 80 I/O pins
  - Virtual GPIO on 64 I/O pins via DSPI serialization (requires external deserialization device)
  - Dedicated input and output registers for setting each GPIO and Virtual GPIO pin
- Internal multiplexing
  - Allows serial and parallel chaining of DSPIs
  - Allows flexible selection of eQADC trigger inputs
  - Allows selection of interrupt requests between external pins and DSPI

3.3.8 ECSM

The error correction status module provides status information regarding platform memory errors reported by error-correcting codes.

3.3.9 Flash

Devices in the SPC563Mxx family provide up to 1.5 MB of programmable, non-volatile, flash memory. The non-volatile memory (NVM) can be used for instruction and/or data storage. The flash module includes a Fetch Accelerator, that optimizes the performance of the flash array to match the CPU architecture and provides single cycle random access to the flash @ 80 MHz. The flash module interfaces the system bus to a dedicated flash memory array controller. For CPU ‘loads’, DMA transfers and CPU instruction fetch, it supports a 64-bit data bus width at the system bus port, and a 128-bit read data interface to flash memory. The module contains a four-entry, 128-bit prefetch buffer and a prefetch controller which prefetches sequential lines of data from the flash array into the buffer. Prefetch buffer hits allow no-wait responses. Normal flash array accesses are registered and are forwarded to the system bus on the following cycle, incurring three wait-states. Prefetch operations may be automatically controlled, and are restricted to instruction fetch.

The Flash memory provides the following features:

- Supports a 64-bit data bus for instruction fetch, CPU loads and DMA access. Byte, halfword, word and doubleword reads are supported. Only aligned word and doubleword writes are supported.
- Fetch accelerator
  - Architected to optimize the performance of the flash with the CPU to provide single cycle random access to the flash up to 80 MHz system clock speed
  - Configurable read buffering and line prefetch support
  - Four line read buffers (128 bits wide) and a prefetch controller
- Hardware and software configurable read and write access protections on a per-master basis
- Interface to the Flash array controller is pipelined with a depth of one, allowing overlapped accesses to proceed in parallel for interleaved or pipelined Flash array designs
- Configurable access timing allowing use in a wide range of system frequencies
- Multiple-mapping support and mapping-based block access timing (0-31 additional cycles) allowing use for emulation of other memory types
- Software programmable block program/erase restriction control
- Erase of selected block(s)
- Read page size of 128 bits (four words)
- ECC with single-bit correction, double-bit detection
- Program page size of 64 bits (two words)
- ECC single-bit error corrections are visible to software
- Minimum program size is two consecutive 32-bit words, aligned on a 0-modulo-8 byte address, due to ECC
- Embedded hardware program and erase algorithm
- Erase suspend
- Shadow information stored in non-volatile shadow block
- Independent program/erase of the shadow block

3.3.10 SRAM

The SPC563Mxx SRAM module provides a general-purpose up to 94 KB memory block. The SRAM controller includes these features:

- Supports read/write accesses mapped to the SRAM memory from any master
- 32 KB or 24 KB block powered by separate supply for standby operation
- Byte, halfword, word and doubleword addressable
- ECC performs single-bit correction, double-bit detection on 32-bit data element

3.3.11 BAM

The BAM (Boot Assist Module) is a block of read-only memory that is programmed once by ST and is identical for all SPC563Mxx MCUs. The BAM program is executed every time the

MCU is powered-on or reset in normal mode. The BAM supports different modes of booting. They are:

- Booting from internal Flash memory
- Serial boot loading (A program is downloaded into RAM via eSCI or the FlexCAN and then executed)
- Booting from external memory on calibration bus

The BAM also reads the reset configuration half word (RCHW) from internal flash memory and configures the SPC563Mxx hardware accordingly. The BAM provides the following features:

- Sets up MMU to cover all resources and mapping all physical address to logical addresses with minimum address translation
- Sets up the MMU to allow user boot code to execute as either Power Architecture code (default) or as VLE code
- Detection of user boot code
- Automatic switch to serial boot mode if internal flash is blank or invalid
- Supports user programmable 64-bit password protection for serial boot mode
- Supports serial bootloading via FlexCAN bus and eSCI using fixed baudrate protocol
- Supports serial bootloading via FlexCAN bus and eSCI with auto baud rate sensing
- Supports serial bootloading of either Power Architecture code (default) or VLE code
- Supports booting from calibration bus interface
- Supports censorship protection for internal Flash memory
- Provides an option to enable the core watchdog timer
- Provides an option to disable the system watchdog timer

3.3.12 eMIOS

The eMIOS (Enhanced Modular Input Output System) module provides the functionality to generate or measure time events. The channels on this module provide a range of operating modes including the capability to perform dual input capture or dual output compare as well as PWM output.

The DSPIs also support these features unique to the DSI and CSI configurations:

- 2 sources of the serialized data:
  - eTPU_A and eMIOS output channels
  - Memory-mapped register in the DSPI
- Destinations for the deserialized data:
  - eTPU_A and eMIOS input channels
  - SIU External Interrupt Request inputs
  - Memory-mapped register in the DSPI
- Deserialized data is provided as Parallel Output signals and as bits in a memory-mapped register
- Transfer initiation conditions:
  - Continuous
  - Edge sensitive hardware trigger
  - Change in data
- Pin serialization/deserialization with interleaved SPI frames for control and diagnostics
- Continuous serial communications clock
- Support for parallel and serial chaining of up to four DSPI blocks

3.3.16 eSCI

The enhanced Serial Communications Interface (eSCI) allows asynchronous serial communications with peripheral devices and other MCUs. It includes special support to

external address and data pins for internal visibility. The NPC block is an integration of several individual Nexus blocks that are selected to provide the development support interface for SPC563Mxx. The NPC block interfaces to the host processor (e200z335), eTPU, and internal buses to provide development support as per the IEEE-ISTO 5001-2003 standard. The development support provided includes program trace and run-time access to the MCUs internal memory map and access to the Power Architecture and eTPU internal registers during halt. The Nexus interface also supports a JTAG only mode using only the JTAG pins. SPC563Mxx in the production LQFP144 supports a 3.3 V reduced (4-bit wide) Auxiliary port. These Nexus port pins can also be used as 5 V I/O signals to increase usable I/O count of the device. When using this Nexus port as IO, Nexus trace is still possible using calibration tool calibration. In the calibration tool calibration package, the full 12-bit Auxiliary port is available.

Note: In the calibration tool package, the full Nexus Auxiliary port shares balls with the addresses of the calibration bus. Therefore multiplexed address/data bus mode must be used for the calibration bus when using full width Nexus trace in calibration tool assembly.

Note: This feature is imprecise due to CPU pipelining.

  - Subset of Power Architecture software debug facilities with OnCE block (Nexus class 1 features)
- eTPU development support features
  - IEEE-ISTO 5001-2003 standard class 1 compliant for the eTPU
  - Nexus based breakpoint configuration and single step support (JTAG feature of the eTPU)
- Run-time access to the on-chip memory map via the Nexus read/write access protocol. This feature supports accesses for run-time internal visibility, calibration variable acquisition, calibration constant tuning, and external rapid prototyping for powertrain automotive development systems.
- All features are independently configurable and controllable via the IEEE 1149.1 I/O port
- Power-on-reset status indication during reset via MDO[0] in disabled and reset modes

JTAG

The JTAGC (JTAG Controller) block provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode. Testing is performed via a boundary scan technique, as defined in the IEEE 1149.1-2001 standard. All data input to and output from the JTAGC block is communicated in serial format. The JTAGC block is compliant with the IEEE 1149.1-2001 standard and supports the following features:

- IEEE 1149.1-2001 Test Access Port (TAP) interface 4 pins (TDI, TMS, TCK, and TDO)
- A 5-bit instruction register that supports the following IEEE 1149.1-2001 defined instructions:
  - BYPASS, IDCODE, EXTEST, SAMPLE, SAMPLE/PRELOAD, HIGHZ, CLAMP
- A 5-bit instruction register that supports the additional following public instructions:
  - ACCESS_AUX_TAP_NPC
  - ACCESS_AUX_TAP_ONCE
  - ACCESS_AUX_TAP_eTPU
  - ACCESS_CENSOR
- 3 test data registers to support JTAG Boundary Scan mode
  - Bypass register
  - Boundary scan register
  - Device identification register
- A TAP controller state machine that controls the operation of the data registers, instruction register and associated circuitry
- Censorship Inhibit Register
  - 64-bit Censorship password register
  - If the external tool writes a 64-bit password that matches the Serial Boot password stored in the internal flash shadow row, Censorship is disabled until the next system reset.

5 Revision history

Table 4. Revision history

Date	Revision	Description
30-Aug-2007	1	Initial release.
7-Nov-2007	2	Removed: – - Section 5: LQFP144 pinout diagram including Figure 2: LQFP144 pinout – - Section 6: LQFP144 pin description including Table 3: LQFP144 pin description – - Section 7: LFBGA208 ballout diagram including Figure 3: LFBGA208 ballout Added – - Section 5: Signal description on page 43 including Section 5.1: Signal properties summary, Table 3: SPC563M60 signal properties, Section 5.2: Detailed signal descriptions, Section 5.3: I/O power/ground segmentation and Table 4: SPC563M60 power/ground segmentation – - Section 6: Device pin outs on page 69 including Section 6.1: LQFP144 pinout, Figure 2: LQFP144 pinout, Section 6.2: LFBGA208 ballout diagram and Figure 3: LFBGA208 ballout diagram Removed parameters D3 and E3 from Figure 4: LQFP144 (20 x 20 x 1.40 mm) package mechanical outline: Removed minimum and maximum values for parameters D, D1, E and E1 and removed parameters D3 and E3 from Table 6: LQFP144 package mechanical data on page 74: Added note about LQFP144 package and JEDEC compliancy to Section 8: Package information on page 73
13-Mar-2009	3	Updated document to include information on all members of the SPC563Mxx family. Replaced references to the core (was “e200z3”, is “e200z335”) and Nexus module (was “Nexus development interface (NDI)”, is “Nexus port controller (NPC)”). Changed the arrangement of V_{STBY}, the standby RAM, and the voltage regulator in the block diagram. Revised the device-comparison table and feature list. In the “Feature List” section, added “(for 100- and 144-pin packages)” to the “Single power supply” operating parameter. In the “Feature Details” section, replaced the CI/NMI text in the INTC description with information on the NMI only. Reformatted company-specific references. Added a revision history. Formatting, spelling, grammar, and layout corrections.

Table 4. Revision history

Date	Revision	Description
08-Jun-2011	5	Replaced in all document "... Architecture Book E compliant..." with "... Architecture technology compliant..." Updated "Introduction": Added "Document overview" and "Description" sections. Made the following changes in the "Description" section: – Added "Floating Point Unit (FPU)" bullet under "Single issue, 32-bit Power Architecture technology compliant e200z335 CPU core complex". – Changed "eTPU" to "eTPU2" in the "32-channel second-generation enhanced time processor unit" sentence. – Changed the "Available in LQFP100, LQFP144, LQFP176 and LBGA208" sentence to "Designed for LQFP100, LQFP144, LQFP176, and LBGA208 packages". Replaced all instances of "Microsecond Bus" with "Microsecond Channel". Replaced all instances of "SPC563M54" and "SPC563M60" with "SPC563M54P"and "SPC563M60P", respectively. Changed the "Standby SRAM size" of the SPC563M60P device from "24" to "32". Replaced all instances of "downlink" with "downstream" and "uplink" with "upstream". Made the following changes in the "Flash" section: Changed "Program page size of 128 bits (four words) to accelerate programming" to "Program page size of 64 bits (two words)". Changed "Erase suspend, program suspend and erase-suspended program" to "Erase suspend". Made editorial changes in the "BAM" section: Updated the conditional tags in the "Supports serial bootloading..." sentences. Changed "Shared time bases with the eTPU through the counter buses" to "Shared time bases with the eTPU2 through the counter buses" in the "eMIOS" section. Removed the following sentences from the "eTPU2" section: "For Monaco 1.5M, the eTPU2 has been further enhanced with these features:" "Timebases and channels are run at full system clock speed" "Programmable channel mode allows customization of channel function" "More flexibility in requesting DMA and interrupt service" "Channel flags can be tested" Added the following sentence in the "eQADC" section under the "Priority based Queues" bullet: "Streaming mode operation of Queue_0 to execute some commands several times". Changed the following sentences in the "DSPI" section: "The DSPI can be configured ... that implements ... the Microsecond Bus protocol" to "The DSPI can be configured ... that supports ... the Microsecond Channel protocol". "The DSPI pins support 5 V logic levels or Low Voltage Differential Signalling (LVDS) to improve high speed operation." to "The DSPI ouput pins support 5 V logic levels or Low Voltage Differential Signalling (LVDS) according to the Microsecond Channel specification."

Table 4. Revision history

Date	Revision	Description
08-Jun-2011	5	Made the following changes in the DSPI section: Changed “bus downlink” to “channel downstream”, “Microsecond bus” to “Microsecond channel”, “SIN” to “LVDS pads are for outputs only”, “1 to 16” to “4”, “bus standard” to “channel upstream”, and “17-pin Full Port interface in calibration tool calibration package” to “17-pin Full Port interface in calibration package used on calibration tool boards”. Updated the Order codes table summary table and figures. Changed the “Processor core” information of the SPC563M54P device to: “32-bit e200z335 with SPE and FPU support”. Added the following to the “Available only in the calibration package” sentence in the Features section (496 CSP package).
17-Sep-2013	6	Updated Disclaimer