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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	e200z3
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, EBI/EMI, LINbus, SCI, SPI, UART/USART
Peripherals	DMA, POR, PWM, WDT
Number of I/O	80
Program Memory Size	1.5MB (1.5M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	94K x 8
Voltage - Supply (Vcc/Vdd)	1.14V ~ 1.32V
Data Converters	A/D 34x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	176-LQFP
Supplier Device Package	176-LQFP (24x24)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/spc563m64l7coar

Contents

The SPC563Mxx has a single level of memory hierarchy consisting of up to 94 KB on-chip SRAM and up to 1.5 MB of internal Flash memory. The SPC563Mxx also has an external bus interface (EBI) for 'calibration'[(b)].

On-chip modules include:

- Single issue, 32-bit Power Architecture technology compliant e200z335 CPU core complex
  - Includes Variable Length Encoding (VLE) enhancements for code size reduction
  - Floating Point Unit (FPU)
- 32-channel direct memory access controller (DMA)
- Interrupt controller (INTC) capable of handling 364 selectable-priority interrupt sources—191 peripheral interrupt sources, 8 software interrupts and 165 reserved interrupts.
- Frequency-modulated phase-locked loop (FMPLL)
- Calibration external bus interface (EBI)[b]
- System integration unit (SIU)
- Up to 1.5 MB on-chip flash with flash controller
  - Fetch Accelerator for single cycle flash access @80 MHz
- Up to 94 KB on-chip static RAM (including up to 32 KB standby RAM)
- Boot assist module (BAM)
- 32-channel second-generation enhanced time processor unit (eTPU2)
  - 32 standard eTPU channels
  - Architectural enhancements to improve code efficiency and added flexibility
- 16-channels enhanced modular input-output system (eMIOS)
- Enhanced queued analog-to-digital converter (eQADC)
- Decimation filter (part of eQADC)
- Silicon die temperature sensor
- Two deserial serial peripheral interface (DSPI) modules (compatible with Microsecond Channel)
- Two enhanced serial communication interface (eSCI) modules compatible with LIN
- Two Controller Area Network (FlexCAN) modules that support CAN 2.0B
- Nexus port controller (NPC) per IEEE-ISTO 5001-2003 standard
- IEEE 1149.1 (JTAG) support
- Nexus interface
- On-chip voltage regulator controller that provides 1.2 V and 3.3 V internal supplies from a 5 V external source
- Designed for LQFP100, LQFP144, LQFP176, and LBGA208 packages

b. The external bus interface is only accessible when using the calibration tool. It is not available on production packages.

  - 9-bit vector
    Unique vector for each interrupt request source
    Provided by hardware connection to processor or read from register
  - Each interrupt source can be programmed to one of 16 priorities
  - Preemption
    Preemptive prioritized interrupt requests to processor
    ISR at a higher priority preempts ISRs or tasks at lower priorities
    Automatic pushing or popping of preempted priority to or from a LIFO
    Ability to modify the ISR or task priority. Modifying the priority can be used to implement the Priority Ceiling Protocol for accessing shared resources.
  - Low latency—three clocks from receipt of interrupt request from peripheral to interrupt request to processor
- Frequency Modulating Phase-locked loop (FMPLL)
  - Reference clock pre-divider (PREDIV) for finer frequency synthesis resolution
  - Reduced frequency divider (RFD) for reducing the FMPLL output clock frequency without forcing the FMPLL to re-lock
  - System clock divider (SYSDIV) for reducing the system clock frequency in normal or bypass mode
  - Input clock frequency range from 4 MHz to 20 MHz before the pre-divider, and from 4 MHz to 16 MHz at the FMPLL input
  - Voltage controlled oscillator (VCO) range from 256 MHz to 512 MHz
  - VCO free-running frequency range from 25 MHz to 125 MHz
  - Four bypass modes: crystal or external reference with PLL on or off
  - Two normal modes: crystal or external reference
  - Programmable frequency modulation
    Triangle wave modulation
    Register programmable modulation frequency and depth
  - Lock detect circuitry reports when the FMPLL has achieved frequency lock and continuously monitors lock status to report loss of lock conditions
    User-selectable ability to generate an interrupt request upon loss of lock
    User-selectable ability to generate a system reset upon loss of lock
  - Clock quality monitor (CQM) module provides loss-of-clock detection for the FMPLL reference and output clocks
    User-selectable ability to generate an interrupt request upon loss of clock
    User-selectable ability to generate a system reset upon loss of clock
    Backup clock (reference clock or FMPLL free-running) can be applied to the system in case of loss of clock
- Calibration bus interface (EBI)
  - Available only in the calibration package (496 CSP package)
  - 1.8 V to 3.3 V ± 10% I/O (1.6 V to 3.6 V)
  - Memory controller with support for various memory types
  - 16-bit data bus, up to 22-bit address bus
  - Selectable drive strength

  - Configurable bus speed modes
  - Bus monitor
  - Configurable wait states
- System integration unit (SIU)
  - Centralized GPIO control of 80 I/O pins
  - Centralized pad control on a per-pin basis
    Pin function selection
    Configurable weak pull-up or pull-down
    Drive strength
    Slew rate
    Hysteresis
  - System reset monitoring and generation
  - External interrupt inputs, filtering and control
  - Critical Interrupt control
  - Non-Maskable Interrupt control
  - Internal multiplexer subblock (IMUX)
    Allows flexible selection of eQADC trigger inputs (eTPU, eMIOS and external signals)
    Allows selection of interrupt requests between external pins and DSPI
- Error correction status module (ECSM)
  - Configurable error-correcting codes (ECC) reporting
  - Single-bit error correction reporting
- On-chip Flash memory
  - Up to 1.5 MB flash memory, accessed via a 64-bit wide bus interface
  - 16 KB shadow block
  - Fetch Accelerator
    Provide single cycle flash access at 80 MHz
    Quadruple 128-bit wide prefetch/burst buffers
    Prefetch buffers can be configured to prefetch code or data or both
  - Censorship protection scheme to prevent flash content visibility
  - Flash divided into two independent arrays, allowing reading from one array while erasing/programming the other array (used for EEPROM emulation)
  - Memory block:
    For SPC563M64: 18 blocks (4×16 KB, 2×32 KB, 2×64 KB, 10×128 KB)
    For SPC563M60P: 14 blocks (4×16 KB, 2×32 KB, 2×64 KB, 6×128 KB)
    For SPC563M54P: 12 blocks (4×16 KB, 2×32 KB, 2×64 KB, 4×128 KB)
  - Hardware programming state machine
- On-chip static RAM
  - For SPC563M64: 94 KB general purpose RAM of which 32 KB are on standby power supply
  - For SPC563M60P: 64 KB general purpose RAM of which 32 KB are on standby power supply
  - For SPC563M54P: 48 KB general purpose RAM of which 24 KB are on standby

  - One with 32 message buffers; the second with 64 message buffers
  - Full implementation of the CAN protocol specification, Version 2.0B
  - Programmable acceptance filters
  - Short latency time for high priority transmit messages
  - Arbitration scheme according to message ID or message buffer number
  - Listen only mode capabilities
  - Programmable clock source: system clock or oscillator clock
  - Message buffers may be configured as mailboxes or as FIFO
- Nexus port controller (NPC)
  - Per IEEE-ISTO 5001-2003
  - Real time development support for Power Architecture core and eTPU engine through Nexus class 2/1
  - Read and write access (Nexus class 3 feature that is supported on this device)
    Run-time access of entire memory map
    Calibration
  - Support for data value breakpoints / watchpoints
    Run-time access of entire memory map
    Calibration
    Table constants calibrated using MMU and internal and external RAM
    Scalar constants calibrated using cache line locking
  - Configured via the IEEE 1149.1 (JTAG) port
- IEEE 1149.1 JTAG controller (JTAGC)
  - IEEE 1149.1-2001 Test Access Port (TAP) interface
  - 5-bit instruction register that supports IEEE 1149.1-2001 defined instructions
  - 5-bit instruction register that supports additional public instructions
  - Three test data registers: a bypass register, a boundary scan register, and a device identification register
  - Censorship disable register. By writing the 64-bit serial boot password to this register, Censorship may be disabled until the next reset
  - TAP controller state machine that controls the operation of the data registers, instruction register and associated circuitry
- On-chip Voltage Regulator for single 5 V supply operation
  - On-chip regulator 5 V to 3.3 V for internal supplies
  - On-chip regulator controller 5 V to 1.2 V (with external bypass transistor) for core logic
- Low-power modes
  - SLOW Mode. Allows device to be run at very low speed (approximately 1 MHz), with modules (including the PLL) selectively disabled in software
  - STOP Mode. System clock stopped to all modules including the CPU. Wake-up timer used to restart the system clock after a predetermined time

For high priority interrupt requests, the time from the assertion of the interrupt request from the peripheral to when the processor is executing the interrupt service routine (ISR) has been minimized. The INTC provides a unique vector for each interrupt request source for quick determination of which ISR needs to be executed. It also provides an ample number of priorities so that lower priority ISRs do not delay the execution of higher priority ISRs. To allow the appropriate priorities for each source of interrupt request, the priority of each interrupt request is software configurable.

When multiple tasks share a resource, coherent accesses to that resource need to be supported. The INTC supports the priority ceiling protocol for coherent accesses. By providing a modifiable priority mask, the priority can be raised temporarily so that all tasks which share the resource can not preempt each other.

Multiple processors can assert interrupt requests to each other through software setable interrupt requests. These same software setable interrupt requests also can be used to break the work involved in servicing an interrupt request into a high priority portion and a low priority portion. The high priority portion is initiated by a peripheral interrupt request, but then the ISR asserts a software setable interrupt request to finish the servicing in a lower priority ISR. Therefore these software setable interrupt requests can be used instead of the peripheral ISR scheduling a task through the RTOS.

The INTC provides the following features:

- 356 peripheral interrupt request sources
- 8 software setable interrupt request sources
- 9-bit vector addresses
- Unique vector for each interrupt request source
- Hardware connection to processor or read from register
- Each interrupt source can be programmed to one of 16 priorities
- Preemptive prioritized interrupt requests to processor
- ISR at a higher priority preempts executing ISRs or tasks at lower priorities
- Automatic pushing or popping of preempted priority to or from a LIFO
- Ability to modify the ISR or task priority to implement the priority ceiling protocol for accessing shared resources
- Low latency—three clocks from receipt of interrupt request from peripheral to interrupt request to processor

This device also includes a non-maskable interrupt (NMI) pin that bypasses the INTC and multiplexing logic.

3.3.5 FMPLL

The FMPLL allows the user to generate high speed system clocks from a 4 MHz to 20 MHz crystal oscillator or external clock generator. Further, the FMPLL supports programmable frequency modulation of the system clock. The PLL multiplication factor, output clock divider ratio are all software configurable.

Note: The calibration EBI must be configured in multiplexed mode when the extended Nexus trace is used on the VertiCal Calibration Systemcalibration tool. This is because Nexus signals and address lines of the calibration bus share the same balls in the calibration package.

- Memory controller with support for various memory types:
  - Asynchronous/legacy flash and SRAM
- Bus monitor
  - User selectable
  - Programmable time-out period (with 8 external bus clock resolution)
- Configurable wait states (via chip selects)
- 3 chip-select (Cal_$\overline{CS}$[0], Cal_$\overline{CS}$[2:3]) signals (Multiplexed with 2 most significant address signals)
- 2 write/byte enable (WE[0:1]/BE[0:1]) signals
- Configurable bus speed modes
  - system frequency
  - 1/2 of system frequency
  - 1/4 of system frequency
- Optional automatic CLKOUT gating to save power and reduce EMI
- Selectable drive strengths; 10 pF, 20 pF, 30 pF, 50 pF

3.3.7 SIU

The SPC563Mxx SIU controls MCU reset configuration, pad configuration, external interrupt, general purpose I/O (GPIO), internal peripheral multiplexing, and the system reset operation. The reset configuration block contains the external pin boot configuration logic. The pad configuration block controls the static electrical characteristics of I/O pins. The GPIO block provides uniform and discrete input/output control of the I/O pins of the MCU. The reset controller performs reset monitoring of internal and external reset sources, and

drives the $\overline{\text{RSTOUT}}$ pin. Communication between the SIU and the e200z335 CPU core is via the crossbar switch. The SIU provides the following features:

- System configuration
  - MCU reset configuration via external pins
  - Pad configuration control for each pad
  - Pad configuration control for virtual I/O via DSPI serialization
- System reset monitoring and generation
  - Power-on reset support
  - Reset status register provides last reset source to software
  - Glitch detection on reset input
  - Software controlled reset assertion
- External interrupt
  - 11 interrupt requests
  - Rising or falling edge event detection
  - Programmable digital filter for glitch rejection
  - Critical Interrupt request
  - Non-Maskable Interrupt request
- GPIO
  - GPIO function on 80 I/O pins
  - Virtual GPIO on 64 I/O pins via DSPI serialization (requires external deserialization device)
  - Dedicated input and output registers for setting each GPIO and Virtual GPIO pin
- Internal multiplexing
  - Allows serial and parallel chaining of DSPIs
  - Allows flexible selection of eQADC trigger inputs
  - Allows selection of interrupt requests between external pins and DSPI

3.3.8 ECSM

The error correction status module provides status information regarding platform memory errors reported by error-correcting codes.

3.3.9 Flash

Devices in the SPC563Mxx family provide up to 1.5 MB of programmable, non-volatile, flash memory. The non-volatile memory (NVM) can be used for instruction and/or data storage. The flash module includes a Fetch Accelerator, that optimizes the performance of the flash array to match the CPU architecture and provides single cycle random access to the flash @ 80 MHz. The flash module interfaces the system bus to a dedicated flash memory array controller. For CPU ‘loads’, DMA transfers and CPU instruction fetch, it supports a 64-bit data bus width at the system bus port, and a 128-bit read data interface to flash memory. The module contains a four-entry, 128-bit prefetch buffer and a prefetch controller which prefetches sequential lines of data from the flash array into the buffer. Prefetch buffer hits allow no-wait responses. Normal flash array accesses are registered and are forwarded to the system bus on the following cycle, incurring three wait-states. Prefetch operations may be automatically controlled, and are restricted to instruction fetch.

The Flash memory provides the following features:

- Supports a 64-bit data bus for instruction fetch, CPU loads and DMA access. Byte, halfword, word and doubleword reads are supported. Only aligned word and doubleword writes are supported.
- Fetch accelerator
  - Architected to optimize the performance of the flash with the CPU to provide single cycle random access to the flash up to 80 MHz system clock speed
  - Configurable read buffering and line prefetch support
  - Four line read buffers (128 bits wide) and a prefetch controller
- Hardware and software configurable read and write access protections on a per-master basis
- Interface to the Flash array controller is pipelined with a depth of one, allowing overlapped accesses to proceed in parallel for interleaved or pipelined Flash array designs
- Configurable access timing allowing use in a wide range of system frequencies
- Multiple-mapping support and mapping-based block access timing (0-31 additional cycles) allowing use for emulation of other memory types
- Software programmable block program/erase restriction control
- Erase of selected block(s)
- Read page size of 128 bits (four words)
- ECC with single-bit correction, double-bit detection
- Program page size of 64 bits (two words)
- ECC single-bit error corrections are visible to software
- Minimum program size is two consecutive 32-bit words, aligned on a 0-modulo-8 byte address, due to ECC
- Embedded hardware program and erase algorithm
- Erase suspend
- Shadow information stored in non-volatile shadow block
- Independent program/erase of the shadow block

3.3.10 SRAM

The SPC563Mxx SRAM module provides a general-purpose up to 94 KB memory block. The SRAM controller includes these features:

- Supports read/write accesses mapped to the SRAM memory from any master
- 32 KB or 24 KB block powered by separate supply for standby operation
- Byte, halfword, word and doubleword addressable
- ECC performs single-bit correction, double-bit detection on 32-bit data element

3.3.11 BAM

The BAM (Boot Assist Module) is a block of read-only memory that is programmed once by ST and is identical for all SPC563Mxx MCUs. The BAM program is executed every time the

The eTPU2 includes these distinctive features:

- The Timer Counter (TCR1), channel logic and digital filters (both channel and the external timer clock input [TCRCLK]) now have an option to run at full system clock speed or system clock / 2.
- Channels support unordered transitions: transition 2 can now be detected before transition 1. Related to this enhancement, the transition detection latches (TDL1 and TDL2) can now be independently negated by microcode.
- A new User Programmable Channel Mode has been added: the blocking, enabling, service request and capture characteristics of this channel mode can be programmed via microcode.
- Microinstructions now provide an option to issue Interrupt and Data Transfer requests selected by channel. They can also be requested simultaneously at the same instruction.
- Channel Flags 0 and 1 can now be tested for branching, in addition to selecting the entry point.
- Channel digital filters can be bypassed.
- The Timer Counter (TCR1), channel logic and digital filters (both channel and the external timer clock input [TCRCLK]) now have an option to run at full system clock speed or system clock / 2.
- Channels support unordered transitions: transition 2 can now be detected before transition 1. Related to this enhancement, the transition detection latches (TDL1 and TDL2) can now be independently negated by microcode.
- A new User Programmable Channel Mode has been added: the blocking, enabling, service request and capture characteristics of this channel mode can be programmed via microcode.
- Microinstructions now provide an option to issue Interrupt and Data Transfer requests selected by channel. They can also be requested simultaneously at the same instruction.
- Channel Flags 0 and 1 can now be tested for branching, in addition to selecting the entry point.
- Channel digital filters can be bypassed.
- 32 channels, each channel is associated with one input and one output signal
  - Enhanced input digital filters on the input pins for improved noise immunity.
  - Identical, orthogonal channels: each channel can perform any time function. Each time function can be assigned to more than one channel at a given time, so each signal can have any functionality.
  - Each channel has an event mechanism which supports single and double action functionality in various combinations. It includes two 24-bit capture registers, two 24-bit match registers, 24-bit greater-equal and equal-only comparators
  - Input and output signal states visible from the host
- 2 independent 24-bit time bases for channel synchronization:
  - First time base clocked by system clock with programmable prescale division from 2 to 512 (in steps of 2), or by output of second time base prescaler
  - Second time base counter can work as a continuous angle counter, enabling angle based applications to match angle instead of time
  - Both time bases can be exported to the eMIOS timer module
  - Both time bases visible from the host

- Event-triggered microengine:
  - Fixed-length instruction execution in two-system-clock microcycle
  - 14 KB of code memory (SCM)
  - 3 KB of parameter (data) RAM (SPRAM)
  - Parallel execution of data memory, ALU, channel control and flow control sub-instructions in selected combinations
  - 32-bit microengine registers and 24-bit wide ALU, with 1 microcycle addition and subtraction, absolute value, bitwise logical operations on 24-bit, 16-bit, or byte operands, single-bit manipulation, shift operations, sign extension and conditional execution
  - Additional 24-bit Multiply/MAC/Divide unit which supports all signed/unsigned Multiply/MAC combinations, and unsigned 24-bit divide. The MAC/Divide unit works in parallel with the regular microcode commands
- Resource sharing features support channel use of common channel registers, memory and microengine time:
  - Hardware scheduler works as a “task management” unit, dispatching event service routines by predefined, host-configured priority
  - Automatic channel context switch when a “task switch” occurs, i.e., one function thread ends and another begins to service a request from other channel: channel-specific registers, flags and parameter base address are automatically loaded for the next serviced channel
  - SPRAM shared between host CPU and eTPU2, supporting communication either between channels and host or inter-channel
  - Dual-parameter coherency hardware support allows atomic access to two parameters by host
- Test and development support features:
  - Nexus Class 1 debug, supporting single-step execution, arbitrary microinstruction execution, hardware breakpoints and watchpoints on several conditions
  - Software breakpoints
  - SCM continuous signature-check built-in self test (MISC — multiple input signature calculator), runs concurrently with eTPU2 normal operation
- System enhancements
  - Software watchdog with programmable timeout
  - Real-time performance information
- Channel enhancements
  - Channels 1 and 2 can optionally drive angle clock hardware
- Programming enhancements
  - Engine relative addressing mode

3.3.14 eQADC

The enhanced queued analog to digital converter (eQADC) block provides accurate and fast conversions for a wide range of applications. The eQADC provides a parallel interface to two on-chip analog to digital converters (ADC), and a single master to single slave serial interface to an off-chip external device. Both on-chip ADCs have access to all the analog channels.

The eQADC prioritizes and transfers commands from six command conversion command ‘queues’ to the on-chip ADCs or to the external device. The block can also receive data from the on-chip ADCs or from an off-chip external device into the six result queues, in parallel, independently of the command queues. The six command queues are prioritized with Queue_0 having the highest priority and Queue_5 the lowest. Queue_0 also has the added ability to bypass all buffering and queuing and abort a currently running conversion on either ADC and start a Queue_0 conversion. This means that Queue_0 will always have a deterministic time from trigger to start of conversion, irrespective of what tasks the ADCs were performing when the trigger occurred. The eQADC supports software and external hardware triggers from other blocks to initiate transfers of commands from the queues to the on-chip ADCs or to the external device. It also monitors the fullness of command queues and result queues, and accordingly generates DMA or interrupt requests to control data movement between the queues and the system memory, which is external to the eQADC.

The ADCs also support features designed to allow the direct connection of high impedance acoustic sensors that might be used in a system for detecting engine knock. These features include differential inputs; integrated variable gain amplifiers for increasing the dynamic range; programmable pull-up and pull-down resistors for biasing and sensor diagnostics.

The eQADC also integrates a programmable decimation filter capable of taking in ADC conversion results at a high rate, passing them through a hardware low pass filter, then down-sampling the output of the filter and feeding the lower sample rate results to the result FIFOs. This allows the ADCs to sample the sensor at a rate high enough to avoid aliasing of out-of-band noise; while providing a reduced sample rate output to minimize the amount DSP processing bandwidth required to fully process the digitized waveform.

The DSPIs also support these features unique to the DSI and CSI configurations:

- 2 sources of the serialized data:
  - eTPU_A and eMIOS output channels
  - Memory-mapped register in the DSPI
- Destinations for the deserialized data:
  - eTPU_A and eMIOS input channels
  - SIU External Interrupt Request inputs
  - Memory-mapped register in the DSPI
- Deserialized data is provided as Parallel Output signals and as bits in a memory-mapped register
- Transfer initiation conditions:
  - Continuous
  - Edge sensitive hardware trigger
  - Change in data
- Pin serialization/deserialization with interleaved SPI frames for control and diagnostics
- Continuous serial communications clock
- Support for parallel and serial chaining of up to four DSPI blocks

3.3.16 eSCI

The enhanced Serial Communications Interface (eSCI) allows asynchronous serial communications with peripheral devices and other MCUs. It includes special support to

The FlexCAN module provides the following features:

- Full Implementation of the CAN protocol specification, Version 2.0B
  - Standard data and remote frames
  - Extended data and remote frames
  - Zero to eight bytes data length
  - Programmable bit rate up to 1 Mbit/s
- Content-related addressing
- 64 / 32 message buffers of zero to eight bytes data length
- Individual Rx Mask Register per message buffer
- Each message buffer configurable as Rx or Tx, all supporting standard and extended messages
- Includes 1056 / 544 bytes of embedded memory for message buffer storage
- Includes a 256-byte and a 128-byte memories for storing individual Rx mask registers
- Full featured Rx FIFO with storage capacity for six frames and internal pointer handling
- Powerful Rx FIFO ID filtering, capable of matching incoming IDs against 8 extended, 16 standard or 32 partial (8 bits) IDs, with individual masking capability
- Selectable backwards compatibility with previous FlexCAN versions
- Programmable clock source to the CAN Protocol Interface, either system clock or oscillator clock
- Listen only mode capability
- Programmable loop-back mode supporting self-test operation
- 3 programmable Mask Registers
- Programmable transmit-first scheme: lowest ID, lowest buffer number or highest priority
- Time Stamp based on 16-bit free-running timer
- Global network time, synchronized by a specific message
- Maskable interrupts
- Warning interrupts when the Rx and Tx Error Counters reach 96
- Independent of the transmission medium (an external transceiver is assumed)
- Multi master concept
- High immunity to EMI
- Short latency time due to an arbitration scheme for high-priority messages
- Low power mode, with programmable wake-up on bus activity

3.3.18 System timers

The system timers provide two distinct types of system timer:

- Periodic interrupts/triggers using the Peripheral Interrupt Timer (PIT)
- Operating system task monitors using the System Timer Module (STM)

Peripheral Interrupt Timer (PIT)

The PIT provides five independent timer channels, capable of producing periodic interrupts and periodic triggers. The PIT has no external input or output pins and is intended to be used to provide system ‘tick’ signals to the operating system, as well as periodic triggers for eQADC queues. Of the five channels in the PIT, four are clocked by the system clock, one is

clocked by the crystal clock. This one channel is also referred to as Real Time Interrupt (RTI) and is used to wakeup the device from low power stop mode.

The following features are implemented in the PIT:

- 5 independent timer channels
- Each channel includes 32-bit wide down counter with automatic reload
- 4 channels clocked from system clock
- 1 channel clocked from crystal clock (wake-up timer)
- Wake-up timer remains active when System STOP mode is entered. Used to restart system clock after predefined time-out period
- Each channel can optionally generate an interrupt request or a trigger event (to trigger eQADC queues) when the timer reaches zero

System Timer Module (STM)

The System Timer Module (STM) is designed to implement the software task monitor as defined by AUTOSAR (see http://www.autosar.org). It consists of a single 32-bit counter, clocked by the system clock, and four independent timer comparators. These comparators produce a CPU interrupt when the timer exceeds the programmed value.

The following features are implemented in the STM:

- One 32-bit up counter with 8-bit prescaler
- Four 32-bit compare channels
- Independent interrupt source for each channel
- Counter can be stopped in debug mode

3.3.19 Software Watchdog Timer (SWT)

The Software Watchdog Timer (SWT) is a second watchdog module to complement the standard Power Architecture watchdog integrated in the CPU core. The SWT is a 32-bit modulus counter, clocked by the system clock or the crystal clock, that can provide a system reset or interrupt request when the correct software key is not written within the required time window.

The following features are implemented:

- 32-bit modulus counter
- Clocked by system clock or crystal clock
- Optional programmable watchdog window mode
- Can optionally cause system reset or interrupt request on timeout
- Reset by writing a software key to memory mapped register
- Enabled out of reset
- Configuration is protected by a software key or a write-once register

3.3.20 Debug features

Nexus port controller

The NPC (Nexus Port Controller) block provides real-time development support capabilities for the SPC563Mxx Power Architecture-based MCU in compliance with the IEEE-ISTO 5001-2003 standard. This development support is supplied for MCUs without requiring

Note: This feature is imprecise due to CPU pipelining.

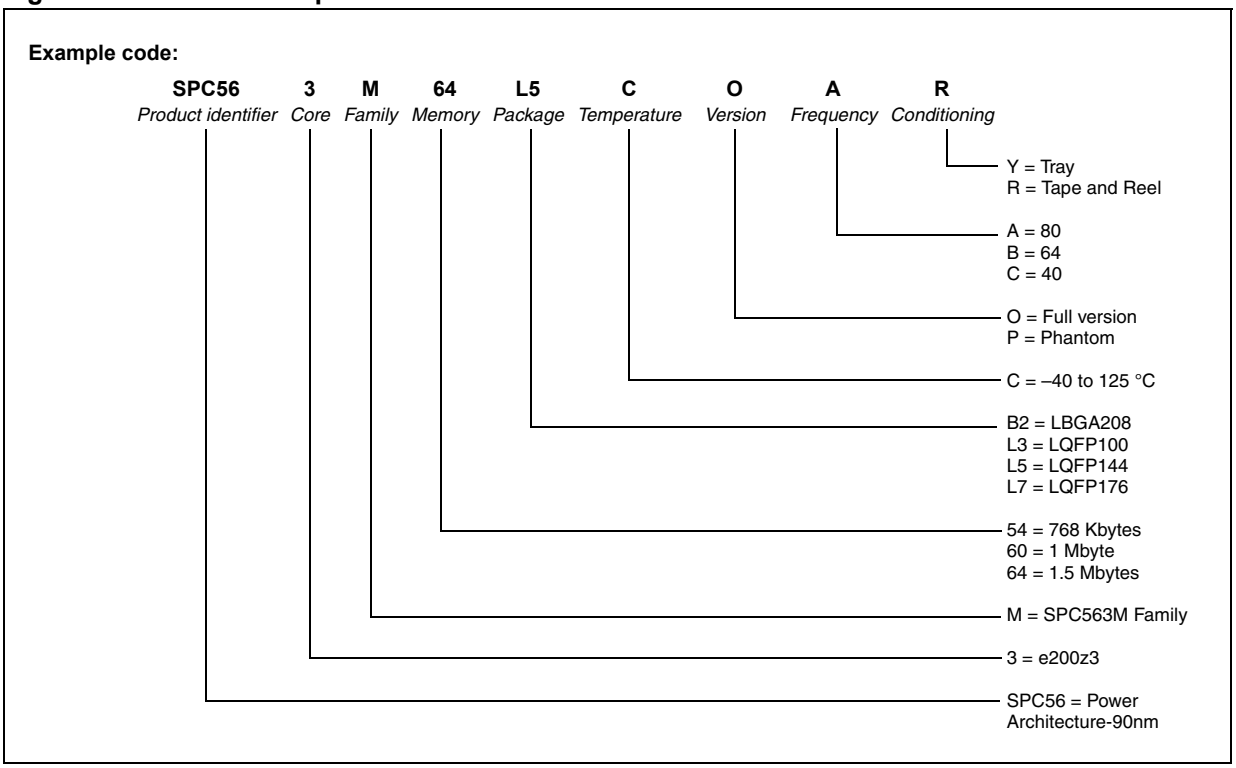
  - Subset of Power Architecture software debug facilities with OnCE block (Nexus class 1 features)
- eTPU development support features
  - IEEE-ISTO 5001-2003 standard class 1 compliant for the eTPU
  - Nexus based breakpoint configuration and single step support (JTAG feature of the eTPU)
- Run-time access to the on-chip memory map via the Nexus read/write access protocol. This feature supports accesses for run-time internal visibility, calibration variable acquisition, calibration constant tuning, and external rapid prototyping for powertrain automotive development systems.
- All features are independently configurable and controllable via the IEEE 1149.1 I/O port
- Power-on-reset status indication during reset via MDO[0] in disabled and reset modes

JTAG

The JTAGC (JTAG Controller) block provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode. Testing is performed via a boundary scan technique, as defined in the IEEE 1149.1-2001 standard. All data input to and output from the JTAGC block is communicated in serial format. The JTAGC block is compliant with the IEEE 1149.1-2001 standard and supports the following features:

- IEEE 1149.1-2001 Test Access Port (TAP) interface 4 pins (TDI, TMS, TCK, and TDO)
- A 5-bit instruction register that supports the following IEEE 1149.1-2001 defined instructions:
  - BYPASS, IDCODE, EXTEST, SAMPLE, SAMPLE/PRELOAD, HIGHZ, CLAMP
- A 5-bit instruction register that supports the additional following public instructions:
  - ACCESS_AUX_TAP_NPC
  - ACCESS_AUX_TAP_ONCE
  - ACCESS_AUX_TAP_eTPU
  - ACCESS_CENSOR
- 3 test data registers to support JTAG Boundary Scan mode
  - Bypass register
  - Boundary scan register
  - Device identification register
- A TAP controller state machine that controls the operation of the data registers, instruction register and associated circuitry
- Censorship Inhibit Register
  - 64-bit Censorship password register
  - If the external tool writes a 64-bit password that matches the Serial Boot password stored in the internal flash shadow row, Censorship is disabled until the next system reset.

Figure 2. Commercial product code structure



5 Revision history

Table 4. Revision history

Date	Revision	Description
30-Aug-2007	1	Initial release.
7-Nov-2007	2	Removed: – - Section 5: LQFP144 pinout diagram including Figure 2: LQFP144 pinout – - Section 6: LQFP144 pin description including Table 3: LQFP144 pin description – - Section 7: LFBGA208 ballout diagram including Figure 3: LFBGA208 ballout Added – - Section 5: Signal description on page 43 including Section 5.1: Signal properties summary, Table 3: SPC563M60 signal properties, Section 5.2: Detailed signal descriptions, Section 5.3: I/O power/ground segmentation and Table 4: SPC563M60 power/ground segmentation – - Section 6: Device pin outs on page 69 including Section 6.1: LQFP144 pinout, Figure 2: LQFP144 pinout, Section 6.2: LFBGA208 ballout diagram and Figure 3: LFBGA208 ballout diagram Removed parameters D3 and E3 from Figure 4: LQFP144 (20 x 20 x 1.40 mm) package mechanical outline: Removed minimum and maximum values for parameters D, D1, E and E1 and removed parameters D3 and E3 from Table 6: LQFP144 package mechanical data on page 74: Added note about LQFP144 package and JEDEC compliancy to Section 8: Package information on page 73
13-Mar-2009	3	Updated document to include information on all members of the SPC563Mxx family. Replaced references to the core (was “e200z3”, is “e200z335”) and Nexus module (was “Nexus development interface (NDI)”, is “Nexus port controller (NPC)”). Changed the arrangement of V_{STBY}, the standby RAM, and the voltage regulator in the block diagram. Revised the device-comparison table and feature list. In the “Feature List” section, added “(for 100- and 144-pin packages)” to the “Single power supply” operating parameter. In the “Feature Details” section, replaced the CI/NMI text in the INTC description with information on the NMI only. Reformatted company-specific references. Added a revision history. Formatting, spelling, grammar, and layout corrections.

Table 4. Revision history

Date	Revision	Description
08-Jun-2011	5	Replaced in all document "... Architecture Book E compliant..." with "... Architecture technology compliant..." Updated "Introduction": Added "Document overview" and "Description" sections. Made the following changes in the "Description" section: – Added "Floating Point Unit (FPU)" bullet under "Single issue, 32-bit Power Architecture technology compliant e200z335 CPU core complex". – Changed "eTPU" to "eTPU2" in the "32-channel second-generation enhanced time processor unit" sentence. – Changed the "Available in LQFP100, LQFP144, LQFP176 and LBGA208" sentence to "Designed for LQFP100, LQFP144, LQFP176, and LBGA208 packages". Replaced all instances of "Microsecond Bus" with "Microsecond Channel". Replaced all instances of "SPC563M54" and "SPC563M60" with "SPC563M54P"and "SPC563M60P", respectively. Changed the "Standby SRAM size" of the SPC563M60P device from "24" to "32". Replaced all instances of "downlink" with "downstream" and "uplink" with "upstream". Made the following changes in the "Flash" section: Changed "Program page size of 128 bits (four words) to accelerate programming" to "Program page size of 64 bits (two words)". Changed "Erase suspend, program suspend and erase-suspended program" to "Erase suspend". Made editorial changes in the "BAM" section: Updated the conditional tags in the "Supports serial bootloading..." sentences. Changed "Shared time bases with the eTPU through the counter buses" to "Shared time bases with the eTPU2 through the counter buses" in the "eMIOS" section. Removed the following sentences from the "eTPU2" section: "For Monaco 1.5M, the eTPU2 has been further enhanced with these features:" "Timebases and channels are run at full system clock speed" "Programmable channel mode allows customization of channel function" "More flexibility in requesting DMA and interrupt service" "Channel flags can be tested" Added the following sentence in the "eQADC" section under the "Priority based Queues" bullet: "Streaming mode operation of Queue_0 to execute some commands several times". Changed the following sentences in the "DSPI" section: "The DSPI can be configured ... that implements ... the Microsecond Bus protocol" to "The DSPI can be configured ... that supports ... the Microsecond Channel protocol". "The DSPI pins support 5 V logic levels or Low Voltage Differential Signalling (LVDS) to improve high speed operation." to "The DSPI ouput pins support 5 V logic levels or Low Voltage Differential Signalling (LVDS) according to the Microsecond Channel specification."

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