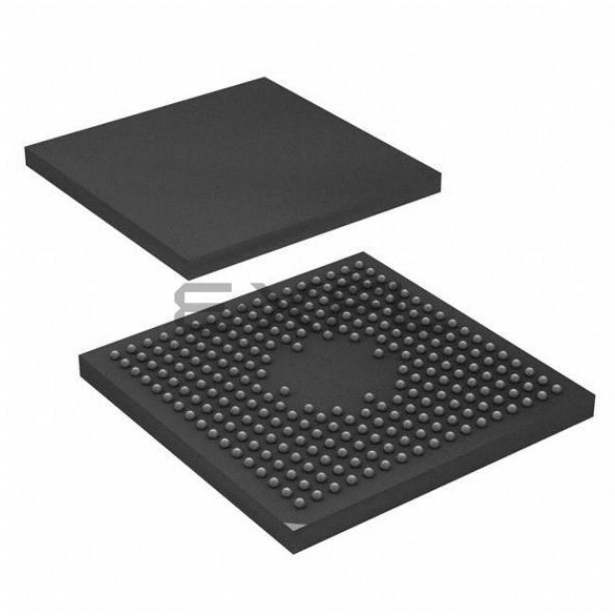
Microchip Technology - AT91RM9200-CJ-002 Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM920T
Core Size	16/32-Bit
Speed	180MHz
Connectivity	EBI/EMI, Ethernet, I²C, Memory Card, SPI, SSC, UART/USART, USB
Peripherals	POR
Number of I/O	122
Program Memory Size	128KB (128K x 8)
Program Memory Type	ROM
EEPROM Size	-
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 1.95V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	256-LFBGA
Supplier Device Package	256-BGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at91rm9200-cj-002

2. Block Diagram

Bold arrows (⟶) indicate master-to-slave dependency.

Figure 2-1. AT91RM9200 Block Diagram

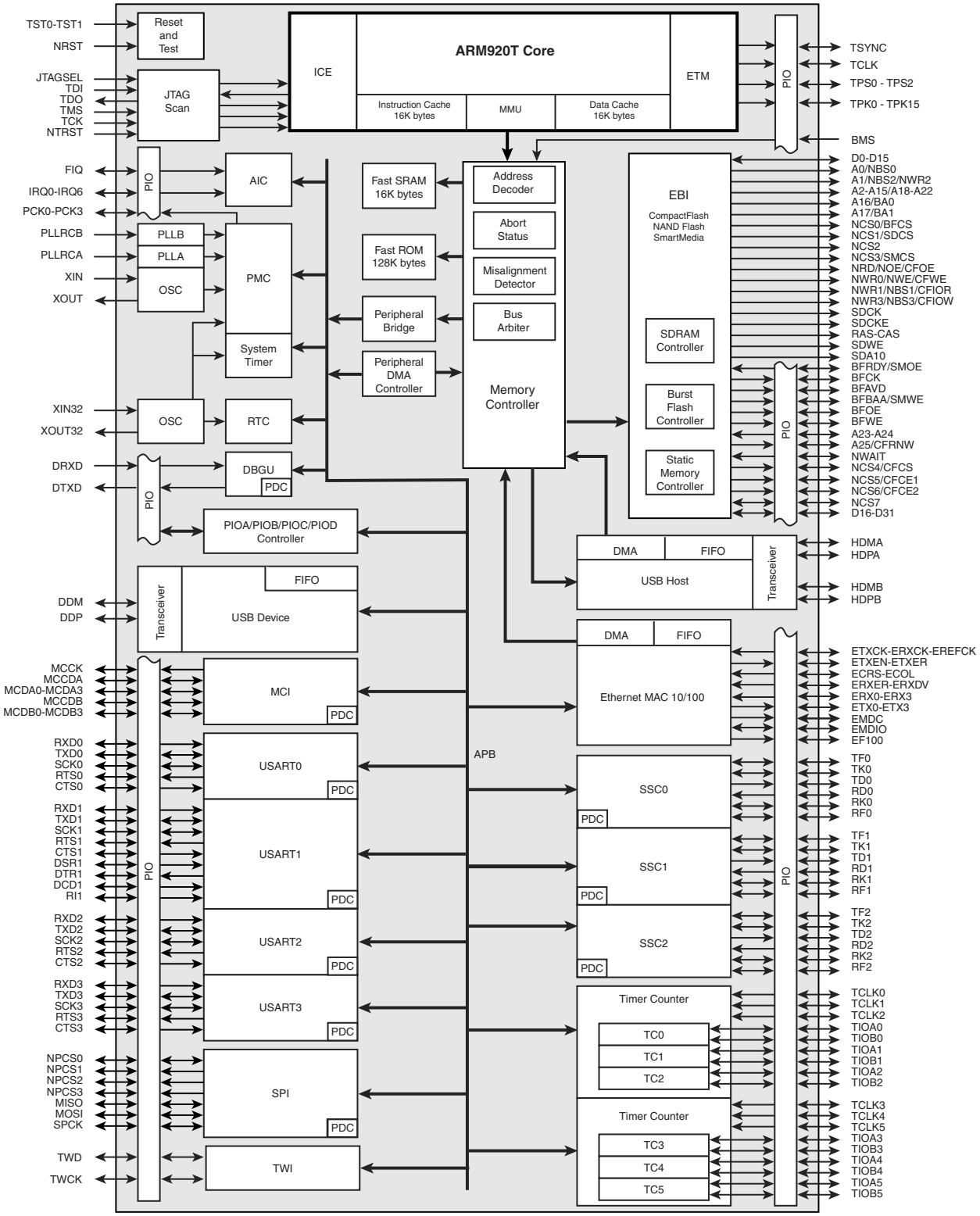


Table 3-1. Signal Description by Peripheral

Pin Name	Function	Type	Active Level	Comments
Memory Controller				
BMS	Boot Mode Select	Input		
Debug Unit				
DRXD	Debug Receive Data	Input		Debug Receive Data
DTXD	Debug Transmit Data	Output		Debug Transmit Data
AIC				
IRQ0 - IRQ6	External Interrupt Inputs	Input		
FIQ	Fast Interrupt Input	Input		
PIO				
PA0 - PA31	Parallel IO Controller A	I/O		Pulled-up input at reset
PB0 - PB29	Parallel IO Controller B	I/O		Pulled-up input at reset
PC0 - PC31	Parallel IO Controller C	I/O		Pulled-up input at reset
PD0 - PD27	Parallel IO Controller D	I/O		Pulled-up input at reset
EBI				
D0 - D31	Data Bus	I/O		Pulled-up input at reset
A0 - A25	Address Bus	Output		0 at reset
SMC				
NCS0 - NCS7	Chip Select Lines	Output	Low	1 at reset
NWR0 - NWR3	Write Signal	Output	Low	1 at reset
NOE	Output Enable	Output	Low	1 at reset
NRD	Read Signal	Output	Low	1 at reset
NUB	Upper Byte Select	Output	Low	1 at reset
NLB	Lower Byte Select	Output	Low	1 at reset
NWE	Write Enable	Output	Low	1 at reset
NWAIT	Wait Signal	Input	Low	
NBS0 - NBS3	Byte Mask Signal	Output	Low	1 at reset
EBI for CompactFlash Support				
CFCE1 - CFCE2	CompactFlash Chip Enable	Output	Low	
CFOE	CompactFlash Output Enable	Output	Low	
CFWE	CompactFlash Write Enable	Output	Low	
CFIOR	CompactFlash IO Read	Output	Low	
CFIOW	CompactFlash IO Write	Output	Low	
CFRNW	CompactFlash Read Not Write	Output		
CFCS	CompactFlash Chip Select	Output	Low	

Table 3-1. Signal Description by Peripheral

Pin Name	Function	Type	Active Level	Comments
EBI for NAND Flash/SmartMedia Support				
SMCS	NAND Flash/SmartMedia Chip Select	Output	Low	
SMOE	NAND Flash/SmartMedia Output Enable	Output	Low	
SMWE	NAND Flash/SmartMedia Write Enable	Output	Low	
SDRAM Controller				
SDCK	SDRAM Clock	Output		
SDCKE	SDRAM Clock Enable	Output	High	
SDCS	SDRAM Controller Chip Select	Output	Low	
BA0 - BA1	Bank Select	Output		
SDWE	SDRAM Write Enable	Output	Low	
RAS - CAS	Row and Column Signal	Output	Low	
SDA10	SDRAM Address 10 Line	Output		
Burst Flash Controller				
BFCK	Burst Flash Clock	Output		
BFCS	Burst Flash Chip Select	Output	Low	
BFAVD	Burst Flash Address Valid	Output	Low	
BFBAA	Burst Flash Address Advance	Output	Low	
BFOE	Burst Flash Output Enable	Output	Low	
BFRDY	Burst Flash Ready	Input	High	
BFWE	Burst Flash Write Enable	Output	Low	
Multimedia Card Interface				
MCCK	Multimedia Card Clock	Output		
MCCDA	Multimedia Card A Command	I/O		
MCDA0 - MCDA3	Multimedia Card A Data	I/O		
MCCDB	Multimedia Card B Command	I/O		
MCDB0 - MCDB3	Multimedia Card B Data	I/O		
USART				
SCK0 - SCK3	Serial Clock	I/O		
TXD0 - TXD3	Transmit Data	Output		
RXD0 - RXD3	Receive Data	Input		
RTS0 - RTS3	Ready To Send	Output		
CTS0 - CTS3	Clear To Send	Input		
DSR1	Data Set Ready	Input		
DTR1	Data Terminal Ready	Output		
DCD1	Data Carrier Detect	Input		
RI1	Ring Indicator	Input		

Table 3-1. Signal Description by Peripheral

Pin Name	Function	Type	Active Level	Comments
SPI				
MISO	Master In Slave Out	I/O		
MOSI	Master Out Slave In	I/O		
SPCK	SPI Serial Clock	I/O		
NPCS0	SPI Peripheral Chip Select 0	I/O	Low	
NPCS1 - NPCS3	SPI Peripheral Chip Select	Output	Low	
Two-Wire Interface				
TWD	Two-wire Serial Data	I/O		
TWCK	Two-wire Serial Clock	I/O		

4. Package and Pinout

The AT91RM9200 is available in two packages:

- 208-pin PQFP, 31.2 x 31.2 mm, 0.5 mm pitch
- 256-ball BGA, 15 x 15 mm, 0.8 mm ball pitch

The product features of the 256-ball BGA package are extended compared to the 208-lead PQFP package. The features that are available only with the 256-ball BGA package are:

- Parallel I/O Controller D
- ETM port with outputs multiplexed on the PIO Controller D
- a second USB Host transceiver, opening the Hub capabilities of the embedded USB Host.

4.1 208-pin PQFP Package Outline

Figure 1-1 shows the orientation of the 208-pin PQFP package.

A detailed mechanical description is given in the section “AT91RM9200 Mechanical Characteristics” of the product datasheet.

Figure 4-1. 208-pin PQFP Package (Top View)

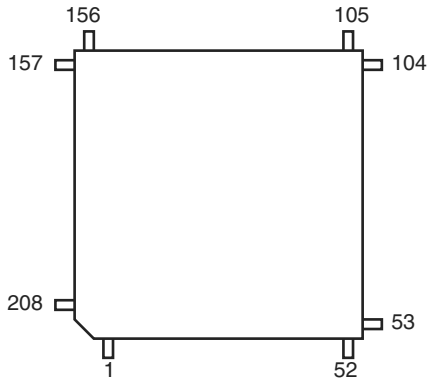


Table 4-1. AT91RM9200 Pinout for 208-pin PQFP Package (Continued)

Pin Number	Signal Name	Pin Number	Signal Name	Pin Number	Signal Name	Pin Number	Signal Name
145	A11	161	PC7	177	CAS	193	D10
146	VDDIOM	162	PC8	178	SDWE	194	D11
147	GND	163	PC9	179	D0	195	D12
148	A12	164	VDDIOM	180	D1	196	D13
149	A13	165	GND	181	D2	197	D14
150	A14	166	NCS0/BFCS	182	D3	198	D15
151	A15	167	NCS1/SDCS	183	VDDIOM	199	VDDIOM
152	VDDCORE	168	NCS2	184	GND	200	GND
153	GND	169	NCS3/SMCS	185	D4	201	PC16
154	A16/BA0	170	NRD/NOE/CFOE	186	D5	202	PC17
155	A17/BA1	171	NWR0/NWE/CFWE	187	D6	203	PC18
156	A18	172	NWR1/NBS1/CFIOR	188	VDDCORE	204	PC19
157	A19	173	NWR3/NBS3/CFIOW	189	GND	205	PC20
158	A20	174	SDCK	190	D7	206	PC21
159	A21	175	SDCKE	191	D8	207	PC22
160	A22	176	RAS	192	D9	208	PC23

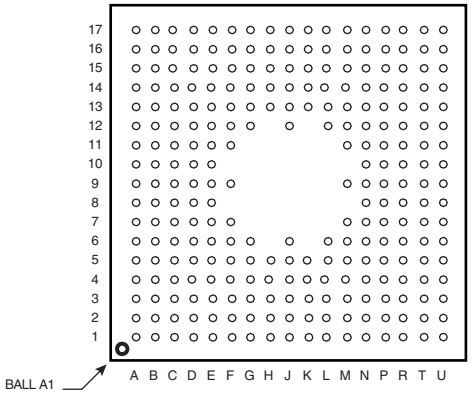
Note: 1. Shaded cells define the pins powered by VDDIOM.

4.3 256-ball BGA Package Outline

Figure 4-2 shows the orientation of the 256-ball LFBGA package.

A detailed mechanical description is given in the section “AT91RM9200 Mechanical Characteristics” of the product datasheet.

Figure 4-2. 256-ball LFBGA Package (Top View)



4.4 256-ball BGA Package Pinout

Table 4-2. AT91RM9200 Pinout for 256-ball BGA Package

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A1	TDI	C3	PD14	E5	TCK	G14	PA1
A2	JTAGSEL	C4	PB22	E6	GND	G15	PA2
A3	PB20	C5	PB19	E7	PB15	G16	PA3
A4	PB17	C6	PD10	E8	GND	G17	XIN32
A5	PD11	C7	PB13	E9	PB7	H1	PD23
A6	PD8	C8	PB12	E10	PB3	H2	PD20
A7	VDDIOP	C9	PB6	E11	PA29	H3	PD22
A8	PB9	C10	PB1	E12	PA26	H4	PD21
A9	PB4	C11	GND	E13	PA25	H5	VDDIOP
A10	PA31/BMS	C12	PA20	E14	PA9	H13	VDDPLL
A11	VDDIOP	C13	PA18	E15	PA6	H14	VDDIOP
A12	PA23	C14	VDDCORE	E16	PD3	H15	GNDPLL
A13	PA19	C15	GND	E17	PD0	H16	GND
A14	GND	C16	PA8	F1	PD16	H17	XOUT32
A15	PA14	C17	PD5	F2	GND	J1	PD25
A16	VDDIOP	D1	TST1	F3	PB23	J2	PD27
A17	PA13	D2	VDDIOP	F4	PB25	J3	PD24
B1	TDO	D3	VDDIOP	F5	PB24	J4	PD26
B2	PD13	D4	GND	F6	VDDCORE	J5	PB28
B3	PB18	D5	VDDIOP	F7	PB16	J6	PB29
B4	PB21	D6	PD7	F9	PB11	J12	GND
B5	PD12	D7	PB14	F11	PA30	J13	GNDOSC
B6	PD9	D8	VDDIOP	F12	PA28	J14	VDDOSC
B7	GND	D9	PB8	F13	PA4	J15	VDDPLL
B8	PB10	D10	PB2	F14	PD2	J16	GNDPLL
B9	PB5	D11	GND	F15	PD1	J17	XIN
B10	PB0	D12	PA22	F16	PA5	K1	HDPA
B11	VDDIOP	D13	PA21	F17	PLLRCB	K2	DDM
B12	PA24	D14	PA16	G1	PD19	K3	HDMA
B13	PA17	D15	PA10	G2	PD17	K4	VDDIOP
B14	PA15	D16	PD6	G3	GND	K5	DDP
B15	PA11	D17	PD4	G4	PB26	K13	PC5
B16	PA12	E1	NRST	G5	PD18	K14	PC4
B17	PA7	E2	NTRST	G6	PB27	K15	PC6
C1	TMS	E3	GND	G12	PA27	K16	VDDIOM
C2	PD15	E4	TST0	G13	PA0	K17	XOUT

- Debug Unit
  - Two-pin UART
  - Debug Communication Channel
  - Chip ID Register
- Embedded Trace Macrocell: ETM9™ Rev2a
  - Medium Level Implementation
  - Half-rate Clock Mode
  - Four Pairs of Address Comparators
  - Two Data Comparators
  - Eight Memory Map Decoder Inputs
  - Two Counters
  - One Sequencer
  - One 18-byte FIFO
- IEEE1149.1 JTAG Boundary Scan on all Digital Pins

7.3 Boot Program

- Default Boot Program stored in ROM-based products
- Downloads and runs an application from external storage media into internal SRAM
- Downloaded code size depends on embedded SRAM size
- Automatic detection of valid application
- Bootloader supporting a wide range of non-volatile memories
  - SPI DataFlash® connected on SPI NPCS0
  - Two-wire EEPROM
  - 8-bit parallel memories on NCS0
- Boot Uploader in case no valid program is detected in external NVM and supporting several communication media
- Serial communication on a DBGU (XModem protocol)
- USB Device Port (DFU Protocol)

7.4 Embedded Software Services

- Compliant with ATPCS
- Compliant with AINSI/ISO Standard C
- Compiled in ARM/Thumb Interworking
- ROM Entry Service
- Tempo, Xmodem and DataFlash services
- CRC and Sine tables

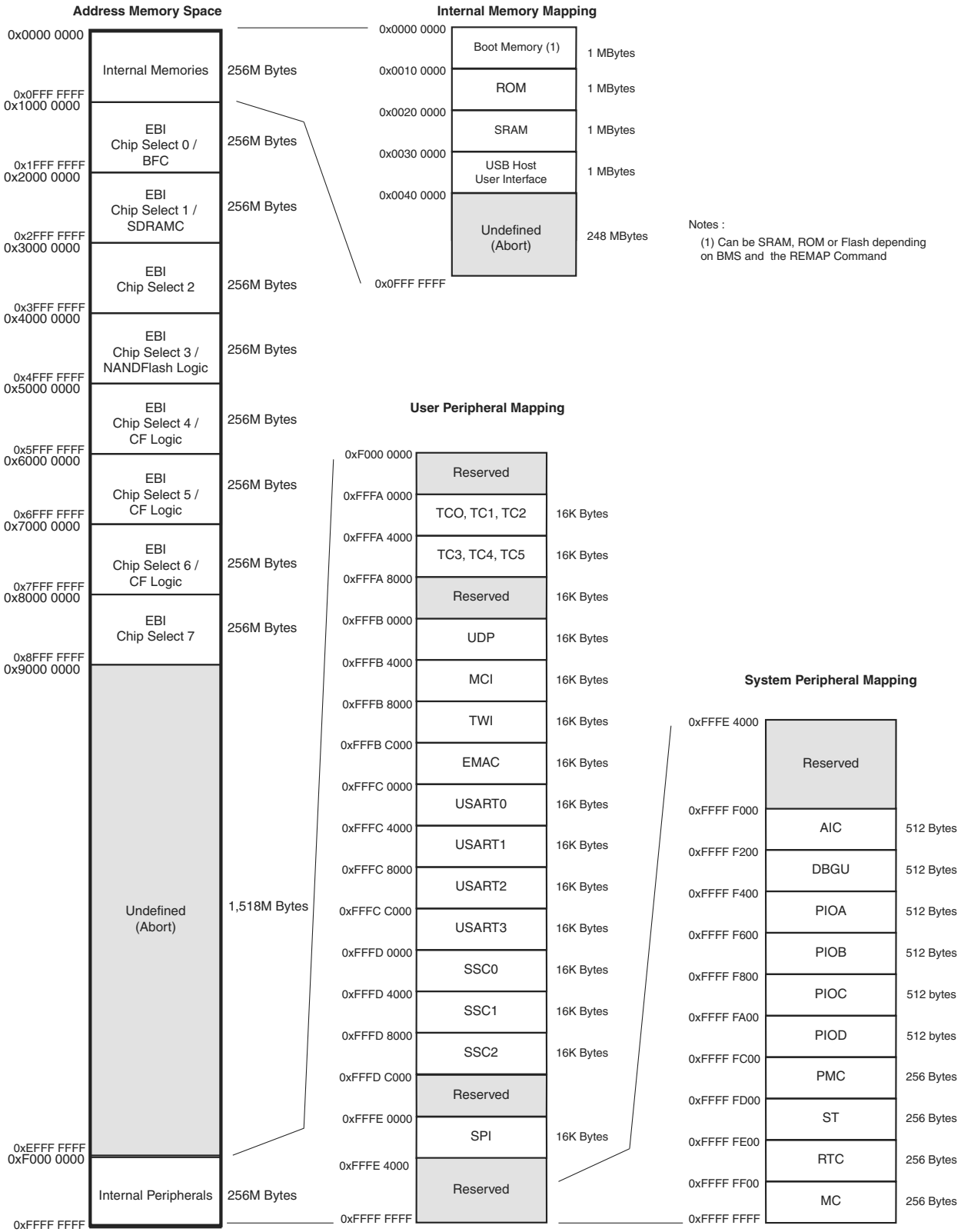
7.5 Memory Controller

- Programmable Bus Arbiter handling four Masters
  - Internal Bus is shared by ARM920T, PDC, USB Host Port and Ethernet MAC Masters
  - Each Master can be assigned a priority between 0 and 7

- Address Decoder provides selection for
  - Eight external 256-Mbyte memory areas
  - Four internal 1-Mbyte memory areas
  - One 256-Mbyte embedded peripheral area
- Boot Mode Select Option
  - Non-volatile Boot Memory can be internal or external
  - Selection is made by BMS pin sampled at reset
- Abort Status Registers
  - Source, Type and all parameters of the access leading to an abort are saved
- Misalignment Detector
  - Alignment checking of all data accesses
  - Abort generation in case of misalignment
- Remap command
  - Provides remapping of an internal SRAM in place of the boot NVM

8. Memories

Figure 8-1. AT91RM9200 Memory Mapping



9. System Peripherals

A complete memory map is shown in Figure 8-1 on page 17.

9.1 Reset Controller

- Two reset input lines (NRST and NTRST) providing, respectively:
- Initialization of the User Interface registers (defined in the user interface of each peripheral) and:
  - Sample the signals needed at bootup
  - Compel the processor to fetch the next instruction at address zero
- Initialization of the embedded ICE TAP controller

9.2 Advanced Interrupt Controller

- Controls the interrupt lines (nIRQ and nFIQ) of an ARM Processor
- Thirty-two individually maskable and vectored interrupt sources
  - Source 0 is reserved for the Fast Interrupt Input (FIQ)
  - Source 1 is reserved for system peripherals (ST, RTC, PMC, DBGU…)
  - Source 2 to Source 31 control thirty embedded peripheral interrupts or external interrupts
  - Programmable Edge-triggered or Level-sensitive Internal Sources
  - Programmable Positive/Negative Edge-triggered or High/Low Level-sensitive External Sources
- 8-level Priority Controller
  - Drives the Normal Interrupt of the processor
  - Handles priority of the interrupt sources 1 to 31
  - Higher priority interrupts can be served during service of lower priority interrupt
- Vectoring
  - Optimizes Interrupt Service Routine Branch and Execution
  - One 32-bit Vector Register per interrupt source
  - Interrupt Vector Register reads the corresponding current Interrupt Vector
- Protect Mode
  - Easy debugging by preventing automatic operations
- General Interrupt Mask
  - Provides processor synchronization on events without triggering an interrupt

9.3 Power Management Controller

- Optimizes the power consumption of the whole system
- Embeds and controls:
  - One Main Oscillator and One Slow Clock Oscillator (32.768Hz)
  - Two Phase Locked Loops (PLLs) and Dividers
  - Clock Prescalers
- Provides:
  - the Processor Clock PCK

  - the Master Clock MCK
  - the USB Clocks, UHPCK and UDPCK, respectively for the USB Host Port and the USB Device Port
  - Programmable automatic PLL switch-off in USB Device suspend conditions
  - up to thirty peripheral clocks
  - four programmable clock outputs PCK0 to PCK3
- Four operating modes:
  - Normal Mode, Idle Mode, Slow Clock Mode, Standby Mode

9.4 Debug Unit

- System peripheral to facilitate debug of Atmel's ARM-based systems
- Composed of the following functions
  - Two-pin UART
  - Debug Communication Channel (DCC) support
  - Chip ID Registers
- Two-pin UART
  - Implemented features are 100% compatible with the standard Atmel USART
  - Independent receiver and transmitter with a common programmable Baud Rate Generator
  - Even, Odd, Mark or Space Parity Generation
  - Parity, Framing and Overrun Error Detection
  - Automatic Echo, Local Loopback and Remote Loopback Channel Modes
  - Interrupt generation
  - Support for two PDC channels with connection to receiver and transmitter
- Debug Communication Channel Support
  - Offers visibility of COMMRX and COMMTX signals from the ARM Processor
  - Interrupt generation
- Chip ID Registers
  - Identification of the device revision, sizes of the embedded memories, set of peripherals

9.5 PIO Controller

- Up to 32 programmable I/O Lines
- Fully programmable through Set/Clear Registers
- Multiplexing of two peripheral functions per I/O Line
- For each I/O Line (whether assigned to a peripheral or used as general purpose I/O)
  - Input change interrupt
  - Glitch filter
  - Multi-drive option enables driving in open drain
  - Programmable pull up on each I/O line
  - Pin data status register, supplies visibility of the level on the pin at any time

- Synchronous output, provides Set and Clear of several I/O lines in a single write

10. User Peripherals

10.1 User Interface

The User Peripherals are mapped in the upper 256M bytes of the address space, between the addresses 0xFFFA 0000 and 0xFFFE 3FFF. Each peripheral has a 16-Kbyte address space.

A complete memory map is presented in Figure 8-1 on page 17.

10.2 Peripheral Identifiers

The AT91RM9200 embeds a wide range of peripherals. Table 10-1 defines the peripheral identifiers of the AT91RM9200. A peripheral identifier is required for the control of the peripheral interrupt with the Advanced Interrupt Controller and for the control of the peripheral clock with the Power Management Controller.

Table 10-1. Peripheral Identifiers

Peripheral ID	Peripheral Mnemonic	Peripheral Name	External Interrupt
0	AIC	Advanced Interrupt Controller	FIQ
1	SYSIRQ		
2	PIOA	Parallel I/O Controller A	
3	PIOB	Parallel I/O Controller B	
4	PIOC	Parallel I/O Controller C	
5	PIOD	Parallel I/O Controller D	
6	US0	USART 0	
7	US1	USART 1	
8	US2	USART 2	
9	US3	USART 3	
10	MCI	Multimedia Card Interface	
11	UDP	USB Device Port	
12	TWI	Two-wire Interface	
13	SPI	Serial Peripheral Interface	
14	SSC0	Synchronous Serial Controller 0	
15	SSC1	Synchronous Serial Controller 1	
16	SSC2	Synchronous Serial Controller 2	
17	TC0	Timer/Counter 0	
18	TC1	Timer/Counter 1	
19	TC2	Timer/Counter 2	
20	TC3	Timer/Counter 3	
21	TC4	Timer/Counter 4	
22	TC5	Timer/Counter 5	
23	UHP	USB Host Port	

10.3.1 PIO Controller A Multiplexing

Table 10-2. Multiplexing on PIO Controller A

PIO Controller A				Application Usage	
I/O Line	Peripheral A	Peripheral B	Reset State	Function	Comments
PA0	MISO	PCK3	I/O		
PA1	MOSI	PCK0	I/O		
PA2	SPCK	IRQ4	I/O		
PA3	NPCS0	IRQ5	I/O		
PA4	NPCS1	PCK1	I/O		
PA5	NPCS2	TXD3	I/O		
PA6	NPCS3	RXD3	I/O		
PA7	ETXCK/EREFCK	PCK2	I/O		
PA8	ETXEN	MCCDB	I/O		
PA9	ETX0	MCDB0	I/O		
PA10	ETX1	MCDB1	I/O		
PA11	ECRS/ECRSDV	MCDB2	I/O		
PA12	ERX0	MCDB3	I/O		
PA13	ERX1	TCLK0	I/O		
PA14	ERXER	TCLK1	I/O		
PA15	EMDC	TCLK2	I/O		
PA16	EMDIO	IRQ6	I/O		
PA17	TXD0	TIOA0	I/O		
PA18	RXD0	TIOB0	I/O		
PA19	SCK0	TIOA1	I/O		
PA20	CTS0	TIOB1	I/O		
PA21	RTS0	TIOA2	I/O		
PA22	RXD2	TIOB2	I/O		
PA23	TXD2	IRQ3	I/O		
PA24	SCK2	PCK1	I/O		
PA25	TWD	IRQ2	I/O		
PA26	TWCK	IRQ1	I/O		
PA27	MCCK	TCLK3	I/O		
PA28	MCCDA	TCLK4	I/O		
PA29	MCDA0	TCLK5	I/O		
PA30	DRXD	CTS2	I/O		
PA31	DTXD	RTS2	I/O		

10.8 Peripheral DMA Controller (PDC)

- Generates transfers to/from peripherals such as DBGU, USART, SSC, SPI and MCI
- Twenty channels
- One Master Clock cycle needed for a transfer from memory to peripheral
- Two Master Clock cycles needed for a transfer from peripheral to memory

10.9 System Timer

- One Period Interval Timer, 16-bit programmable counter
- One Watchdog Timer, 16-bit programmable counter
- One Real-time Timer, 20-bit free-running counter
- Interrupt Generation on event

10.10 Real-time Clock

- Low power consumption
- Full asynchronous design
- Two hundred year calendar
- Programmable Periodic Interrupt
- Alarm and update parallel load
- Control of alarm and update Time/Calendar Data In

10.11 USB Host Port

- Compliance with Open HCI Rev 1.0 specification
- Compliance with USB V2.0 Full-speed and Low-speed Specification
- Supports both Low-speed 1.5 Mbps and Full-speed 12 Mbps USB devices
- Root hub integrated with two downstream USB ports
- Two embedded USB transceivers
- Supports power management
- Operates as a master on the Memory Controller

10.12 USB Device Port

- USB V2.0 full-speed compliant, 12 Mbits per second
- Embedded USB V2.0 full-speed transceiver
- Embedded dual-port RAM for endpoints
- Suspend/Resume logic
- Ping-pong mode (two memory banks) for isochronous and bulk endpoints
- Six general-purpose endpoints
  - Endpoint 0, Endpoint 3: 8 bytes, no ping-pong mode
  - Endpoint 1, Endpoint 2: 64 bytes, ping-pong mode
  - Endpoint 4, Endpoint 5: 256 bytes, ping-pong mode

10.13 Ethernet MAC

- Compatibility with IEEE Standard 802.3

11. Package Drawings

Figure 11-1. 208-lead PQFP Package Drawing

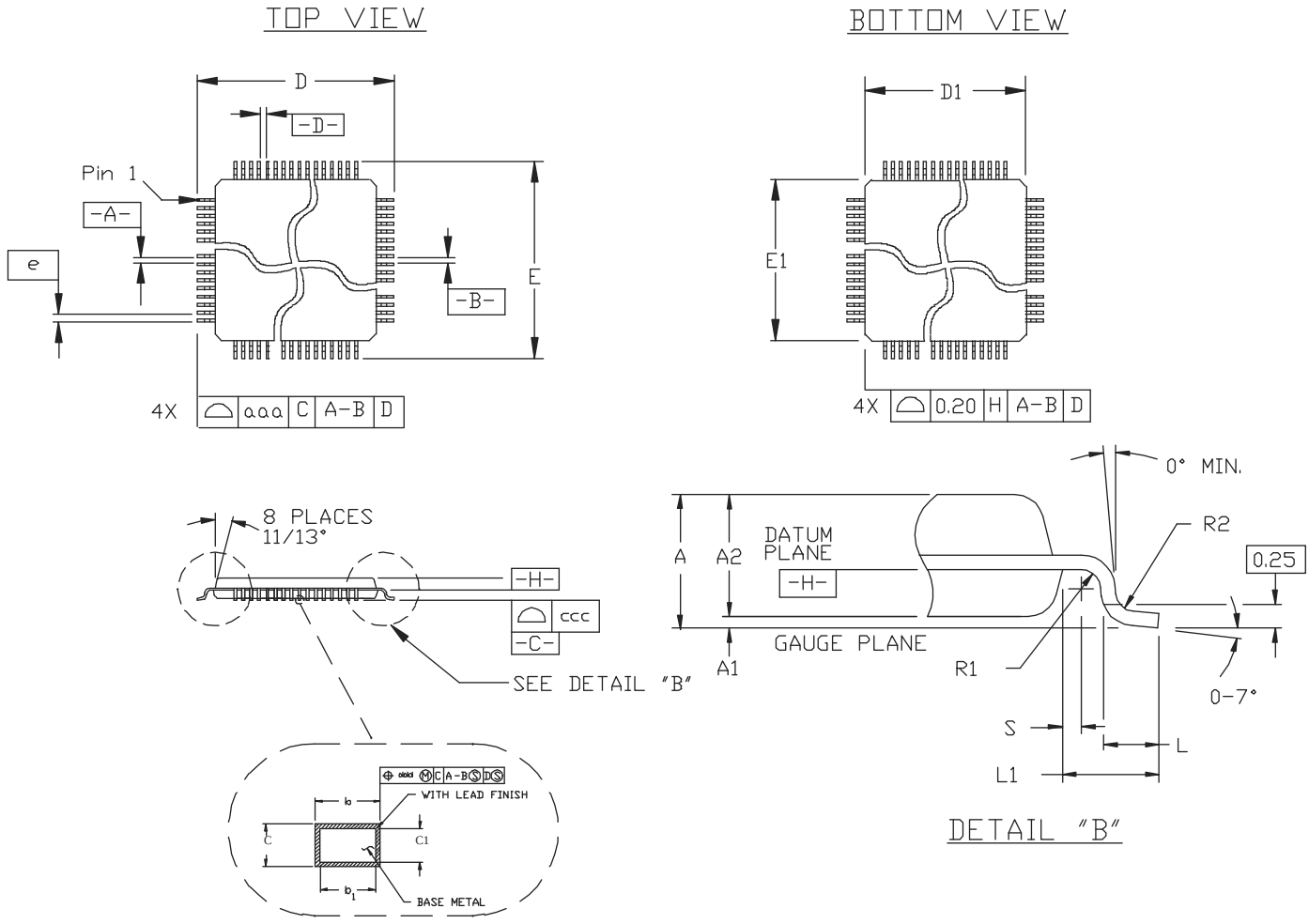
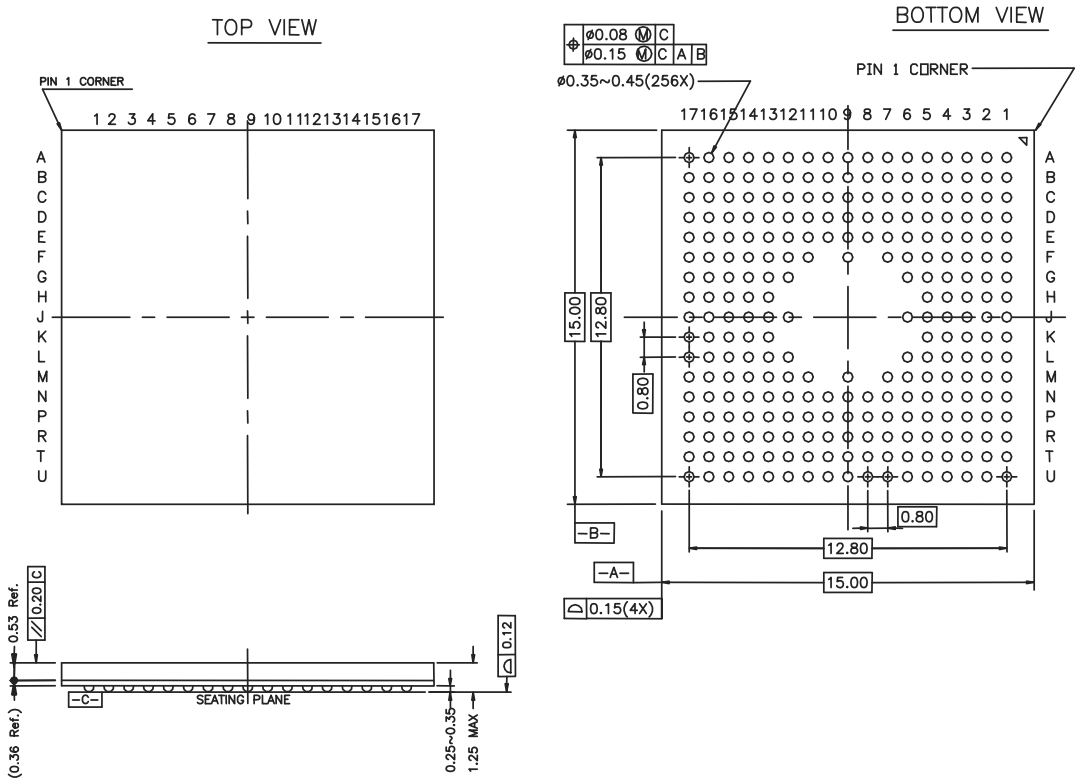


Table 11-1. 208-lead PQFP Package Dimensions (in mm)

Symbol	Min	Nom	Max	Symbol	Min	Nom	Max
c	0.11		0.23	b1	0.17	0.20	0.23
c1	0.11	0.15	0.19	ddd	0.10		
L	0.65	0.88	1.03	**Tolerances of Form and Position**			
L1	1.60 REF			aaa		0.25	
R2	0.13		0.3	ccc			0.1
R1	0.13			**BSC**			
S	0.4			D	31.20		
A	4.10			D1	28.00		
A1	0.25		0.50	E	31.20		
A2	3.20	3.40	3.60	E1	28.00		
b	0.17		0.27	e	0.50		

Figure 11-2. 256-ball BGA Package Drawing



12. AT91RM9200 Ordering Information

Table 12-1. Ordering Information

Ordering Code	Package	Package Type	Temperature Operating Range
AT91RM9200-QU-002	PQFP 208	Green	Industrial (-40· C to 85· C)
AT91RM9200-CJ-002	BGA 256	RoHS-compliant	

Revision History (cont.)

Document Ref.	Comments	Change Request Ref.
1768JS	Reformatted Section 8. ”Memories” on page 17. Inserted new figure Figure 8-1 on page 17 with overall product memory map.	
	Added Section 11. “Package Drawings” on page 33.	
1768KS	Updated “Features” and Section 4. ”Package and Pinout” on page 8 with additional details on package options.	
	Updated Table 40-1, “Ordering Information,” on page 661.	
1768LS	Ordering code AT91RM9200-CI-002 removed from Section 12. “AT91RM9200 Ordering Information” on page 35	6423
1768MS	USART3 0XFFECC000 changed into 0XFFFCC000 in Figure 8-1 on page 17	5067

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