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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM920T
Core Size	16/32-Bit
Speed	180MHz
Connectivity	EBI/EMI, Ethernet, I²C, Memory Card, SPI, SSC, UART/USART, USB
Peripherals	POR
Number of I/O	122
Program Memory Size	128KB (128K x 8)
Program Memory Type	ROM
EEPROM Size	-
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 1.95V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at91rm9200-qi-002-t

- **Two 3-channel, 16-bit Timer/Counters (TC)**
  - **Three External Clock Inputs, Two Multi-purpose I/O Pins per Channel**
  - **Double PWM Generation, Capture/Waveform Mode, Up/Down Capability**
- **Two-wire Interface (TWI)**
  - **Master Mode Support, All 2-wire Atmel EEPROMs Supported**
- **IEEE® 1149.1 JTAG Boundary Scan on All Digital Pins**
- **Power Supplies**
  - **1.65V to 1.95V for VDDCORE, VDDOSC and VDDPLL**
  - **3.0V to 3.6V for VDDIOP (Peripheral I/Os) and for VDDIOM (Memory I/Os)**
- **Available in a 208-pin Green PQFP or 256-ball RoHS-compliant BGA Package**

1. Description

The AT91RM9200 is a complete system-on-chip built around the ARM920T ARM Thumb processor. It incorporates a rich set of system and application peripherals and standard interfaces in order to provide a single-chip solution for a wide range of compute-intensive applications that require maximum functionality at minimum power consumption at lowest cost.

The AT91RM9200 incorporates a high-speed on-chip SRAM workspace, and a low-latency External Bus Interface (EBI) for seamless connection to whatever configuration of off-chip memories and memory-mapped peripherals is required by the application. The EBI incorporates controllers for synchronous DRAM (SDRAM), Burst Flash and Static memories and features specific circuitry facilitating the interface for NAND Flash/SmartMedia and Compact Flash.

The Advanced Interrupt Controller (AIC) enhances the interrupt handling performance of the ARM920T processor by providing multiple vectored, prioritized interrupt sources and reducing the time taken to transfer to an interrupt handler.

The Peripheral DMA Controller (PDC) provides DMA channels for all the serial peripherals, enabling them to transfer data to or from on- and off-chip memories without processor intervention. This reduces the processor overhead when dealing with transfers of continuous data streams.The AT91RM9200 benefits from a new generation of PDC which includes dual pointers that simplify significantly buffer chaining.

The set of Parallel I/O (PIO) controllers multiplex the peripheral input/output lines with general-purpose data I/Os for maximum flexibility in device configuration. An input change interrupt, open drain capability and programmable pull-up resistor is included on each line.

The Power Management Controller (PMC) keeps system power consumption to a minimum by selectively enabling/disabling the processor and various peripherals under software control. It uses an enhanced clock generator to provide a selection of clock signals including a slow clock (32 kHz) to optimize power consumption and performance at all times.

The AT91RM9200 integrates a wide range of standard interfaces including USB 2.0 Full Speed Host and Device and Ethernet 10/100 Base-T Media Access Controller (MAC), which provides connection to a extensive range of external peripheral devices and a widely used networking layer. In addition, it provides an extensive set of peripherals that operate in accordance with several industry standards, such as those used in audio, telecom, Flash Card, infrared and Smart Card applications.

To complete the offer, the AT91RM9200 benefits from the integration of a wide range of debug features including JTAG-ICE, a dedicated UART debug channel (DBGU) and an embedded real time trace. This enables the development and debug of all applications, especially those with real-time constraints.

3. Signal Description

Table 3-1. Signal Description by Peripheral

Pin Name	Function	Type	Active Level	Comments
Power				
VDDIOM	Memory I/O Lines Power Supply	Power		3.0V to 3.6V
VDDIOP	Peripheral I/O Lines Power Supply	Power		3.0V to 3.6V
VDDPLL	Oscillator and PLL Power Supply	Power		1.65V to 1.95V
VDDCORE	Core Chip Power Supply	Power		1.65V to 1.95V
VDDOSC	Oscillator Power Supply	Power		1.65V to 1.95V
GND	Ground	Ground		
GNDPLL	PLL Ground	Ground		
GNDOSC	Oscillator Ground	Ground		
Clocks, Oscillators and PLLs				
XIN	Main Crystal Input	Input		
XOUT	Main Crystal Output	Output		
XIN32	32KHz Crystal Input	Input		
XOUT32	32KHz Crystal Output	Output		
PLLRCA	PLL A Filter	Input		
PLLRCB	PLL B Filter	Input		
PCK0 - PCK3	Programmable Clock Output	Output		
ICE and JTAG				
TCK	Test Clock	Input		Schmitt trigger
TDI	Test Data In	Input		Internal Pull-up, Schmitt trigger
TDO	Test Data Out	Output		Tri-state
TMS	Test Mode Select	Input		Internal Pull-up, Schmitt trigger
NTRST	Test Reset Signal	Input	Low	Internal Pull-up, Schmitt trigger
JTAGSEL	JTAG Selection	Input		Schmitt trigger
ETM™				
TSYNC	Trace Synchronization Signal	Output		
TCLK	Trace Clock	Output		
TPS0 - TPS2	Trace ARM Pipeline Status	Output		
TPK0 - TPK15	Trace Packet Port	Output		
Reset/Test				
NRST	Microcontroller Reset	Input	Low	No on-chip pull-up, Schmitt trigger
TST0 - TST1	Test Mode Select	Input		Must be tied low for normal operation, Schmitt trigger

Table 3-1. Signal Description by Peripheral

Pin Name	Function	Type	Active Level	Comments
SPI				
MISO	Master In Slave Out	I/O		
MOSI	Master Out Slave In	I/O		
SPCK	SPI Serial Clock	I/O		
NPCS0	SPI Peripheral Chip Select 0	I/O	Low	
NPCS1 - NPCS3	SPI Peripheral Chip Select	Output	Low	
Two-Wire Interface				
TWD	Two-wire Serial Data	I/O		
TWCK	Two-wire Serial Clock	I/O		

4. Package and Pinout

The AT91RM9200 is available in two packages:

- 208-pin PQFP, 31.2 x 31.2 mm, 0.5 mm pitch
- 256-ball BGA, 15 x 15 mm, 0.8 mm ball pitch

The product features of the 256-ball BGA package are extended compared to the 208-lead PQFP package. The features that are available only with the 256-ball BGA package are:

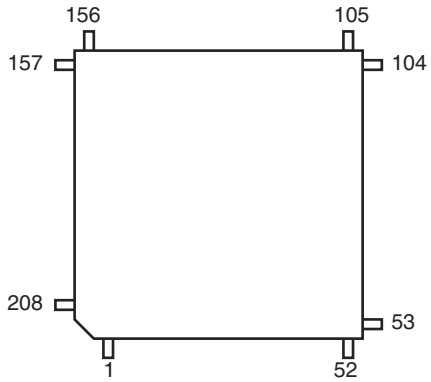
- Parallel I/O Controller D
- ETM port with outputs multiplexed on the PIO Controller D
- a second USB Host transceiver, opening the Hub capabilities of the embedded USB Host.

4.1 208-pin PQFP Package Outline

Figure 1-1 shows the orientation of the 208-pin PQFP package.

A detailed mechanical description is given in the section “AT91RM9200 Mechanical Characteristics” of the product datasheet.

Figure 4-1. 208-pin PQFP Package (Top View)



4.4 256-ball BGA Package Pinout

Table 4-2. AT91RM9200 Pinout for 256-ball BGA Package

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A1	TDI	C3	PD14	E5	TCK	G14	PA1
A2	JTAGSEL	C4	PB22	E6	GND	G15	PA2
A3	PB20	C5	PB19	E7	PB15	G16	PA3
A4	PB17	C6	PD10	E8	GND	G17	XIN32
A5	PD11	C7	PB13	E9	PB7	H1	PD23
A6	PD8	C8	PB12	E10	PB3	H2	PD20
A7	VDDIOP	C9	PB6	E11	PA29	H3	PD22
A8	PB9	C10	PB1	E12	PA26	H4	PD21
A9	PB4	C11	GND	E13	PA25	H5	VDDIOP
A10	PA31/BMS	C12	PA20	E14	PA9	H13	VDDPLL
A11	VDDIOP	C13	PA18	E15	PA6	H14	VDDIOP
A12	PA23	C14	VDDCORE	E16	PD3	H15	GNDPLL
A13	PA19	C15	GND	E17	PD0	H16	GND
A14	GND	C16	PA8	F1	PD16	H17	XOUT32
A15	PA14	C17	PD5	F2	GND	J1	PD25
A16	VDDIOP	D1	TST1	F3	PB23	J2	PD27
A17	PA13	D2	VDDIOP	F4	PB25	J3	PD24
B1	TDO	D3	VDDIOP	F5	PB24	J4	PD26
B2	PD13	D4	GND	F6	VDDCORE	J5	PB28
B3	PB18	D5	VDDIOP	F7	PB16	J6	PB29
B4	PB21	D6	PD7	F9	PB11	J12	GND
B5	PD12	D7	PB14	F11	PA30	J13	GNDOSC
B6	PD9	D8	VDDIOP	F12	PA28	J14	VDDOSC
B7	GND	D9	PB8	F13	PA4	J15	VDDPLL
B8	PB10	D10	PB2	F14	PD2	J16	GNDPLL
B9	PB5	D11	GND	F15	PD1	J17	XIN
B10	PB0	D12	PA22	F16	PA5	K1	HDPA
B11	VDDIOP	D13	PA21	F17	PLLRCB	K2	DDM
B12	PA24	D14	PA16	G1	PD19	K3	HDMA
B13	PA17	D15	PA10	G2	PD17	K4	VDDIOP
B14	PA15	D16	PD6	G3	GND	K5	DDP
B15	PA11	D17	PD4	G4	PB26	K13	PC5
B16	PA12	E1	NRST	G5	PD18	K14	PC4
B17	PA7	E2	NTRST	G6	PB27	K15	PC6
C1	TMS	E3	GND	G12	PA27	K16	VDDIOM
C2	PD15	E4	TST0	G13	PA0	K17	XOUT

- Debug Unit
  - Two-pin UART
  - Debug Communication Channel
  - Chip ID Register
- Embedded Trace Macrocell: ETM9™ Rev2a
  - Medium Level Implementation
  - Half-rate Clock Mode
  - Four Pairs of Address Comparators
  - Two Data Comparators
  - Eight Memory Map Decoder Inputs
  - Two Counters
  - One Sequencer
  - One 18-byte FIFO
- IEEE1149.1 JTAG Boundary Scan on all Digital Pins

7.3 Boot Program

- Default Boot Program stored in ROM-based products
- Downloads and runs an application from external storage media into internal SRAM
- Downloaded code size depends on embedded SRAM size
- Automatic detection of valid application
- Bootloader supporting a wide range of non-volatile memories
  - SPI DataFlash® connected on SPI NPCS0
  - Two-wire EEPROM
  - 8-bit parallel memories on NCS0
- Boot Uploader in case no valid program is detected in external NVM and supporting several communication media
- Serial communication on a DBGU (XModem protocol)
- USB Device Port (DFU Protocol)

7.4 Embedded Software Services

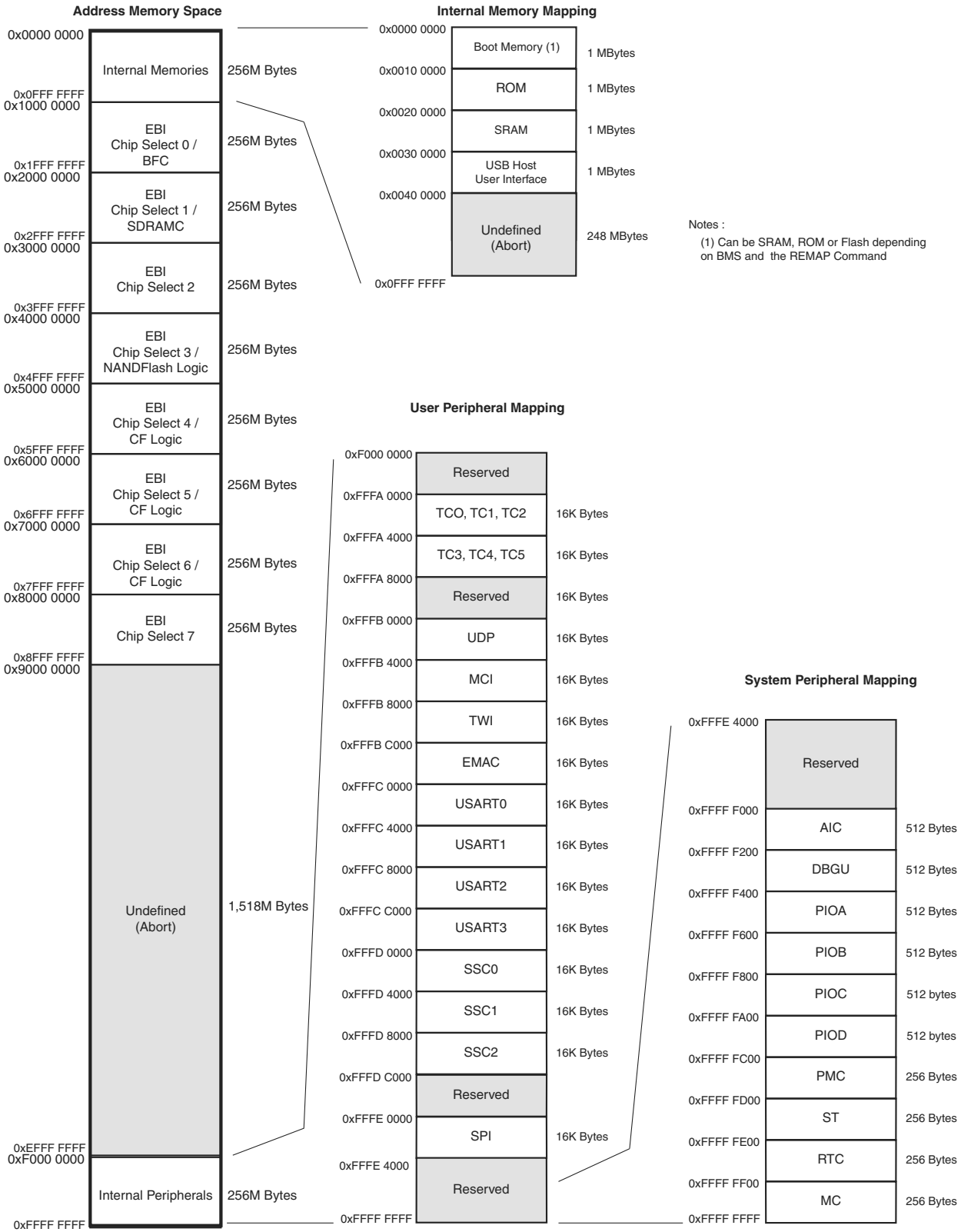
- Compliant with ATPCS
- Compliant with AINSI/ISO Standard C
- Compiled in ARM/Thumb Interworking
- ROM Entry Service
- Tempo, Xmodem and DataFlash services
- CRC and Sine tables

7.5 Memory Controller

- Programmable Bus Arbiter handling four Masters
  - Internal Bus is shared by ARM920T, PDC, USB Host Port and Ethernet MAC Masters
  - Each Master can be assigned a priority between 0 and 7

8. Memories

Figure 8-1. AT91RM9200 Memory Mapping



A first level of address decoding is performed by the Memory Controller, i.e., by the implementation of the Advanced System Bus (ASB) with additional features.

Decoding splits the 4G bytes of address space into 16 areas of 256M bytes. The areas 1 to 8 are directed to the EBI that associates these areas to the external chip selects NC0 to NCS7. The area 0 is reserved for the addressing of the internal memories, and a second level of decoding provides 1M bytes of internal memory area. The area 15 is reserved for the peripherals and provides access to the Advanced Peripheral Bus (APB).

Other areas are unused and performing an access within them provides an abort to the master requesting such an access.

8.1 Embedded Memories

8.1.1 Internal Memory Mapping

8.1.1.1 Internal RAM

The AT91RM9200 integrates a high-speed, 16-Kbyte internal SRAM. After reset and until the Remap Command is performed, the SRAM is only accessible at address 0x20 0000. After Remap, the SRAM is also available at address 0x0.

8.1.1.2 Internal ROM

The AT91RM9200 integrates a 128-Kbyte Internal ROM. At any time, the ROM is mapped at address 0x10 0000. It is also accessible at address 0x0 after reset and before the Remap Command if the BMS is tied high during reset.

8.1.1.3 USB Host Port

The AT91RM9200 integrates a USB Host Port Open Host Controller Interface (OHCI). The registers of this interface are directly accessible on the ASB Bus and are mapped like a standard internal memory at address 0x30 0000.

  - the Master Clock MCK
  - the USB Clocks, UHPCK and UDPCK, respectively for the USB Host Port and the USB Device Port
  - Programmable automatic PLL switch-off in USB Device suspend conditions
  - up to thirty peripheral clocks
  - four programmable clock outputs PCK0 to PCK3
- Four operating modes:
  - Normal Mode, Idle Mode, Slow Clock Mode, Standby Mode

9.4 Debug Unit

- System peripheral to facilitate debug of Atmel's ARM-based systems
- Composed of the following functions
  - Two-pin UART
  - Debug Communication Channel (DCC) support
  - Chip ID Registers
- Two-pin UART
  - Implemented features are 100% compatible with the standard Atmel USART
  - Independent receiver and transmitter with a common programmable Baud Rate Generator
  - Even, Odd, Mark or Space Parity Generation
  - Parity, Framing and Overrun Error Detection
  - Automatic Echo, Local Loopback and Remote Loopback Channel Modes
  - Interrupt generation
  - Support for two PDC channels with connection to receiver and transmitter
- Debug Communication Channel Support
  - Offers visibility of COMMRX and COMMTX signals from the ARM Processor
  - Interrupt generation
- Chip ID Registers
  - Identification of the device revision, sizes of the embedded memories, set of peripherals

9.5 PIO Controller

- Up to 32 programmable I/O Lines
- Fully programmable through Set/Clear Registers
- Multiplexing of two peripheral functions per I/O Line
- For each I/O Line (whether assigned to a peripheral or used as general purpose I/O)
  - Input change interrupt
  - Glitch filter
  - Multi-drive option enables driving in open drain
  - Programmable pull up on each I/O line
  - Pin data status register, supplies visibility of the level on the pin at any time

Table 10-1. Peripheral Identifiers (Continued)

Peripheral ID	Peripheral Mnemonic	Peripheral Name	External Interrupt
24	EMAC	Ethernet MAC	
25	AIC	Advanced Interrupt Controller	IRQ0
26	AIC	Advanced Interrupt Controller	IRQ1
27	AIC	Advanced Interrupt Controller	IRQ2
28	AIC	Advanced Interrupt Controller	IRQ3
29	AIC	Advanced Interrupt Controller	IRQ4
30	AIC	Advanced Interrupt Controller	IRQ5
31	AIC	Advanced Interrupt Controller	IRQ6

10.3 Peripheral Multiplexing on PIO Lines

The AT91RM9200 features four PIO controllers:

- PIOA and PIOB, multiplexing I/O lines of the peripheral set
- PIOC, multiplexing the data bus bits 16 to 31 and several External Bus Interface control signals. Using PIOC pins increases the number of general-purpose I/O lines available but prevents 32-bit memory access
- PIOD, available in the 256-ball BGA package option only, multiplexing outputs of the peripheral set and the ETM port

Each PIO Controller controls up to 32 lines. Each line can be assigned to one of two peripheral functions, A or B. The tables in the following paragraphs define how the I/O lines of the peripherals A and B are multiplexed on the PIO Controllers A, B, C and D. The two columns “Function” and “Comments” have been inserted for the user’s own comments; they may be used to track how pins are defined in an application.

The column “Reset State” indicates whether the PIO line resets in I/O mode or in peripheral mode. If equal to “I/O”, the PIO line resets in input with the pull-up enabled so that the device is maintained in a static state as soon as the NRST pin is asserted. As a result, the bit corresponding to the PIO line in the register PIO_PSR (Peripheral Status Register) resets low.

If a signal name is in the “Reset State” column, the PIO line is assigned to this function and the corresponding bit in PIO_PSR resets high. This is the case for pins controlling memories, either address lines or chip selects, and that require the pin to be driven as soon as NRST raises. Note that the pull-up resistor is also enabled in this case.

See Table 10-2 on page 23, Table 10-3 on page 24, Table 10-4 on page 25 and Table 10-5 on page 26.

10.3.2 PIO Controller B Multiplexing

Table 10-3. Multiplexing on PIO Controller B

PIO Controller B				Application Usage	
I/O Line	Peripheral A	Peripheral B	Reset State	Function	Comments
PB0	TF0	RTS3	I/O		
PB1	TK0	CTS3	I/O		
PB2	TD0	SCK3	I/O		
PB3	RD0	MCDA1	I/O		
PB4	RK0	MCDA2	I/O		
PB5	RF0	MCDA3	I/O		
PB6	TF1	TIOA3	I/O		
PB7	TK1	TIOB3	I/O		
PB8	TD1	TIOA4	I/O		
PB9	RD1	TIOB4	I/O		
PB10	RK1	TIOA5	I/O		
PB11	RF1	TIOB5	I/O		
PB12	TF2	ETX2	I/O		
PB13	TK2	ETX3	I/O		
PB14	TD2	ETXER	I/O		
PB15	RD2	ERX2	I/O		
PB16	RK2	ERX3	I/O		
PB17	RF2	ERXDV	I/O		
PB18	RI1	ECOL	I/O		
PB19	DTR1	ERXCK	I/O		
PB20	TXD1		I/O		
PB21	RXD1		I/O		
PB22	SCK1		I/O		
PB23	DCD1		I/O		
PB24	CTS1		I/O		
PB25	DSR1	EF100	I/O		
PB26	RTS1		I/O		
PB27	PCK0		I/O		
PB28	FIQ		I/O		
PB29	IRQ0		I/O		

  - Compliant with LCD Module
  - Programmable Setup Time Read/Write
  - Programmable Hold Time Read/Write
- Multiple Wait State Management
  - Programmable Wait State Generation
  - External Wait Request
  - Programmable Data Float Time

10.6 SDRAM Controller

- Numerous configurations supported
  - 2K, 4K, 8K Row Address Memory Parts
  - SDRAM with two or four Internal Banks
  - SDRAM with 16- or 32-bit Data Path
- Programming facilities
  - Word, half-word, byte access
  - Automatic page break when Memory Boundary has been reached
  - Multibank Ping-pong Access
  - Timing parameters specified by software
  - Automatic refresh operation, refresh rate is programmable
- Energy-saving capabilities
  - Self-refresh and Low-power Modes supported
- Error detection
  - Refresh Error Interrupt
- SDRAM Power-up Initialization by software
- Latency is set to two clocks (CAS Latency of 1, 3 Not Supported)
- Auto Precharge Command not used

10.7 Burst Flash Controller

- Multiple Access Modes supported
  - Asynchronous or Burst Mode Byte, Half-word or Word Read Accesses
  - Asynchronous Mode Half-word Write Accesses
- Adaptability to different device speed grades
  - Programmable Burst Flash Clock Rate
  - Programmable Data Access Time
  - Programmable Latency after Output Enable
- Adaptability to different device access protocols and bus interfaces
  - Two Burst Read Protocols: Clock Control Address Advance or Signal Controlled Address Advance
  - Multiplexed or separate address and data buses
  - Continuous Burst and Page Mode Accesses supported

10.8 Peripheral DMA Controller (PDC)

- Generates transfers to/from peripherals such as DBGU, USART, SSC, SPI and MCI
- Twenty channels
- One Master Clock cycle needed for a transfer from memory to peripheral
- Two Master Clock cycles needed for a transfer from peripheral to memory

10.9 System Timer

- One Period Interval Timer, 16-bit programmable counter
- One Watchdog Timer, 16-bit programmable counter
- One Real-time Timer, 20-bit free-running counter
- Interrupt Generation on event

10.10 Real-time Clock

- Low power consumption
- Full asynchronous design
- Two hundred year calendar
- Programmable Periodic Interrupt
- Alarm and update parallel load
- Control of alarm and update Time/Calendar Data In

10.11 USB Host Port

- Compliance with Open HCI Rev 1.0 specification
- Compliance with USB V2.0 Full-speed and Low-speed Specification
- Supports both Low-speed 1.5 Mbps and Full-speed 12 Mbps USB devices
- Root hub integrated with two downstream USB ports
- Two embedded USB transceivers
- Supports power management
- Operates as a master on the Memory Controller

10.12 USB Device Port

- USB V2.0 full-speed compliant, 12 Mbits per second
- Embedded USB V2.0 full-speed transceiver
- Embedded dual-port RAM for endpoints
- Suspend/Resume logic
- Ping-pong mode (two memory banks) for isochronous and bulk endpoints
- Six general-purpose endpoints
  - Endpoint 0, Endpoint 3: 8 bytes, no ping-pong mode
  - Endpoint 1, Endpoint 2: 64 bytes, ping-pong mode
  - Endpoint 4, Endpoint 5: 256 bytes, ping-pong mode

10.13 Ethernet MAC

- Compatibility with IEEE Standard 802.3

- 10 and 100 Mbits per second data throughput capability
- Full- and half-duplex operation
- MII or RMII interface to the physical layer
- Register interface to address, status and control registers
- DMA interface, operating as a master on the Memory Controller
- Interrupt generation to signal receive and transmit completion
- 28-byte transmit and 28-byte receive FIFOs
- Automatic pad and CRC generation on transmitted frames
- Address checking logic to recognize four 48-bit addresses
- Supports promiscuous mode where all valid frames are copied to memory
- Supports physical layer management through MDIO interface

10.14 Serial Peripheral Interface

- Supports communication with serial external devices
  - Four chip selects with external decoder support allow communication with up to 15 peripherals
  - Serial memories, such as DataFlash and 3-wire EEPROMs
  - Serial peripherals, such as ADCs, DACs, LCD Controllers, CAN Controllers and Sensors
  - External co-processors
- Master or slave serial peripheral bus interface
  - 8- to 16-bit programmable data length per chip select
  - Programmable phase and polarity per chip select
  - Programmable transfer delays between consecutive transfers and between clock and data per chip select
  - Programmable delay between consecutive transfers
  - Selectable mode fault detection
- Connection to PDC channel optimizes data transfers
  - One channel for the receiver, one channel for the transmitter
  - Next buffer support

10.15 Two-wire Interface

- Compatibility with standard two-wire serial memory
- One, two or three bytes for slave address
- Sequential Read/Write operations

10.16 USART

- Programmable Baud Rate Generator
- 5- to 9-bit full-duplex synchronous or asynchronous serial communications
  - 1, 1.5 or 2 stop bits in Asynchronous Mode or 1 or 2 stop bits in Synchronous Mode
  - Parity generation and error detection
  - Framing error detection, overrun error detection

  - MSB- or LSB-first
  - Optional break generation and detection
  - By 8 or by-16 over-sampling receiver frequency
  - Optional hardware handshaking RTS-CTS
  - Optional modem signal management DTR-DSR-DCD-RI
  - Receiver time-out and transmitter timeguard
  - Optional Multi-drop Mode with address generation and detection
- RS485 with driver control signal
- ISO7816, T = 0 or T = 1 Protocols for interfacing with smart cards
  - NACK handling, error counter with repetition and iteration limit
- IrDA modulation and demodulation
  - Communication at up to 115.2 Kbps
- Test Modes
  - Remote Loopback, Local Loopback, Automatic Echo
- Connection of two Peripheral DMA Controller (PDC) channels
  - Offers buffer transfer without processor intervention

The USART describes features allowing management of the Modem Signals DTR, DSR, DCD and RI. For details, see ”Modem Mode” on page 435.

In the AT91RM9200, only the USART1 implements these signals, named DTR1, DSR1, DCD1 and RI1.

The USART0, USART2 and USART3 do not implement all the modem signals. Only RTS and CTS (RTS0 and CTS0, RTS2 and CTS2, RTS3 and CTS3, respectively) are implemented in these USARTs for other features.

Thus, programming the USART0, USART2 or the USART3 in Modem Mode may lead to unpredictable results. In these USARTs, the commands relating to the Modem Mode have no effect and the status bits relating the status of the modem signals are never activated.

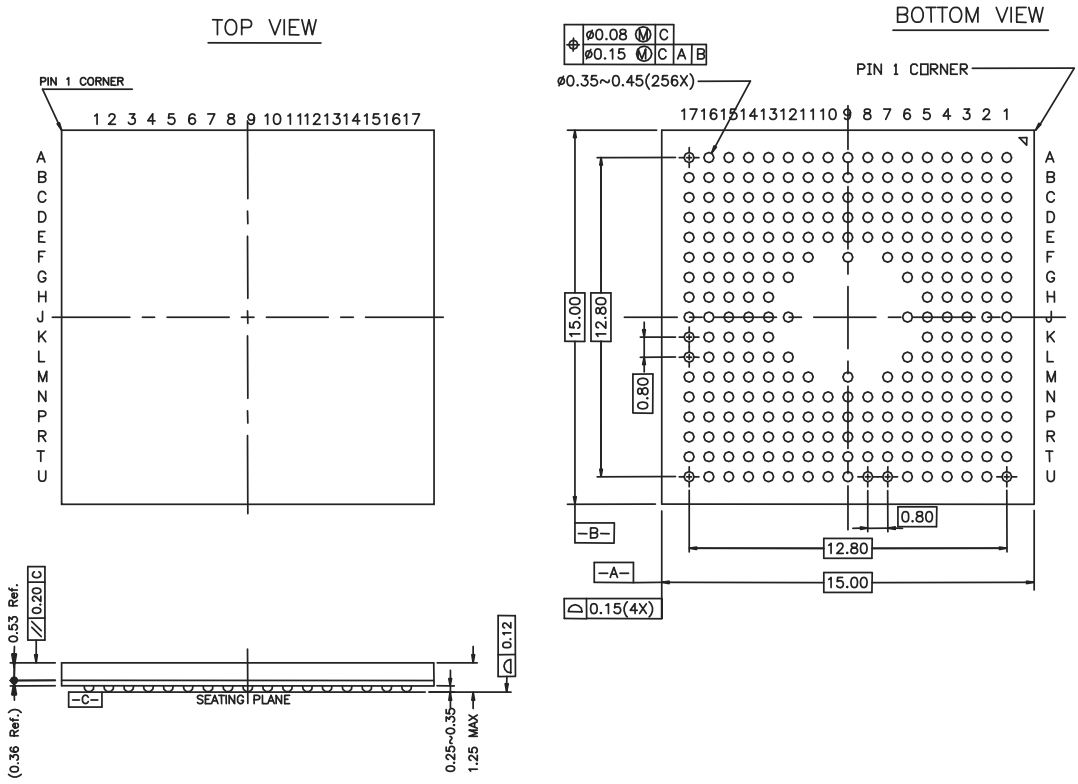
10.17 Serial Synchronous Controller

- Provides serial synchronous communication links used in audio and telecom applications
- Contains an independent receiver and transmitter and a common clock divider
- Interfaced with two PDC channels to reduce processor overhead
- Offers a configurable frame sync and data length
- Receiver and transmitter can be programmed to start automatically or on detection of different event on the frame sync signal
- Receiver and transmitter include a data signal, a clock signal and a frame synchronization signal

10.18 Timer Counter

- Three 16-bit Timer Counter Channels
- Wide range of functions including:
  - Frequency Measurement
  - Event Counting

Figure 11-2. 256-ball BGA Package Drawing



13. Revision History

Doc. Rev	Source	Comments
Lit°1768A		• **Date Qualified:** May 2001
Lit°1768B		• **Date Qualified:** September 2001
Lit°1768C		• **Date Qualified:** November 2001
Lit°1768D		• **Date Qualified:** 5 Mar-02
Lit°1768E		• **Date Qualified:** 12-Jul-02
Lit°1768F		• **Date Qualified:** 5 Feb-03
Doc. Rev	**Source**	**Comments**
1768GS	Review	• **Date Qualified:** 04-Sep-03
		• Page 2; Added Description.
		• Page 3; Updated Figure 1, Block Diagram, remove reference to Multi-master Memory Controller.
		• Page 4; Added section Key Features. Updated all descriptions of key blocks
		• Page 17; Added text to section Peripheral Multiplexing on PIO Lines.
		• Page 18; Expanded Table 3, Multiplexing on PIO Controller A.
		• Page 19: Expanded Table 4, Multiplexing on PIO Controller B.
		• Page 20; Expanded Table 5, Multiplexing on PIO Controller C.
		• Page 21; Expanded Table 6, Multiplexing on PIO Controller D.
		• Page 27; Updated Table 8, Peripheral Identifiers, Peripheral ID 1 description.
		• Page 28; Added section Product Memory Mapping.
		• Page 30; Updated and corrected Figure 6, System Peripherals Mapping.
		• Page 31; Updated and corrected Figure 7, User Peripherals Mapping.
Doc. Rev	**Source**	**Comments**
1768HS	CSRs/Review	• **Date Qualified:** Unqualified/Internal on Intranet 27-Jan-05
		• Global; Reformat in Corporate Template.
		• Global; Peripheral Data Controller (PDC) renamed Peripheral DMA Controller.
	CSR 04-066	• Page 1; Features: USART Hardware Handshaking. Software Handshaking removed.
	CSR 03-209	• Page 3; Figure 1: NWAIT pin added to block diagram.
	CSR 03-244	• Page 14; Table 1. AT91RM9200 Pinout for 208-lead PQFP package, pins 28, 30, 37 and 39 names changed
	CSR 04-315	• Page 23; Table 7. Pin Description, ICE and JTAG description, “Internal Pullup” added to comments for all signals, except TDO.
	CSR 03-209	• Page 24; Table 7. Pin Description, NWAIT pin added.
Doc. Rev	**Source**	**Comments**
1768IS		Corrected power consumption values on page 1.
	CSR 05-348	In Table 4-7, “Pin Description List,” on page 24 added mention of Schmitt trigger for pins JTAGSEL, TDI, TCK, TMS, NTRST, TST0, TST1 and NRST.

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