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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM920T
Core Size	16/32-Bit
Speed	180MHz
Connectivity	EBI/EMI, Ethernet, I²C, Memory Card, SPI, SSC, UART/USART, USB
Peripherals	POR
Number of I/O	122
Program Memory Size	128KB (128K x 8)
Program Memory Type	ROM
EEPROM Size	-
RAM Size	48K x 8
Voltage - Supply (Vcc/Vdd)	1.65V ~ 1.95V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/at91rm9200-qi-002

- **Two 3-channel, 16-bit Timer/Counters (TC)**
  - **Three External Clock Inputs, Two Multi-purpose I/O Pins per Channel**
  - **Double PWM Generation, Capture/Waveform Mode, Up/Down Capability**
- **Two-wire Interface (TWI)**
  - **Master Mode Support, All 2-wire Atmel EEPROMs Supported**
- **IEEE® 1149.1 JTAG Boundary Scan on All Digital Pins**
- **Power Supplies**
  - **1.65V to 1.95V for VDDCORE, VDDOSC and VDDPLL**
  - **3.0V to 3.6V for VDDIOP (Peripheral I/Os) and for VDDIOM (Memory I/Os)**
- **Available in a 208-pin Green PQFP or 256-ball RoHS-compliant BGA Package**

1. Description

The AT91RM9200 is a complete system-on-chip built around the ARM920T ARM Thumb processor. It incorporates a rich set of system and application peripherals and standard interfaces in order to provide a single-chip solution for a wide range of compute-intensive applications that require maximum functionality at minimum power consumption at lowest cost.

The AT91RM9200 incorporates a high-speed on-chip SRAM workspace, and a low-latency External Bus Interface (EBI) for seamless connection to whatever configuration of off-chip memories and memory-mapped peripherals is required by the application. The EBI incorporates controllers for synchronous DRAM (SDRAM), Burst Flash and Static memories and features specific circuitry facilitating the interface for NAND Flash/SmartMedia and Compact Flash.

The Advanced Interrupt Controller (AIC) enhances the interrupt handling performance of the ARM920T processor by providing multiple vectored, prioritized interrupt sources and reducing the time taken to transfer to an interrupt handler.

The Peripheral DMA Controller (PDC) provides DMA channels for all the serial peripherals, enabling them to transfer data to or from on- and off-chip memories without processor intervention. This reduces the processor overhead when dealing with transfers of continuous data streams.The AT91RM9200 benefits from a new generation of PDC which includes dual pointers that simplify significantly buffer chaining.

The set of Parallel I/O (PIO) controllers multiplex the peripheral input/output lines with general-purpose data I/Os for maximum flexibility in device configuration. An input change interrupt, open drain capability and programmable pull-up resistor is included on each line.

The Power Management Controller (PMC) keeps system power consumption to a minimum by selectively enabling/disabling the processor and various peripherals under software control. It uses an enhanced clock generator to provide a selection of clock signals including a slow clock (32 kHz) to optimize power consumption and performance at all times.

The AT91RM9200 integrates a wide range of standard interfaces including USB 2.0 Full Speed Host and Device and Ethernet 10/100 Base-T Media Access Controller (MAC), which provides connection to a extensive range of external peripheral devices and a widely used networking layer. In addition, it provides an extensive set of peripherals that operate in accordance with several industry standards, such as those used in audio, telecom, Flash Card, infrared and Smart Card applications.

To complete the offer, the AT91RM9200 benefits from the integration of a wide range of debug features including JTAG-ICE, a dedicated UART debug channel (DBGU) and an embedded real time trace. This enables the development and debug of all applications, especially those with real-time constraints.

2. Block Diagram

Bold arrows (⟶) indicate master-to-slave dependency.

Figure 2-1. AT91RM9200 Block Diagram

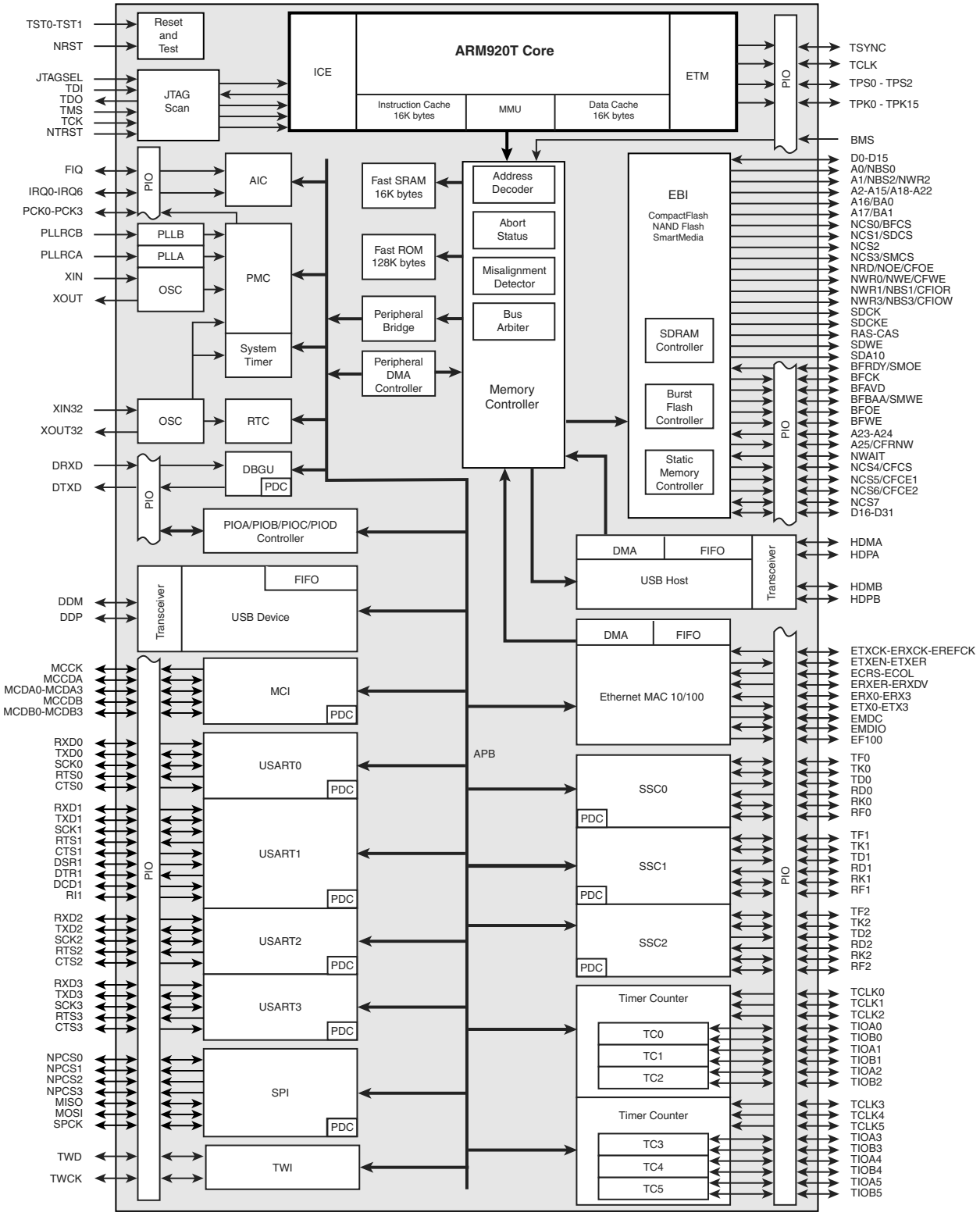

Table 3-1. Signal Description by Peripheral

Pin Name	Function	Type	Active Level	Comments
Memory Controller				
BMS	Boot Mode Select	Input		
Debug Unit				
DRXD	Debug Receive Data	Input		Debug Receive Data
DTXD	Debug Transmit Data	Output		Debug Transmit Data
AIC				
IRQ0 - IRQ6	External Interrupt Inputs	Input		
FIQ	Fast Interrupt Input	Input		
PIO				
PA0 - PA31	Parallel IO Controller A	I/O		Pulled-up input at reset
PB0 - PB29	Parallel IO Controller B	I/O		Pulled-up input at reset
PC0 - PC31	Parallel IO Controller C	I/O		Pulled-up input at reset
PD0 - PD27	Parallel IO Controller D	I/O		Pulled-up input at reset
EBI				
D0 - D31	Data Bus	I/O		Pulled-up input at reset
A0 - A25	Address Bus	Output		0 at reset
SMC				
NCS0 - NCS7	Chip Select Lines	Output	Low	1 at reset
NWR0 - NWR3	Write Signal	Output	Low	1 at reset
NOE	Output Enable	Output	Low	1 at reset
NRD	Read Signal	Output	Low	1 at reset
NUB	Upper Byte Select	Output	Low	1 at reset
NLB	Lower Byte Select	Output	Low	1 at reset
NWE	Write Enable	Output	Low	1 at reset
NWAIT	Wait Signal	Input	Low	
NBS0 - NBS3	Byte Mask Signal	Output	Low	1 at reset
EBI for CompactFlash Support				
CFCE1 - CFCE2	CompactFlash Chip Enable	Output	Low	
CFOE	CompactFlash Output Enable	Output	Low	
CFWE	CompactFlash Write Enable	Output	Low	
CFIOR	CompactFlash IO Read	Output	Low	
CFIOW	CompactFlash IO Write	Output	Low	
CFRNW	CompactFlash Read Not Write	Output		
CFCS	CompactFlash Chip Select	Output	Low	

Table 3-1. Signal Description by Peripheral

Pin Name	Function	Type	Active Level	Comments
EBI for NAND Flash/SmartMedia Support				
SMCS	NAND Flash/SmartMedia Chip Select	Output	Low	
SMOE	NAND Flash/SmartMedia Output Enable	Output	Low	
SMWE	NAND Flash/SmartMedia Write Enable	Output	Low	
SDRAM Controller				
SDCK	SDRAM Clock	Output		
SDCKE	SDRAM Clock Enable	Output	High	
SDCS	SDRAM Controller Chip Select	Output	Low	
BA0 - BA1	Bank Select	Output		
SDWE	SDRAM Write Enable	Output	Low	
RAS - CAS	Row and Column Signal	Output	Low	
SDA10	SDRAM Address 10 Line	Output		
Burst Flash Controller				
BFCK	Burst Flash Clock	Output		
BFCS	Burst Flash Chip Select	Output	Low	
BFAVD	Burst Flash Address Valid	Output	Low	
BFBAA	Burst Flash Address Advance	Output	Low	
BFOE	Burst Flash Output Enable	Output	Low	
BFRDY	Burst Flash Ready	Input	High	
BFWE	Burst Flash Write Enable	Output	Low	
Multimedia Card Interface				
MCCK	Multimedia Card Clock	Output		
MCCDA	Multimedia Card A Command	I/O		
MCDA0 - MCDA3	Multimedia Card A Data	I/O		
MCCDB	Multimedia Card B Command	I/O		
MCDB0 - MCDB3	Multimedia Card B Data	I/O		
USART				
SCK0 - SCK3	Serial Clock	I/O		
TXD0 - TXD3	Transmit Data	Output		
RXD0 - RXD3	Receive Data	Input		
RTS0 - RTS3	Ready To Send	Output		
CTS0 - CTS3	Clear To Send	Input		
DSR1	Data Set Ready	Input		
DTR1	Data Terminal Ready	Output		
DCD1	Data Carrier Detect	Input		
RI1	Ring Indicator	Input		

4.4 256-ball BGA Package Pinout

Table 4-2. AT91RM9200 Pinout for 256-ball BGA Package

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A1	TDI	C3	PD14	E5	TCK	G14	PA1
A2	JTAGSEL	C4	PB22	E6	GND	G15	PA2
A3	PB20	C5	PB19	E7	PB15	G16	PA3
A4	PB17	C6	PD10	E8	GND	G17	XIN32
A5	PD11	C7	PB13	E9	PB7	H1	PD23
A6	PD8	C8	PB12	E10	PB3	H2	PD20
A7	VDDIOP	C9	PB6	E11	PA29	H3	PD22
A8	PB9	C10	PB1	E12	PA26	H4	PD21
A9	PB4	C11	GND	E13	PA25	H5	VDDIOP
A10	PA31/BMS	C12	PA20	E14	PA9	H13	VDDPLL
A11	VDDIOP	C13	PA18	E15	PA6	H14	VDDIOP
A12	PA23	C14	VDDCORE	E16	PD3	H15	GNDPLL
A13	PA19	C15	GND	E17	PD0	H16	GND
A14	GND	C16	PA8	F1	PD16	H17	XOUT32
A15	PA14	C17	PD5	F2	GND	J1	PD25
A16	VDDIOP	D1	TST1	F3	PB23	J2	PD27
A17	PA13	D2	VDDIOP	F4	PB25	J3	PD24
B1	TDO	D3	VDDIOP	F5	PB24	J4	PD26
B2	PD13	D4	GND	F6	VDDCORE	J5	PB28
B3	PB18	D5	VDDIOP	F7	PB16	J6	PB29
B4	PB21	D6	PD7	F9	PB11	J12	GND
B5	PD12	D7	PB14	F11	PA30	J13	GNDOSC
B6	PD9	D8	VDDIOP	F12	PA28	J14	VDDOSC
B7	GND	D9	PB8	F13	PA4	J15	VDDPLL
B8	PB10	D10	PB2	F14	PD2	J16	GNDPLL
B9	PB5	D11	GND	F15	PD1	J17	XIN
B10	PB0	D12	PA22	F16	PA5	K1	HDPA
B11	VDDIOP	D13	PA21	F17	PLLRCB	K2	DDM
B12	PA24	D14	PA16	G1	PD19	K3	HDMA
B13	PA17	D15	PA10	G2	PD17	K4	VDDIOP
B14	PA15	D16	PD6	G3	GND	K5	DDP
B15	PA11	D17	PD4	G4	PB26	K13	PC5
B16	PA12	E1	NRST	G5	PD18	K14	PC4
B17	PA7	E2	NTRST	G6	PB27	K15	PC6
C1	TMS	E3	GND	G12	PA27	K16	VDDIOM
C2	PD15	E4	TST0	G13	PA0	K17	XOUT

6.4 PIO Controller A, B, C and D Lines

All the I/O lines PA0 to PA31, PB0 to PB29, PC0 to PC31 and PD0 to PD27 integrate a programmable pull-up resistor of 15 kOhm typical. Programming of this pull-up resistor is performed independently for each I/O line through the PIO Controllers.

After reset, all the I/O lines default as inputs with pull-up resistors enabled, except those which are multiplexed with the External Bus Interface signals that must be enabled as peripherals at reset. This is explicitly indicated in the column "Reset State" of the PIO Controller multiplexing tables.

7. Processor and Architecture

7.1 ARM920T Processor

- ARM9TDMI™-based on ARM Architecture v4T
- Two instruction sets
  - ARM High-performance 32-bit Instruction Set
  - Thumb High Code Density 16-bit Instruction Set
- 5-Stage Pipeline Architecture:
  - Instruction Fetch (F)
  - Instruction Decode (D)
  - Execute (E)
  - Data Memory (M)
  - Register Write (W)
- 16-Kbyte Data Cache, 16-Kbyte Instruction Cache
  - Virtually-addressed 64-way Associative Cache
  - 8 words per line
  - Write-though and write-back operation
  - Pseudo-random or Round-robin replacement
  - Low-power CAM RAM implementation
- Write Buffer
  - 16-word Data Buffer
  - 4-address Address Buffer
  - Software Control Drain
- Standard ARMv4 Memory Management Unit (MMU)
  - Access permission for sections
  - Access permission for large pages and small pages can be specified separately for each quarter of the pages
  - 16 embedded domains
  - 64 Entry Instruction TLB and 64 Entry Data TLB

8-, 16-, 32-bit Data Bus for Instructions and Data

7.2 Debug and Test

- Integrated EmbeddedICE