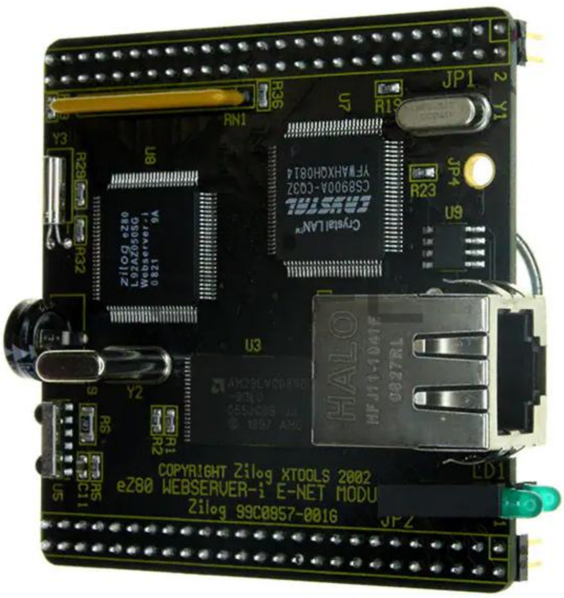

Welcome to E-XFL.COM

Understanding Embedded - Microcontroller, Microprocessor, FPGA Modules

Embedded - Microcontroller, Microprocessor, and FPGA Modules are fundamental components in modern electronic systems, offering a wide range of functionalities and capabilities. Microcontrollers are compact integrated circuits designed to execute specific control tasks within an embedded system. They typically include a processor, memory, and input/output peripherals on a single chip. Microprocessors, on the other hand, are more powerful processing units used in complex computing tasks, often requiring external memory and peripherals. FPGAs (Field Programmable Gate Arrays) are highly flexible devices that can be configured by the user to perform specific logic functions, making them invaluable in applications requiring customization and adaptability.

Applications of Embedded - Microcontroller,

Details	
Product Status	Obsolete
Module/Board Type	MCU Core
Core Processor	eZ80L92
Co-Processor	-
Speed	48MHz
Flash Size	1MB
RAM Size	512KB
Connector Type	Header 2x25
Size / Dimension	2.5" x 2.5" (64mm x 64mm)
Operating Temperature	0°C ~ 70°C
Purchase URL	https://www.e-xfl.com/product-detail/zilog/ez80l925048modg

List of Tables

The eZ80L92 Module

The eZ80L92 Module is a compact, high-performance Ethernet module specially designed for the rapid development and deployment of embedded systems requiring control and Internet/Intranet connectivity.

This low-cost, expandable module is powered by ZiLOG's latest power-efficient, high-speed, optimized pipeline architecture eZ80L92 device (eZ80L925048MOD), a member of ZILOG's new eZ80® microprocessor family.

The eZ80L92 microprocessor is a high-speed single-cycle instruction-fetch microprocessor, which can operate with a clock speed of 48MHz. It can operate in Z80-compatible addressing mode (64KB) or full 24-bit addressing mode (16MB).

The rich peripheral set of the eZ80L92 Module makes it suitable for a variety of applications, including industrial control, IrDA connectivity, communication, security, automation, point-of-sale terminals, and embedded networking applications.

Module Features

- eZ80L92 MPU default factory operating clock frequency at 48MHz
- 10Base-T Ethernet Media Access Controller+ PHI with Onboard RJ45 connector
- 512KB zero-wait-state onboard SRAM
- 1MB onboard NOR Flash ROM (90–100ns)
- GoldCap backup for Real-Time Clock
- I/O connector provides 24 general-purpose 5V-tolerant I/O pinouts
- ZiLOG's industry-leading IrDA transceiver—ZiLOG ZHX1810
- In-circuit Flash programming circuitry
- Onboard connector provides I^2C 2-wire SDA/SCL interface
- Onboard connector provides I/O bus for external peripheral connections (IRQ, CS, 24 address, 8 data)
- Low-cost adaptation to carrier board via two 2x25pin (2.54mm) headers
- Horizontal or vertical mounting onto the eZ80® Development Platform
- Small footprint 64x64mm; height is 24mm
- 3.3V power supply
- Standard operating temperature range: 0ºC to +70ºC

eZ80L92 Processor Features

- Single-cycle instruction fetch, high-performance, pipelined eZ80® CPU core
- Low power features including SLEEP mode, HALT mode, and selective peripheral power-down control
- Two UARTs with independent baud rate generators
- SPI with independent clock rate generator
- I^2C with independent clock rate generator
- Infrared Data Association (IrDA)-compliant infrared encoder/decoder
- New DMA-like eZ80® instructions for efficient block data transfer
- Glueless external memory interface with 4 chip selects, individual wait state generators, and an external WAIT input pin—supports Intel- and Motorola-style buses
- Fixed-priority vectored interrupts (both internal and external) and interrupt controller
- Real-time clock with on-chip 32KHz oscillator, selectable 50/60Hz input, and separate V_{DD} pin for battery backup
- Six 16-bit Counter/Timers with prescalers and direct input/output drive
- Watch-Dog Timer
- 24 bits of general-purpose I/O
- JTAG and ZDI debug interfaces
- 100-pin LQFP package
- 3.0–3.6V supply voltage with 5V tolerant inputs
- Standard operating temperature range: 0ºC to +70ºC

Note: All signals with an $\overline{\text{overline}}$ are active Low. For example, B/$\overline{W}$, for which WORD is active Low, and B/W, for which BYTE is active Low.

Block Diagram

Figure 1 illustrates a block diagram of the eZ80L92 Module.

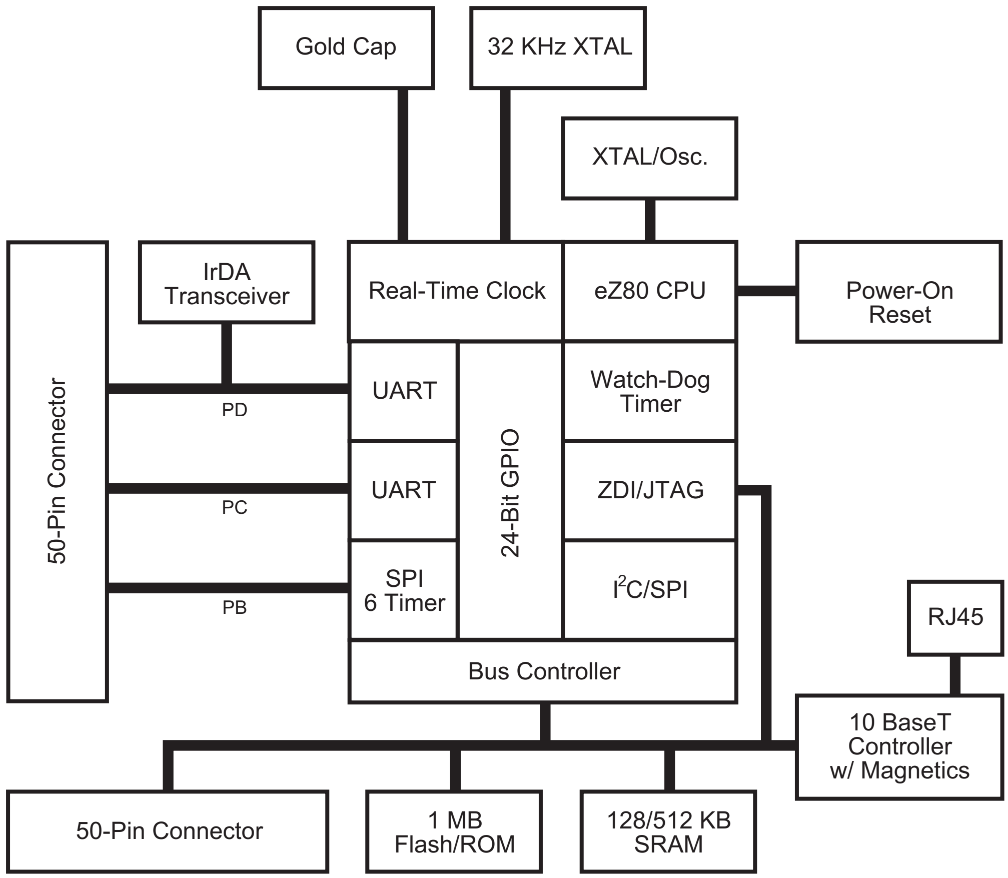

Figure 1. eZ80L92 Module Functional Block Diagram

Pin Description

Peripheral Bus Connector

Figure 2 illustrates the pin layout of the 50-pin I/O Connector, located at position JP1 on the eZ80L92 Module. Table 1 describes the pins and their functions.

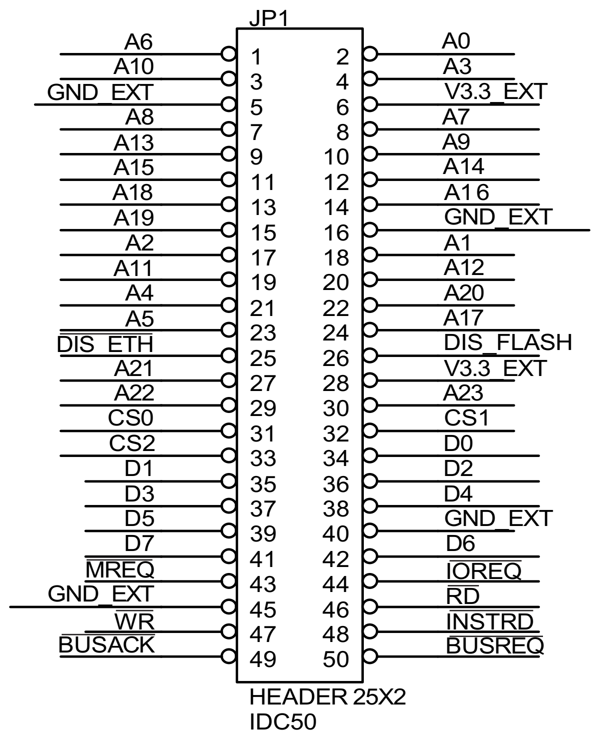

Figure 2. eZ80L92 Module Peripheral Bus Connector Pin Configuration

Table 1. eZ80L92 Module Peripheral Bus Connector Pin Identification* (Continued)

Pin #	Symbol	Pull Up/Down*	Signal Direction	Comments
44	$\overline{\text{IORQ}}$		Bidirectional	
45	GND			V_{SS}/Ground (0V).
46	$\overline{\text{RD}}$		Bidirectional	
47	$\overline{\text{WR}}$		Bidirectional	
48	$\overline{\text{INSTRD}}$		Output	
49	$\overline{\text{BUSACK}}$	PU 10KΩ	Output	
50	$\overline{\text{BUSREQ}}$	PU 10KΩ	Input	

Notes: *External capacitive loads on $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{IORQ}}$, $\overline{\text{MREQ}}$, D0–D7 and A0–A23 should be below 10pF to satisfy timing requirements for the eZ80® CPU.
All unused inputs should be pulled to either V_{DD} or GND, depending on their inactive levels to reduce power consumption and to reduce noise sensitivity.
To prevent EMI, the EZ80CLK output can be deactivated via software in the eZ80L92 Peripheral Power-Down Register.
All inputs are CMOS level 3.3V (5V tolerant), except where otherwise noted.

I/O Connector

Figure 3 illustrates the pin layout of the 50-pin I/O Connector, located at position JP2 of the eZ80L92 Module. Table 2 describes the pins and their functions.

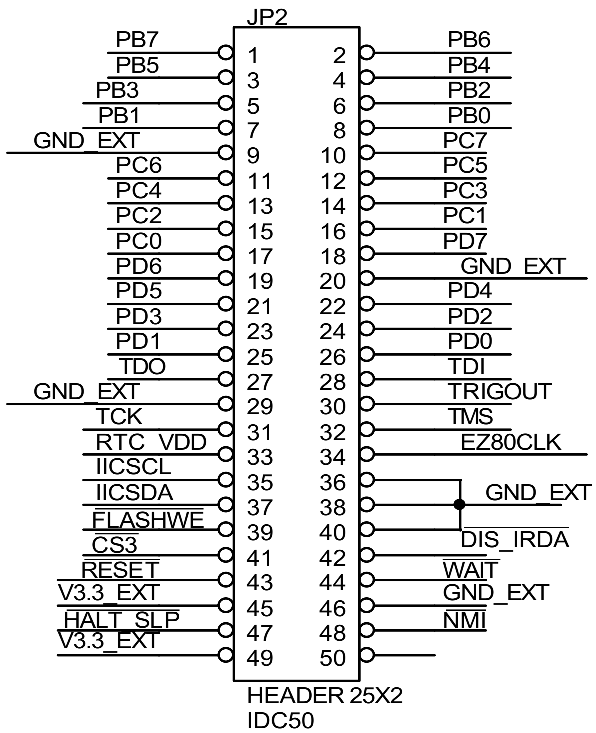

Figure 3. eZ80L92 Module I/O Connector Pin Configuration

Table 2. eZ80L92 Module I/O Connector Pin Identification*

Pin #	Symbol	Pull Up/Down	Signal Direction	Comments
1	PB7		Bidirectional	
2	PB6		Bidirectional	

Notes: *External capacitive loads on $\overline{RD}$, $\overline{WR}$, $\overline{IORQ}$, $\overline{MREQ}$, D0–D7 and A0–A23 should be below 10pF to satisfy timing requirements for the CPU.
All unused inputs should be pulled to either V_{DD} or GND, depending on their inactive levels, to reduce power consumption and to reduce noise sensitivity.
To prevent EMI, the EZ80CLK output can be deactivated via software in the eZ80F91 Peripheral Power-Down Register.
All inputs are CMOS level 3.3V (5V tolerant), except where otherwise noted.

Table 2. eZ80L92 Module I/O Connector Pin Identification* (Continued)

Pin #	Symbol	Pull Up/Down	Signal Direction	Comments
27	TDO		Output	JTAG data output pin.
28	TDI/ZDA	PU 10KΩ	Input	JTAG data input pin.
29	GND			V_{SS}/Ground (0V).
30	TRIGOUT		Output	Active High trigger event indicator.
31	TCK/ZCL	PU 10KΩ	Input	JTAG clock. High on reset enables ZDI mode; Low on reset enables OCI debug.
32	TMS	PU 10KΩ	Input	JTAG Test Mode Select.
33	RTC_V_{DD}			RTC supply from GoldCap (or external battery).
34	EZ80CLK		Output	48MHz synchronous CPU clock.
35	SCL	PU 4k7	Bidirectional	I^2C Bus Clock.
36	GND			V_{SS}/Ground (0V).
37	SDA	PU 4k7	Bidirectional	I^2C Bus Data.
38	GND			V_{SS}/Ground (0V).
39	$\overline{\text{FlashWE}}$	PU 10KΩ	Input	Low enables Write to onboard Flash memory. If this pin is unconnected, the Flash memory is write-protected.
40	GND			V_{SS}/Ground (0V).
41	$\overline{\text{CS3}}$		Output	Used on module for CS8900 EMAC.
42	$\overline{\text{DIS\_IRDA}}$	PU 10KΩ	Input	Low disables onboard IRDA transceiver to use PD0/PD1 UART pins externally.
43	$\overline{\text{RESET}}$	PU 2k2	Bidirectional	Reset output from Module or push-button reset.
44	$\overline{\text{WAIT}}$	PU 2k2	Input	Driving the $\overline{\text{WAIT}}$ pin Low forces the eZ80® CPU to provide additional clock cycles for an external peripheral or external memory to complete its Read or Write operation.
45	V_{DD}			3.3V supply input pin.

Notes: *External capacitive loads on $\overline{\text{RD}}$, $\overline{\text{WR}}$, $\overline{\text{IORQ}}$, $\overline{\text{MREQ}}$, D0–D7 and A0–A23 should be below 10pF to satisfy timing requirements for the CPU.
All unused inputs should be pulled to either V_{DD} or GND, depending on their inactive levels, to reduce power consumption and to reduce noise sensitivity.
To prevent EMI, the EZ80CLK output can be deactivated via software in the eZ80F91 Peripheral Power-Down Register.
All inputs are CMOS level 3.3V (5V tolerant), except where otherwise noted.

Onboard Component Description

Logic-Level I/Os

The I/O connector features 24 general-purpose 3.3V CMOS I/O pins that can be used as outputs or inputs interfacing to external logic. All I/Os are 5V tolerant. Some of the General-Purpose I/O pins support dual mode functions (SPI, Timer I/O, UARTs and bit I/O with edge- or level-triggered interrupt functions on each pin). For more information on eZ80L92 dual modes, please refer to the eZ80L92 Product Specification (PS0130).

Onboard Battery Backup

An onboard 0.1F capacitor (GoldCap) is used to bridge power outages of 2–4 hours if the power supply to the module is disconnected. The capacitor is charged to 3.1V during normal operation and is discharged through the on-chip Real Time Clock. The V_{RTC} pin is available on the I/O connector of the module to connect external components to a power supply or to a larger GoldCap.

Caution: Do not connect a Lithium Battery to the GoldCap capacitor, because onboard charging circuitry for the capacitor can destroy the lithium battery.

Ethernet Media Access Controller

The eZ80L92 Module contains a CS8900A EMAC (MAC, PHI, and RAM) which is attached to the data/address bus of the processor. This chip is connected to the processor's CS3 Chip Select, A0–A3, D0–D7, RD, WR, and PD4 pins for interrupt purposes. Connection of pins PD6 and PD7 for LANACT (wake-up from sleep) and SLEEP is optional and resistor-selectable onboard (see below).

Ethernet LEDs

There are two green LEDs, a Link LED and a LAN LED, that are located adjacent to each other on the eZ80L92 Module. A flashing LAN LED (top) indicates received link pulses from the 10Base-T Ethernet. This LAN LED should be ON if RX+ is connected to TX+ and RX– is connected to TX–. A steady Link LED (bottom) indicates Traffic (RX or TX) on the LAN.

the module is required for this function. In this case, the PD6 pin is not available for GPIO on the I/O connector.

EMAC Ports

Chip Select CS3 is used for selecting the EMAC via I/O decoding. The I/O base address is user-selectable. The EMAC is connected as an 8- or 16-bit device with 8-word-wide I/O registers:

EMAC Wait States

The CS8900A EMAC should be operated in Intel bus mode so that the setup and hold times for the I/O access are met. For 48 MHz operation, first set CS3_BMC (I/O address `0xF3h`) to `84h` (Intel bus mode with four system clock cycles per bus cycle) and then CS3_CTL (I/O Address `0xB3`) to `18h` (0 wait states for I/O). For a 20.8 ns CPU Clock cycle time, the Read and Write access time is:

2 x 4 x 20.8 ns–16 ns (for capacitive and chip delays) = 150 ns

Memory

The eZ80L92 Module offers SRAM and Flash memories and the wait states that support memory operations, as described in this section.

Wait States

To ensure that valid data is read from or written to slower memories, a number of wait states must be inserted into the memory or I/O access operations by the processor. The number of wait states that are required should be added by programming the chip select control registers. To calculate the minimum number of wait states required, refer to Table 4.

Table 4. Chip Frequency to Wait State Cycle Time Calculation

MHz	Cycle Time
12	83.3 ns
20	50.0 ns
24	41.7 ns
36	27.8 ns
40	25.0 ns
48	20.8 ns

Static RAM

The eZ80L92 Module features 512KB of fast SRAM. Access speed is typically 12ns or faster, allowing zero-wait-state operation at 48MHz. With the CPU at 48MHz, onboard SRAM can be accessed with zero wait states in eZ80 mode. CS1_CTL (chip select CS1) can be set to `08h` (no wait states).

Flash Memory

The Flash Boot Loader, application code, and user configuration data are held permanently in NOR Flash memory. A typical application requires eight times more ROM for code than RAM. As an example, for 128KB onboard SRAM, 1MB of ROM is required. The eZ80L92 Module allows NOR Flash memories between 4megabits (512KB) and 32 megabits (4MB) to be used. The chips are housed in wide TSOP40 cases. Flash ROM access times are 55–150ns; typically 90ns.

NOR Flash should be operated in Intel bus mode to satisfy setup and hold times and to prevent bus contention with a Write cycle that could possibly follow. For proper CPU operation at 48MHz, first set the bus mode control register CS0_BMC (I/O address `0xF0h`) to `82h`, then set the Chip Select Control register CS0_CTL (I/O address `0xAAh`) to `08h`. These settings select Intel Bus Mode with two system clocks per bus cycle and zero wait states.

IrDA Transceiver

An onboard IrDA transceiver (ZiLOG ZHX1810) is connected to PD0 (TX), PD1 (RX), and PD2 (Shutdown, R_SD). The IrDA transceiver is of the LED type 870nm Class 1.

The receiver supply current is 90–150µA and the transmitter supply current is 260mA when the LED is active.The IrDA transceiver is accessible via the IrDA controller attached to UART0 on the eZ80L92 device. The UART0 console and the IrDA transceiver cannot be used simultaneously.

To use the UART0 for console or to save power, the transceiver can be disabled by the software or by an off-board signal when using the proper jumper selection. The transceiver is disabled by setting PD2 (IR_SD) High or by pulling the DIS_IRDA pin on the I/O connector Low. The shutdown is used for power savings. To enable the IrDA transceiver, DIS_IRDA is left floating and PD2 is set to Low.

Reset Generator

The onboard Reset Generator Chip performs reliable Power-On Reset. The chip generates a reset pulse with a duration of 200ms if the power supply drops below

2.93V. This reset pulse ensures that the board always starts in a defined condition. The RESET pin on the I/O connector reflects the status of the RESET line. It is a bidirectional pin for resetting external peripheral components or for resetting the eZ80L92 Module with a low-impedance output (e.g. a 100-Ohm pushbutton).

Serial Interface Ports

The processor contains two 16550-style UARTs with programmable baud rate generators. UART0 is typically used for console I/O and initial boot code upload or to connect remote peripherals that can be controlled and monitored via Ethernet. UART0 is connected to GPIO PD[0:3] on the I/O connector. There are no RS232-level shifters on the eZ80L92 Module.

Note: Do not connect an RS-232 interface without level shifters.

UART1 can be used for modem attachment or as a communications port to a host computer, where the embedded Ethernet module emulates an AT-style modem for internet access. UART1 does not offer onboard RS232-level shifters.

Physical Dimensions

The size of the eZ80L92 Module PCB is 64x64mm. With an RJ45 Ethernet connector, the overall height is 25mm, as shown in Figure 4.

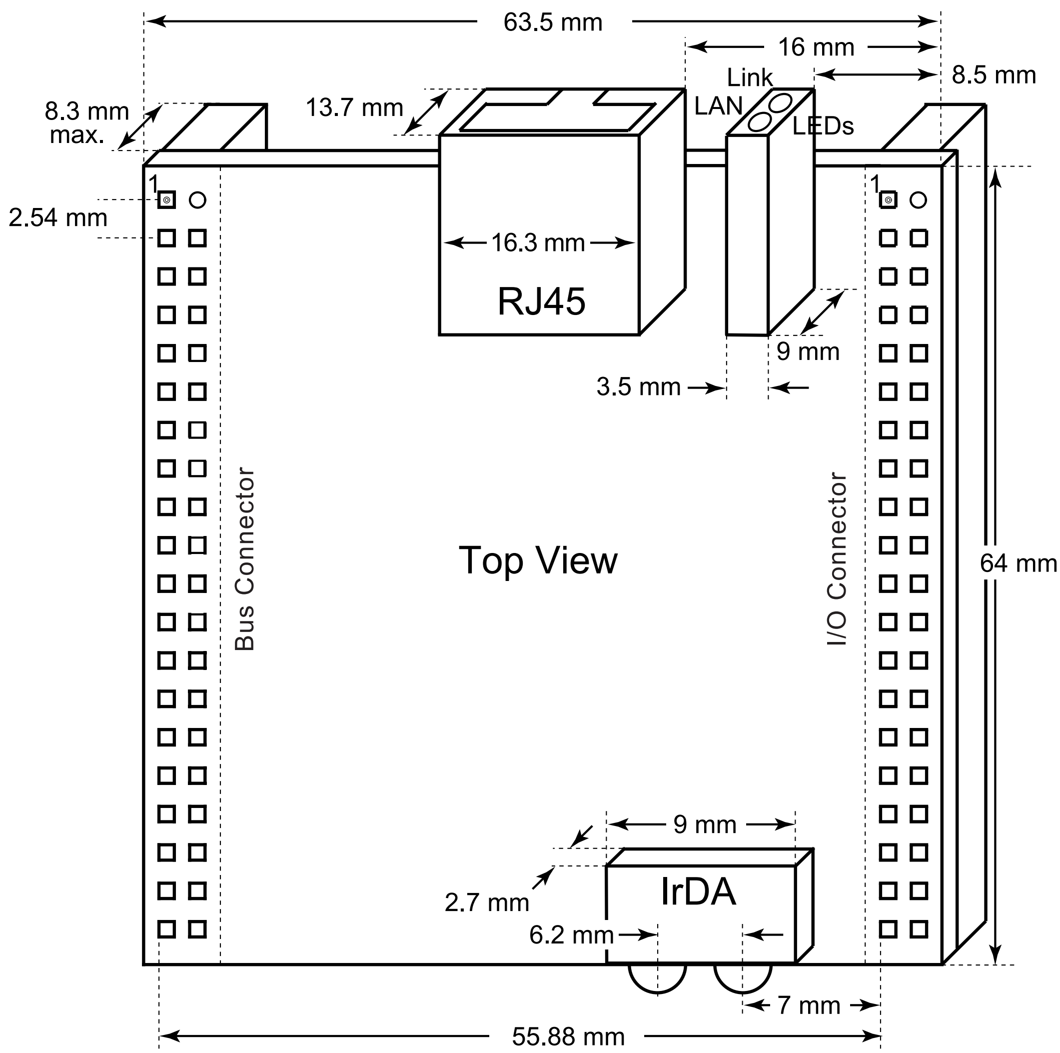

Figure 4. Dimension Drawing

Mounting the Module onto the eZ80® Development Platform

The eZ80L92 Module can be mounted in several positions. Depending on volume and area restrictions, it can be mounted horizontally or vertically with or without components between the connectors on the eZ80® Development Platform. See Figure 8 for examples.

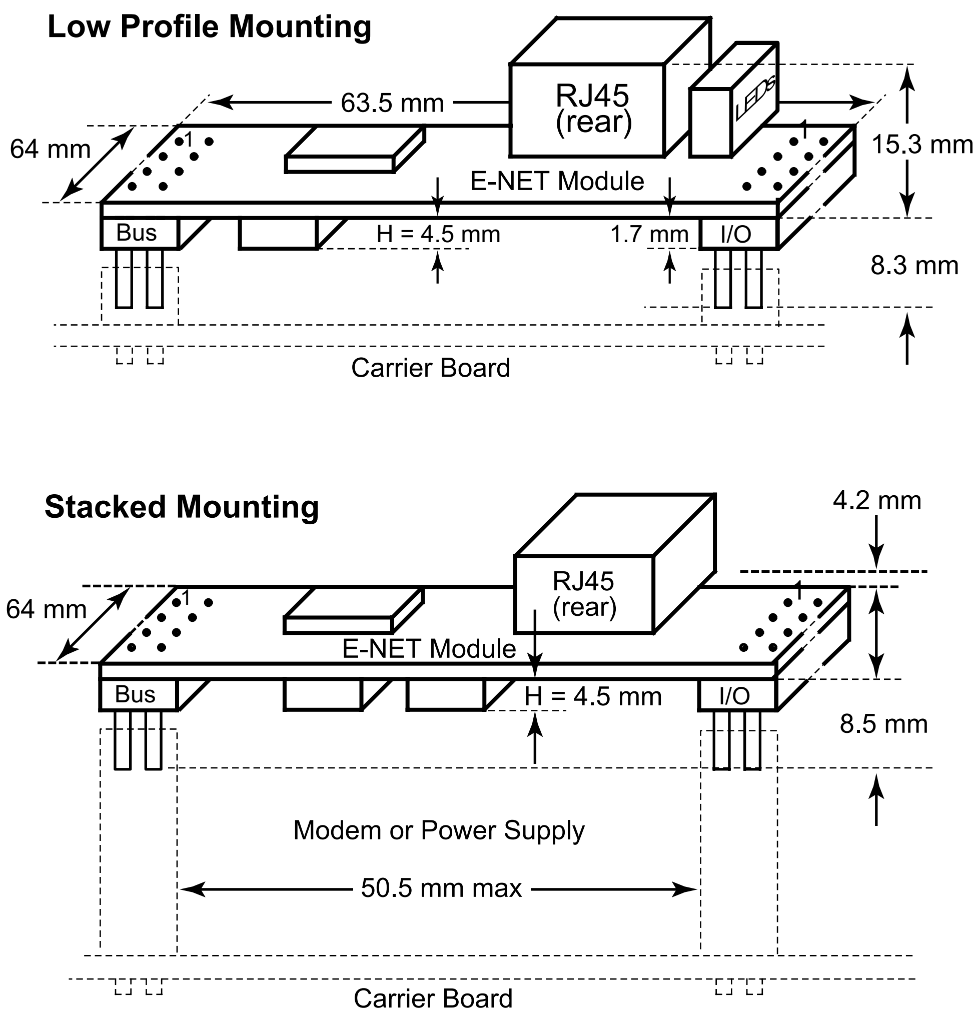

Figure 7. Mounting Examples

ESD/EMI Protection

Caution: The eZ80L92 Module is a component that is intended to be part of a system design for end-user devices. Therefore, the user must exercise caution to use ESD protection on the I/O pins.

The EMAC can be additionally protected by placing an ESD protection array on the eZ80L92 Module at position U9. Either use ESDA25B1 from ST Microelectronics or LCDA15C-6 from Semtech. A mounting hole on the board can be used for grounding the shield of the Ethernet RJ45 jack to prevent surge or ESD currents from flowing through the digital circuitry.

The RJ45 Ethernet Connector on the eZ80L92 Module contains a transformer and common mode chokes for EMI suppression.

Caution: CMOS I/Os are ESD-sensitive and must be handled with care. Handling of the module should be performed in ESD-safe environments (for example with a wrist-wrap attached). When developing applications, the user must provide for proper ESD protection on external, user-accessible I/Os (e.g. suppressor arrays for the I/Os).

The components are mounted on a multilayer PCB to provide a stable ground plane for onboard components. The module features several GND pins next to pins with higher switching frequency for short ground returns. If unused, the clock output can be separated from the module header by removing a series resistor on the module. Removing the series resistor further reduces electromagnetic emissions.

Absolute Maximum Ratings

Stresses greater than those listed in Table 5 can cause permanent damage to the device. These ratings are stress ratings only. Operation of the device at any condition outside those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. For improved reliability, unused inputs should be tied to one of the supply voltages (V_{DD} or V_{SS}).

Table 5. Absolute Maximum Ratings

Parameter	Min	Max	Units
Standard operating temperature	0	+70	ºC
Storage temperature	–45	+85	ºC
Operating Humidity (RH @ 50ºC)	25%	90%	
Operating Voltage (±5%)	—	3.3	V

Power Supply

The eZ80L92 Module requires a regulated external 3.3VDC/0.5A power supply. You may use a Low Dropout Regulator (LDO) to get 3.3V from 5V or use the following switcher circuit to generate 3.3V from unregulated 10-28V power supply.

Power connections follow these conventional descriptions:

Connection	Circuit	Device
Power	V_{CC}	V_{DD}
Ground	GND	V_{SS}

Figure 8 offers two typical power supply examples.

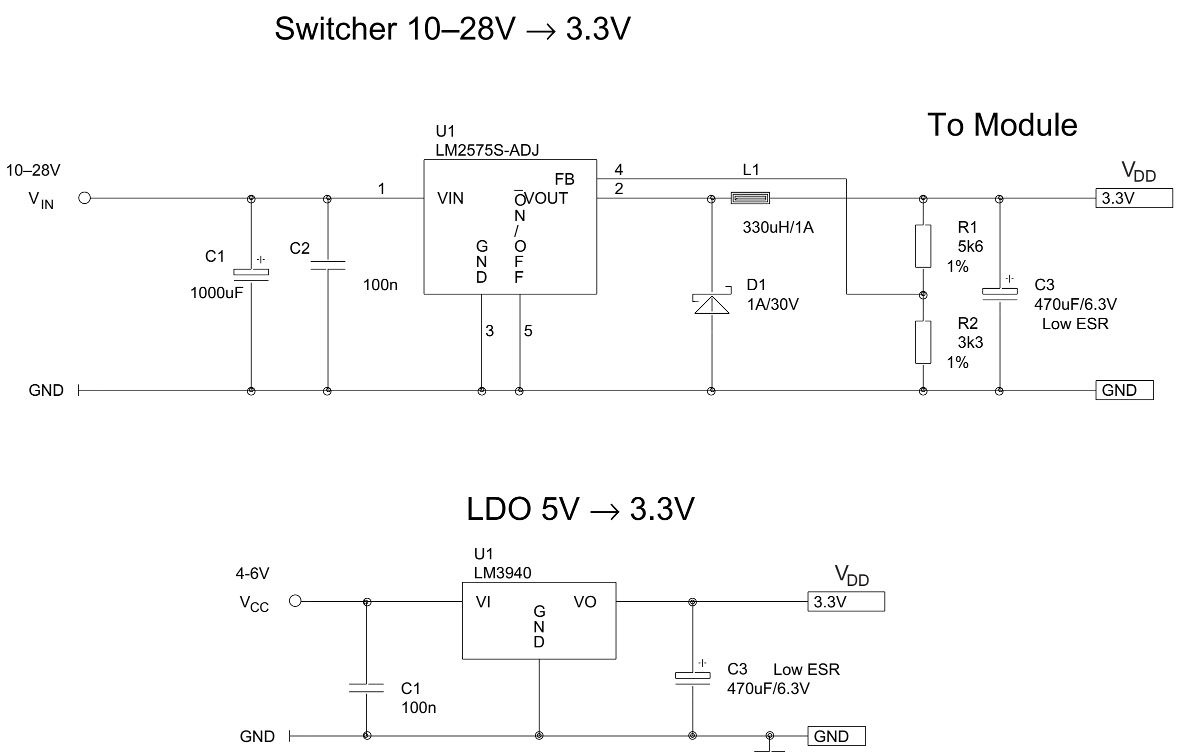

Figure 8. Power Supply Examples

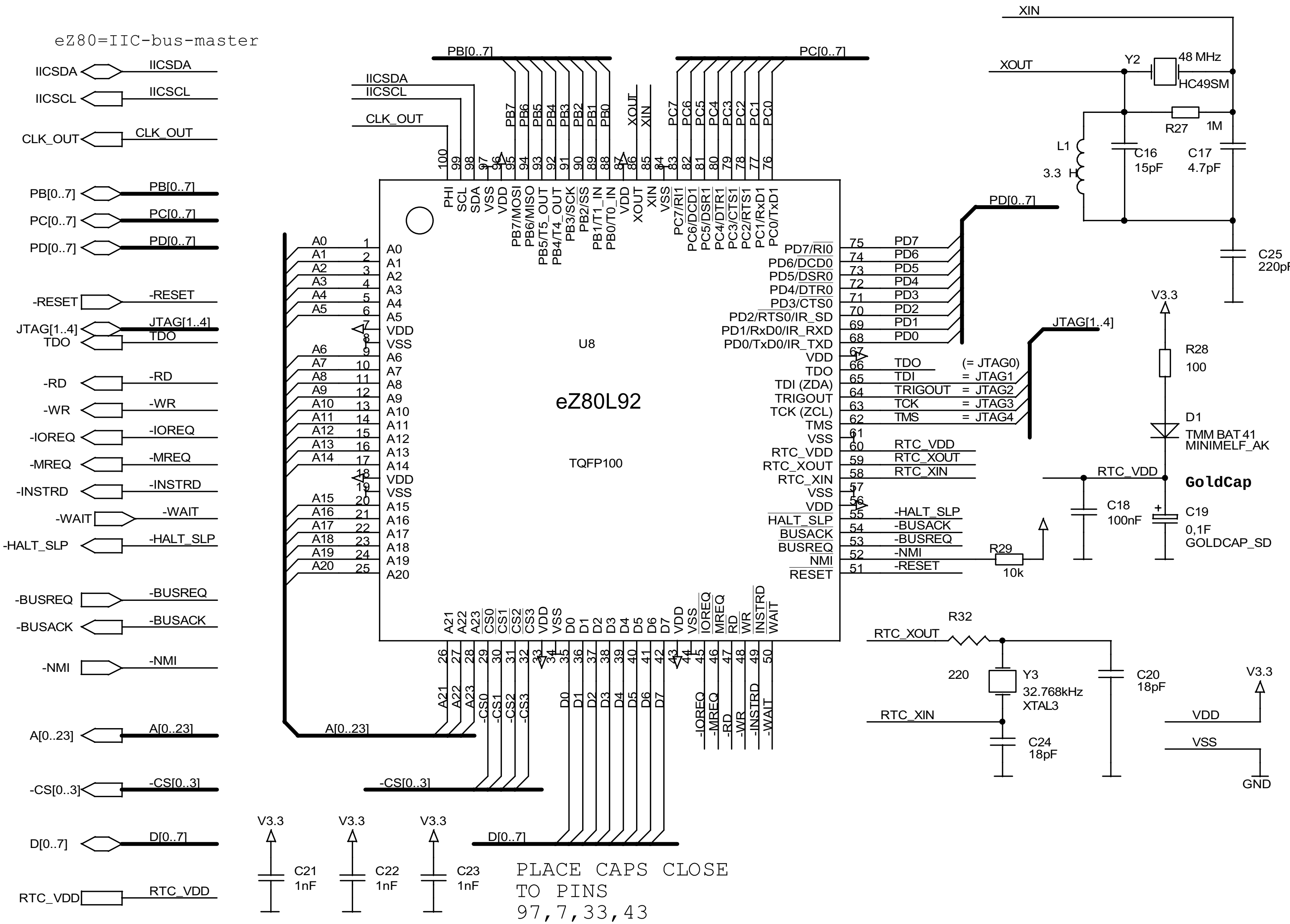

Figure 10. eZ80L92 Module Schematic Diagram, #2 of 9—100-Pin QFP eZ80L92 Device

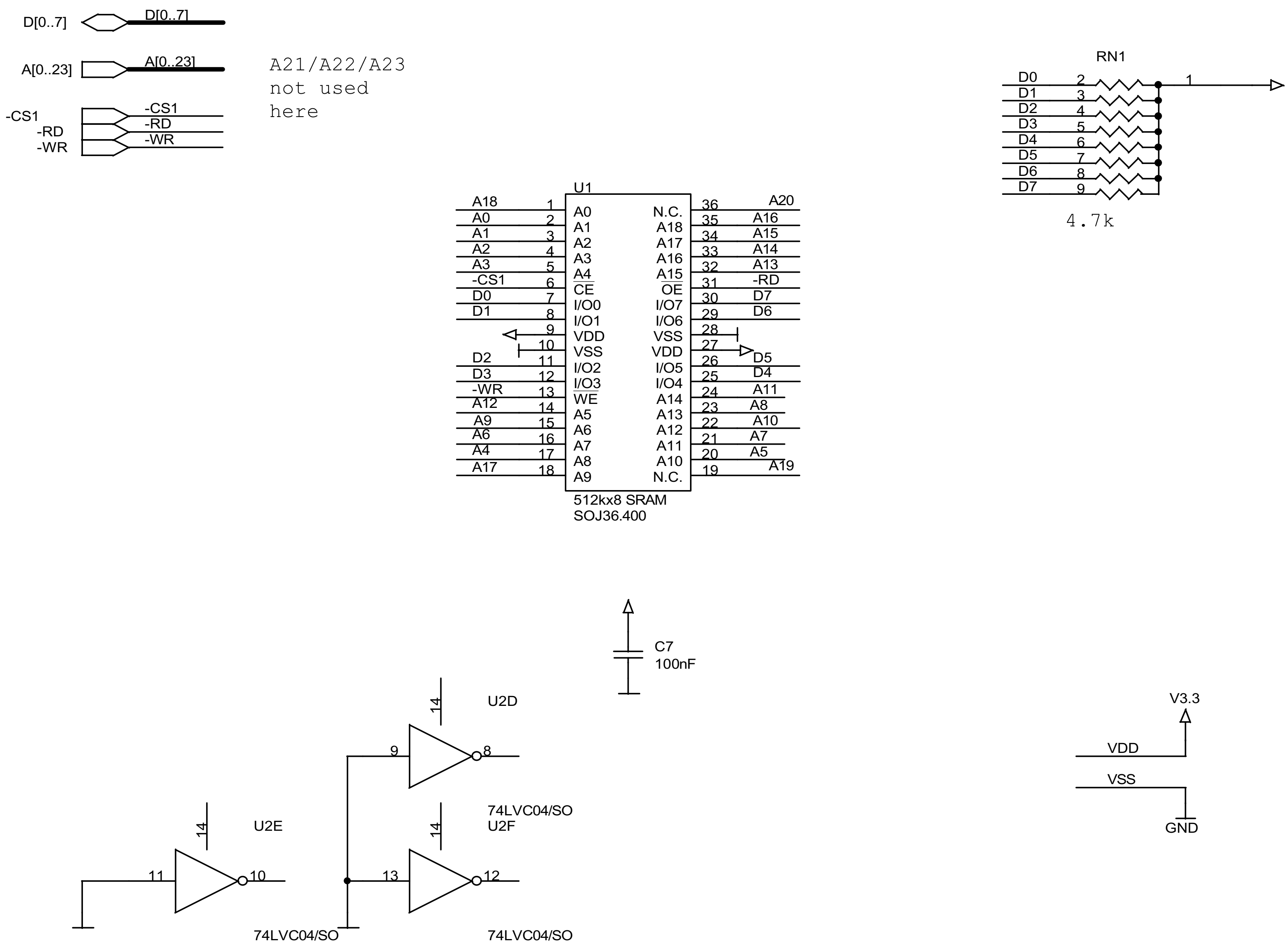

Figure 11. eZ80L92 Module Schematic Diagram, #3 of 9—36-Pin SRAM Device

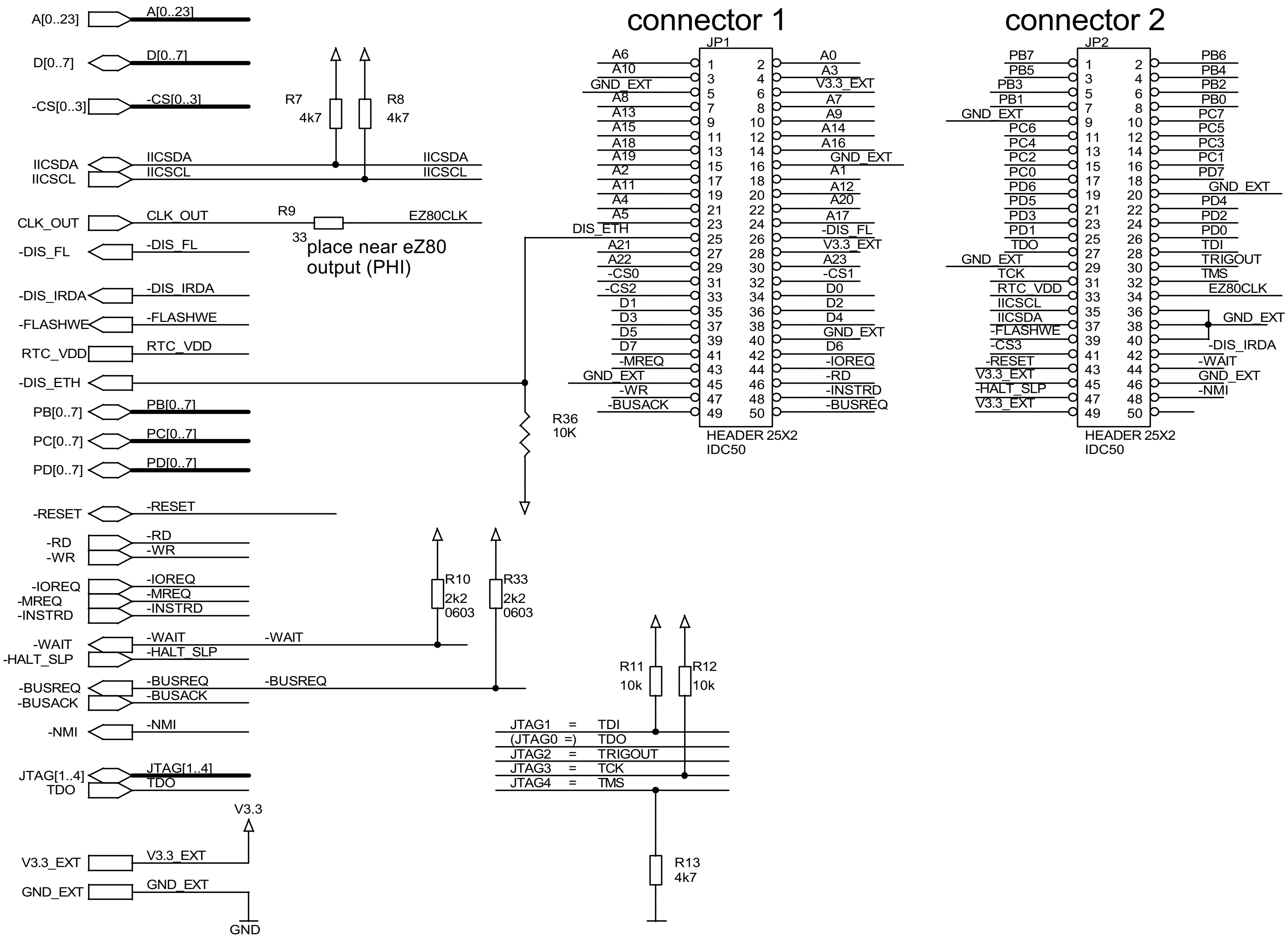

Figure 15. eZ80L92 Module Schematic Diagram, #7 of 9—Headers

Customer Feedback Form

The eZ80L92 Module Product Specification

If you experience any problems while operating this product, or if you note any inaccuracies while reading this Product Specification, please copy and complete this form, then mail or fax it to ZiLOG (see *Return Information*, below). We also welcome your suggestions!

Customer Information

Name	Country
Company	Phone
Address	Fax
City/State/Zip	Email

Product Information

Serial # or Board Fab #/Rev. #
Software Version
Document Number
Host Computer Description/Type

Return Information

ZiLOG
System Test/Customer Support
532 Race Street
San Jose, CA 95126
Phone: (408) 558-8500
Fax: (408) 558-8536
ZiLOG Customer Support

Problem Description or Suggestion

Provide a complete description of the problem or your suggestion. If you are reporting a specific problem, include all steps leading up to the occurrence of the problem. Attach additional pages as necessary.