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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	-
Number of Cores/Bus Width	-
Speed	-
Co-Processors/DSP	-
RAM Controllers	-
Graphics Acceleration	-
Display & Interface Controllers	-
Ethernet	-
SATA	-
USB	-
Voltage - I/O	-
Operating Temperature	-
Security Features	-
Package / Case	-
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8314cvradda

- Signal (RCK) can be configured as either input or output
- Frame sync and data signals can be programmed to be sampled either on the rising edge or on the falling edge of the clock
- Frame sync can be programmed as active low or active high
- Selectable delay (0–3 bits) between the Frame Sync signal and the beginning of the frame
- MSB or LSB first support

2.7 USB Dual-Role Controller

The USB controller includes the following features:

- Designed to comply with *USB Specification, Rev. 2.0*
- Supports operation as a stand-alone USB device
  - Supports one upstream facing port
  - Supports three programmable USB endpoints
- Supports operation as a stand-alone USB host controller
  - Supports USB root hub with one downstream-facing port
  - Enhanced host controller interface (EHCI) compatible
- Supports high-speed (480 Mbps), full-speed (12 Mbps), and low-speed (1.5 Mbps) operation. Low-speed operation is supported only in host mode.
- Supports UTMI+ low pin interface (ULPI) or on-chip USB-2.0 full-speed/high-speed PHY
- Supports USB on-the-go mode, which includes both device and host functionality, when using an external ULPI PHY

2.8 Dual PCI Express Interfaces

The PCI Express interfaces have the following features:

- PCI Express 1.0a compatible
- x1 link width
- Selectable operation as root complex or endpoint
- Both 32- and 64-bit addressing
- 128-byte maximum payload size
- Support for MSI and INTx interrupt messages
- Virtual channel 0 only
- Selectable Traffic Class
- Full 64-bit decode with 32-bit wide windows
- Dedicated descriptor based DMA engine per interface with separate read and write channels

2.13 DMA Controller, I^{2}C, DUART, Enhanced Local Bus Controller (eLBC), and Timers

The integrated four-channel DMA controller includes the following features:

- Allows chaining (both extended and direct) through local memory-mapped chain descriptors (accessible by local masters)
- Misaligned transfer capability for source/destination address
- Supports external DREQ, DACK and DONE signals

There is one I^{2}C controller. This synchronous, multi-master buses can be connected to additional devices for expansion and system development.

The DUART supports full-duplex operation and is compatible with the PC16450 and PC16550 programming models. 16-byte FIFOs are supported for both the transmitter and the receiver.

The eLBC port allows connections with a wide variety of external DSPs and ASICs. Three separate state machines share the same external pins and can be programmed separately to access different types of devices. The general-purpose chip select machine (GPCM) controls accesses to asynchronous devices using a simple handshake protocol. The three user programmable machines (UPMs) can be programmed to interface to synchronous devices or custom ASIC interfaces. Each chip select can be configured so that the associated chip interface can be controlled by the GPCM or UPM controller. Both may exist in the same system. The local bus can operate at up to 66 MHz.

The system timers include the following features: periodic interrupt timer, real time clock, software watchdog timer, and two general-purpose timer blocks.

3 Electrical Characteristics

This section provides the AC and DC electrical specifications and thermal characteristics for the MPC8314E, which is currently targeted to these specifications. Some of these specifications are independent of the I/O cell, but they are included for complete reference. These are not purely I/O buffer design specifications.

3.1 Overall DC Electrical Characteristics

This section covers the ratings, conditions, and other characteristics.

3.1.1 Absolute Maximum Ratings

This table provides the absolute maximum ratings.

Table 1. Absolute Maximum Ratings [1]

Characteristic	Symbol	Max Value	Unit	Note
Core supply voltage	VDD	–0.3 to 1.26	V	—
PLL supply voltage	AVDD	–0.3 to 1.26	V	—
DDR1 DRAM I/O supply voltage	GVDD	–0.3 to 2.7	V	—

Table 9. RESET Initialization Timing Specifications (continued)

Note:
1. $t_{PCI\_SYNC\_IN}$ is the clock period of the input clock applied to PCI_SYNC_IN. When the device is In PCI host mode the primary clock is applied to the SYS_CLK_IN input, and PCI_SYNC_IN period depends on the value of CFG_SYS_CLKIN_DIV.
2. $t_{SYS\_CLK\_IN}$ is the clock period of the input clock applied to SYS_CLK_IN. It is only valid when the device is in PCI host mode.
3. POR configuration signals consists of CFG_RESET_SOURCE[0:3] and CFG_SYS_CLKIN_DIV.
4. The parameter names CFG_SYS_CLKIN_DIV and CFG_CLKIN_DIV are used interchangeably in this document.

This table provides the PLL lock times.

Table 10. PLL Lock Times

Parameter/Condition	Min	Max	Unit	Note
System PLL lock times	—	100	μs	—
e300 core PLL lock times	—	100	μs	—
SerDes (SGMII/PCI Exp Phy) PLL lock times	—	100	μs	—
USB phy PLL lock times	—	100	μs	—

7 DDR and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface of the MPC8314E. Note that DDR SDRAM is GVDD(typ) = 2.5 V and DDR2 SDRAM is GVDD(typ) = 1.8 V.

7.1 DDR and DDR2 SDRAM DC Electrical Characteristics

This table provides the recommended operating conditions for the DDR2 SDRAM component(s) of the MPC8314E when GVDD(typ) = 1.8 V.

Table 11. DDR2 SDRAM DC Electrical Characteristics for GVDD(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Note
I/O supply voltage	GVDD	1.7	1.9	V	1
I/O reference voltage	MVREF	0.49 × GVDD	0.51 × GVDD	V	2
I/O termination voltage	V_{TT}	MVREF – 0.04	MVREF + 0.04	V	3
Input high voltage	V_{IH}	MVREF+ 0.125	GVDD + 0.3	V	—
Input low voltage	V_{IL}	–0.3	MVREF – 0.125	V	—
Output leakage current	I_{OZ}	–9.9	9.9	μA	4
Output high current (V_{OUT} = 1.420 V, GVDD= 1.7V)	I_{OH}	–13.4	—	mA	—
Output low current (V_{OUT} = 0.280 V)	I_{OL}	13.4	—	mA	

Note:
1. GVDD is expected to be within 50 mV of the DRAM GVDD at all times.
2. MVREF is expected to be equal to 0.5 × GVDD, and to track GVDD DC variations as measured at the receiver. Peak-to-peak noise on MVREF may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MVREF. This rail should track variations in the DC level of MVREF.
4. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GVDD.

Table 20. DDR and DDR2 SDRAM Output AC Timing Specifications (continued)

At recommended operating conditions

Parameter	Symbol [1]	Min	Max	Unit	Note
$\overline{\text{MCS}}$[n] output hold with respect to MCK 266 MHz 200 MHz	t_{DDKHCX}	 3.15 4.20	 — —	ns	3
MCK to MDQS Skew	t_{DDKHMH}	–0.6	0.6	ns	4
MDQ//MDM output setup with respect to MDQS 266 MHz 200 MHz	t_{DDKHDS}, t_{DDKLDS}	 900 1000	 — —	ps	5
MDQ//MDM output hold with respect to MDQS 266 MHz 200 MHz	t_{DDKHDX}, t_{DDKLDX}	 1100 1200	 — —	ps	5
MDQS preamble start	t_{DDKHMP}	$-0.5 \times t_{MCK} - 0.6$	$-0.5 \times t_{MCK} + 0.6$	ns	6
MDQS epilogue end	t_{DDKHME}	–0.6	0.6	ns	6

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, t_{DDKHAS} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, t_{DDKLDX} symbolizes DDR timing (DD) for the time t_{MCK} memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals ±0.1 V.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ//MDM/MDQS.
4. Note that t_{DDKHMH} follows the symbol conventions described in note 1. For example, t_{DDKHMH} describes the DDR timing (DD) from the rising edge of the MCK[n] clock (KH) until the MDQS signal is valid (MH). t_{DDKHMH} can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This is typically set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these 2 parameters have been set to the same adjustment value. See the *MPC8315E PowerQUICC II Pro Integrated Host Processor Family Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the microprocessor.
6. All outputs are referenced to the rising edge of MCK[n] at the pins of the microprocessor. Note that t_{DDKHMP} follows the symbol conventions described in note 1.

9.2.1.2 MII Receive AC Timing Specifications

This table provides the MII receive AC timing specifications.

Table 26. MII Receive AC Timing Specifications

At recommended operating conditions with LVDD of 3.3 V ± 300 mv

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
RX_CLK clock period 10 Mbps	t_{MRX}	—	400	—	ns
RX_CLK clock period 100 Mbps	t_{MRX}	—	40	—	ns
RX_CLK duty cycle	t_{MRXH}/t_{MRX}	35	—	65	%
RXD[3:0], RX_DV, RX_ER setup time to RX_CLK	t_{MRDVKH}	10.0	—	—	ns
RXD[3:0], RX_DV, RX_ER hold time to RX_CLK	t_{MRDXKH}	10.0	—	—	ns
RX_CLK clock rise V_{IL}(min) to V_{IH}(max)	t_{MRXR}	1.0	—	4.0	ns
RX_CLK clock fall time V_{IH}(max) to V_{IL}(min)	t_{MRXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MRDVKH} symbolizes MII receive timing (MR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{MRX} clock reference (K) going to the high (H) state or setup time. Also, t_{MRDXKL} symbolizes MII receive timing (GR) with respect to the time data input signals (D) went invalid (X) relative to the t_{MRX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{MRX} represents the MII (M) receive (RX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. The frequency of RX_CLK should not exceed the TX_CLK by more than 300 ppm

This figure provides the AC test load for eTSEC.

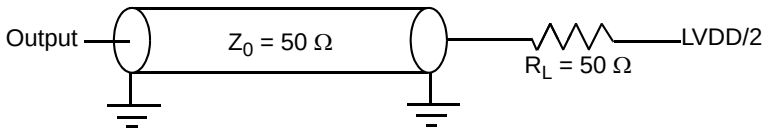


Figure 10. eTSEC AC Test Load

This figure shows the MII receive AC timing diagram.

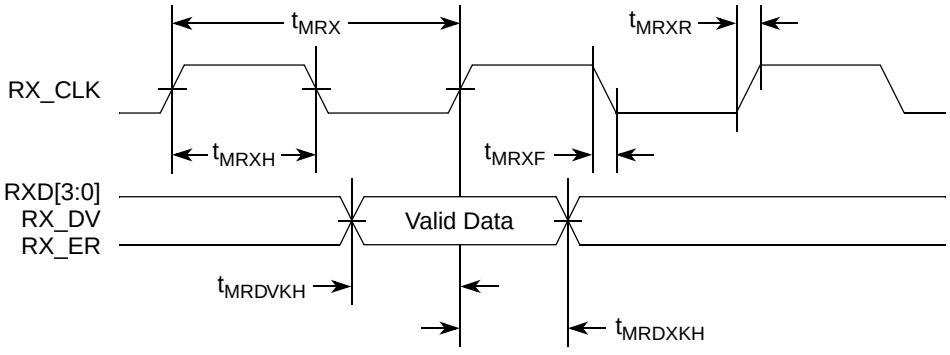


Figure 11. MII Receive AC Timing Diagram RMII AC Timing Specifications

Table 29. RGMII and RTBI AC Timing Specifications (continued)

At recommended operating conditions (see Table 2)

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
Clock cycle duration [3]	t_{RGT}	7.2	8.0	8.8	ns
Duty cycle for 1000Base-T [4, 5]	t_{RGTH}/t_{RGT}	45	50	55	%
Duty cycle for 10BASE-T and 100BASE-TX [3, 5]	t_{RGTH}/t_{RGT}	40	50	60	%
Rise time (20%–80%)	t_{RGTR}	—	—	0.75	ns
Fall time (20%–80%)	t_{RGTF}	—	—	0.75	ns
GTX_CLK125 reference clock period	t_{G12} [6]	—	8.0	—	ns
GTX_CLK125 reference clock duty cycle	t_{G125H}/t_{G125}	47	—	53	%

Note:

1. Note that, in general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the RTBI (T) receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. This implies that PC board design requires clocks to be routed so that an additional trace delay of greater than 1.5 ns is added to the associated clock signal.
3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
5. Duty cycle reference is LVDD/2.
6. This symbol is used to represent the external GTX_CLK125 and does not follow the original symbol naming convention. GTX_CLK supply voltage is fixed at 3.3V inside the chip. If PHY supplies a 2.5 V Clock signal on this input, set TSCOMOBI bit of System I/O configuration register (SICRH) as 1. See the *MPC8315E PowerQUICC II Pro Integrated Host Processor Family Reference Manual*.
7. The frequency of RX_CLK should not exceed the TX_CLK by more than 300 ppm

Table 33. 1588 Timer AC Specifications (continued)

Parameter	Symbol	Min	Max	Unit	Note

Note:
1. The timer can operate on rtc_clock or tmr_clock. These clocks get muxed and any one of them can be selected.
2. Asynchronous signals.
3. Inputs need to be stable at least one TMR clock.

9.5 SGMII Interface Electrical Characteristics

Each SGMII port features a 4-wire AC-Coupled serial link from the dedicated SerDes interface of MPC8315E as shown in Figure 17, where C_{TX} is the external (on board) AC-Coupled capacitor. Each output pin of the SerDes transmitter differential pair features 50-Ω output impedance. Each input of the SerDes receiver differential pair features 50-Ω on-die termination to XCOREVSS. The reference circuit of the SerDes transmitter and receiver is shown in Figure 48.

When an eTSEC port is configured to operate in SGMII mode, the parallel interface's output signals of this eTSEC port can be left floating. The input signals should be terminated based on the guidelines described in Section 25.4, "Connection Recommendations," as long as such termination does not violate the desired POR configuration requirement on these pins, if applicable.

When operating in SGMII mode, the TSEC_GTX_CLK125 clock is not required for this port. Instead, SerDes reference clock is required on SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ pins.

9.5.1 DC Requirements for SGMII SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$

The characteristics and DC requirements of the separate SerDes reference clock are described in Section 15, "High-Speed Serial Interfaces (HSSI)."

9.5.2 AC Requirements for SGMII SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$

This table lists the SGMII SerDes reference clock AC requirements. Please note that SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ are not intended to be used with, and should not be clocked by, a spread spectrum clock source.

Table 34. SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ AC Requirements

Symbol	Parameter Description	Min	Typical	Max	Unit	Note
t_{REF}	REFCLK cycle time	—	8	—	ns	—
t_{REFCJ}	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles	—	—	100	ps	—
t_{REFPJ}	Phase jitter. Deviation in edge location with respect to mean edge location	–50	—	50	ps	—

9.5.3 SGMII Transmitter and Receiver DC Electrical Characteristics

Table 35 and Table 36 describe the SGMII SerDes transmitter and receiver AC-coupled DC electrical characteristics. Transmitter DC characteristics are measured at the transmitter outputs (SD_TX[n] and $\overline{\text{SD\_TX[n]}}$) as depicted in Figure 16.

Table 36. SGMII DC Receiver Electrical Characteristics (continued)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Input AC common mode voltage	$V_{CM\_ACp\text{-}p}$	—	—	100	mV	5
Receiver differential input impedance	Z_{RX_DIFF}	80	100	120	Ω	—
Receiver common mode input impedance	Z_{RX_CM}	20	—	35	Ω	—
Common mode input voltage	V_{CM}	—	$V_{xcorevss}$	—	V	6

Note:
1. Input must be externally AC-coupled.
2. $V_{RX\_DIFFp\text{-}p}$ is also referred to as peak to peak input differential voltage
3. The concept of this parameter is equivalent to the Electrical Idle Detect Threshold parameter in PCI Express. Refer to PCI Express Differential Receiver (RX) Input Specifications section for further explanation.
4. The EQ shown in the table refers to the RXEQA or RXEQE bit field of MPC8315E's SerDes Control Register 0.
5. $V_{CM\_ACp\text{-}p}$ is also referred to as peak to peak AC common mode voltage.
6. On-chip termination to XCOREVSS.

9.5.4 SGMII AC Timing Specifications

This section describes the SGMII transmit and receive AC timing specifications. Transmitter and receiver characteristics are measured at the transmitter outputs (TX[n] and $\overline{\text{TX}}$[n]) or at the receiver inputs (RX[n] and $\overline{\text{RX}}$[n]) as depicted in Figure 20 respectively.

9.5.4.1 SGMII Transmit AC Timing Specifications

This table provides the SGMII transmit AC timing targets. A source synchronous clock is not provided.

Table 37. SGMII Transmit AC Timing Specifications

At recommended operating conditions with XCOREVDD = 1.0V ± 5%.

Parameter	Symbol	Min	Typ	Max	Unit	Note
Deterministic Jitter	JD	—	—	0.17	UI p-p	—
Total Jitter	JT	—	—	0.35	UI p-p	—
Unit Interval	UI	799.92	800	800.08	ps	—
V_{OD} fall time (80%-20%)	tfall	50	—	120	ps	—
V_{OD} rise time (20%-80%)	t_{rise}	50	—	120	ps	—

Note:
1. Each UI is 800 ps ± 100 ppm.

9.5.4.2 SGMII Receive AC Timing Specifications

This table provides the SGMII receive AC timing specifications. Source synchronous clocking is not supported. Clock is recovered from the data. Figure 19 shows the SGMII Receiver Input Compliance Mask eye diagram.

Table 41. USB_CLK_IN DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
Input high voltage	V_{IH}	2.7	NV_{DD} + 0.3	V
Input low voltage	V_{IL}	–0.3	0.4	V

This table provides the USB clock input (USB_CLK_IN) AC timing specifications.

Table 42. USB_CLK_IN AC Timing Specifications

Parameter/Condition	Conditions	Symbol	Min	Typical	Max	Unit
Frequency range	—	$f_{USB\_CLK\_IN}$	—	24	—	MHz
Clock frequency tolerance	—	t_{CLK_TOL}	–0.005	0	0.005	%
Reference clock duty cycle	Measured at 1.6 V	t_{CLK_DUTY}	40	50	60	%
Total input jitter/Time interval error	Peak to peak value measured with a second order high-pass filter of 500 KHz bandwidth	t_{CLK_PJ}	—	—	200	ps

11 Local Bus

This section describes the DC and AC electrical specifications for the local bus interface of the MPC8314E.

11.1 Local Bus DC Electrical Characteristics

This table provides the DC electrical characteristics for the local bus interface.

Table 43. DC Electrical Characteristics (when Operating at 3.3 V)

Parameter	Symbol	Min	Max	Unit
Output high voltage (NVDD = min, I_{OH} = –2 mA)	V_{OH}	NVDD – 0.2	—	V
Output low voltage (NVDD = min, I_{OL} = 2 mA)	V_{OL}	—	0.2	V
Input high voltage	V_{IH}	2	NVDD + 0.3	V
Input low voltage	V_{IL}	–0.3	0.8	V
Input high current (V_{IN} = 0 V or V_{IN} = NVDD)	I_{IN}	—	±5	μA

11.2 Local Bus AC Electrical Specifications

This table describes the general timing parameters of the local bus interface of the MPC8314E.

Table 44. Local Bus General Timing Parameters

Parameter	Symbol [1]	Min	Max	Unit	Note
Local bus cycle time	t_{LBK}	15	—	ns	2
Input setup to local bus clock	t_{LBIVKH}	7	—	ns	3, 4

Table 50. PCI AC Timing Specifications at 66 MHz (continued)

Parameter	Symbol [1]	Min	Max	Unit	Note
Input hold from clock	t_{PCIXKH}	0	—	ns	2, 4

Note:

1. Note that the symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.3 Local Bus Specifications*.
3. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. Input timings are measured at the pin.

This table shows the PCI AC Timing Specifications at 33 MHz.

Table 51. PCI AC Timing Specifications at 33 MHz

Parameter	Symbol [1]	Min	Max	Unit	Note
Clock to output valid	t_{PCKHOV}	—	11	ns	2
Output hold from clock	t_{PCKHOX}	2	—	ns	2
Clock to output high impedance	t_{PCKHOZ}	—	14	ns	2, 3
Input setup to clock	t_{PCIVKH}	4.0	—	ns	2, 4
Input hold from clock	t_{PCIXKH}	0	—	ns	2, 4

Note:

1. Note that the symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.3 Local Bus Specifications*.
3. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. Input timings are measured at the pin.

This figure provides the AC test load for PCI.

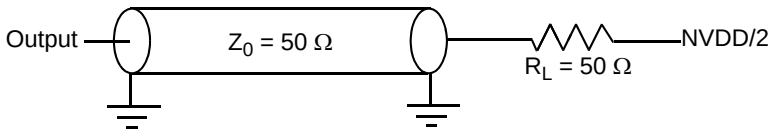


Figure 34. PCI AC Test Load

assumes that the LVPECL clock driver's output impedance is 50Ω. R1 is used to DC-bias the LVPECL outputs prior to AC-coupling. Its value could be ranged from 140Ω to 240Ω depending on clock driver vendor's requirement. R2 is used together with the SerDes reference clock receiver's 50-Ω termination resistor to attenuate the LVPECL output's differential peak level such that it meets the MPC8315E SerDes reference clock's differential input amplitude requirement (between 200mV and 800mV differential peak). For example, if the LVPECL output's differential peak is 900mV and the desired SerDes reference clock input amplitude is selected as 600mV, the attenuation factor is 0.67, which requires R2 = 25Ω. Please consult clock driver chip manufacturer to verify whether this connection scheme is compatible with a particular clock driver chip.

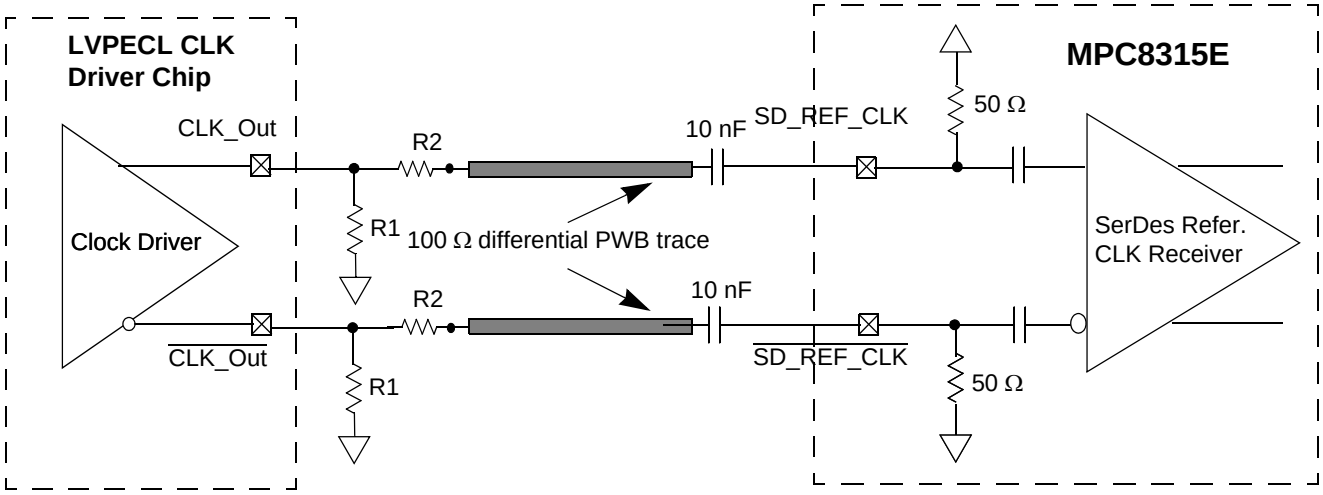


Figure 44. AC-Coupled Differential Connection with LVPECL Clock Driver (Reference Only)

This figure shows the SerDes reference clock connection reference circuits for a single-ended clock driver. It assumes the DC levels of the clock driver are compatible with MPC8315E SerDes reference clock input's DC requirement.

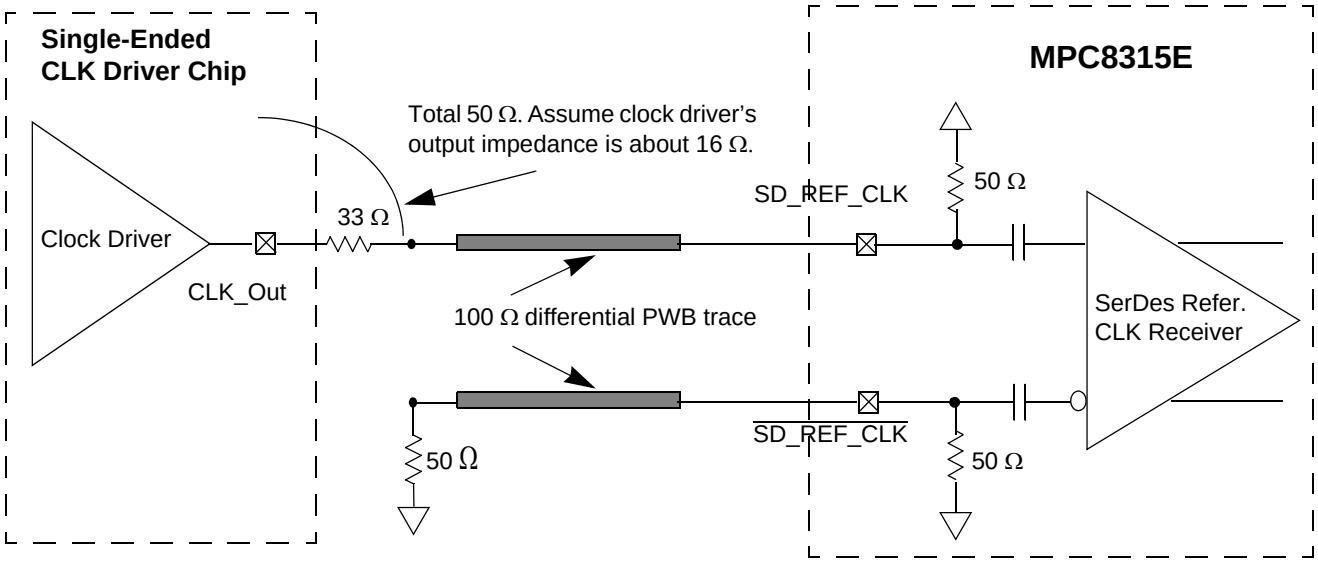


Figure 45. Single-Ended Connection (Reference Only)

16.5 Receiver Compliance Eye Diagrams

The RX eye diagram in Figure 50 is specified using the passive compliance/test measurement load (see Figure 51) in place of any real PCI Express RX component. In general, the minimum receiver eye diagram measured with the compliance/test measurement load (see Figure 51) is larger than the minimum receiver eye diagram measured over a range of systems at the input receiver of any real PCI Express component. The degraded eye diagram at the input Receiver is due to traces internal to the package as well as silicon parasitic characteristics which cause the real PCI Express component to vary in impedance from the compliance/test measurement load. The input receiver eye diagram is implementation specific and is not specified. RX component designer should provide additional margin to adequately compensate for the degraded minimum Receiver eye diagram (shown in Figure 50) expected at the input receiver based on an adequate combination of system simulations and the return loss measured looking into the RX package and silicon. The RX eye diagram must be aligned in time using the jitter median to locate the center of the eye diagram.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

NOTE

The reference impedance for return loss measurements is 50 Ω to ground for both the D+ and D- line (that is, as measured by a Vector Network Analyzer with 50 Ω probes—see Figure 51). Note that the series capacitors, $C_{PEACCTX}$, are optional for the return loss measurement.

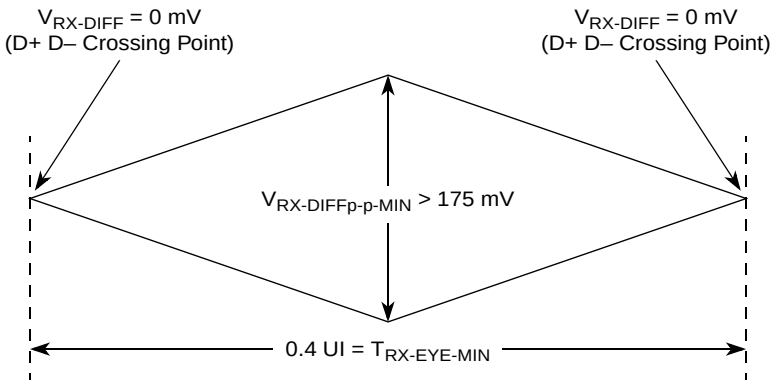


Figure 50. Minimum Receiver Eye Timing and Voltage Compliance Specification

16.5.1 Compliance Test and Measurement Load

The AC timing and voltage parameters must be verified at the measurement point, as specified within 0.2 inches of the package pins, into a test/measurement load shown in Figure 51.

NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D– not being exactly matched in length at the package pin boundary.

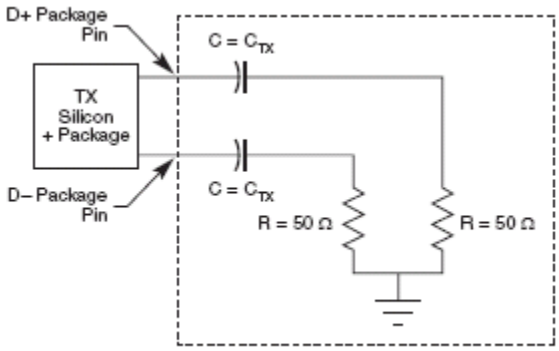


Figure 51. Compliance Test/Measurement Load

17 Timers

This section describes the DC and AC electrical specifications for the timers of the MPC8314E.

17.1 Timers DC Electrical Characteristics

This table provides the DC electrical characteristics for the timers pins, including TIN, $\overline{\text{TOUT}}$, $\overline{\text{TGATE}}$, and RTC_CLK.

Table 56. Timers DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.1	NVDD + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	0 V ≤ V_{IN} ≤ NVDD	—	± 5	μA

17.2 Timers AC Timing Specifications

This table provides the timers input and output AC timing specifications.

Table 57. Timers Input AC Timing Specifications

Characteristic	Symbol [1]	Min	Unit
Timers inputs—minimum pulse width	t_{TIWID}	20	ns

Table 57. Timers Input AC Timing Specifications

Characteristic	Symbol [1]	Min	Unit

Note:
1. Timers inputs and outputs are asynchronous to any visible clock. Timers outputs should be synchronized before use by any external synchronous logic. Timers input are required to be valid for at least t_{TIWID} ns to ensure proper operation.

This figure provides the AC test load for the Timers.

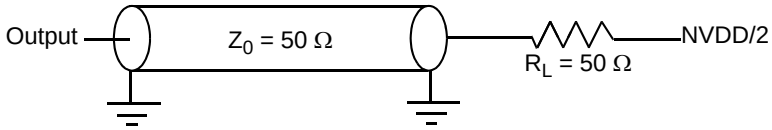


Figure 52. Timers AC Test Load

18 GPIO

This section describes the DC and AC electrical specifications for the GPIO of the MPC8314E.

18.1 GPIO DC Electrical Characteristics

This table provides the DC electrical characteristics for the GPIO.

Table 58. GPIO DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.1	NVDD + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	$0 V \le V_{IN} \le$ NVDD	—	± 5	μA

18.2 GPIO AC Timing Specifications

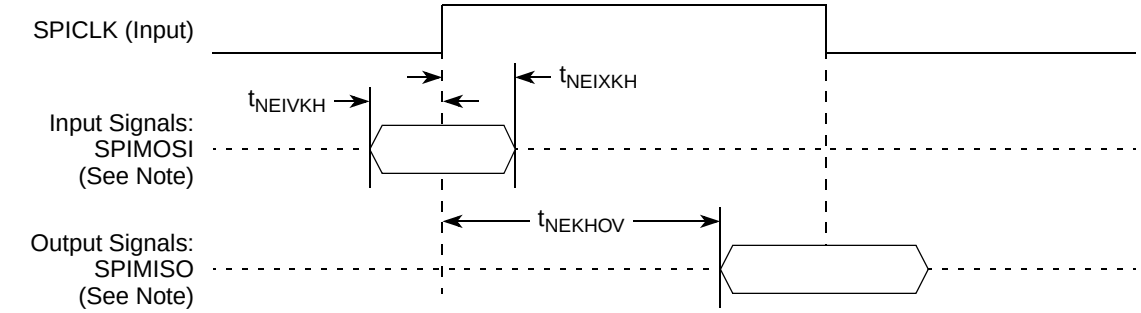
This table provides the GPIO input and output AC timing specifications.

Table 59. GPIO Input AC Timing Specifications

Characteristic	Symbol [1]	Min	Unit
GPIO inputs—minimum pulse width	t_{PIWID}	20	ns

Note:
1. GPIO inputs and outputs are asynchronous to any visible clock. GPIO outputs should be synchronized before use by any external synchronous logic. GPIO inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation.

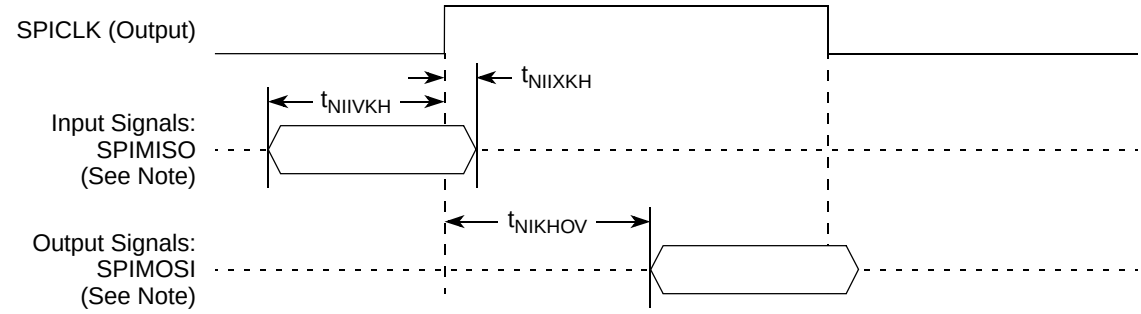
This figure shows the SPI timing in slave mode (external clock).



Note: The clock edge is selectable on SPI.

Figure 55. SPI AC Timing in Slave Mode (External Clock) Diagram

This figure shows the SPI timing in master mode (internal clock).



Note: The clock edge is selectable on SPI.

Figure 56. SPI AC Timing in Master Mode (Internal Clock) Diagram

21 TDM

This section describes the DC and AC electrical specifications for the TDM of the MPC8314E.

21.1 TDM DC Electrical Characteristics

This table provides the DC electrical characteristics TDM.

Table 64. TDM DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.1	NVDD + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	0 V ≤ V_{IN} ≤ NVDD	—	± 5	μA

Table 66. MPC8314E TEPBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
GPIO_1/DMA_DACK1/GTM1_TIN2/GTM2_TIN1	A4	I/O	$NVDD1_{ON}$	—
GPIO_2/DMA_DONE1/GTM1_TGATE2/GTM2_TGATE1	K3	I/O	$NVDD4_{OFF}$	—
GPIO_3/GTM1_TIN3/GTM2_TIN4	K1	I/O	$NVDD4_{OFF}$	—
GPIO_4/GTM1_TGATE3/GTM2_TGATE4	K2	I/O	$NVDD4_{OFF}$	—
GPIO_5/GTM1_TOUT3/GTM2_TOUT1	L5	I/O	$NVDD4_{OFF}$	—
GPIO_6/GTM1_TIN4/GTM2_TIN3	L3	I/O	$NVDD4_{OFF}$	—
GPIO_7/GTM1_TGATE4/GTM2_TGATE3	L1	I/O	$NVDD4_{OFF}$	—
GPIO_8/USBDR_DRIVE_VBUS/GTM1_TIN1/GTM2_TIN2	M1	I/O	$NVDD4_{OFF}$	—
GPIO_9/USBDR_PWRFAULT/GTM1_TGATE1/GTM2_TGATE2	M2	I/O	$NVDD4_{OFF}$	—
GPIO_10/USBDR_PCTL0/GTM1_TOUT2/GTM2_TOUT1	M5	I/O	$NVDD4_{OFF}$	—
GPIO_11/USBDR_PCTL1/GTM1_TOUT4/GTM2_TOUT3	M4	I/O	$NVDD4_{OFF}$	—
SPI				
SPIMOSI/GPIO_15	W3	I/O	$NVDD1_{OFF}$	—
SPIMISO/GPIO_16	W4	I/O	$NVDD1_{OFF}$	—
SPICLK	Y1	I/O	$NVDD1_{OFF}$	—
SPISEL/GPIO_17	W2	I/O	$NVDD1_{OFF}$	—
Power and Ground Supplies				
GVDD	Y11, Y12, Y14, Y15, Y17, AC8, AC11, AC14, AC17, AD6, AD9, AD17, AE8, AE13, AE19, AF10, AF15, AF21, AG2, AG3, AG8, AG13, AG19, AH2	I	—	—
$LVDD1_{OFF}$	H6, J3, L6, L9, M9	I	—	—
$LVDD2_{ON}$	C11, D9, E10, F11, J12	I	—	—
$NVDD1_{OFF}$	U9, V9, W10, Y4, Y6, AA3, AB4	I	—	—
$NVDD1_{ON}$	B1, B2, C1, D5, E7, F5, F9, J11, K10	I	—	—
$NVDD2_{OFF}$	B22, B27, C19, E16, F15, F18, F21, F25, H25, J17, J18, J23, L20, M20	I	—	—
$NVDD2_{ON}$	L26, N19	I	—	—
$NVDD3_{OFF}$	U20, V20, V23, V26, W19, Y18, Y26, AA23, AA25, AC20, AC25, AD23, AE25, AG25, AG27, T27, U27	I	—	—
$NVDD4_{OFF}$	K4, L2, M6, N10	I	—	—

Table 66. MPC8314E TEPBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
VDD	J15, K15, K16, K17, K18, K19, L10, L19, M10, T10, U10, U19, V10, V19, W11, W12, W13, W14, W15, W16, W17, W18, P23, R23, T19, M26, N26, P28, R28, U23, N27	I	—	—
VDDC	J14, K11, K12, K13, K14, M19	I	—	—
VSS	A3, A27, B3, B12, B24, B28, C6, C8, C13, C17, C21, C23, C26, D2, D7, D15, D18, D20, D22, E4, E6, E11, E24, E26, F8, F12, F14, F17, F20, G3, G26, H4, H23, J6, J26, K25, L4, L11, L12, L13, L14, L15, L16, L17, L18, L23, L28, M3, M11, M12, M13, M14, M15, M16, M17, M18, N5, N11, N12, N13, N14, N15, N16, N17, N18, P6, P11, P12, P13, P14, P15, P16, P17, P18, R6, R11, R12, R13, R14, R15, R16, R17, R18, T11, T12, T13, T14, T15, T16, T17, T18, U5, U6, U11, U12, U13, U14, U15, U16, U17, U18, V6, V11, V12, V13, V14, V15, V16, V17, V18, W5, W25, W27, Y2, Y23, AA6, AA27, AB2, AB26, AC5, AC9, AC12, AC18, AC21, AD3, AD14, AD16, AD20, AD26, AE2, AE7, AE11, AE16, AE22, AE24, AF2, AF9, AF12, AF18, AF20, AF23, AF27, AG1, AG5, AG11, AG16, AG22, AG28, AH27, U28,N28, M28, T28, V27, M27, V28, T26, P24, R19, R20, R24, M24, N24, P19, P20, P25, P27, R25, R27, T24	I	—	—
XCOREVDD	P2, P10, R2, T1	I	—	—
XCOREVSS	R3, R10, U2, V2	I	—	—
XPADVDD	P3, R9, U3	I	—	—
XPADVSS	P5, P9, V3	I	—	—

Note:

1. This pin is an open drain signal. A weak pull-up resistor (1 kΩ) should be placed on this pin to NVDD.
2. This pin is an open drain signal. A weak pull-up resistor (2–10 kΩ) should be placed on this pin to NVDD.
3. This output is actively driven during reset rather than being three-stated during reset.
4. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
5. This pin should have a weak pull up if the chip is in PCI host mode. Follow PCI specifications recommendation.
6. This pin must always be tied to VSS.
7. Thermal sensitive resistor.
8. This pin should be connected to USB_VSSA_BIAS through 10K precision resistor.
9. The LB_POR_CFG_BOOT_ECC functionality for this pin is only available in MPC8314E revision 1.1 and later. The LB_POR_CFG_BOOT_ECC is sampled only during the $\overline{\text{PORESET}}$ negation. This pin with an internal pull down resistor enables the ECC by default. To disable the ECC an external strong pull up resistor or a tristate buffer is needed.
10. This pin has a weak internal pull-down.
11. This pin has a weak internal pull-up.

The primary clock source can be one of two inputs, SYS_CLK_IN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. When the device is configured as a PCI host device, SYS_CLK_IN is its primary input clock. SYS_CLK_IN feeds the PCI clock divider (÷2) and the multiplexors for PCI_SYNC_OUT and PCI_CLK_OUT. The $\overline{\text{CFG\_SYS\_CLKIN\_DIV}}$ configuration input selects whether SYS_CLK_IN or SYS_CLK_IN/2 is driven out on the PCI_SYNC_OUT signal.

PCI_SYNC_OUT is connected externally to PCI_SYNC_IN to allow the internal clock subsystem to synchronize to the system PCI clocks. PCI_SYNC_OUT must be connected properly to PCI_SYNC_IN, with equal delay to all PCI agent devices in the system, to allow the device to function. When the device is configured as a PCI agent device, PCI_CLK is the primary input clock. When the device is configured as a PCI agent device the SYS_CLK_IN signal should be tied to GND.

As shown in Figure 60, the primary clock input (frequency) is multiplied up by the system phase-locked loop (PLL) and the clock unit to create the coherent system bus clock (*csb_clk*), the internal clock for the DDR controller (*ddr_clk*), and the internal clock for the local bus interface unit (*lbiu_clk*).

The *csb_clk* frequency is derived from a complex set of factors that can be simplified into the following equation:

$$csb\_clk = \{\text{PCI\_SYNC\_IN} \times (1 + \sim \overline{\text{CFG\_SYS\_CLKIN\_DIV}})\} \times \text{SPMF}$$

In PCI host mode, PCI_SYNC_IN × (1 + ~ $\overline{\text{CFG\_SYS\_CLKIN\_DIV}}$) is the SYS_CLK_IN frequency.

The *csb_clk* serves as the clock input to the e300 core. A second PLL inside the e300 core multiplies up the *csb_clk* frequency to create the internal clock for the e300 core (*core_clk*). The system and core PLL multipliers are selected by the SPMF and COREPLL fields in the reset configuration word low (RCWL) which is loaded at power-on reset or by one of the hard-coded reset options. See Chapter 4, “Reset, Clocking, and Initialization,” in the *MPC8315E PowerQUICC II Pro Integrated Host Processor Family Reference Manual* for more information on the clock subsystem.

The internal *ddr_clk* frequency is determined by the following equation:

$$ddr\_clk = csb\_clk \times (1 + \text{RCWL[DDRCM]})$$

Note that *ddr_clk* is not the external memory bus frequency; *ddr_clk* passes through the DDR clock divider (÷2) to create the differential DDR memory bus clock outputs (MCK and $\overline{\text{MCK}}$). However, the data rate is the same frequency as *ddr_clk*.

The internal *lbiu_clk* frequency is determined by the following equation:

$$lbiu\_clk = csb\_clk \times (1 + \text{RCWL[LBCM]})$$

Note that *lbiu_clk* is not the external local bus frequency; *lbiu_clk* passes through the LBIU clock divider to create the external local bus clock outputs (LCLK[0:1]). The LBIU clock divider ratio is controlled by LCRR[CLKDIV].

In addition, some of the internal units may be required to be shut off or operate at lower frequency than the *csb_clk* frequency. Those units have a default clock ratio that can be configured by a memory mapped register after the device comes out of reset. Table 67 specifies which units have a configurable clock frequency.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum Effective Series Inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of package, without the inductance of vias. Note that the RC filter results in lower voltage level on AVDD. This does not imply that the DC specification can be relaxed.

This figure shows the PLL power supply filter circuit.

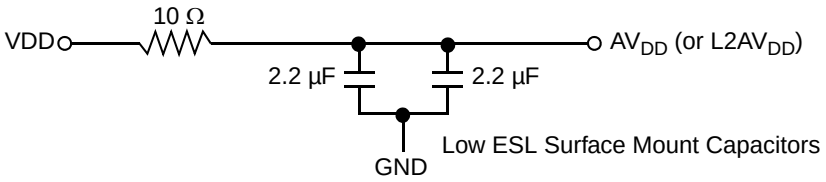


Figure 61. PLL Power Supply Filter Circuit

25.3 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8314E system, and the MPC8314E itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each VDD, NVDD, GVDD, and LVDD pins of the device. These decoupling capacitors should receive their power from separate VDD, NVDD, GVDD, LVDD, and GND power planes in the PCB, utilizing thick and short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the VDD, NVDD, GVDD, and LVDD planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 µF (AVX TPS tantalum or Sanyo OSCON).

25.4 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to NVDD, GVDD, or LVDD as required. Unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected.

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Asia/Pacific:
Freescale Semiconductor China Ltd.
Exchange Building 23F
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Chaoyang District
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China
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