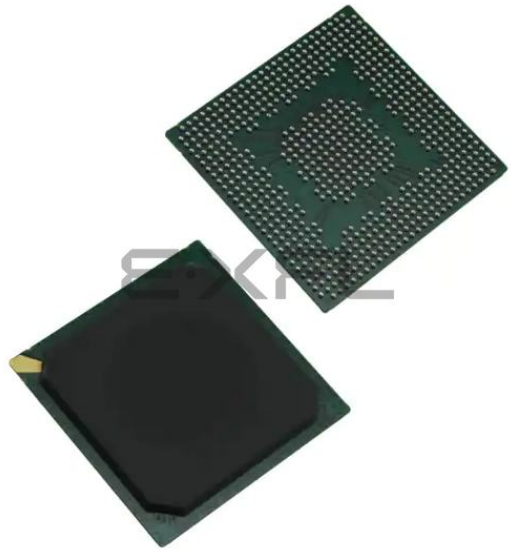

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

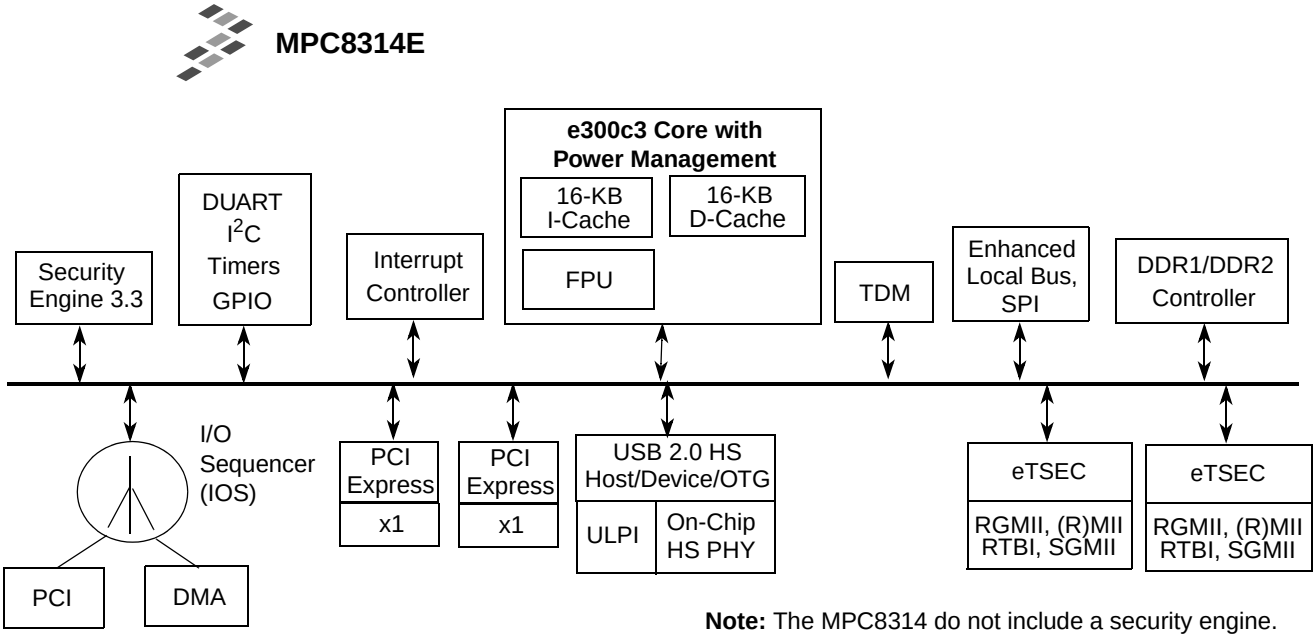
Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	PowerPC e300c3
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	-
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 + PHY (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	-
Package / Case	620-BBGA Exposed Pad
Supplier Device Package	620-HBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8314cvragda

1 Overview

The MPC8314E incorporates the e300c3 (MPC603e-based) core, which includes 16 Kbytes of L1 instruction and data caches, on-chip memory management units (MMUs), and floating-point support. In addition to the e300 core, the SoC platform includes features such as dual enhanced three-speed 10, 100, 1000 Mbps Ethernet controllers (eTSECs) with SGMII support, a 32- or 16-bit DDR1/DDR2 SDRAM memory controller, a security engine to accelerate control and data plane security protocols, and a high degree of software compatibility with previous-generation PowerQUICC processor-based designs for backward compatibility and easier software migration. The MPC8314E also offers peripheral interfaces such as a 32-bit PCI interface with up to 66 MHz operation, 16-bit enhanced local bus interface with up to 66 MHz operation, TDM interface, and USB 2.0 with an on-chip USB 2.0 PHY.

8314E offers additional high-speed interconnect support with dual single-lane PCI Express interfaces. When not used for PCI Express, the SerDes interface may be configured to support SGMII. The MPC8314E security engine (SEC 3.3) allows CPU-intensive cryptographic operations to be offloaded from the main CPU core. This figure shows a block diagram of the MPC8314E.



Note: The MPC8314 do not include a security engine.

Figure 1. MPC8314E Block Diagram

2 MPC8314E Features

The following features are supported in the MPC8314E.

2.1 e300 Core

The e300 core has the following features:

- Operates at up to 400 MHz
- 16-Kbyte instruction cache, 16-Kbyte data cache

3.1.2 Power Supply Voltage Specification

This table provides the recommended operating conditions for theMPC8314E. Note that the values in this table are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 2. Recommended Operating Conditions

Characteristic	Symbol	Recommended Value[1]	Unit	Status in D3 Warm mode	Note
SerDes internal digital power	XCOREVDD	1.0 ± 50 mv	V	Switched Off	—
SerDes internal digital power	XCOREVSS	0.0	V	—	—
SerDes I/O digital power	XPADVDD	1.0 ± 50 mv	V	Switched Off	—
SerDes I/O digital power	XPADVSS	0.0	V	—	—
SerDes analog power for PLL	SDAVDD	1.0 ± 50 mv	V	Switched Off	—
SerDes analog power for PLL	SDAVSS	0.0	V	—	—
Dedicated 3.3 V analog power for USB PLL	USB_PLL_PWR3	3.3 ± 165mv	V	Switched Off	—
Dedicated 1.0 Vanalog power for USB PLL	USB_PLL_PWR1	1.0 ± 50 mv	V	Switched Off	—
Dedicated analog ground for USB PLL	USB_PLL_GND	0.0	V	—	—
Dedicated USB power for USB bias circuit	USB_VDDA_BIAS	3.3 ± 300 mv	V	Switched Off	—
Dedicated USB ground for USB bias circuit	USB_VSSA_BIAS	0.0	V	—	—
Dedicated power for USB transceiver	USB_VDDA	3.3 ± 300 mv	V	Switched Off	—
Dedicated ground for USB transceiver	USB_VSSA	0.0	V	—	—
Core supply voltage	VDD	1.0 ± 50 mv	V	Switched Off	—
Core supply voltage	VDDC	1.0 ± 50 mv	V	Switched On	—
Analog power for e300 core APLL	AVDD1	1.0 ± 50 mv	V	Switched Off	6
Analog power for system APLL	AVDD2	1.0 ± 50 mv	V	Switched On	6
DDR and DDR2 DRAM I/O voltage	GVDD	2.5 ± 200 mv 1.8 ± 100 mv	V	Switched Off	—
Differential reference voltage for DDR and DDR2 controller	MVREF	GVDD /2	V	Switched Off	—
Standard I/O voltage	NVDD1_ON	3.3 ± 300 mv	V	Switched On	1
Standard I/O voltage	NVDD2_ON	3.3 ± 300 mv	V	Switched On	1
Standard I/O voltage	NVDD1_OFF	3.3 ± 300 mv	V	Switched Off	2
Standard I/O voltage	NVDD2_OFF	3.3 ± 300 mv	V	Switched Off	2
Standard I/O voltage	NVDD3_OFF	3.3 ± 300 mv	V	Switched Off	2
Standard I/O voltage	NVDD4_OFF	3.3 ± 300 mv	V	Switched Off	2
eTSEC/USBdr I/O supply	LVDD1_OFF	2.5 ± 125 mv 3.3 ± 300 mv	V	Switched Off	—
eTSEC I/O supply	LVDD2_ON	2.5 ± 125 mv 3.3 ± 300 mv	V	Switched On	—
Analog and digital ground	VSS	0.0	V	—	—
Junction temperature range	T_A/T_J	0 to105	°C	—	3

5.1 DC Electrical Characteristics

This table provides the clock input (SYS_CLK_IN/PCI_SYNC_IN) DC timing specifications for the MPC8314E.

Table 6. SYS_CLK_IN DC Electrical Characteristics

Parameter	Condition	Symbol	Min	Max	Unit
Input high voltage	—	V_{IH}	2.4	NVDD + 0.3	V
Input low voltage	—	V_{IL}	-0.3	0.4	V
SYS_CLK_IN input current	0 V ≤V_{IN} ≤ NVDD	I_{IN}	—	±10	μA
SYS_XTAL_IN input current	0 V ≤V_{IN} ≤ NVDD	I_{IN}	—	±40	μA
PCI_SYNC_IN input current	0 V ≤V_{IN} ≤ NVDD	I_{IN}	—	±10	μA
RTC_CLK input current	0 V ≤V_{IN} ≤ NVDD	I_{IN}	—	±10	μA
USB_CLK_IN input current	0 V ≤ V_{IN} ≤ NVDD	I_{IN}	—	±10	μA
USB_XTAL_IN input current	0 V ≤V_{IN} ≤ NVDD	I_{IN}	—	±40	μA

5.2 AC Electrical Characteristics

The primary clock source for the MPC8314E can be one of two inputs, SYS_CLK_IN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. This table provides the clock input (SYS_CLK_IN/PCI_CLK) AC timing specifications for the MPC8314E.

Table 7. SYS_CLK_IN AC Timing Specifications

Parameter/Condition	Symbol	Min	Typical	Max	Unit	Note
SYS_CLK_IN/PCI_CLK frequency	$f_{SYS\_CLK\_IN}$	24	—	66.67	MHz	1, 6, 7
SYS_CLK_IN/PCI_CLK cycle time	$t_{SYS\_CLK\_IN}$	15	—	41.6	ns	6
SYS_CLK_IN rise and fall time	t_{KH}, t_{KL}	0.6	—	4	ns	2, 6
PCI_CLK rise and fall time	t_{PCH}, t_{PCL}	0.6	0.8	1.2	ns	2
SYS_CLK_IN/PCI_CLK duty cycle	$t_{KHK}/t_{SYS\_CLK\_IN}$	40	—	60	%	3, 6
SYS_CLK_IN/PCI_CLK jitter	—	—	—	±150	ps	4, 5, 6

Note:

1. **Caution:** The system, core, and security block must not exceed their respective maximum or minimum operating frequencies.
2. Rise and fall times for SYS_CLK_IN/PCI_CLK are specified at 20% to 80% of signal swing.
3. Timing is guaranteed by design and characterization.
4. This represents the total input jitter—short term and long term—and is guaranteed by design.
5. The SYS_CLK_IN/PCI_CLK driver's closed loop jitter bandwidth should be <500 kHz at –20 dB. The bandwidth must be set low to allow cascade-connected PLL-based devices to track SYS_CLK_IN drivers with the specified jitter.
6. The parameter names PCI_CLK and PCI_SYNC_IN are used interchangeably in this document.
7. Spread spectrum is allowed up to 1% down-spread at 33kHz.(max. rate).

Table 9. RESET Initialization Timing Specifications (continued)

Note:
1. $t_{PCI\_SYNC\_IN}$ is the clock period of the input clock applied to PCI_SYNC_IN. When the device is In PCI host mode the primary clock is applied to the SYS_CLK_IN input, and PCI_SYNC_IN period depends on the value of CFG_SYS_CLKIN_DIV.
2. $t_{SYS\_CLK\_IN}$ is the clock period of the input clock applied to SYS_CLK_IN. It is only valid when the device is in PCI host mode.
3. POR configuration signals consists of CFG_RESET_SOURCE[0:3] and CFG_SYS_CLKIN_DIV.
4. The parameter names CFG_SYS_CLKIN_DIV and CFG_CLKIN_DIV are used interchangeably in this document.

This table provides the PLL lock times.

Table 10. PLL Lock Times

Parameter/Condition	Min	Max	Unit	Note
System PLL lock times	—	100	μs	—
e300 core PLL lock times	—	100	μs	—
SerDes (SGMII/PCI Exp Phy) PLL lock times	—	100	μs	—
USB phy PLL lock times	—	100	μs	—

7 DDR and DDR2 SDRAM

This section describes the DC and AC electrical specifications for the DDR SDRAM interface of the MPC8314E. Note that DDR SDRAM is GVDD(typ) = 2.5 V and DDR2 SDRAM is GVDD(typ) = 1.8 V.

7.1 DDR and DDR2 SDRAM DC Electrical Characteristics

This table provides the recommended operating conditions for the DDR2 SDRAM component(s) of the MPC8314E when GVDD(typ) = 1.8 V.

Table 11. DDR2 SDRAM DC Electrical Characteristics for GVDD(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Note
I/O supply voltage	GVDD	1.7	1.9	V	1
I/O reference voltage	MVREF	0.49 × GVDD	0.51 × GVDD	V	2
I/O termination voltage	V_{TT}	MVREF – 0.04	MVREF + 0.04	V	3
Input high voltage	V_{IH}	MVREF+ 0.125	GVDD + 0.3	V	—
Input low voltage	V_{IL}	–0.3	MVREF – 0.125	V	—
Output leakage current	I_{OZ}	–9.9	9.9	μA	4
Output high current (V_{OUT} = 1.420 V, GVDD= 1.7V)	I_{OH}	–13.4	—	mA	—
Output low current (V_{OUT} = 0.280 V)	I_{OL}	13.4	—	mA	

Note:
1. GVDD is expected to be within 50 mV of the DRAM GVDD at all times.
2. MVREF is expected to be equal to 0.5 × GVDD, and to track GVDD DC variations as measured at the receiver. Peak-to-peak noise on MVREF may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MVREF. This rail should track variations in the DC level of MVREF.
4. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GVDD.

Table 24. RGMII/RTBI (When Operating at 2.5 V) DC Electrical Characteristics (continued)

Parameters	Symbol	Conditions	Min	Max	Unit

Note:
1. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 1 and Table 2.

9.2 MII, RMII, RGMII, and RTBI AC Timing Specifications

The AC timing specifications for MII, RMII, RGMII, and RTBI are presented in this section.

9.2.1 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

9.2.1.1 MII Transmit AC Timing Specifications

This table provides the MII transmit AC timing specifications.

Table 25. MII Transmit AC Timing Specifications

At recommended operating conditions with LVDD of 3.3 V ± 300 mv.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
TX_CLK clock period 10 Mbps	t_{MTX}	—	400	—	ns
TX_CLK clock period 100 Mbps	t_{MTX}	—	40	—	ns
TX_CLK duty cycle	t_{MTXH}/t_{MTX}	35	—	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX}	1	5	15	ns
TX_CLK data clock rise V_{IL}(min) to V_{IH}(max)	t_{MTXR}	1.0	—	4.0	ns
TX_CLK data clock fall V_{IH}(max) to V_{IL}(min)	t_{MTXF}	1.0	—	4.0	ns

Note:
1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure shows the MII transmit AC timing diagram.

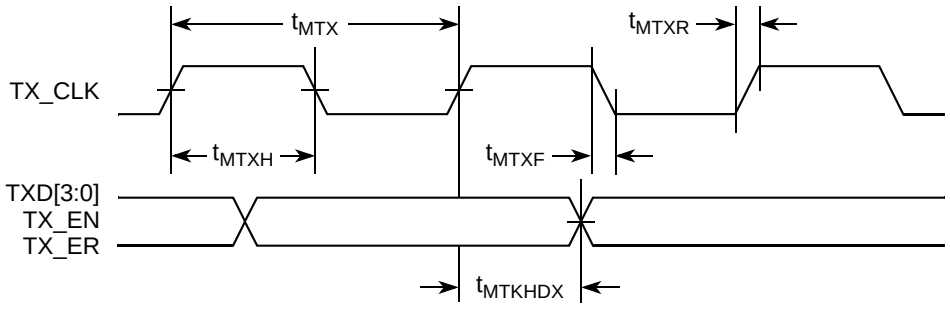


Figure 9. MII Transmit AC Timing Diagram

Table 29. RGMII and RTBI AC Timing Specifications (continued)

At recommended operating conditions (see Table 2)

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
Clock cycle duration [3]	t_{RGT}	7.2	8.0	8.8	ns
Duty cycle for 1000Base-T [4, 5]	t_{RGTH}/t_{RGT}	45	50	55	%
Duty cycle for 10BASE-T and 100BASE-TX [3, 5]	t_{RGTH}/t_{RGT}	40	50	60	%
Rise time (20%–80%)	t_{RGTR}	—	—	0.75	ns
Fall time (20%–80%)	t_{RGTF}	—	—	0.75	ns
GTX_CLK125 reference clock period	t_{G12} [6]	—	8.0	—	ns
GTX_CLK125 reference clock duty cycle	t_{G125H}/t_{G125}	47	—	53	%

Note:

1. Note that, in general, the clock reference symbol representation for this section is based on the symbols RGT to represent RGMII and RTBI timing. For example, the subscript of t_{RGT} represents the RTBI (T) receive (RX) clock. Note also that the notation for rise (R) and fall (F) times follows the clock symbol that is being represented. For symbols representing skews, the subscript is skew (SK) followed by the clock that is being skewed (RGT).
2. This implies that PC board design requires clocks to be routed so that an additional trace delay of greater than 1.5 ns is added to the associated clock signal.
3. For 10 and 100 Mbps, t_{RGT} scales to 400 ns ± 40 ns and 40 ns ± 4 ns, respectively.
4. Duty cycle may be stretched/shrunk during speed changes or while transitioning to a received packet's clock domains as long as the minimum duty cycle is not violated and stretching occurs for no more than three t_{RGT} of the lowest speed transitioned between.
5. Duty cycle reference is LVDD/2.
6. This symbol is used to represent the external GTX_CLK125 and does not follow the original symbol naming convention. GTX_CLK supply voltage is fixed at 3.3V inside the chip. If PHY supplies a 2.5 V Clock signal on this input, set TSCOMOBI bit of System I/O configuration register (SICRH) as 1. See the *MPC8315E PowerQUICC II Pro Integrated Host Processor Family Reference Manual*.
7. The frequency of RX_CLK should not exceed the TX_CLK by more than 300 ppm

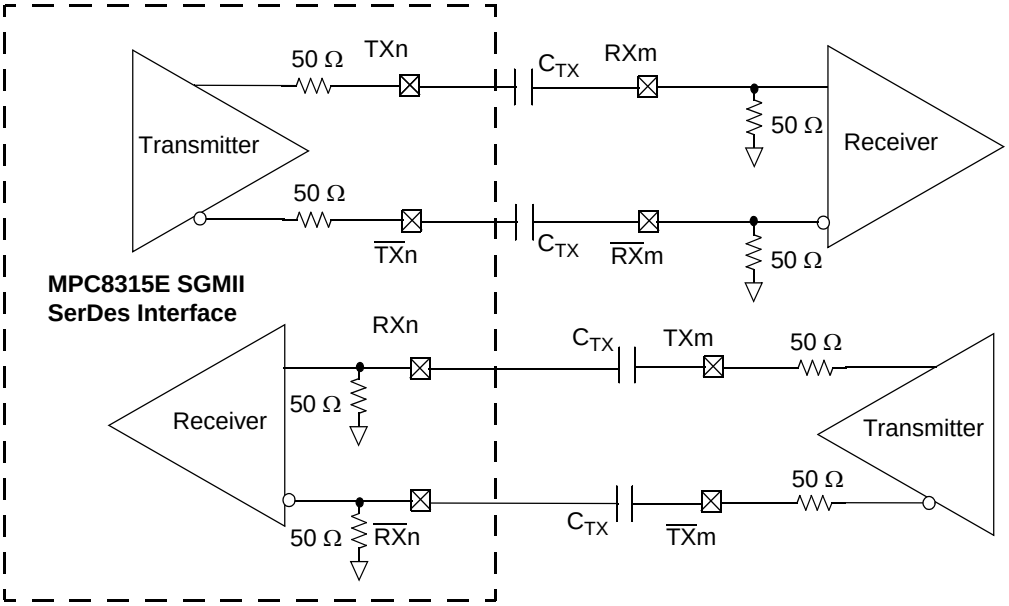


Figure 17. 4-Wire AC-Coupled SGMII Serial Link Connection Example

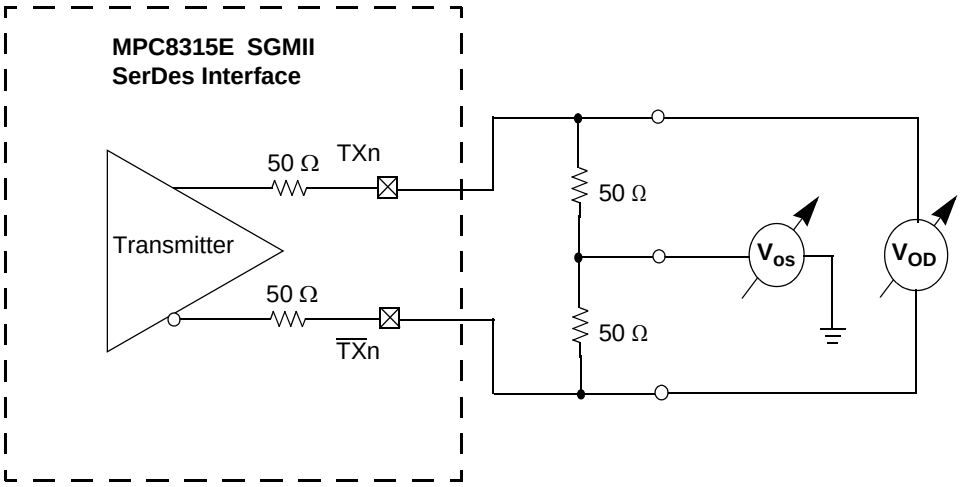


Figure 18. SGMII Transmitter DC Measurement Circuit

Table 36. SGMII DC Receiver Electrical Characteristics

Parameter		Symbol	Min	Typ	Max	Unit	Note
Supply Voltage		XCOREVDD	0.95	1.0	1.05	V	—
DC Input voltage range		—	N/A			—	1
Input differential voltage	EQ = 0	$V_{RX\_DIFFp-p}$	100	—	1200	mV	2, 4
	EQ = 1		175	—			
Loss of signal threshold	EQ = 0	VLOS	30	—	100	mV	3, 4
	EQ = 1		65	—	175		

Table 40. USB General Timing Parameters (continued)

Parameter	Symbol [1]	Min	Max	Unit	Note
USB clock to output valid—all outputs	t_{USKHOV}	—	9	ns	1
Output hold from USB clock—all outputs	t_{USKHOX}	1	—	ns	1

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{USIXKH} symbolizes USB timing (US) for the input (I) to go invalid (X) with respect to the time the USB clock reference (K) goes high (H). Also, t_{USKHOX} symbolizes USB timing (US) for the us clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to USB clock.
3. All signals are measured from NVDD/2 of the rising edge of USB clock to 0.4 × NVDD of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

Figure 21 and Figure 22 provide the AC test load and signals for the USB, respectively.

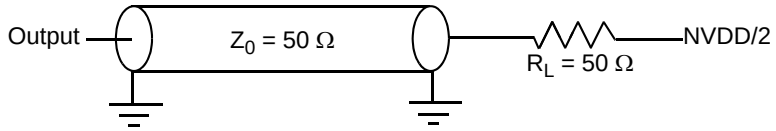


Figure 21. USB AC Test Load

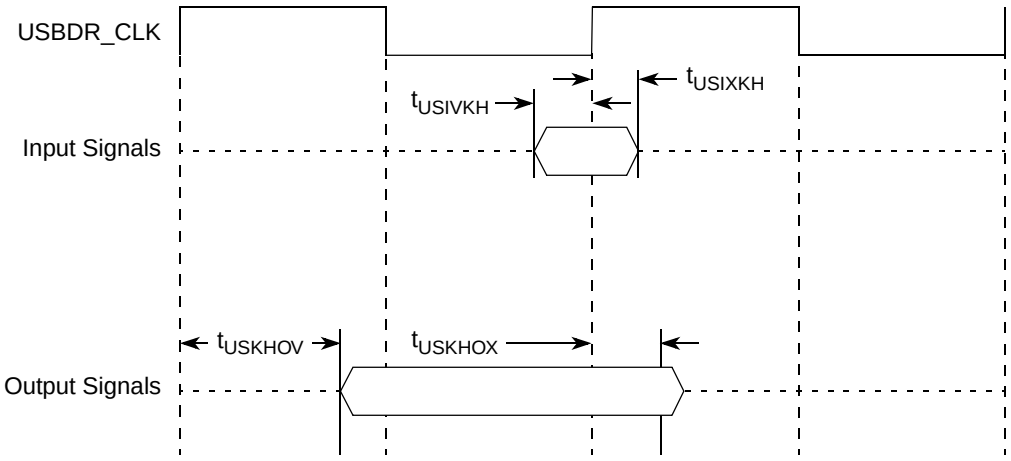


Figure 22. USB Signals

10.2 On-Chip USB PHY

This section provides the AC and DC electrical specifications for the USB PHY interface of the MPC8314E.

For details refer to Tables 7-7 through 7-10, and Table 7-14 in the *USB 2.0 Specifications document*, and the pull-up/down resistors ECN updates, all available at www.usb.org.

This table provides the USB clock input (USB_CLK_IN) DC timing specifications.

Figure 24 through Figure 26 show the local bus signals.

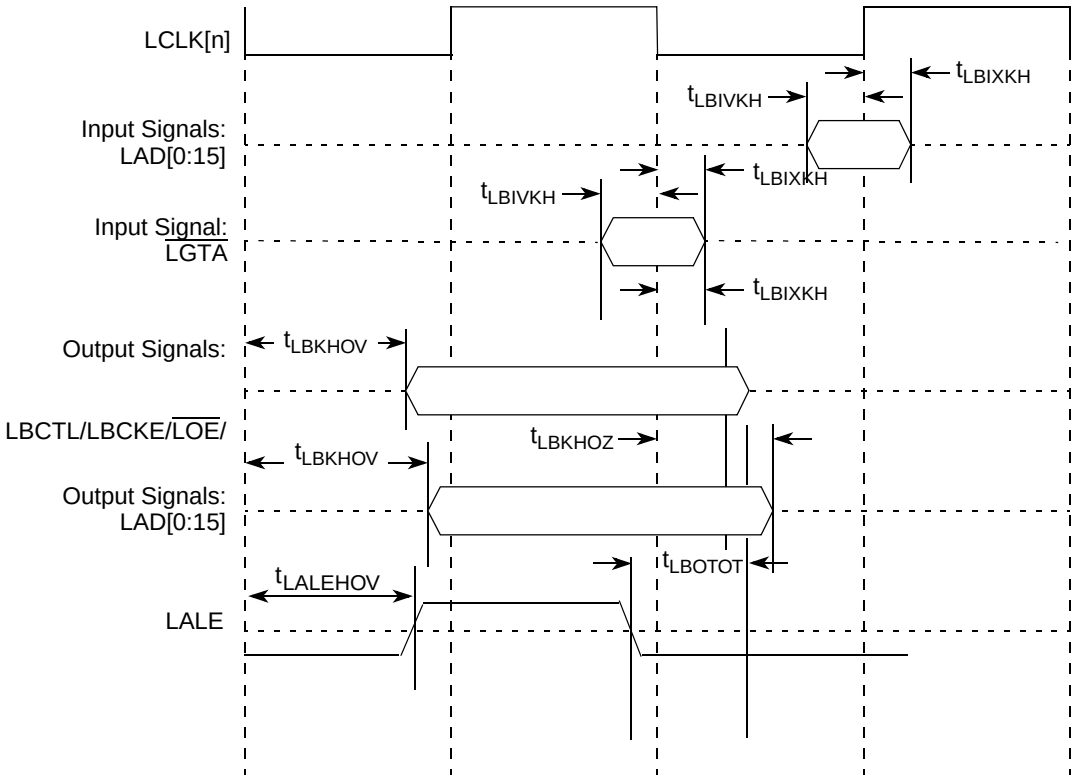


Figure 24. Local Bus Signals, Nonspecial Signals Only

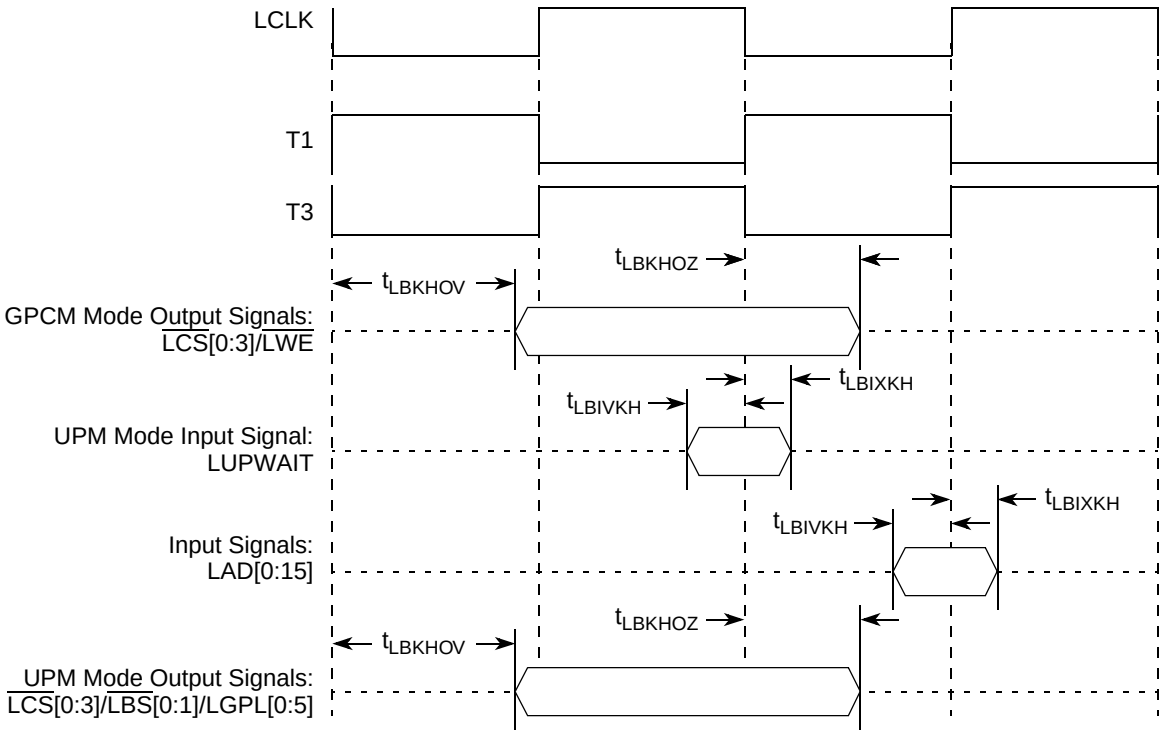


Figure 25. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 2

This figure provides the test access port timing diagram.

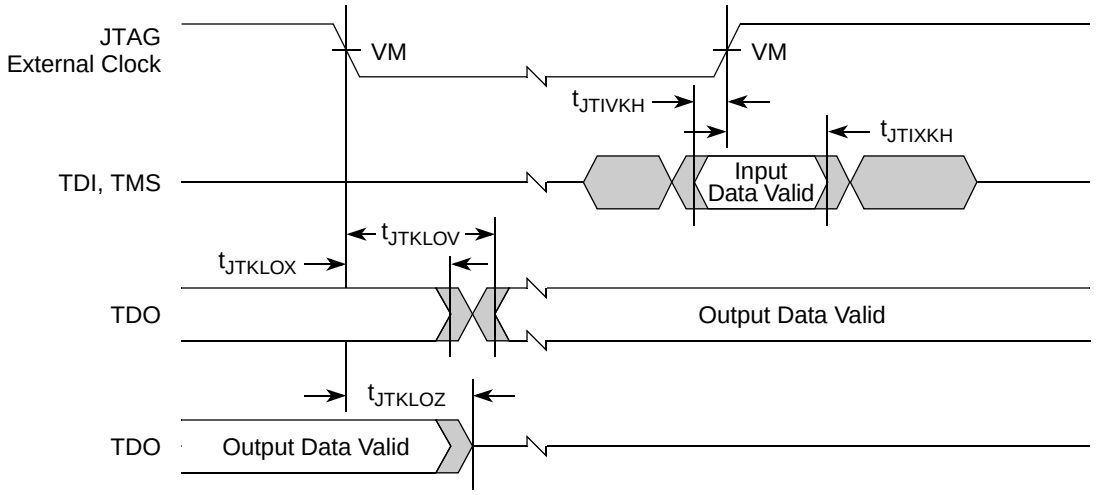


Figure 31. Test Access Port Timing Diagram

13 I²C

This section describes the DC and AC electrical characteristics for the I²C interface of the MPC8314E.

13.1 I²C DC Electrical Characteristics

This table provides the DC electrical characteristics for the I²C interface.

Table 47. I²C DC Electrical Characteristics

At recommended operating conditions with NVDD of 3.3 V ± 300 mv

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage level	V_{IH}	0.7 × NVDD	NVDD + 0.3	V	—
Input low voltage level	V_{IL}	–0.3	0.3 × NVDD	V	—
Low level output voltage	V_{OL}	0	0.2 × NVDD	V	1
High level output voltage	V_{OH}	0.8 × NVDD	NVDD + 0.3	V	—
Output fall time from V_{IH}(min) to V_{IL}(max) with a bus capacitance from 10 to 400 pF	t_{I2KLKV}	20 + 0.1 × C_B	250	ns	2
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	3
Capacitance for each I/O pin	C_I	—	10	pF	—
Input current (0 V ≤V_{IN} ≤ NVDD)	I_{IN}	—	± 5	μA	4

Note:

1. Output voltage (open drain or open collector) condition = 3 mA sink current.
2. C_B = capacitance of one bus line in pF.
3. See the *MPC8315E PowerQUICC II Pro Integrated Host Processor Family Reference Manual* for information on the digital filter used.
4. I/O pins obstruct the SDA and SCL lines if NVDD is switched off.

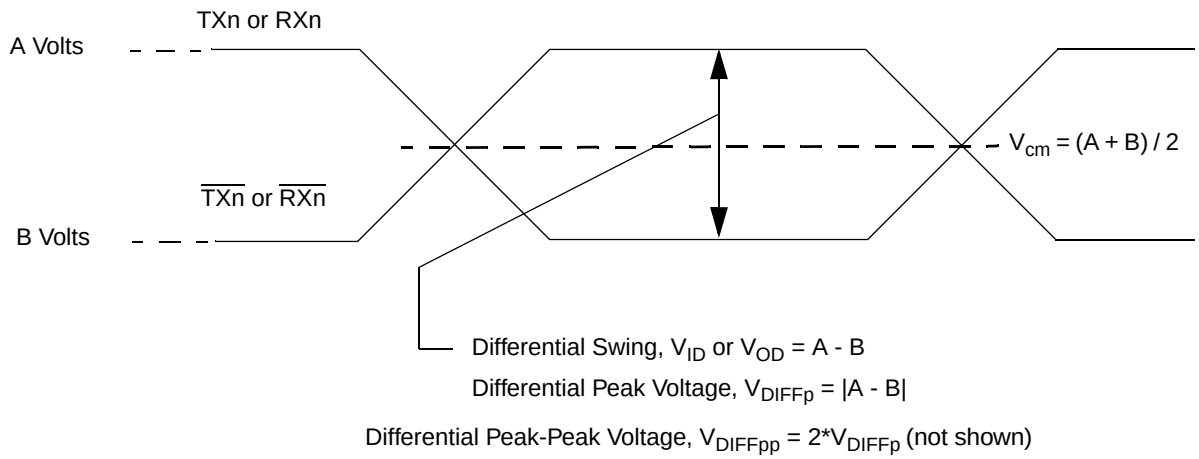


Figure 37. Differential Voltage Definitions for Transmitter or Receiver

To illustrate these definitions using real values, consider the case of a CML (Current Mode Logic) transmitter that has a common mode voltage of 2.25 V and each of its outputs, TD and $\overline{TD}$, has a swing that goes between 2.5V and 2.0V. Using these values, the peak-to-peak voltage swing of each signal (TD or $\overline{TD}$) is 500 mV p-p, which is referred as the single-ended swing for each signal. In this example, since the differential signaling environment is fully symmetrical, the transmitter output's differential swing (V_{OD}) has the same amplitude as each signal's single-ended swing. The differential output signal ranges between 500 mV and –500 mV, in other words, V_{OD} is 500 mV in one phase and –500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage ($V_{DIFFp-p}$) is 1000 mV p-p.

15.2 SerDes Reference Clocks

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clocks input is SD_REF_CLK and $\overline{SD\_REF\_CLK}$ for PCI Express and SGMII interface.

The following sections describe the SerDes reference clock requirements and some application information.

15.2.1 SerDes Reference Clock Receiver Characteristics

Figure 38 shows a receiver reference diagram of the SerDes reference clocks.

- The supply voltage requirements for XCOREVDD are specified in Table 1 and Table 2.
- SerDes Reference Clock Receiver Reference Circuit Structure
  - The SD_REF_CLK and $\overline{SD\_REF\_CLK}$ are internally AC-coupled differential inputs as shown in Figure 38. Each differential clock input (SD_REF_CLK or $\overline{SD\_REF\_CLK}$) has a 50-Ω termination to XCOREVSS followed by on-chip AC-coupling.
  - The external reference clock driver must be able to drive this termination.
  - The SerDes reference clock input can be either differential or single-ended. Refer to the Differential Mode and Single-ended Mode description below for further detailed requirements.

16.4.2 Transmitter Compliance Eye Diagrams

The TX eye diagram in Figure 49 is specified using the passive compliance/test measurement load (see Figure 51) in place of any real PCI Express interconnect + RX component. There are two eye diagrams that must be met for the transmitter. Both diagrams must be aligned in time using the jitter median to locate the center of the eye diagram. The different eye diagrams differ in voltage depending on whether it is a transition bit or a de-emphasized bit. The exact reduced voltage level of the de-emphasized bit is always relative to the transition bit.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

NOTE

It is recommended that the recovered TX UI be calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function (that is, least squares and median deviation fits).

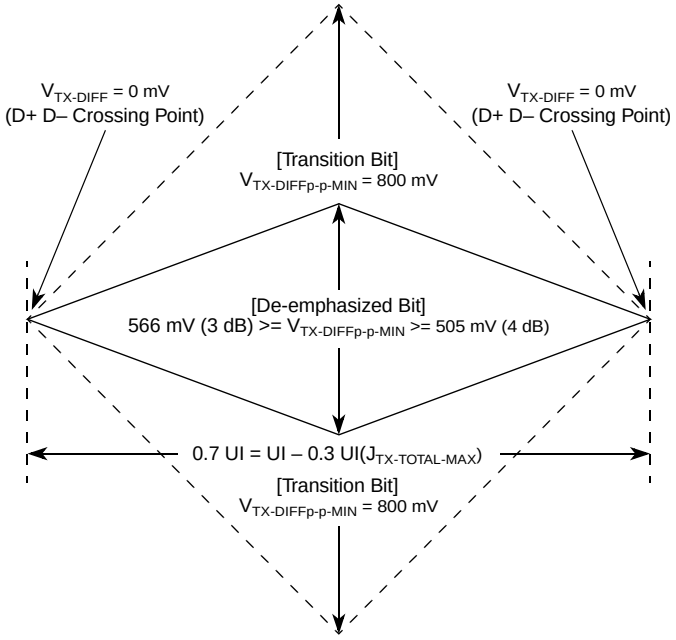


Figure 49. Minimum Transmitter Timing and Voltage Output Compliance Specifications

16.5 Receiver Compliance Eye Diagrams

The RX eye diagram in Figure 50 is specified using the passive compliance/test measurement load (see Figure 51) in place of any real PCI Express RX component. In general, the minimum receiver eye diagram measured with the compliance/test measurement load (see Figure 51) is larger than the minimum receiver eye diagram measured over a range of systems at the input receiver of any real PCI Express component. The degraded eye diagram at the input Receiver is due to traces internal to the package as well as silicon parasitic characteristics which cause the real PCI Express component to vary in impedance from the compliance/test measurement load. The input receiver eye diagram is implementation specific and is not specified. RX component designer should provide additional margin to adequately compensate for the degraded minimum Receiver eye diagram (shown in Figure 50) expected at the input receiver based on an adequate combination of system simulations and the return loss measured looking into the RX package and silicon. The RX eye diagram must be aligned in time using the jitter median to locate the center of the eye diagram.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.

NOTE

The reference impedance for return loss measurements is 50 Ω to ground for both the D+ and D- line (that is, as measured by a Vector Network Analyzer with 50 Ω probes—see Figure 51). Note that the series capacitors, $C_{PEACCTX}$, are optional for the return loss measurement.

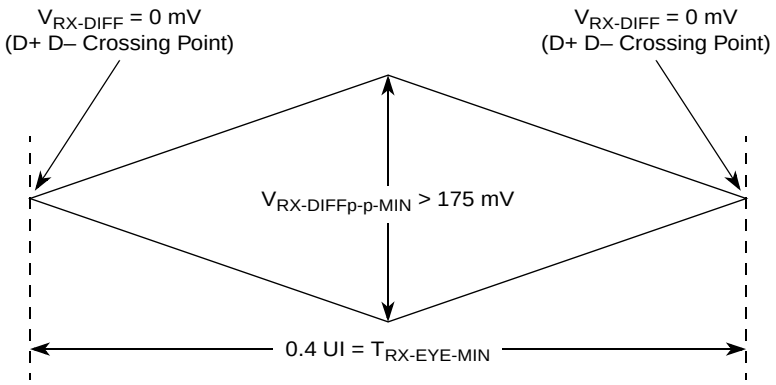


Figure 50. Minimum Receiver Eye Timing and Voltage Compliance Specification

16.5.1 Compliance Test and Measurement Load

The AC timing and voltage parameters must be verified at the measurement point, as specified within 0.2 inches of the package pins, into a test/measurement load shown in Figure 51.

NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D– not being exactly matched in length at the package pin boundary.

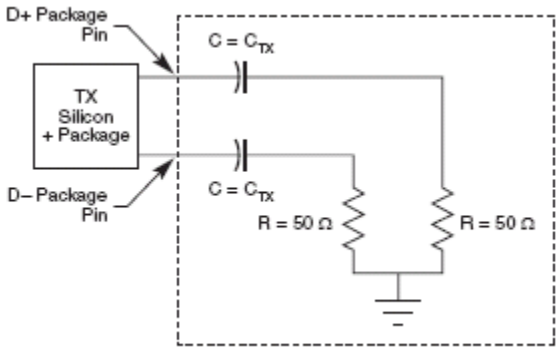


Figure 51. Compliance Test/Measurement Load

17 Timers

This section describes the DC and AC electrical specifications for the timers of the MPC8314E.

17.1 Timers DC Electrical Characteristics

This table provides the DC electrical characteristics for the timers pins, including TIN, $\overline{\text{TOUT}}$, $\overline{\text{TGATE}}$, and RTC_CLK.

Table 56. Timers DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.1	NVDD + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	0 V ≤ V_{IN} ≤ NVDD	—	± 5	μA

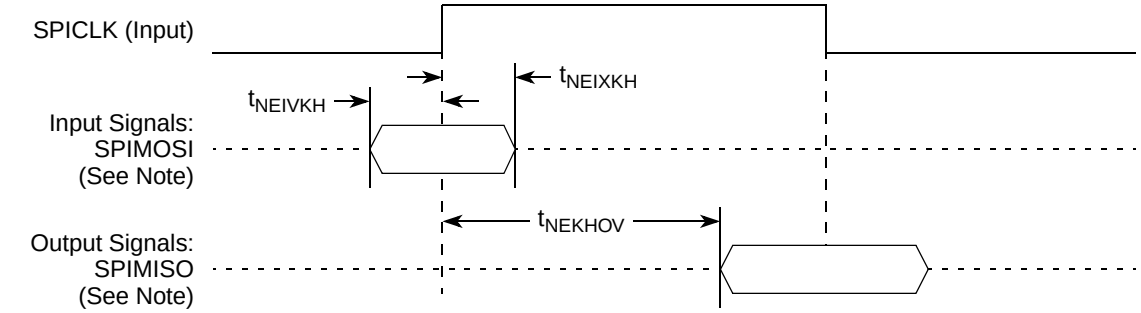
17.2 Timers AC Timing Specifications

This table provides the timers input and output AC timing specifications.

Table 57. Timers Input AC Timing Specifications

Characteristic	Symbol [1]	Min	Unit
Timers inputs—minimum pulse width	t_{TIWID}	20	ns

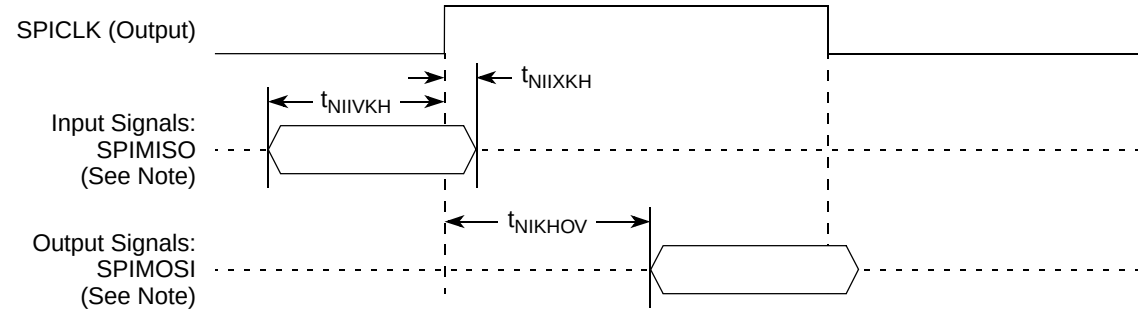
This figure shows the SPI timing in slave mode (external clock).



Note: The clock edge is selectable on SPI.

Figure 55. SPI AC Timing in Slave Mode (External Clock) Diagram

This figure shows the SPI timing in master mode (internal clock).



Note: The clock edge is selectable on SPI.

Figure 56. SPI AC Timing in Master Mode (Internal Clock) Diagram

21 TDM

This section describes the DC and AC electrical specifications for the TDM of the MPC8314E.

21.1 TDM DC Electrical Characteristics

This table provides the DC electrical characteristics TDM.

Table 64. TDM DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.1	NVDD + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	0 V ≤ V_{IN} ≤ NVDD	—	± 5	μA

Table 66. MPC8314E TEPBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
PCI_AD[23]	C22	I/O	$NVDD2_{OFF}$	—
PCI_AD[24]	E19	I/O	$NVDD2_{OFF}$	—
PCI_AD[25]	A22	I/O	$NVDD2_{OFF}$	—
PCI_AD[26]	C20	I/O	$NVDD2_{OFF}$	—
PCI_AD[27]	B21	I/O	$NVDD2_{OFF}$	—
PCI_AD[28]	D19	I/O	$NVDD2_{OFF}$	—
PCI_AD[29]	A19	I/O	$NVDD2_{OFF}$	—
PCI_AD[30]	A21	I/O	$NVDD2_{OFF}$	—
PCI_AD[31]	B19	I/O	$NVDD2_{OFF}$	—
PCI_C/$\overline{BE}$[0]	H24	I/O	$NVDD2_{OFF}$	—
PCI_C/$\overline{BE}$[1]	C27	I/O	$NVDD2_{OFF}$	—
PCI_C/$\overline{BE}$[2]	A25	I/O	$NVDD2_{OFF}$	—
PCI_C/$\overline{BE}$[3]	E21	I/O	$NVDD2_{OFF}$	—
PCI_PAR	G24	I/O	$NVDD2_{OFF}$	—
$\overline{PCI\_FRAME}$	C28	I/O	$NVDD2_{OFF}$	5
$\overline{PCI\_TRDY}$	A24	I/O	$NVDD2_{OFF}$	5
$\overline{PCI\_IRDY}$	D25	I/O	$NVDD2_{OFF}$	5
$\overline{PCI\_STOP}$	D23	I/O	$NVDD2_{OFF}$	5
$\overline{PCI\_DEVSEL}$	E22	I/O	$NVDD2_{OFF}$	5
PCI_IDSEL	D26	I	$NVDD2_{OFF}$	—
$\overline{PCI\_SERR}$	C25	I/O	$NVDD2_{OFF}$	5
$\overline{PCI\_PERR}$	D21	I/O	$NVDD2_{OFF}$	5
$\overline{PCI\_REQ0}$	E18	I/O	$NVDD2_{OFF}$	—
$\overline{PCI\_REQ1}$/CPCI_HS_ES	C18	I	$NVDD2_{OFF}$	—
$\overline{PCI\_REQ2}$	E17	I	$NVDD2_{OFF}$	—
$\overline{PCI\_GNT0}$	B20	I/O	$NVDD2_{OFF}$	—
$\overline{PCI\_GNT1}$/CPCI_HS_LED	D17	O	$NVDD2_{OFF}$	—
$\overline{PCI\_GNT2}$/CPCI_HS_ENUM	E15	O	$NVDD2_{OFF}$	—
M66EN	L24	I	$NVDD2_{OFF}$	—
PCI_CLK0	E23	O	$NVDD2_{OFF}$	—
PCI_CLK1	F24	O	$NVDD2_{OFF}$	—
PCI_CLK2	E25	O	$NVDD2_{OFF}$	—
$\overline{PCI\_PME}$	B23	I/O	$NVDD2_{OFF}$	2
ETSEC1/_USBULPI				
GPIO_24/TSEC1_COL/USBDR_TXDRXD0	J1	I/O	$LVDD1_{OFF}$	—
GPIO_25/TSEC1_CRS/USBDR_TXDRXD1	H1	I/O	$LVDD1_{OFF}$	—

Table 66. MPC8314E TEPBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
VDD	J15, K15, K16, K17, K18, K19, L10, L19, M10, T10, U10, U19, V10, V19, W11, W12, W13, W14, W15, W16, W17, W18, P23, R23, T19, M26, N26, P28, R28, U23, N27	I	—	—
VDDC	J14, K11, K12, K13, K14, M19	I	—	—
VSS	A3, A27, B3, B12, B24, B28, C6, C8, C13, C17, C21, C23, C26, D2, D7, D15, D18, D20, D22, E4, E6, E11, E24, E26, F8, F12, F14, F17, F20, G3, G26, H4, H23, J6, J26, K25, L4, L11, L12, L13, L14, L15, L16, L17, L18, L23, L28, M3, M11, M12, M13, M14, M15, M16, M17, M18, N5, N11, N12, N13, N14, N15, N16, N17, N18, P6, P11, P12, P13, P14, P15, P16, P17, P18, R6, R11, R12, R13, R14, R15, R16, R17, R18, T11, T12, T13, T14, T15, T16, T17, T18, U5, U6, U11, U12, U13, U14, U15, U16, U17, U18, V6, V11, V12, V13, V14, V15, V16, V17, V18, W5, W25, W27, Y2, Y23, AA6, AA27, AB2, AB26, AC5, AC9, AC12, AC18, AC21, AD3, AD14, AD16, AD20, AD26, AE2, AE7, AE11, AE16, AE22, AE24, AF2, AF9, AF12, AF18, AF20, AF23, AF27, AG1, AG5, AG11, AG16, AG22, AG28, AH27, U28,N28, M28, T28, V27, M27, V28, T26, P24, R19, R20, R24, M24, N24, P19, P20, P25, P27, R25, R27, T24	I	—	—
XCOREVDD	P2, P10, R2, T1	I	—	—
XCOREVSS	R3, R10, U2, V2	I	—	—
XPADVDD	P3, R9, U3	I	—	—
XPADVSS	P5, P9, V3	I	—	—

Note:

1. This pin is an open drain signal. A weak pull-up resistor (1 kΩ) should be placed on this pin to NVDD.
2. This pin is an open drain signal. A weak pull-up resistor (2–10 kΩ) should be placed on this pin to NVDD.
3. This output is actively driven during reset rather than being three-stated during reset.
4. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
5. This pin should have a weak pull up if the chip is in PCI host mode. Follow PCI specifications recommendation.
6. This pin must always be tied to VSS.
7. Thermal sensitive resistor.
8. This pin should be connected to USB_VSSA_BIAS through 10K precision resistor.
9. The LB_POR_CFG_BOOT_ECC functionality for this pin is only available in MPC8314E revision 1.1 and later. The LB_POR_CFG_BOOT_ECC is sampled only during the $\overline{\text{PORESET}}$ negation. This pin with an internal pull down resistor enables the ECC by default. To disable the ECC an external strong pull up resistor or a tristate buffer is needed.
10. This pin has a weak internal pull-down.
11. This pin has a weak internal pull-up.

24.2 Thermal Management Information

For the following sections, $P_D = (VDD \times I_{DD}) + P_{I/O}$ where $P_{I/O}$ is the power dissipation of the I/O drivers.

24.2.1 Estimation of Junction Temperature with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_J = junction temperature (°C)

T_A = ambient temperature for the package (°C)

$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. As a general statement, the value obtained on a single layer board is appropriate for a tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated. Test cases have demonstrated that errors of a factor of two (in the quantity T_J - T_A) are possible.

24.2.2 Estimation of Junction Temperature with Junction-to-Board Thermal Resistance

The thermal performance of a device cannot be adequately predicted from the junction to ambient thermal resistance. The thermal performance of any component is strongly dependent on the power dissipation of surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

T_J = junction temperature (°C)

T_B = board temperature at the package perimeter (°C)

$R_{\theta JB}$ = junction to board thermal resistance (°C/W) per JESD51-8

P_D = power dissipation in the package (W)

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. The application board should be similar to the thermal test condition: the component is soldered to a board with internal planes.

Table 75. Heat Sinks and Junction-to-Case Thermal Resistance of MPC8314E TEPBGA II

Heat Sink Assuming Thermal Grease	Air Flow	29 × 29 mm TEBGA II
		Junction-to-Ambient Thermal Resistance
AAVID 30 x 30 x 9.4 mm Pin Fin	Natural Convection	14.4
AAVID 30 x 30 x 9.4 mm Pin Fin	0.5 m/s	11.4
AAVID 30 x 30 x 9.4 mm Pin Fin	1 m/s	10.1
AAVID 30 x 30 x 9.4 mm Pin Fin	2 m/s	8.9
AAVID 35 x 31 x 23 mm Pin Fin	Natural Convection	12.3
AAVID 35 x 31 x 23 mm Pin Fin	0.5 m/s	9.3
AAVID 35 x 31 x 23 mm Pin Fin	1 m/s	8.5
AAVID 35 x 31 x 23 mm Pin Fin	2 m/s	7.9
AAVID 43 x 41 x 16.5 mm Pin Fin	Natural Convection	12.5
AAVID 43 x 41 x 16.5 mm Pin Fin	0.5 m/s	9.7
AAVID 43 x 41 x 16.5 mm Pin Fin	1 m/s	8.5
AAVID 43 x 41 x 16.5 mm Pin Fin	2 m/s	7.7
Wakefield, 53 x 53 x 25 mm Pin Fin	Natural Convection	10.9
Wakefield, 53 x 53 x 25 mm Pin Fin	0.5 m/s	8.5
Wakefield, 53 x 53 x 25 mm Pin Fin	1 m/s	7.5
Wakefield, 53 x 53 x 25 mm Pin Fin	2 m/s	7.1

Accurate thermal design requires thermal modeling of the application environment using computational fluid dynamics software which can model both the conduction cooling and the convection cooling of the air moving through the application. Simplified thermal models of the packages can be assembled using the junction-to-case and junction-to-board thermal resistances listed in the thermal resistance table. More detailed thermal models can be made available on request.

Heat sink vendors include the following list:

Aavid Thermalloy 603-224-9988
80 Commercial St.
Concord, NH 03301
Internet: www.aavidthermalloy.com

Alpha Novatech 408-749-7601
473 Sapena Ct. #12
Santa Clara, CA 95054
Internet: www.alphanovatech.com

International Electronic Research Corporation (IERC) 818-842-7277
413 North Moss St.
Burbank, CA 91502
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