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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

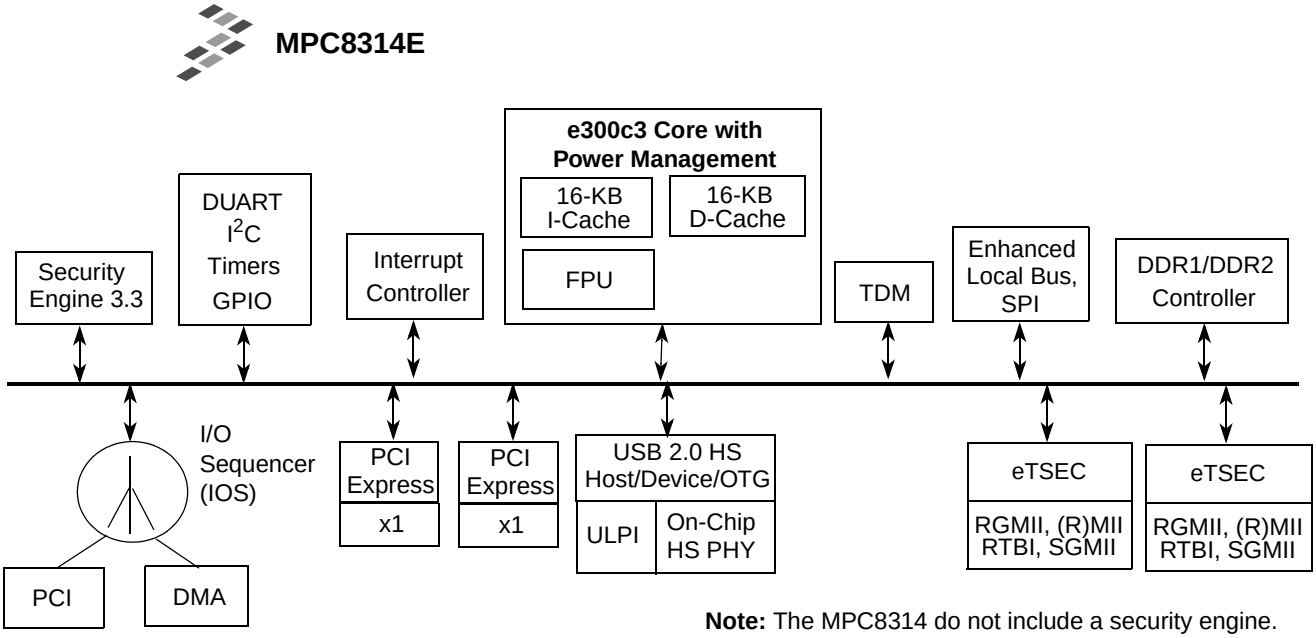
Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	PowerPC e300c3
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	333MHz
Co-Processors/DSP	Security; SEC 3.3
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 + PHY (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	620-BBGA Exposed Pad
Supplier Device Package	620-HBGA (29x29)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8314ecvrafda

1 Overview

The MPC8314E incorporates the e300c3 (MPC603e-based) core, which includes 16 Kbytes of L1 instruction and data caches, on-chip memory management units (MMUs), and floating-point support. In addition to the e300 core, the SoC platform includes features such as dual enhanced three-speed 10, 100, 1000 Mbps Ethernet controllers (eTSECs) with SGMII support, a 32- or 16-bit DDR1/DDR2 SDRAM memory controller, a security engine to accelerate control and data plane security protocols, and a high degree of software compatibility with previous-generation PowerQUICC processor-based designs for backward compatibility and easier software migration. The MPC8314E also offers peripheral interfaces such as a 32-bit PCI interface with up to 66 MHz operation, 16-bit enhanced local bus interface with up to 66 MHz operation, TDM interface, and USB 2.0 with an on-chip USB 2.0 PHY.

8314E offers additional high-speed interconnect support with dual single-lane PCI Express interfaces. When not used for PCI Express, the SerDes interface may be configured to support SGMII. The MPC8314E security engine (SEC 3.3) allows CPU-intensive cryptographic operations to be offloaded from the main CPU core. This figure shows a block diagram of the MPC8314E.



Note: The MPC8314 do not include a security engine.

Figure 1. MPC8314E Block Diagram

2 MPC8314E Features

The following features are supported in the MPC8314E.

2.1 e300 Core

The e300 core has the following features:

- Operates at up to 400 MHz
- 16-Kbyte instruction cache, 16-Kbyte data cache

- One floating point unit and two integer units
- Software-compatible with the Freescale processor families implementing the PowerPC Architecture
- Performance monitor

2.2 Serial Interfaces

The following interfaces are supported in the MPC8314E.

- Two enhanced TSECs (eTSECs)
- Two Ethernet interfaces using one RGMII/MII/RMII/RTBI or SGMII (no GMII)
- Dual UART, one I^2C, and one SPI interface

2.3 Security Engine

The security engine is optimized to handle all the algorithms associated with IPSec, 802.11i, and iSCSI. The security engine contains one crypto-channel, a controller, and a set of crypto execution units (EUs). The execution units are:

- Public key execution unit (PKEU)
  - RSA and Diffie-Hellman (to 4096 bits)
  - Programmable field size up to 2048 bits
  - Elliptic curve cryptography (1023 bits)
  - F2m and F(p) modes
  - Programmable field size up to 511 bits
- Data encryption standard execution unit (DEU)
  - DES, 3DES
  - Two key (K1, K2) or three key (K1, K2, K3)
  - ECB, CBC, CFB-64 and OFB-64 modes for both DES and 3DES
- Advanced encryption standard unit (AESU)
  - Implements the Rinjdael symmetric key cipher
  - Key lengths of 128, 192, and 256 bits
  - ECB, CBC, CCM, CTR, GCM, CMAC, OFB, CFB, XCBC-MAC and LRW modes
  - XOR acceleration
- Message digest execution unit (MDEU)
  - SHA with 160-bit, 256-bit, 384-bit and 512-bit message digest
  - SHA-384/512
  - MD5 with 128-bit message digest
  - HMAC with either algorithm
- Random number generator (RNG)

2.9 Dual Enhanced Three-Speed Ethernet Controllers (eTSECs)

The eTSECs include the following features:

- Two SGMII/RGMII/MII/RMII/RTBI interfaces
- Two controllers designed to comply with IEEE Std 802.3™, IEEE 802.3u™, IEEE 802.3x™, IEEE 802.3z™, IEEE 802.3au™, IEEE 802.3ab™, and IEEE Std 1588™
- Support for Wake-on-Magic Packet™, a method to bring the device from standby to full operating mode
- MII management interface for external PHY control and status.

2.10 Integrated Programmable Interrupt Controller (IPIC)

The integrated programmable interrupt controller (IPIC) provides a flexible solution for general-purpose interrupt control. The IPIC programming model is compatible with the MPC8260 interrupt controller and supports external and internal discrete interrupt sources. Interrupts can also be redirected to an external interrupt controller.

2.11 Power Management Controller (PMC)

The MPC8314E supports a range of power management states that significantly lower power consumption under the control of the power management controller. The PMC includes the following features:

- Provides power management when the device is used in both PCI host and agent modes
- PCI Power Management 1.2 D0, D1, D2, D3hot, and D3cold states
- PME generation in PCI agent mode, PME detection in PCI host mode
- Wake-up from Ethernet (magic packet), USB, GPIO, and PCI (PME input as host) while in the D1, D2 and D3hot states
- A new low-power standby power management state called D3warm
  - The PMC, one Ethernet port, and the GTM block remain powered via a split power supply controlled through an external power switch
  - Wake-up events include Ethernet (magic packet), GTM, GPIO, or IRQ inputs and cause the device to transition back to normal operation
  - PCI agent mode is not be supported in D3warm state
- PCI Express-based PME events are not supported

2.12 Serial Peripheral Interface (SPI)

The serial peripheral interface (SPI) allows the MPC8314E to exchange data between other PowerQUICC family chips, Ethernet PHYs for configuration, and peripheral devices such as EEPROMs, real-time clocks, A/D converters, and ISDN devices.

The SPI is a full-duplex, synchronous, character-oriented channel that supports a four-wire interface (receive, transmit, clock, and slave select). The SPI block consists of transmitter and receiver sections, an independent baud-rate generator, and a control unit.

CAUTION

When the device is in D3 warm (standby) mode, all external voltage supplies applied to any I/O pins, with the exception of wake-up pins, must be turned off. Applying supplied external voltage to any I/O pins, except the wake up pins, while the device is in D3 warm standby mode may cause permanent damage to the device.

An example of the power-up sequence is shown in Figure 4 when implemented along with low power D3 warm mode.

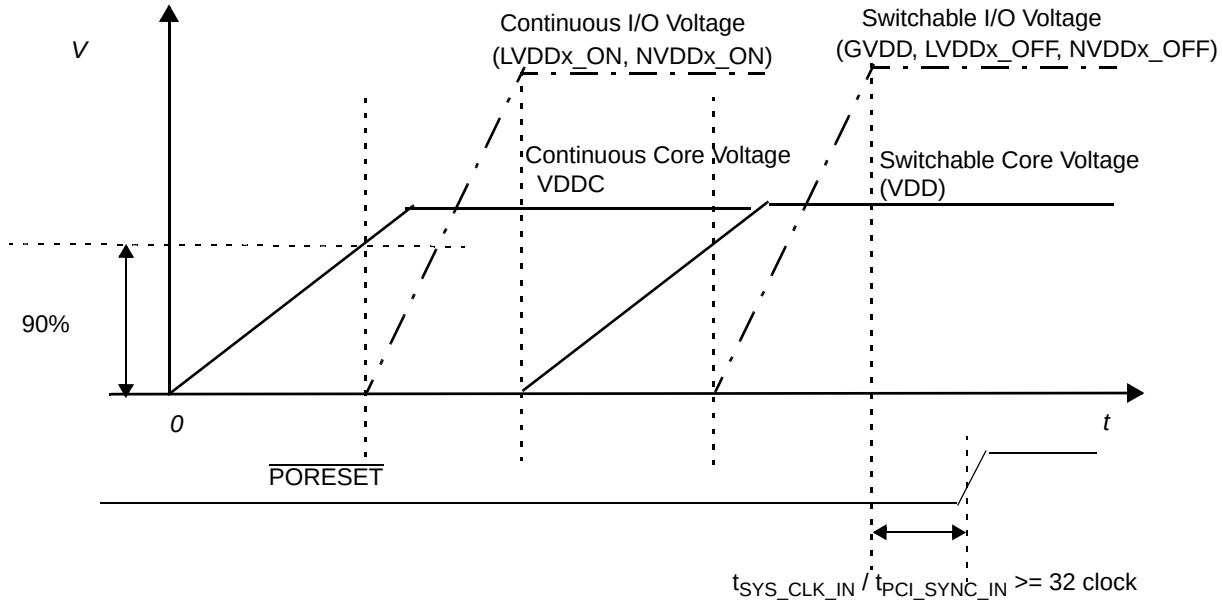


Figure 4. Power Up Sequencing Example with Low power D3 Warm Mode

4 Power Characteristics

This table shows the estimated typical power dissipation for this family of devices.

Table 4. MPC8314E Power Dissipation

(Does not include I/O power dissipation)

Core Frequency (MHz)	CSB Frequency (MHz)	Typical [1,3]	Maximum [1,2]	Unit
266	133	1.116	1.646	W
333	133	1.142	1.665	W
400	133	1.167	1.690	W

Note:

1. The values do not include I/O supply power, but do include core, AVDD, USB PLL, and digital SerDes power.
2. Maximum power is based on a voltage of V_{dd} = 1.05V, a junction temperature of T_j = 105°C, and an artificial smoker test.
3. Typical power is based on a voltage of V_{dd} = 1.05V, and an artificial smoker test running at room temperature.

This table shows the estimated typical I/O power dissipation for this family of devices.

Table 5. MPC8314E Power Dissipation

Interface	Frequency	GV_{DD} (1.8 V)	GV_{DD} (2.5 V)	NV_{DD} (3.3 V)	LVDD1_OFF/ LVDD2_ON (3.3V)	LVDD2 _ON (3.3V)	VDD33PLL, VDD33ANA (3.3V)	SATA_VDD, VDD1IO, VDD1ANA (1.0V)	XCOREVDD, XPADVDD, SDAVDD (1.0V)	Unit
DDR 1 Rs = 22Ω Rt = 50Ω	266MHz, 32 bits	—	0.323	—	—	—	—	—	—	W
	200MHz, 32 bits	—	0.291	—	—	—	—	—	—	W
DDR 2 Rs = 22Ω Rt = 75Ω	266MHz, 32 bits	0.246	—	—	—	—	—	—	—	W
	200MHz, 32bits	0.225	—	—	—	—	—	—	—	W
PCI I/O load = 50pF	33 MHz	—	—	0.120	—	—	—	—	—	W
	66 MHz	—	—	0.249	—	—	—	—	—	W
Local bus I/O load = 20pF	66 MHz	—	—	—	—	0.056	—	—	—	W
	50 MHz	—	—	—	—	0.040	—	—	—	W
eTSEC I/O load = 20pF Multiple by number of interface used	MII, 25MHz	—	—	—	0.008	—	—	—	—	W
	RGMII, 125MHz (3.3V)	—	—	—	0.078	—	—	—	—	W
	RGMII, 125MHz (2.5V)	—	—	—	0.044	—	—	—	—	W
USBDR Controller (ULPI mode) load =20pF	60 MHz	—	—	—	0.078	—	—	—	—	W
USBDR+ Internal PHY (UTMI mode)	480 MHz	—	—	—	0.274	—	—	—	—	W
PCI Express two x1lane	2.5 GHz	—	—	—	—	—	—	—	0.190	W
Other I/O	—	—	—	0.015	—	—	—	—	—	W

5 Clock Input Timing

This section provides the clock input DC and AC electrical characteristics for the MPC8314E.

This table provides the DDR2 capacitance when GVDD(typ) = 1.8 V.

Table 12. DDR2 SDRAM Capacitance for GVDD(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Note
Input/output capacitance: DQ, DQS	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. GVDD = 1.8 V ± 0.090 V, f = 1 MHz, T_A = 25°C, V_{OUT} = GVDD/2, V_{OUT} (peak-to-peak) = 0.2 V.

This table provides the recommended operating conditions for the DDR SDRAM component(s) of the MPC8314E when GVDD(typ) = 2.5 V.

Table 13. DDR SDRAM DC Electrical Characteristics for GVDD(typ) = 2.5 V

Parameter/Condition	Symbol	Min	Max	Unit	Note
I/O supply voltage	GVDD	2.3	2.7	V	1
I/O reference voltage	MVREF	0.49 × GVDD	0.51 × GVDD	V	2
I/O termination voltage	V_{TT}	MVREF – 0.04	MVREF + 0.04	V	3
Input high voltage	V_{IH}	MVREF + 0.15	GVDD + 0.3	V	—
Input low voltage	V_{IL}	–0.3	MVREF – 0.15	V	—
Output leakage current	I_{OZ}	–9.9	–9.9	μA	4
Output high current (V_{OUT} = 1.95 V, GVDD = 2.3V)	I_{OH}	–16.2	—	mA	—
Output low current (V_{OUT} = 0.35 V)	I_{OL}	16.2	—	mA	—

Note:
1. GVDD is expected to be within 50 mV of the DRAM GVDD at all times.
2. MVREF is expected to be equal to 0.5 × GVDD, and to track GVDD DC variations as measured at the receiver. Peak-to-peak noise on MVREF may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MVREF. This rail should track variations in the DC level of MVREF.
4. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GVDD.

This table provides the DDR capacitance when GVDD(typ) = 2.5 V.

Table 14. DDR SDRAM Capacitance for GVDD(typ) = 2.5 V Interface

Parameter/Condition	Symbol	Min	Max	Unit	Note
Input/output capacitance: DQ,DQS	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. GVDD = 2.5 V ± 0.125 V, f = 1 MHz, T_A = 25°C, V_{OUT} = GVDD/2, V_{OUT} (peak-to-peak) = 0.2 V.

This table provides the current draw characteristics for MV_{REF}.

Table 15. Current Draw Characteristics for MV_{REF}

Parameter / Condition	Symbol	Min	Max	Unit	Note
Current draw for MV_{REF}	I_{MVREF}	—	500	μA	1

Table 15. Current Draw Characteristics for MV_{REF}

Parameter / Condition	Symbol	Min	Max	Unit	Note

Note:
1. The voltage regulator for MV_{REF} must be able to supply up to 500 μA current.

7.2 DDR and DDR2 SDRAM AC Electrical Characteristics

This section provides the AC electrical characteristics for the DDR and DDR2 SDRAM interface.

7.2.1 DDR and DDR2 SDRAM Input AC Timing Specifications

This table lists the input AC timing specifications for the DDR2 SDRAM (GVDD(typ) = 1.8 V).

Table 16. DDR2 SDRAM Input AC Timing Specifications for 1.8-V Interface

At recommended operating conditions with GVDD of 1.8V ± 100 mV

Parameter	Symbol	Min	Max	Unit	Note
AC input low voltage	V_{IL}	—	MVREF – 0.45	V	—
AC input high voltage	V_{IH}	MVREF + 0.45	—	V	—

This table lists the input AC timing specifications for the DDR SDRAM when GVDD(typ)=2.5 V.

Table 17. DDR SDRAM Input AC Timing Specifications for 2.5 V Interface

At recommended operating conditions with GVDD of 2.5V ± 200 mV

Parameter	Symbol	Min	Max	Unit	Note
AC input low voltage	V_{IL}	—	MVREF – 0.51	V	
AC input high voltage	V_{IH}	MVREF + 0.51	—	V	

The following two tables list the input AC timing specifications for the DDR SDRAM interface.

Table 18. DDR2 SDRAM Input AC Timing Specifications

At recommended operating conditions with GVDD of (1.8 V± 100 mV)

Parameter	Symbol	Min	Max	Unit	Note
Controller Skew for MDQS—MDQ 266 MHz 200 MHz	t_{CISKEW}	 –875 –1250	 875 1250	ps	1, 2, 3

Note:
1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit to be captured with MDQS[n]. This should be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}.This can be determined by the following equation: tDISKEW =+/–(T/4 – abs(t_{CISKEW})) where T is the clock period and abs(t_{CISKEW}) is the absolute value of t_{CISKEW}.
3. Memory controller ODT value of 150 Ω is recommended.

Table 19. DDR SDRAM Input AC Timing Specifications

At recommended operating conditions with GVDD of (2.5V ± 200 mV)

Parameter	Symbol	Min	Max	Unit	Note

This figure shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

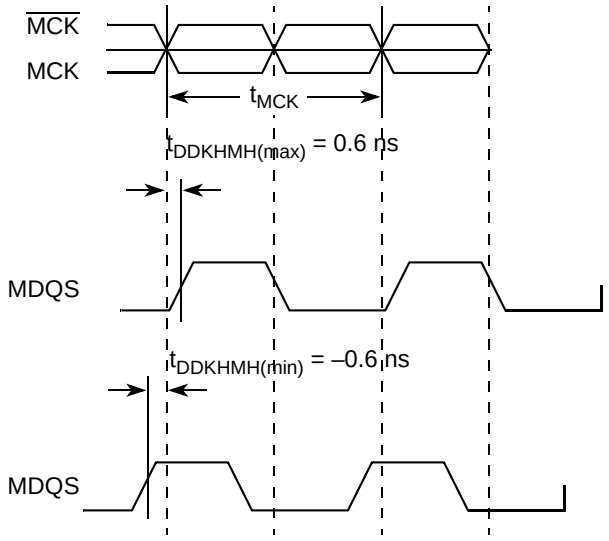


Figure 6. Timing Diagram for t_{DDKHMH}

This figure shows the DDR and DDR2 SDRAM output timing diagram.

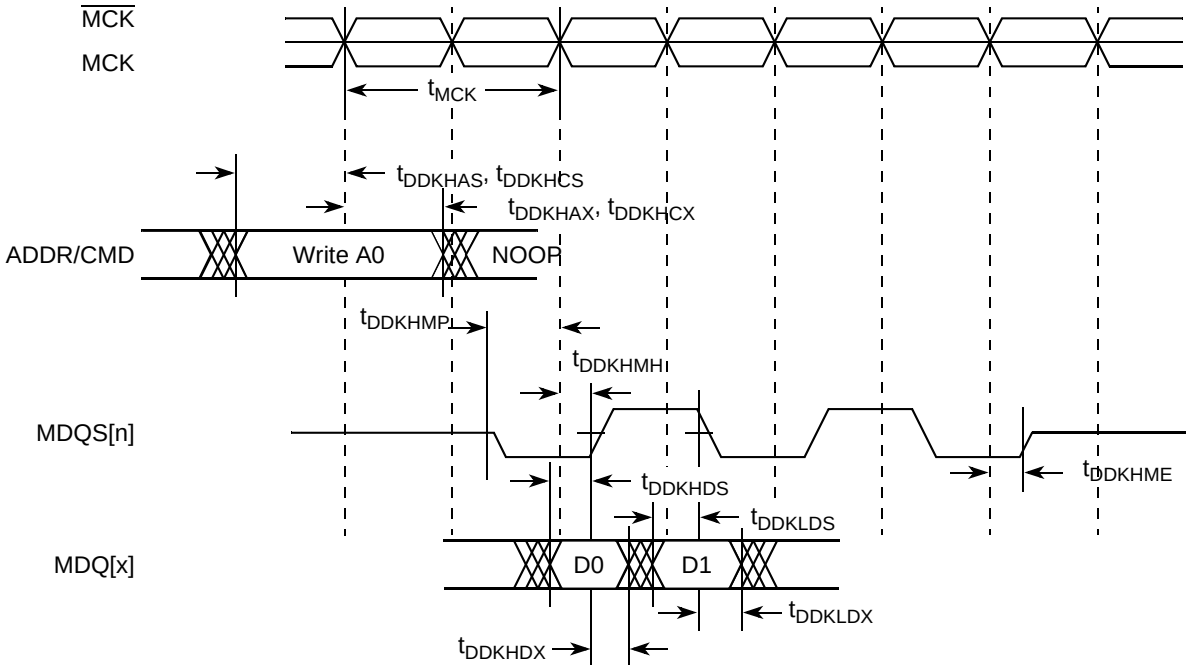


Figure 7. DDR and DDR2 SDRAM Output Timing Diagram

Table 28. RMII Receive AC Timing Specifications (continued)

At recommended operating conditions with LVDD of 3.3 V ± 300 mv

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
RXD[1:0], CRS_DV, RX_ER setup time to REF_CLK	$t_{RMRDVKH}$	4.0	—	—	ns
RXD[1:0], CRS_DV, RX_ER hold time to REF_CLK	$t_{RMRDXKH}$	2.0	—	—	ns
REF_CLK clock rise V_{IL}(min) to V_{IH}(max)	t_{RMXR}	1.0	—	4.0	ns
REF_CLK clock fall time V_{IH}(max) to V_{IL}(min)	t_{RMXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{RMRDVKH}$ symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{RMX} clock reference (K) going to the high (H) state or setup time. Also, $t_{RMRDXKL}$ symbolizes RMII receive timing (RMR) with respect to the time data input signals (D) went invalid (X) relative to the t_{RMX} clock reference (K) going to the low (L) state or hold time. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For example, the subscript of t_{RMX} represents the RMII (RM) reference (X) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure provides the AC test load.

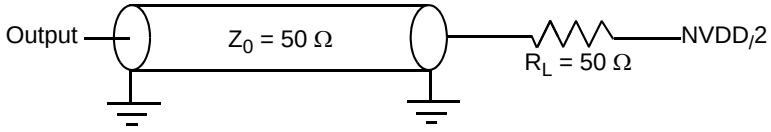


Figure 13. AC Test Load

This figure shows the RMII receive AC timing diagram.

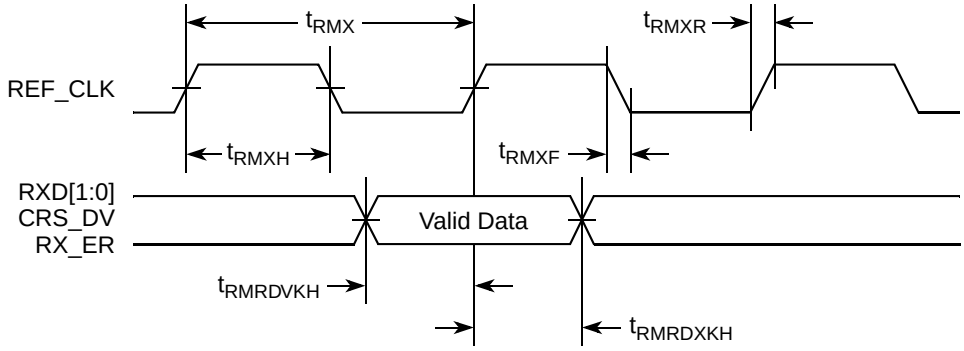


Figure 14. RMII Receive AC Timing Diagram

9.2.3 RGMII and RTBI AC Timing Specifications

This table presents the RGMII and RTBI AC timing specifications.

Table 29. RGMII and RTBI AC Timing Specifications

At recommended operating conditions (see Table 2)

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
Data to clock output skew (at transmitter)	t_{SKRGT}	–0.6	—	0.6	ns
Data to clock input skew (at receiver) [2]	t_{SKRGT}	1.0	—	2.6	ns

13.2 I²C AC Electrical Specifications

This table provides the AC timing parameters for the I²C interface.

Table 48. I²C AC Electrical Specifications

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 47)

Parameter	Symbol [1]	Min	Max	Unit
SCL clock frequency	f_{I2C}	0	400	kHz
Low period of the SCL clock	t_{I2CL}	1.3	—	μs
High period of the SCL clock	t_{I2CH}	0.6	—	μs
Setup time for a repeated START condition	t_{I2SVKH}	0.6	—	μs
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL}	0.6	—	μs
Data setup time	t_{I2DVKH}	100	—	ns
Data hold time: CBUS compatible masters I²C bus devices	t_{I2DXKL}	 — 0 [2]	 — 0.9 [3]	μs
Fall time of both SDA and SCL signals	t_{I2CF} [4]	—	300	ns
Setup time for STOP condition	t_{I2PVKH}	0.6	—	μs
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	μs
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	0.1 × NVDD	—	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	0.2 × NVDD	—	V

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. MPC8314E provides a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
3. The maximum t_{I2DVKH} has to be met only if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
4. MPC8314E does not follow the *I2C-BUS Specifications* version 2.1 regarding the tI2CF AC parameter.

This figure provides the AC test load for the I²C.

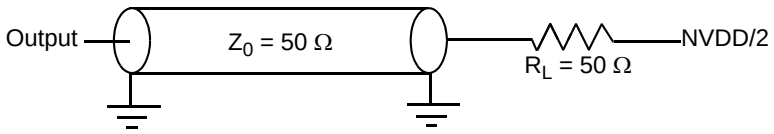


Figure 32. I²C AC Test Load

Table 50. PCI AC Timing Specifications at 66 MHz (continued)

Parameter	Symbol [1]	Min	Max	Unit	Note
Input hold from clock	t_{PCIXKH}	0	—	ns	2, 4

Note:

1. Note that the symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.3 Local Bus Specifications*.
3. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. Input timings are measured at the pin.

This table shows the PCI AC Timing Specifications at 33 MHz.

Table 51. PCI AC Timing Specifications at 33 MHz

Parameter	Symbol [1]	Min	Max	Unit	Note
Clock to output valid	t_{PCKHOV}	—	11	ns	2
Output hold from clock	t_{PCKHOX}	2	—	ns	2
Clock to output high impedance	t_{PCKHOZ}	—	14	ns	2, 3
Input setup to clock	t_{PCIVKH}	4.0	—	ns	2, 4
Input hold from clock	t_{PCIXKH}	0	—	ns	2, 4

Note:

1. Note that the symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{PCIVKH} symbolizes PCI timing (PC) with respect to the time the input signals (I) reach the valid state (V) relative to the PCI_SYNC_IN clock, t_{SYS}, reference (K) going to the high (H) state or setup time. Also, t_{PCRHFV} symbolizes PCI timing (PC) with respect to the time hard reset (R) went high (H) relative to the frame signal (F) going to the valid (V) state.
2. See the timing measurement conditions in the *PCI 2.3 Local Bus Specifications*.
3. For purposes of active/float timing measurements, the Hi-Z or off state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.
4. Input timings are measured at the pin.

This figure provides the AC test load for PCI.

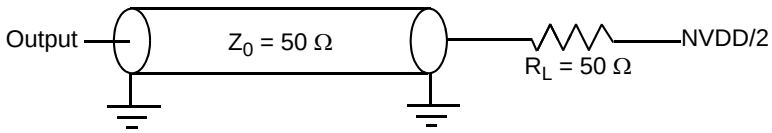


Figure 34. PCI AC Test Load

This figure shows the PCI input AC timing conditions.

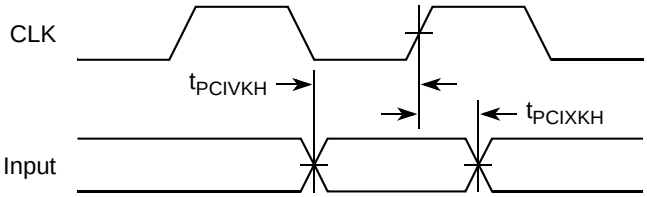


Figure 35. PCI Input AC Timing Measurement Conditions

This figure shows the PCI output AC timing conditions.

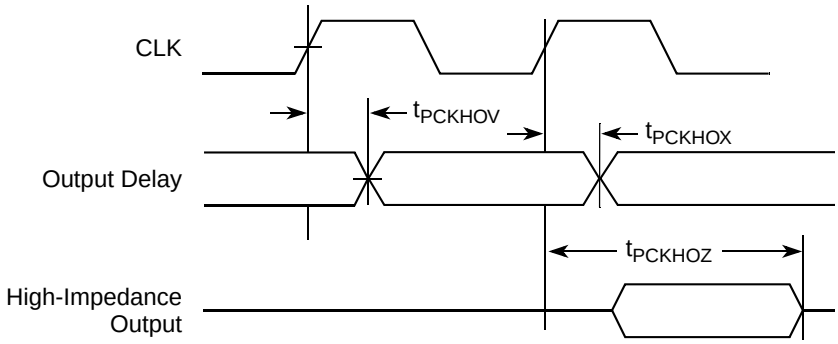


Figure 36. PCI Output AC Timing Measurement Condition

15 High-Speed Serial Interfaces (HSSI)

This section describes the common portion of SerDes DC electrical specifications, which is the DC requirement for SerDes Reference Clocks. The SerDes data lane's transmitter and receiver reference circuits are also shown.

15.1 Signal Terms Definition

The SerDes utilizes differential signaling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals.

Figure 37 shows how the signals are defined. For illustration purpose, only one SerDes lane is used for description. The figure shows waveform for either a transmitter output (TXn and $\overline{\text{TXn}}$) or a receiver input (RXn and $\overline{\text{RXn}}$). Each signal swings between A Volts and B Volts where A > B.

Using this waveform, the definitions are as follows. To simplify illustration, the following definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signaling environment.

1. **Single-Ended Swing**

   The transmitter output signals and the receiver input signals TXn, $\overline{\text{TXn}}$, RXn and $\overline{\text{RXn}}$ each have a peak-to-peak swing of A – B Volts. This is also referred as each signal wire's Single-Ended Swing.
2. **Differential Output Voltage, V_{OD}** (or **Differential Output Swing**):

assumes that the LVPECL clock driver's output impedance is 50Ω. R1 is used to DC-bias the LVPECL outputs prior to AC-coupling. Its value could be ranged from 140Ω to 240Ω depending on clock driver vendor's requirement. R2 is used together with the SerDes reference clock receiver's 50-Ω termination resistor to attenuate the LVPECL output's differential peak level such that it meets the MPC8315E SerDes reference clock's differential input amplitude requirement (between 200mV and 800mV differential peak). For example, if the LVPECL output's differential peak is 900mV and the desired SerDes reference clock input amplitude is selected as 600mV, the attenuation factor is 0.67, which requires R2 = 25Ω. Please consult clock driver chip manufacturer to verify whether this connection scheme is compatible with a particular clock driver chip.

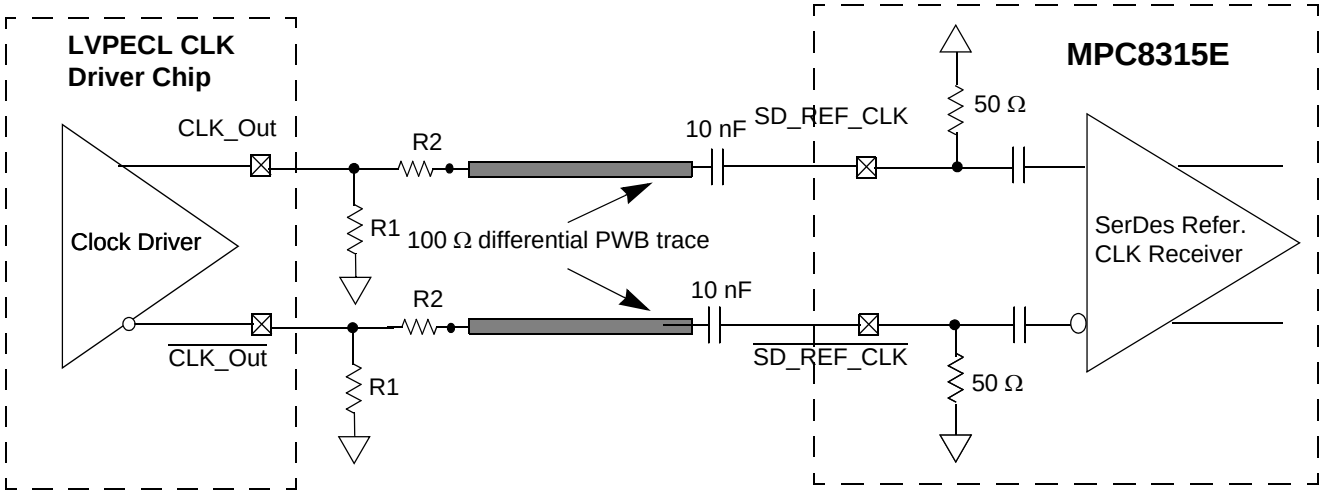


Figure 44. AC-Coupled Differential Connection with LVPECL Clock Driver (Reference Only)

This figure shows the SerDes reference clock connection reference circuits for a single-ended clock driver. It assumes the DC levels of the clock driver are compatible with MPC8315E SerDes reference clock input's DC requirement.

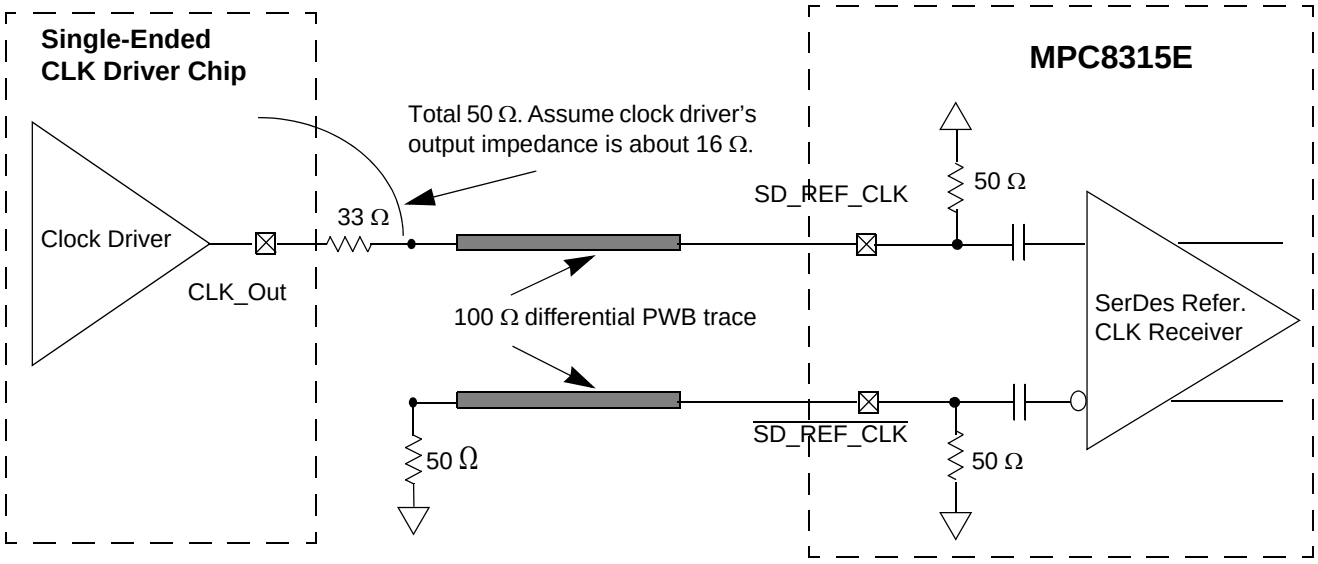


Figure 45. Single-Ended Connection (Reference Only)

15.2.4 AC Requirements for SerDes Reference Clocks

The clock driver selected should provide a high quality reference clock with low phase noise and cycle-to-cycle jitter. Phase noise less than 100KHz can be tracked by the PLL and data recovery loops and is less of a problem. Phase noise above 15MHz is filtered by the PLL. The most problematic phase noise occurs in the 1-15MHz range. The source impedance of the clock driver should be 50 Ω to match the transmission line and reduce reflections which are a source of noise to the system.

This table describes some AC parameters common to SGMII and PCI Express protocols.

Table 52. SerDes Reference Clock Common AC Parameters

At recommended operating conditions with XCOREVDD= 1.0V ± 5%

Parameter	Symbol	Min	Max	Unit	Note
Rising Edge Rate	Rise Edge Rate	1.0	4.0	V/ns	2, 3
Falling Edge Rate	Fall Edge Rate	1.0	4.0	V/ns	2, 3
Differential Input High Voltage	V_{IH}	+200	—	mV	2
Differential Input Low Voltage	V_{IL}	—	–200	mV	2
Rising edge rate (SDn_REF_CLK) to falling edge rate ($\overline{\text{SDn\_REF\_CLK}}$) matching	Rise-Fall Matching	—	20	%	1, 4

Note:

1. Measurement taken from single ended waveform.
2. Measurement taken from differential waveform.
3. Measured from -200 mV to +200 mV on the differential waveform (derived from SDn_REF_CLK minus $\overline{\text{SDn\_REF\_CLK}}$). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See Figure 46.
4. Matching applies to rising edge rate for SDn_REF_CLK and falling edge rate for $\overline{\text{SDn\_REF\_CLK}}$. It is measured using a 200 mV window centered on the median cross point where SDn_REF_CLK rising meets $\overline{\text{SDn\_REF\_CLK}}$ falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of SDn_REF_CLK should be compared to the Fall Edge Rate of $\overline{\text{SDn\_REF\_CLK}}$, the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 47.

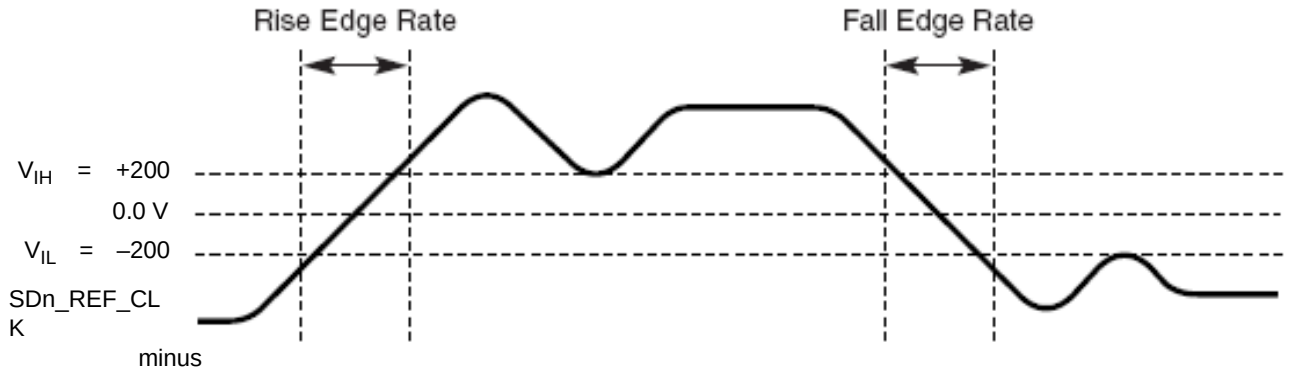


Figure 46. Differential Measurement Points for Rise and Fall Time

NOTE

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D– not being exactly matched in length at the package pin boundary.

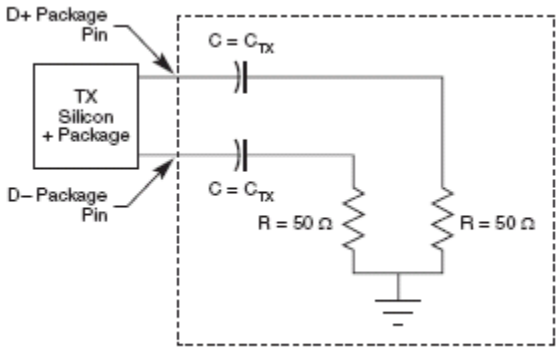


Figure 51. Compliance Test/Measurement Load

17 Timers

This section describes the DC and AC electrical specifications for the timers of the MPC8314E.

17.1 Timers DC Electrical Characteristics

This table provides the DC electrical characteristics for the timers pins, including TIN, $\overline{\text{TOUT}}$, $\overline{\text{TGATE}}$, and RTC_CLK.

Table 56. Timers DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.1	NVDD + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	0 V ≤ V_{IN} ≤ NVDD	—	± 5	μA

17.2 Timers AC Timing Specifications

This table provides the timers input and output AC timing specifications.

Table 57. Timers Input AC Timing Specifications

Characteristic	Symbol [1]	Min	Unit
Timers inputs—minimum pulse width	t_{TIWID}	20	ns

Table 66. MPC8314E TEPBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
PCI_AD[23]	C22	I/O	$NVDD2_{OFF}$	—
PCI_AD[24]	E19	I/O	$NVDD2_{OFF}$	—
PCI_AD[25]	A22	I/O	$NVDD2_{OFF}$	—
PCI_AD[26]	C20	I/O	$NVDD2_{OFF}$	—
PCI_AD[27]	B21	I/O	$NVDD2_{OFF}$	—
PCI_AD[28]	D19	I/O	$NVDD2_{OFF}$	—
PCI_AD[29]	A19	I/O	$NVDD2_{OFF}$	—
PCI_AD[30]	A21	I/O	$NVDD2_{OFF}$	—
PCI_AD[31]	B19	I/O	$NVDD2_{OFF}$	—
PCI_C/$\overline{BE}$[0]	H24	I/O	$NVDD2_{OFF}$	—
PCI_C/$\overline{BE}$[1]	C27	I/O	$NVDD2_{OFF}$	—
PCI_C/$\overline{BE}$[2]	A25	I/O	$NVDD2_{OFF}$	—
PCI_C/$\overline{BE}$[3]	E21	I/O	$NVDD2_{OFF}$	—
PCI_PAR	G24	I/O	$NVDD2_{OFF}$	—
$\overline{PCI\_FRAME}$	C28	I/O	$NVDD2_{OFF}$	5
$\overline{PCI\_TRDY}$	A24	I/O	$NVDD2_{OFF}$	5
$\overline{PCI\_IRDY}$	D25	I/O	$NVDD2_{OFF}$	5
$\overline{PCI\_STOP}$	D23	I/O	$NVDD2_{OFF}$	5
$\overline{PCI\_DEVSEL}$	E22	I/O	$NVDD2_{OFF}$	5
PCI_IDSEL	D26	I	$NVDD2_{OFF}$	—
$\overline{PCI\_SERR}$	C25	I/O	$NVDD2_{OFF}$	5
$\overline{PCI\_PERR}$	D21	I/O	$NVDD2_{OFF}$	5
$\overline{PCI\_REQ0}$	E18	I/O	$NVDD2_{OFF}$	—
$\overline{PCI\_REQ1}$/CPCI_HS_ES	C18	I	$NVDD2_{OFF}$	—
$\overline{PCI\_REQ2}$	E17	I	$NVDD2_{OFF}$	—
$\overline{PCI\_GNT0}$	B20	I/O	$NVDD2_{OFF}$	—
$\overline{PCI\_GNT1}$/CPCI_HS_LED	D17	O	$NVDD2_{OFF}$	—
$\overline{PCI\_GNT2}$/CPCI_HS_ENUM	E15	O	$NVDD2_{OFF}$	—
M66EN	L24	I	$NVDD2_{OFF}$	—
PCI_CLK0	E23	O	$NVDD2_{OFF}$	—
PCI_CLK1	F24	O	$NVDD2_{OFF}$	—
PCI_CLK2	E25	O	$NVDD2_{OFF}$	—
$\overline{PCI\_PME}$	B23	I/O	$NVDD2_{OFF}$	2
ETSEC1/_USBULPI				
GPIO_24/TSEC1_COL/USBDR_TXDRXD0	J1	I/O	$LVDD1_{OFF}$	—
GPIO_25/TSEC1_CRS/USBDR_TXDRXD1	H1	I/O	$LVDD1_{OFF}$	—

The primary clock source can be one of two inputs, SYS_CLK_IN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. When the device is configured as a PCI host device, SYS_CLK_IN is its primary input clock. SYS_CLK_IN feeds the PCI clock divider (÷2) and the multiplexors for PCI_SYNC_OUT and PCI_CLK_OUT. The $\overline{\text{CFG\_SYS\_CLKIN\_DIV}}$ configuration input selects whether SYS_CLK_IN or SYS_CLK_IN/2 is driven out on the PCI_SYNC_OUT signal.

PCI_SYNC_OUT is connected externally to PCI_SYNC_IN to allow the internal clock subsystem to synchronize to the system PCI clocks. PCI_SYNC_OUT must be connected properly to PCI_SYNC_IN, with equal delay to all PCI agent devices in the system, to allow the device to function. When the device is configured as a PCI agent device, PCI_CLK is the primary input clock. When the device is configured as a PCI agent device the SYS_CLK_IN signal should be tied to GND.

As shown in Figure 60, the primary clock input (frequency) is multiplied up by the system phase-locked loop (PLL) and the clock unit to create the coherent system bus clock (*csb_clk*), the internal clock for the DDR controller (*ddr_clk*), and the internal clock for the local bus interface unit (*lbiu_clk*).

The *csb_clk* frequency is derived from a complex set of factors that can be simplified into the following equation:

$$csb\_clk = \{\text{PCI\_SYNC\_IN} \times (1 + \sim \overline{\text{CFG\_SYS\_CLKIN\_DIV}})\} \times \text{SPMF}$$

In PCI host mode, PCI_SYNC_IN × (1 + ~ $\overline{\text{CFG\_SYS\_CLKIN\_DIV}}$) is the SYS_CLK_IN frequency.

The *csb_clk* serves as the clock input to the e300 core. A second PLL inside the e300 core multiplies up the *csb_clk* frequency to create the internal clock for the e300 core (*core_clk*). The system and core PLL multipliers are selected by the SPMF and COREPLL fields in the reset configuration word low (RCWL) which is loaded at power-on reset or by one of the hard-coded reset options. See Chapter 4, “Reset, Clocking, and Initialization,” in the *MPC8315E PowerQUICC II Pro Integrated Host Processor Family Reference Manual* for more information on the clock subsystem.

The internal *ddr_clk* frequency is determined by the following equation:

$$ddr\_clk = csb\_clk \times (1 + \text{RCWL[DDRCM]})$$

Note that *ddr_clk* is not the external memory bus frequency; *ddr_clk* passes through the DDR clock divider (÷2) to create the differential DDR memory bus clock outputs (MCK and $\overline{\text{MCK}}$). However, the data rate is the same frequency as *ddr_clk*.

The internal *lbiu_clk* frequency is determined by the following equation:

$$lbiu\_clk = csb\_clk \times (1 + \text{RCWL[LBCM]})$$

Note that *lbiu_clk* is not the external local bus frequency; *lbiu_clk* passes through the LBIU clock divider to create the external local bus clock outputs (LCLK[0:1]). The LBIU clock divider ratio is controlled by LCRR[CLKDIV].

In addition, some of the internal units may be required to be shut off or operate at lower frequency than the *csb_clk* frequency. Those units have a default clock ratio that can be configured by a memory mapped register after the device comes out of reset. Table 67 specifies which units have a configurable clock frequency.

Table 73. Suggested PLL Configurations

Conf. No.	SPMF	Core\PLL	Input Clock Frequency (MHz)	CSB Frequency (MHz)	Core Frequency (MHz)
6	0010	0000101	66.67	133.33	333.33
7	0101	0000110	25	125	375
8	0100	0000110	33.33	133.33	400
9	0010	0000110	66.67	133.33	400

24 Thermal

This section describes the thermal specifications of the MPC8314E.

24.1 Thermal Characteristics

This table provides the package thermal characteristics for the 620 29 × 29 mm TEPBGA II.

Table 74. Package Thermal Characteristics for TEPBGA II

Characteristic	Board type	Symbol	Value	Unit	Note
Junction to ambient natural convection	Single layer board (1s)	$R_{\theta JA}$	23	°C/W	1, 2
Junction to ambient natural convection	Four layer board (2s2p)	$R_{\theta JA}$	16	°C/W	1, 2, 3
Junction to ambient (@200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	18	°C/W	1, 3
Junction to ambient (@200 ft/min)	Four layer board (2s2p)	$R_{\theta JMA}$	13	°C/W	1, 3
Junction to board	—	$R_{\theta JB}$	8	°C/W	4
Junction to case	—	$R_{\theta JC}$	6	°C/W	5
Junction to package top	Natural convection	Ψ_{JT}	6	°C/W	6

Note:

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

Millennium Electronics (MEI) Loroco Sites 671 East Brokaw Road San Jose, CA 95112 Internet: www.mei-thermal.com	408-436-8770
Tyco Electronics Chip Coolers™ P.O. Box 3668 Harrisburg, PA 17105 Internet: www.tycoelectronics.com	800-522-6752
Wakefield Engineering 33 Bridge St. Pelham, NH 03076 Internet: www.wakefield.com	603-635-2800

Interface material vendors include the following:

Chomerics, Inc. 77 Dragon Ct. Woburn, MA 01801 Internet: www.chomerics.com	781-935-4850
Dow-Corning Corporation Corporate Center PO BOX 994 Midland, MI 48686-0994 Internet: www.dowcorning.com	800-248-2481
Shin-Etsu MicroSi, Inc. 10028 S. 51st St. Phoenix, AZ 85044 Internet: www.microsi.com	888-642-7674
The Bergquist Company 18930 West 78th St. Chanhassen, MN 55317 Internet: www.bergquistcompany.com	800-347-4572

24.3 Heat Sink Attachment

When attaching heat sinks to these devices, an interface material is required. The best method is to use thermal grease and a spring clip. The spring clip should connect to the printed circuit board, either to the board itself, to hooks soldered to the board, or to a plastic stiffener. Avoid attachment forces which would lift the edge of the package or peel the package from the board. Such peeling forces reduce the solder joint lifetime of the package. Recommended maximum force on the top of the package is 10 lb force (45 Newtons). If an adhesive attachment is planned, the adhesive should be intended for attachment to painted or plastic surfaces and its performance verified under the application requirements.

Power and ground connections must be made to all external VDD, GVDD, LVDD, NVDD, and GND pins of the device.

25.5 Output Buffer DC Impedance

The MPC8314E drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I^2C).

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to NVDD or GND. Then, the value of each resistor is varied until the pad voltage is NVDD/2 (see Figure 62). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and R_P is trimmed until the voltage at the pad equals NVDD/2. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

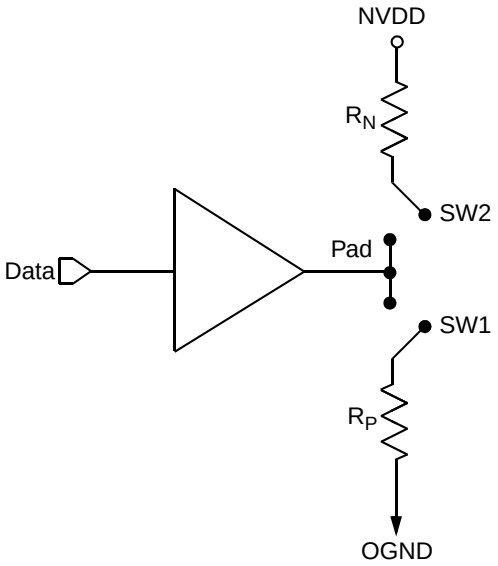


Figure 62. Driver Impedance Measurement

The value of this resistance and the strength of the driver's current source can be found by making two measurements. First, the output voltage is measured while driving logic 1 without an external differential termination resistor. The measured voltage is $V_1 = R_{source} \times I_{source}$. Second, the output voltage is measured while driving logic 1 with an external precision differential termination resistor of value R_{term}. The measured voltage is $V_2 = (1/(1/R_1 + 1/R_2)) \times I_{source}$. Solving for the output impedance gives $R_{source} = R_{term} \times (V_1/V_2 - 1)$. The drive current is then $I_{source} = V_1/R_{source}$.