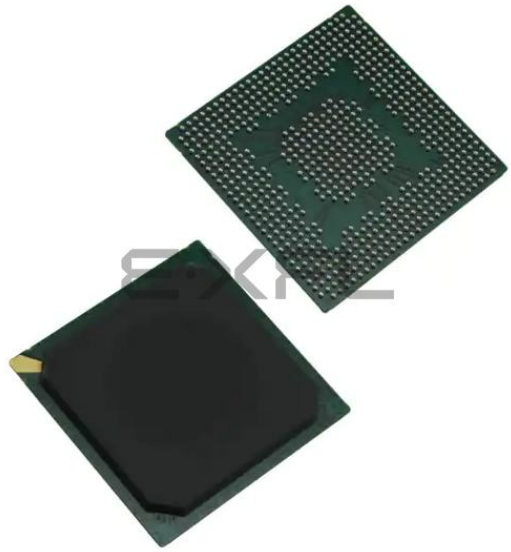

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

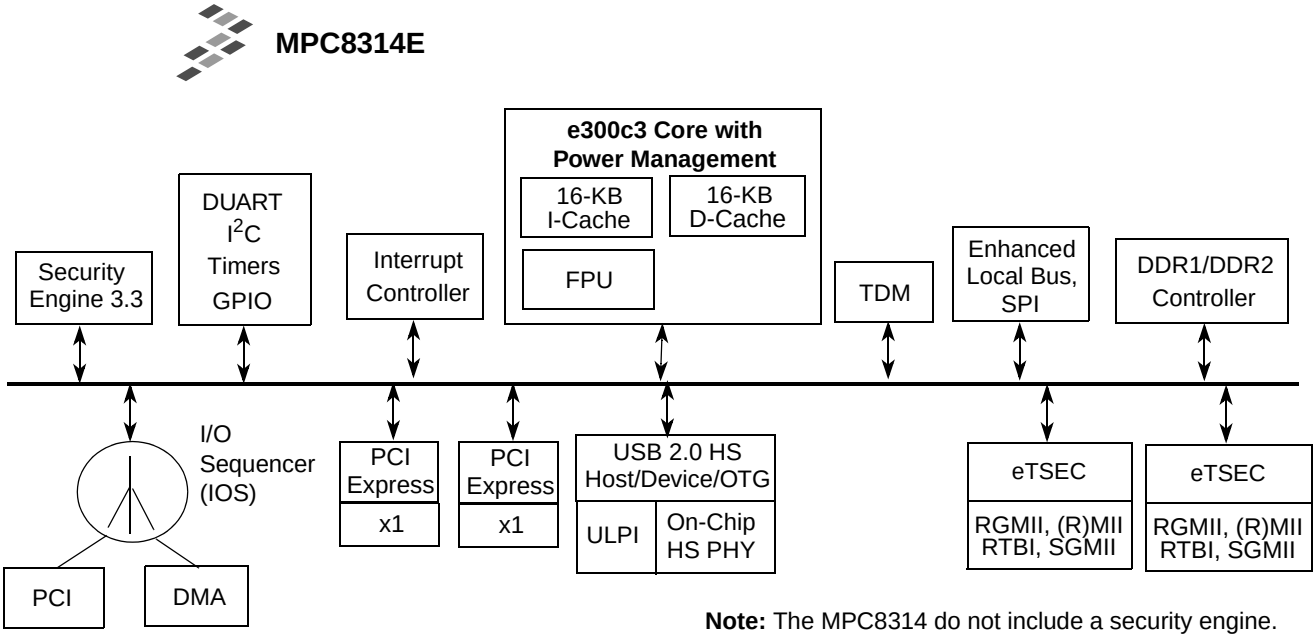
Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	PowerPC e300c3
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	400MHz
Co-Processors/DSP	Security; SEC 3.3
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 + PHY (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	-40°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	620-BBGA Exposed Pad
Supplier Device Package	620-HBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8314ecvragda

1 Overview

The MPC8314E incorporates the e300c3 (MPC603e-based) core, which includes 16 Kbytes of L1 instruction and data caches, on-chip memory management units (MMUs), and floating-point support. In addition to the e300 core, the SoC platform includes features such as dual enhanced three-speed 10, 100, 1000 Mbps Ethernet controllers (eTSECs) with SGMII support, a 32- or 16-bit DDR1/DDR2 SDRAM memory controller, a security engine to accelerate control and data plane security protocols, and a high degree of software compatibility with previous-generation PowerQUICC processor-based designs for backward compatibility and easier software migration. The MPC8314E also offers peripheral interfaces such as a 32-bit PCI interface with up to 66 MHz operation, 16-bit enhanced local bus interface with up to 66 MHz operation, TDM interface, and USB 2.0 with an on-chip USB 2.0 PHY.

8314E offers additional high-speed interconnect support with dual single-lane PCI Express interfaces. When not used for PCI Express, the SerDes interface may be configured to support SGMII. The MPC8314E security engine (SEC 3.3) allows CPU-intensive cryptographic operations to be offloaded from the main CPU core. This figure shows a block diagram of the MPC8314E.



Note: The MPC8314 do not include a security engine.

Figure 1. MPC8314E Block Diagram

2 MPC8314E Features

The following features are supported in the MPC8314E.

2.1 e300 Core

The e300 core has the following features:

- Operates at up to 400 MHz
- 16-Kbyte instruction cache, 16-Kbyte data cache

  - Combines a True Random Number Generator (TRNG) and a NIST-approved Pseudo-Random Number Generator (PRNG) (as described in Annex C of FIPS140-2 and ANSI X9.62).
- Cyclical Redundancy Check Hardware Accelerator (CRCA)
  - Implements CRC32C as required for iSCSI header and payload checksums, CRC32 as required for IEEE 802 packets, as well as for programmable 32 bit CRC polynomials

2.4 DDR Memory Controller

The DDR1/DDR2 memory controller includes the following features:

- Single 16- or 32-bit interface supporting both DDR1 and DDR2 SDRAM
- Support for up to 266 MHz data rate
- Support for two physical banks (chip selects), each bank independently addressable
- 64-Mbit to 2-Gbit (for DDR1) and to 4-Gbit (for DDR2) devices with x8/x16 data ports (no direct x4 support)
- Support for one 16-bit device or two 8-bit devices on a 16-bit bus or two 16-bit devices on a 32-bit bus
- Support for up to 16 simultaneous open pages
- Supports auto refresh
- On-the-fly power management using CKE
- 1.8-/2.5-V SSTL2 compatible I/O

2.5 PCI Controller

The PCI controller includes the following features:

- Designed to comply with *PCI Local Bus Specification Revision 2.3*
- Single 32-bit data PCI interface operates at up to 66 MHz
- PCI 3.3-V compatible (not 5-V compatible)
- Support for host and agent modes
- On-chip arbitration, supporting three external masters on PCI
- Selectable hardware-enforced coherency

2.6 TDM Interface

The TDM interface includes the following features:

- Independent receive and transmit with dedicated data, clock and frame sync line
- Separate or shared RCK and TCK whose source can be either internal or external
- Glueless interface to E1/T1 frames and MVIP, SCAS, and H.110 buses
- Up to 128 time slots, where each slot can be programmed to be active or inactive
- 8- or 16-bit word widths
- The TDM Transmitter Sync Signal (TFS), Transmitter Clock Signal (TCK) and Receiver Clock

Table 1. Absolute Maximum Ratings [1] (continued)

Characteristic		Symbol	Max Value	Unit	Note
DDR2 DRAM I/O supply voltage		GVDD	–0.3 to 1.9	V	—
PCI, local bus, DUART, system control and power management, I^2C, Ethernet management, 1588 timer and JTAG I/O voltage		NVDD	–0.3 to 3.6	V	7
USB, and eTSEC I/O voltage		LVDD	–0.3 to 2.75 or –0.3 to 3.6	V	6, 8
PHY voltage	USB PHY	USB_PLL_PWR1	–0.3 to 1.26	V	—
		USB_PLL_PWR3, USB_VDDA_BIAS, VDDA	–0.3 to 3.6	V	—
	SERDES PHY	XCOREVDD, XPADVDD, SDAVDD	–0.3 to 1.26	V	—
Input voltage	DDR DRAM signals	MV_{IN}	–0.3 to (GVDD + 0.3)	V	2, 4
	DDR DRAM reference	MVREF	–0.3 to (GVDD + 0.3)	V	2, 4
	eTSEC signals	LV_{IN}	–0.3 to (LVDD + 0.3)	V	3, 4
	Local bus, DUART, SYS_CLK_IN, system control and power management, I^2C, and JTAG signals	NV_{IN}	–0.3 to (NVDD + 0.3)	V	3, 4
	PCI	NV_{IN}	–0.3 to (NVDD + 0.3)	V	5
Storage temperature range		T_{STG}	–55 to150	°C	—

Note:

1. Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution:** MV_{IN} must not exceed GVDD by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
3. **Caution:** (N,L)V_{IN} must not exceed (N,L)VDD by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. (M,N,L)V_{IN} and MVREF may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.
5. NV_{IN} on the PCI interface may overshoot/undershoot according to the PCI Electrical Specification for 3.3-V operation, as shown in Figure 2.
6. The max value of supply voltage should be selected based on the RGMII mode.
7. NVDD means NVDD1_OFF, NVDD1_ON, NVDD2_OFF, NVDD2_ON, NVDD3_OFF, NVDD4_OFF
8. LVDD means LVDD1_OFF and LVDD2_ON

3.1.2 Power Supply Voltage Specification

This table provides the recommended operating conditions for theMPC8314E. Note that the values in this table are the recommended and tested operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 2. Recommended Operating Conditions

Characteristic	Symbol	Recommended Value[1]	Unit	Status in D3 Warm mode	Note
SerDes internal digital power	XCOREVDD	1.0 ± 50 mv	V	Switched Off	—
SerDes internal digital power	XCOREVSS	0.0	V	—	—
SerDes I/O digital power	XPADVDD	1.0 ± 50 mv	V	Switched Off	—
SerDes I/O digital power	XPADVSS	0.0	V	—	—
SerDes analog power for PLL	SDAVDD	1.0 ± 50 mv	V	Switched Off	—
SerDes analog power for PLL	SDAVSS	0.0	V	—	—
Dedicated 3.3 V analog power for USB PLL	USB_PLL_PWR3	3.3 ± 165mv	V	Switched Off	—
Dedicated 1.0 Vanalog power for USB PLL	USB_PLL_PWR1	1.0 ± 50 mv	V	Switched Off	—
Dedicated analog ground for USB PLL	USB_PLL_GND	0.0	V	—	—
Dedicated USB power for USB bias circuit	USB_VDDA_BIAS	3.3 ± 300 mv	V	Switched Off	—
Dedicated USB ground for USB bias circuit	USB_VSSA_BIAS	0.0	V	—	—
Dedicated power for USB transceiver	USB_VDDA	3.3 ± 300 mv	V	Switched Off	—
Dedicated ground for USB transceiver	USB_VSSA	0.0	V	—	—
Core supply voltage	VDD	1.0 ± 50 mv	V	Switched Off	—
Core supply voltage	VDDC	1.0 ± 50 mv	V	Switched On	—
Analog power for e300 core APLL	AVDD1	1.0 ± 50 mv	V	Switched Off	6
Analog power for system APLL	AVDD2	1.0 ± 50 mv	V	Switched On	6
DDR and DDR2 DRAM I/O voltage	GVDD	2.5 ± 200 mv 1.8 ± 100 mv	V	Switched Off	—
Differential reference voltage for DDR and DDR2 controller	MVREF	GVDD /2	V	Switched Off	—
Standard I/O voltage	NVDD1_ON	3.3 ± 300 mv	V	Switched On	1
Standard I/O voltage	NVDD2_ON	3.3 ± 300 mv	V	Switched On	1
Standard I/O voltage	NVDD1_OFF	3.3 ± 300 mv	V	Switched Off	2
Standard I/O voltage	NVDD2_OFF	3.3 ± 300 mv	V	Switched Off	2
Standard I/O voltage	NVDD3_OFF	3.3 ± 300 mv	V	Switched Off	2
Standard I/O voltage	NVDD4_OFF	3.3 ± 300 mv	V	Switched Off	2
eTSEC/USBdr I/O supply	LVDD1_OFF	2.5 ± 125 mv 3.3 ± 300 mv	V	Switched Off	—
eTSEC I/O supply	LVDD2_ON	2.5 ± 125 mv 3.3 ± 300 mv	V	Switched On	—
Analog and digital ground	VSS	0.0	V	—	—
Junction temperature range	T_A/T_J	0 to105	°C	—	3

CAUTION

When the device is in D3 warm (standby) mode, all external voltage supplies applied to any I/O pins, with the exception of wake-up pins, must be turned off. Applying supplied external voltage to any I/O pins, except the wake up pins, while the device is in D3 warm standby mode may cause permanent damage to the device.

An example of the power-up sequence is shown in Figure 4 when implemented along with low power D3 warm mode.

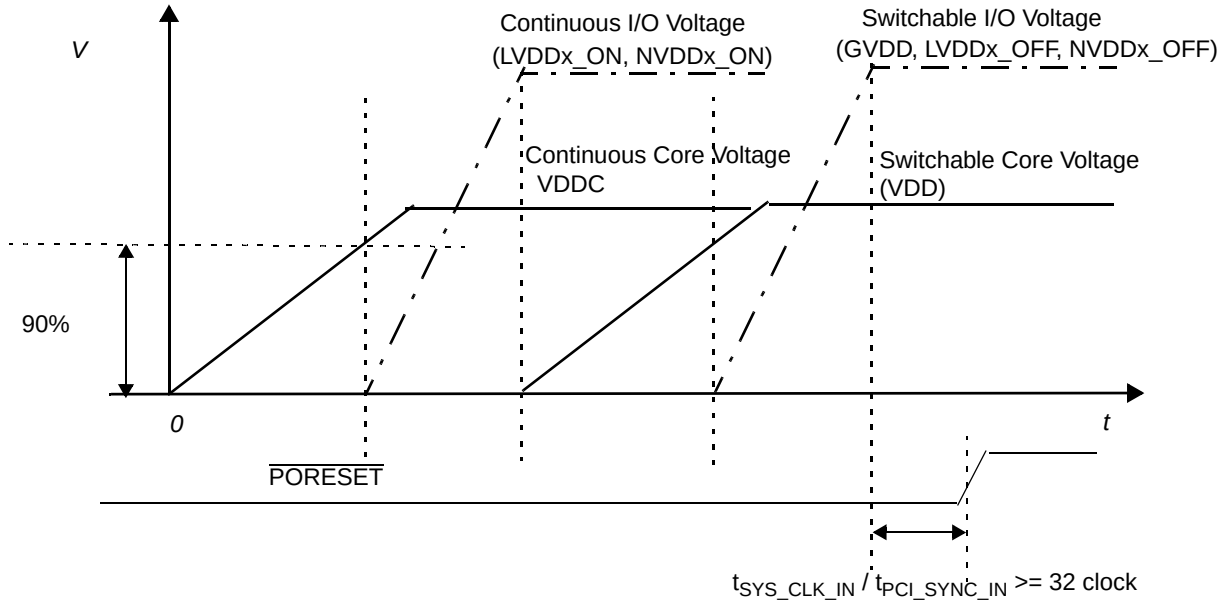


Figure 4. Power Up Sequencing Example with Low power D3 Warm Mode

4 Power Characteristics

This table shows the estimated typical power dissipation for this family of devices.

Table 4. MPC8314E Power Dissipation

(Does not include I/O power dissipation)

Core Frequency (MHz)	CSB Frequency (MHz)	Typical [1,3]	Maximum [1,2]	Unit
266	133	1.116	1.646	W
333	133	1.142	1.665	W
400	133	1.167	1.690	W

Note:

1. The values do not include I/O supply power, but do include core, AVDD, USB PLL, and digital SerDes power.
2. Maximum power is based on a voltage of V_{dd} = 1.05V, a junction temperature of T_j = 105°C, and an artificial smoker test.
3. Typical power is based on a voltage of V_{dd} = 1.05V, and an artificial smoker test running at room temperature.

This table shows the estimated typical I/O power dissipation for this family of devices.

Table 5. MPC8314E Power Dissipation

Interface	Frequency	GV_{DD} (1.8 V)	GV_{DD} (2.5 V)	NV_{DD} (3.3 V)	LVDD1_OFF/ LVDD2_ON (3.3V)	LVDD2 _ON (3.3V)	VDD33PLL, VDD33ANA (3.3V)	SATA_VDD, VDD1IO, VDD1ANA (1.0V)	XCOREVDD, XPADVDD, SDAVDD (1.0V)	Unit
DDR 1 Rs = 22Ω Rt = 50Ω	266MHz, 32 bits	—	0.323	—	—	—	—	—	—	W
	200MHz, 32 bits	—	0.291	—	—	—	—	—	—	W
DDR 2 Rs = 22Ω Rt = 75Ω	266MHz, 32 bits	0.246	—	—	—	—	—	—	—	W
	200MHz, 32bits	0.225	—	—	—	—	—	—	—	W
PCI I/O load = 50pF	33 MHz	—	—	0.120	—	—	—	—	—	W
	66 MHz	—	—	0.249	—	—	—	—	—	W
Local bus I/O load = 20pF	66 MHz	—	—	—	—	0.056	—	—	—	W
	50 MHz	—	—	—	—	0.040	—	—	—	W
eTSEC I/O load = 20pF Multiple by number of interface used	MII, 25MHz	—	—	—	0.008	—	—	—	—	W
	RGMII, 125MHz (3.3V)	—	—	—	0.078	—	—	—	—	W
	RGMII, 125MHz (2.5V)	—	—	—	0.044	—	—	—	—	W
USBDR Controller (ULPI mode) load =20pF	60 MHz	—	—	—	0.078	—	—	—	—	W
USBDR+ Internal PHY (UTMI mode)	480 MHz	—	—	—	0.274	—	—	—	—	W
PCI Express two x1lane	2.5 GHz	—	—	—	—	—	—	—	0.190	W
Other I/O	—	—	—	0.015	—	—	—	—	—	W

5 Clock Input Timing

This section provides the clock input DC and AC electrical characteristics for the MPC8314E.

This table provides the DDR2 capacitance when GVDD(typ) = 1.8 V.

Table 12. DDR2 SDRAM Capacitance for GVDD(typ) = 1.8 V

Parameter/Condition	Symbol	Min	Max	Unit	Note
Input/output capacitance: DQ, DQS	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. GVDD = 1.8 V ± 0.090 V, f = 1 MHz, T_A = 25°C, V_{OUT} = GVDD/2, V_{OUT} (peak-to-peak) = 0.2 V.

This table provides the recommended operating conditions for the DDR SDRAM component(s) of the MPC8314E when GVDD(typ) = 2.5 V.

Table 13. DDR SDRAM DC Electrical Characteristics for GVDD(typ) = 2.5 V

Parameter/Condition	Symbol	Min	Max	Unit	Note
I/O supply voltage	GVDD	2.3	2.7	V	1
I/O reference voltage	MVREF	0.49 × GVDD	0.51 × GVDD	V	2
I/O termination voltage	V_{TT}	MVREF – 0.04	MVREF + 0.04	V	3
Input high voltage	V_{IH}	MVREF + 0.15	GVDD + 0.3	V	—
Input low voltage	V_{IL}	–0.3	MVREF – 0.15	V	—
Output leakage current	I_{OZ}	–9.9	–9.9	μA	4
Output high current (V_{OUT} = 1.95 V, GVDD = 2.3V)	I_{OH}	–16.2	—	mA	—
Output low current (V_{OUT} = 0.35 V)	I_{OL}	16.2	—	mA	—

Note:
1. GVDD is expected to be within 50 mV of the DRAM GVDD at all times.
2. MVREF is expected to be equal to 0.5 × GVDD, and to track GVDD DC variations as measured at the receiver. Peak-to-peak noise on MVREF may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MVREF. This rail should track variations in the DC level of MVREF.
4. Output leakage is measured with all outputs disabled, 0 V ≤ V_{OUT} ≤ GVDD.

This table provides the DDR capacitance when GVDD(typ) = 2.5 V.

Table 14. DDR SDRAM Capacitance for GVDD(typ) = 2.5 V Interface

Parameter/Condition	Symbol	Min	Max	Unit	Note
Input/output capacitance: DQ,DQS	C_{IO}	6	8	pF	1
Delta input/output capacitance: DQ, DQS	C_{DIO}	—	0.5	pF	1

Note:
1. This parameter is sampled. GVDD = 2.5 V ± 0.125 V, f = 1 MHz, T_A = 25°C, V_{OUT} = GVDD/2, V_{OUT} (peak-to-peak) = 0.2 V.

This table provides the current draw characteristics for MV_{REF}.

Table 15. Current Draw Characteristics for MV_{REF}

Parameter / Condition	Symbol	Min	Max	Unit	Note
Current draw for MV_{REF}	I_{MVREF}	—	500	μA	1

This figure provides the AC test load for the DDR bus.

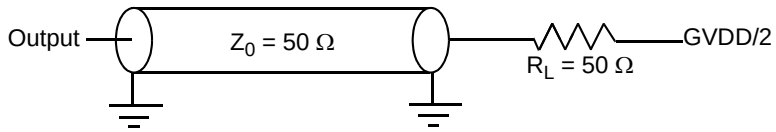


Figure 8. DDR AC Test Load

8 DUART

This section describes the DC and AC electrical specifications for the DUART interface.

8.1 DUART DC Electrical Characteristics

This table lists the DC electrical characteristics for the DUART interface.

Table 21. DUART DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2.1	NVDD + 0.3	V
Low-level input voltage NVDD	V_{IL}	–0.3	0.8	V
High-level output voltage, I_{OH} = –100 μA	V_{OH}	NVDD – 0.2	—	V
Low-level output voltage, I_{OL} = 100 μA	V_{OL}	—	0.2	V
Input current (0 V ≤V_{IN} ≤ NVDD)	I_{IN}	—	± 5	μA

8.2 DUART AC Electrical Specifications

This table lists the AC timing parameters for the DUART interface.

Table 22. DUART AC Timing Specifications

Parameter	Value	Unit	Note
Minimum baud rate	256	baud	—
Maximum baud rate	> 1,000,000	baud	1
Oversample rate	16	—	2

Note:
1. Actual attainable baud rate is limited by the latency of interrupt processing.
2. The middle of a start bit is detected as the eighth sampled 0 after the 1-to-0 transition of the start bit. Subsequent bit values are sampled each sixteenth sample.

9 Ethernet: Three-Speed Ethernet, MII Management

This section provides the AC and DC electrical characteristics for three-speed, 10/100/1000, and MII management.

This figure shows the RGMII and RTBI AC timing and multiplexing diagrams.

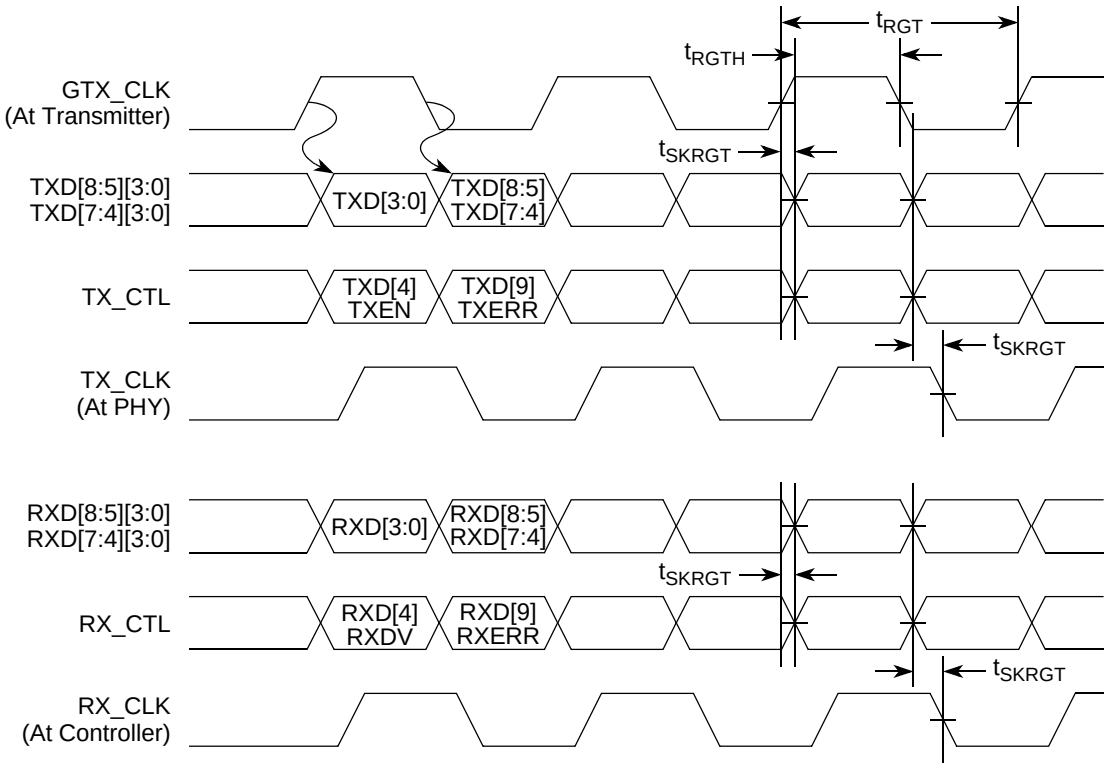


Figure 15. RGMII and RTBI AC Timing and Multiplexing Diagrams

9.3 Ethernet Management Interface Electrical Characteristics

The electrical characteristics specified here apply to MII management interface signals management data input/output (MDIO) and management data clock (MDC). The electrical characteristics for MII, RMII, RGMII, and RTBI are specified in Section 9.1, "eTSEC (10/100/1000 Mbps)—MII/RMII/RGMII/RTBI Electrical Characteristics."

9.3.1 MII Management DC Electrical Characteristics

The MDC and MDIO are defined to operate at a supply voltage of 3.3 V. The DC electrical characteristics for MDIO and MDC are provided in this table.

Table 30. MII Management DC Electrical Characteristics Powered at 3.3 V

Parameter	Symbol	Conditions		Min	Max	Unit
Supply voltage (3.3 V)	NVDD	—	—	3.0	3.6	V
Output high voltage	V_{OH}	I_{OH} = –1.0 mA	NVDD = Min	2.10	NVDD + 0.3	V
Output low voltage	V_{OL}	I_{OL} = 1.0 mA	NVDD = Min	V_{SS}	0.50	V
Input high voltage	V_{IH}	—	—	2.00	—	V
Input low voltage	V_{IL}	—	—	—	0.80	V
Input high current	I_{IH}	NVDD = Max	V_{IN} [1] = 2.1 V	—	40	μA

Table 33. 1588 Timer AC Specifications (continued)

Parameter	Symbol	Min	Max	Unit	Note

Note:
1. The timer can operate on rtc_clock or tmr_clock. These clocks get muxed and any one of them can be selected.
2. Asynchronous signals.
3. Inputs need to be stable at least one TMR clock.

9.5 SGMII Interface Electrical Characteristics

Each SGMII port features a 4-wire AC-Coupled serial link from the dedicated SerDes interface of MPC8315E as shown in Figure 17, where C_{TX} is the external (on board) AC-Coupled capacitor. Each output pin of the SerDes transmitter differential pair features 50-Ω output impedance. Each input of the SerDes receiver differential pair features 50-Ω on-die termination to XCOREVSS. The reference circuit of the SerDes transmitter and receiver is shown in Figure 48.

When an eTSEC port is configured to operate in SGMII mode, the parallel interface's output signals of this eTSEC port can be left floating. The input signals should be terminated based on the guidelines described in Section 25.4, "Connection Recommendations," as long as such termination does not violate the desired POR configuration requirement on these pins, if applicable.

When operating in SGMII mode, the TSEC_GTX_CLK125 clock is not required for this port. Instead, SerDes reference clock is required on SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ pins.

9.5.1 DC Requirements for SGMII SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$

The characteristics and DC requirements of the separate SerDes reference clock are described in Section 15, "High-Speed Serial Interfaces (HSSI)."

9.5.2 AC Requirements for SGMII SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$

This table lists the SGMII SerDes reference clock AC requirements. Please note that SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ are not intended to be used with, and should not be clocked by, a spread spectrum clock source.

Table 34. SD_REF_CLK and $\overline{\text{SD\_REF\_CLK}}$ AC Requirements

Symbol	Parameter Description	Min	Typical	Max	Unit	Note
t_{REF}	REFCLK cycle time	—	8	—	ns	—
t_{REFCJ}	REFCLK cycle-to-cycle jitter. Difference in the period of any two adjacent REFCLK cycles	—	—	100	ps	—
t_{REFPJ}	Phase jitter. Deviation in edge location with respect to mean edge location	–50	—	50	ps	—

9.5.3 SGMII Transmitter and Receiver DC Electrical Characteristics

Table 35 and Table 36 describe the SGMII SerDes transmitter and receiver AC-coupled DC electrical characteristics. Transmitter DC characteristics are measured at the transmitter outputs (SD_TX[n] and $\overline{\text{SD\_TX[n]}}$) as depicted in Figure 16.

Table 35. SGMII DC Transmitter Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply Voltage	XCOREVDD	0.95	1.0	1.05	V	—
Output high voltage	VOH	—	—	$XCOREVDD_{-Typ}/2 + \lvert V_{OD}\rvert_{-max}/2$	mV	1
Output low voltage	VOL	$XCOREVDD_{-Typ}/2 - \lvert V_{OD}\rvert_{-max}/2$	—	—	mV	1
Output ringing	V_{RING}	—	—	10	%	—
Output differential voltage[2, 3, 5]	$\lvert V_{OD}\rvert$	323	500	725	mV	Equalization setting: 1.0x
		296	459	665		Equalization setting: 1.09x
		269	417	604		Equalization setting: 1.2x
		243	376	545		Equalization setting: 1.33x
		215	333	483		Equalization setting: 1.5x
		189	292	424		Equalization setting: 1.71x
		162	250	362		Equalization setting: 2.0x
Output offset voltage	V_{OS}	425	500	575	mV	1, 4
Output impedance (single-ended)	R_O	40	—	60	Ω	—
Mismatch in a pair	ΔR_O	—	—	10	%	—
Change in V_{OD} between “0” and “1”	$\Delta \lvert V_{OD}\rvert$	—	—	25	mV	—
Change in V_{OS} between “0” and “1”	ΔV_{OS}	—	—	25	mV	—
Output current on short to GND	I_{SA}, I_{SB}	—	—	40	mA	—

Note:

1. This will not align to DC-coupled SGMII. $XCOREVDD_{-Typ}$=1.0V.
2. $\lvert V_{OD}\rvert = \lvert V_{TXn} - V_{\overline{TXn}}\rvert$. $\lvert V_{OD}\rvert$ is also referred as output differential peak voltage. $V_{TX-DIFFp-p} = 2*\lvert V_{OD}\rvert$.
3. The $\lvert V_{OD}\rvert$ value shown in the table assumes the following transmit equalization setting in the TXEQA (for SerDes lane A) or TXEQE (for SerDes lane E) bit field of MPC8315E’s SerDes Control Register 0:
   - The LSbits (bit [1:3]) of the above bit field is set based on the equalization setting shown in table.
4. V_{OS} is also referred to as output common mode voltage.
5. The $\lvert V_{OD}\rvert$ value shown in the Typ column is based on the condition of $XCOREVDD_{-Typ}$=1.0V, no common mode offset variation (V_{OS} = 500 mV), SerDes transmitter is terminated with 100-Ω differential load between TX[n] and $\overline{TX}$[n].

This figure shows the AC timing diagram for the I^2C bus.

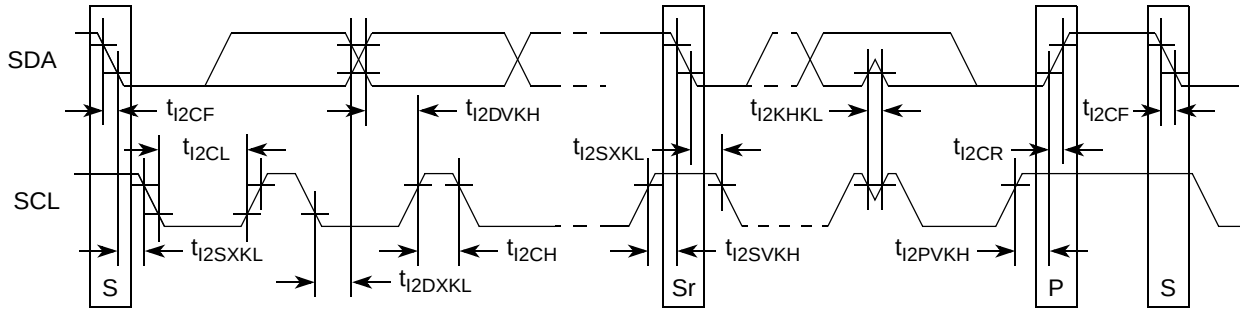


Figure 33. I^2C Bus AC Timing Diagram

14 PCI

This section describes the DC and AC electrical specifications for the PCI bus of the MPC8314E.

14.1 PCI DC Electrical Characteristics

This table provides the DC electrical characteristics for the PCI interface.

Table 49. PCI DC Electrical Characteristics [1]

Parameter	Symbol	Test Condition	Min	Max	Unit
High-level input voltage	V_{IH}	$V_{OUT} \geq V_{OH}$ (min) or	0.5 x NVDD	NVDD + 0.3	V
Low-level input voltage	V_{IL}	$V_{OUT} \leq V_{OL}$ (max)	–0.5	0.3 × NVDD	V
High-level output voltage	V_{OH}	NVDD = min, I_{OH} = –500 µA	0.9 x NVDD	—	V
Low-level output voltage	V_{OL}	NVDD = min, I_{OL} = 1500 µA	—	0.1 x NVDD	V
Input current	I_{IN}	0 V ≤ V_{IN} ≤ NVDD	—	± 10	µA

Note:
1. The symbol V_{IN}, in this case, represents the NV_{IN} symbol referenced in Table 1 and Table 2.

14.2 PCI AC Electrical Specifications

This section describes the general AC timing parameters of the PCI bus. Note that the PCI_CLK or PCI_SYNC_IN signal is used as the PCI input clock depending on whether the MPC8314E is configured as a host or agent device. This table shows the PCI AC timing specifications at 66 MHz.

Table 50. PCI AC Timing Specifications at 66 MHz

Parameter	Symbol [1]	Min	Max	Unit	Note
Clock to output valid	t_{PCKHOV}	—	6.0	ns	2
Output hold from clock	t_{PCKHOX}	1	—	ns	2
Clock to output high impedance	t_{PCKHOZ}	—	14	ns	2, 3
Input setup to clock	t_{PCIVKH}	3.3	—	ns	2, 4

15.2.4 AC Requirements for SerDes Reference Clocks

The clock driver selected should provide a high quality reference clock with low phase noise and cycle-to-cycle jitter. Phase noise less than 100KHz can be tracked by the PLL and data recovery loops and is less of a problem. Phase noise above 15MHz is filtered by the PLL. The most problematic phase noise occurs in the 1-15MHz range. The source impedance of the clock driver should be 50 Ω to match the transmission line and reduce reflections which are a source of noise to the system.

This table describes some AC parameters common to SGMII and PCI Express protocols.

Table 52. SerDes Reference Clock Common AC Parameters

At recommended operating conditions with XCOREVDD= 1.0V ± 5%

Parameter	Symbol	Min	Max	Unit	Note
Rising Edge Rate	Rise Edge Rate	1.0	4.0	V/ns	2, 3
Falling Edge Rate	Fall Edge Rate	1.0	4.0	V/ns	2, 3
Differential Input High Voltage	V_{IH}	+200	—	mV	2
Differential Input Low Voltage	V_{IL}	—	–200	mV	2
Rising edge rate (SDn_REF_CLK) to falling edge rate ($\overline{\text{SDn\_REF\_CLK}}$) matching	Rise-Fall Matching	—	20	%	1, 4

Note:

1. Measurement taken from single ended waveform.
2. Measurement taken from differential waveform.
3. Measured from -200 mV to +200 mV on the differential waveform (derived from SDn_REF_CLK minus $\overline{\text{SDn\_REF\_CLK}}$). The signal must be monotonic through the measurement region for rise and fall time. The 400 mV measurement window is centered on the differential zero crossing. See Figure 46.
4. Matching applies to rising edge rate for SDn_REF_CLK and falling edge rate for $\overline{\text{SDn\_REF\_CLK}}$. It is measured using a 200 mV window centered on the median cross point where SDn_REF_CLK rising meets $\overline{\text{SDn\_REF\_CLK}}$ falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of SDn_REF_CLK should be compared to the Fall Edge Rate of $\overline{\text{SDn\_REF\_CLK}}$, the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 47.

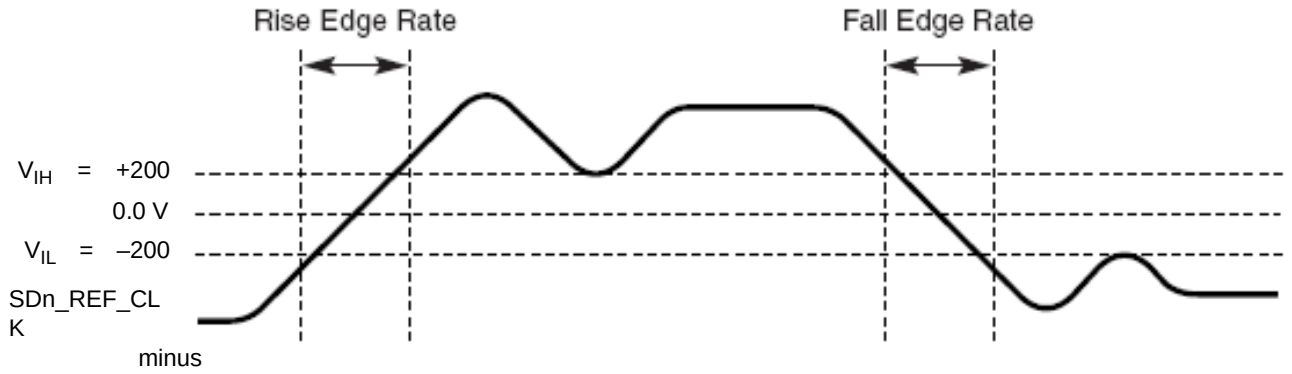


Figure 46. Differential Measurement Points for Rise and Fall Time

This figure provides the AC test load for the GPIO.

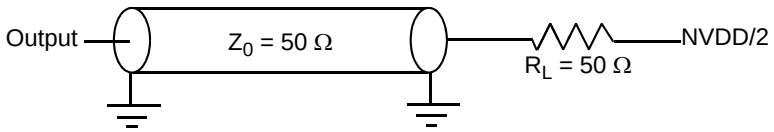


Figure 53. GPIO AC Test Load

19 IPIC

This section describes the DC and AC electrical specifications for the external interrupt pins of the MPC8314E.

19.1 IPIC DC Electrical Characteristics

This table provides the DC electrical characteristics for the external interrupt pins.

Table 60. IPIC DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.1	NVDD + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	—	—	±5	μA
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

19.2 IPIC AC Timing Specifications

This table provides the IPIC input and output AC timing specifications.

Table 61. IPIC Input AC Timing Specifications

Characteristic	Symbol [1]	Min	Unit
IPIC inputs—minimum pulse width	t_{PIWID}	20	ns

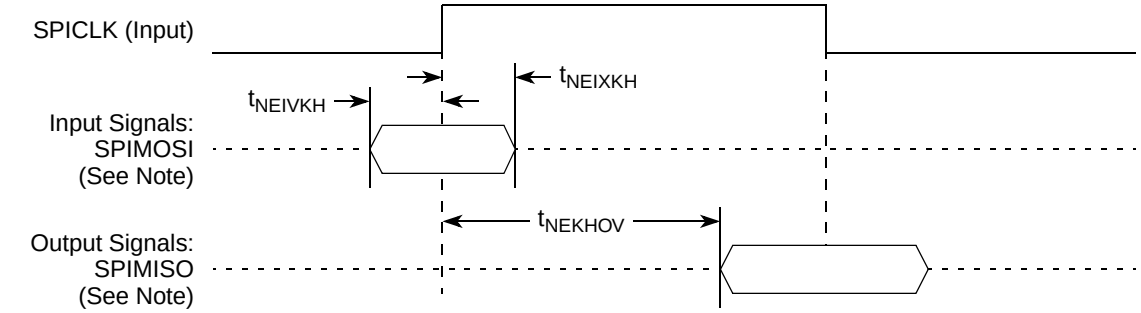
Note:

1. IPIC inputs and outputs are asynchronous to any visible clock. IPIC outputs should be synchronized before use by any external synchronous logic. IPIC inputs are required to be valid for at least t_{PIWID} ns to ensure proper operation when working in edge triggered mode.

20 SPI

This section describes the DC and AC electrical specifications for the SPI of the MPC8314E.

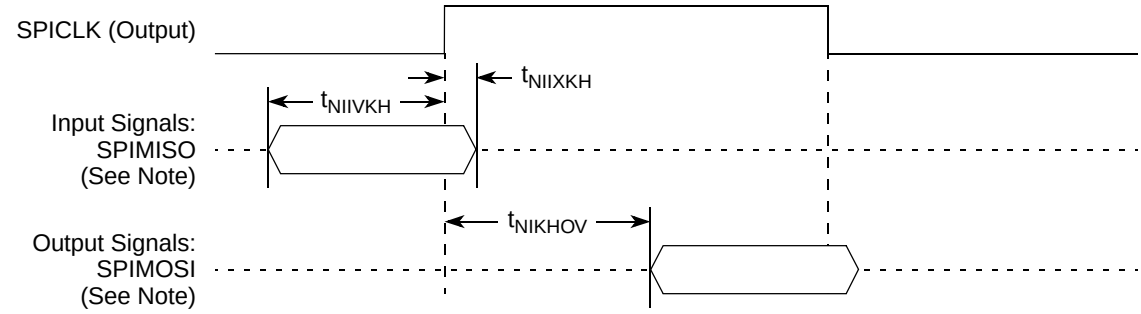
This figure shows the SPI timing in slave mode (external clock).



Note: The clock edge is selectable on SPI.

Figure 55. SPI AC Timing in Slave Mode (External Clock) Diagram

This figure shows the SPI timing in master mode (internal clock).



Note: The clock edge is selectable on SPI.

Figure 56. SPI AC Timing in Master Mode (Internal Clock) Diagram

21 TDM

This section describes the DC and AC electrical specifications for the TDM of the MPC8314E.

21.1 TDM DC Electrical Characteristics

This table provides the DC electrical characteristics TDM.

Table 64. TDM DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.1	NVDD + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	0 V ≤ V_{IN} ≤ NVDD	—	± 5	μA

Table 66. MPC8314E TEPBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
LGPL1/LFALE	AA28	O	$NVDD3_{OFF}$	—
LGPL2/$\overline{\text{LFRE}}$/$\overline{\text{LOE}}$	Y25	O	$NVDD3_{OFF}$	11
LGPL3/$\overline{\text{LFWP}}$	Y24	O	$NVDD3_{OFF}$	—
LGPL4/$\overline{\text{LGTA}}$/LUPWAIT/$\overline{\text{LFRB}}$	AA26	I/O	$NVDD3_{OFF}$	2
LGPL5	AF22	O	$NVDD3_{OFF}$	11
LCLK0	AH25	O	$NVDD3_{OFF}$	10
LCLK1	AD24	O	$NVDD3_{OFF}$	10
DUART				
UART_SOUT1/MSRCID0 (DDR ID)/LSRCID0	C15	O	$NVDD2_{OFF}$	—
UART_SIN1/MSRCID1 (DDR ID)/LSRCID1	B16	I/O	$NVDD2_{OFF}$	—
$\overline{\text{UART\_CTS}}$[1]/MSRCID2 (DDR ID)/LSRCID2	D16	I/O	$NVDD2_{OFF}$	—
$\overline{\text{UART\_RTS}}$[1]/MSRCID3 (DDR ID)/LSRCID3	B17	O	$NVDD2_{OFF}$	—
UART_SOUT2/MSRCID4 (DDR ID)/LSRCID4	A16	O	$NVDD2_{OFF}$	—
UART_SIN2/MDVAL (DDR ID)/LDVAL	C16	I/O	$NVDD2_{OFF}$	—
$\overline{\text{UART\_CTS}}$[2]	A17	I	$NVDD2_{OFF}$	—
$\overline{\text{UART\_RTS}}$[2]	A18	O	$NVDD2_{OFF}$	—
I^2C interface				
IIC_SDA/$\overline{\text{CKSTOP\_OUT}}$	N1	I/O	$NVDD4_{OFF}$	2
IIC_SCL/$\overline{\text{CKSTOP\_IN}}$	N2	I/O	$NVDD4_{OFF}$	2
Interrupts				
$\overline{\text{MCP\_OUT}}$	W1	O	$NVDD1_{OFF}$	2
$\overline{\text{IRQ}}$[0]/$\overline{\text{MCP\_IN}}$	Y3	I	$NVDD1_{OFF}$	—
$\overline{\text{IRQ}}$[1]	E1	I	$NVDD1_{ON}$	—
$\overline{\text{IRQ}}$[2]	A7	I	$NVDD1_{ON}$	—
$\overline{\text{IRQ}}$[3]	AA1	I	$NVDD1_{OFF}$	—
$\overline{\text{IRQ}}$[4]	Y5	I	$NVDD1_{OFF}$	—
$\overline{\text{IRQ}}$[5]/$\overline{\text{CORE\_SRESET\_IN}}$	AA2	I	$NVDD1_{OFF}$	—
$\overline{\text{IRQ}}$[6] /$\overline{\text{CKSTOP\_OUT}}$	AA4	I/O	$NVDD1_{OFF}$	—
$\overline{\text{IRQ}}$[7]/$\overline{\text{CKSTOP\_IN}}$	AA5	I	$NVDD1_{OFF}$	—
Configuration				
$\overline{\text{CFG\_CLKIN\_DIV}}$	A5	I	$NVDD1_{ON}$	11
EXT_PWR_CTRL	D3	O	$NVDD1_{ON}$	11
PMC_PWR_OK	D4	I	—	11

Table 66. MPC8314E TEPBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
VDD	J15, K15, K16, K17, K18, K19, L10, L19, M10, T10, U10, U19, V10, V19, W11, W12, W13, W14, W15, W16, W17, W18, P23, R23, T19, M26, N26, P28, R28, U23, N27	I	—	—
VDDC	J14, K11, K12, K13, K14, M19	I	—	—
VSS	A3, A27, B3, B12, B24, B28, C6, C8, C13, C17, C21, C23, C26, D2, D7, D15, D18, D20, D22, E4, E6, E11, E24, E26, F8, F12, F14, F17, F20, G3, G26, H4, H23, J6, J26, K25, L4, L11, L12, L13, L14, L15, L16, L17, L18, L23, L28, M3, M11, M12, M13, M14, M15, M16, M17, M18, N5, N11, N12, N13, N14, N15, N16, N17, N18, P6, P11, P12, P13, P14, P15, P16, P17, P18, R6, R11, R12, R13, R14, R15, R16, R17, R18, T11, T12, T13, T14, T15, T16, T17, T18, U5, U6, U11, U12, U13, U14, U15, U16, U17, U18, V6, V11, V12, V13, V14, V15, V16, V17, V18, W5, W25, W27, Y2, Y23, AA6, AA27, AB2, AB26, AC5, AC9, AC12, AC18, AC21, AD3, AD14, AD16, AD20, AD26, AE2, AE7, AE11, AE16, AE22, AE24, AF2, AF9, AF12, AF18, AF20, AF23, AF27, AG1, AG5, AG11, AG16, AG22, AG28, AH27, U28,N28, M28, T28, V27, M27, V28, T26, P24, R19, R20, R24, M24, N24, P19, P20, P25, P27, R25, R27, T24	I	—	—
XCOREVDD	P2, P10, R2, T1	I	—	—
XCOREVSS	R3, R10, U2, V2	I	—	—
XPADVDD	P3, R9, U3	I	—	—
XPADVSS	P5, P9, V3	I	—	—

Note:

1. This pin is an open drain signal. A weak pull-up resistor (1 kΩ) should be placed on this pin to NVDD.
2. This pin is an open drain signal. A weak pull-up resistor (2–10 kΩ) should be placed on this pin to NVDD.
3. This output is actively driven during reset rather than being three-stated during reset.
4. These JTAG pins have weak internal pull-up P-FETs that are always enabled.
5. This pin should have a weak pull up if the chip is in PCI host mode. Follow PCI specifications recommendation.
6. This pin must always be tied to VSS.
7. Thermal sensitive resistor.
8. This pin should be connected to USB_VSSA_BIAS through 10K precision resistor.
9. The LB_POR_CFG_BOOT_ECC functionality for this pin is only available in MPC8314E revision 1.1 and later. The LB_POR_CFG_BOOT_ECC is sampled only during the $\overline{\text{PORESET}}$ negation. This pin with an internal pull down resistor enables the ECC by default. To disable the ECC an external strong pull up resistor or a tristate buffer is needed.
10. This pin has a weak internal pull-down.
11. This pin has a weak internal pull-up.

24.2 Thermal Management Information

For the following sections, $P_D = (VDD \times I_{DD}) + P_{I/O}$ where $P_{I/O}$ is the power dissipation of the I/O drivers.

24.2.1 Estimation of Junction Temperature with Junction-to-Ambient Thermal Resistance

An estimation of the chip junction temperature, T_J, can be obtained from the equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

T_J = junction temperature (°C)

T_A = ambient temperature for the package (°C)

$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. As a general statement, the value obtained on a single layer board is appropriate for a tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated. Test cases have demonstrated that errors of a factor of two (in the quantity T_J - T_A) are possible.

24.2.2 Estimation of Junction Temperature with Junction-to-Board Thermal Resistance

The thermal performance of a device cannot be adequately predicted from the junction to ambient thermal resistance. The thermal performance of any component is strongly dependent on the power dissipation of surrounding components. In addition, the ambient temperature varies widely within the application. For many natural convection and especially closed box applications, the board temperature at the perimeter (edge) of the package is approximately the same as the local air temperature near the device. Specifying the local ambient conditions explicitly as the board temperature provides a more precise description of the local ambient conditions that determine the temperature of the device.

At a known board temperature, the junction temperature is estimated using the following equation:

$$T_J = T_B + (R_{\theta JB} \times P_D)$$

where:

T_J = junction temperature (°C)

T_B = board temperature at the package perimeter (°C)

$R_{\theta JB}$ = junction to board thermal resistance (°C/W) per JESD51-8

P_D = power dissipation in the package (W)

When the heat loss from the package case to the air can be ignored, acceptable predictions of junction temperature can be made. The application board should be similar to the thermal test condition: the component is soldered to a board with internal planes.

Table 75. Heat Sinks and Junction-to-Case Thermal Resistance of MPC8314E TEPBGA II

Heat Sink Assuming Thermal Grease	Air Flow	29 × 29 mm TEBGA II
		Junction-to-Ambient Thermal Resistance
AAVID 30 x 30 x 9.4 mm Pin Fin	Natural Convection	14.4
AAVID 30 x 30 x 9.4 mm Pin Fin	0.5 m/s	11.4
AAVID 30 x 30 x 9.4 mm Pin Fin	1 m/s	10.1
AAVID 30 x 30 x 9.4 mm Pin Fin	2 m/s	8.9
AAVID 35 x 31 x 23 mm Pin Fin	Natural Convection	12.3
AAVID 35 x 31 x 23 mm Pin Fin	0.5 m/s	9.3
AAVID 35 x 31 x 23 mm Pin Fin	1 m/s	8.5
AAVID 35 x 31 x 23 mm Pin Fin	2 m/s	7.9
AAVID 43 x 41 x 16.5 mm Pin Fin	Natural Convection	12.5
AAVID 43 x 41 x 16.5 mm Pin Fin	0.5 m/s	9.7
AAVID 43 x 41 x 16.5 mm Pin Fin	1 m/s	8.5
AAVID 43 x 41 x 16.5 mm Pin Fin	2 m/s	7.7
Wakefield, 53 x 53 x 25 mm Pin Fin	Natural Convection	10.9
Wakefield, 53 x 53 x 25 mm Pin Fin	0.5 m/s	8.5
Wakefield, 53 x 53 x 25 mm Pin Fin	1 m/s	7.5
Wakefield, 53 x 53 x 25 mm Pin Fin	2 m/s	7.1

Accurate thermal design requires thermal modeling of the application environment using computational fluid dynamics software which can model both the conduction cooling and the convection cooling of the air moving through the application. Simplified thermal models of the packages can be assembled using the junction-to-case and junction-to-board thermal resistances listed in the thermal resistance table. More detailed thermal models can be made available on request.

Heat sink vendors include the following list:

Aavid Thermalloy 603-224-9988
80 Commercial St.
Concord, NH 03301
Internet: www.aavidthermalloy.com

Alpha Novatech 408-749-7601
473 Sapena Ct. #12
Santa Clara, CA 95054
Internet: www.alphanovatech.com

International Electronic Research Corporation (IERC) 818-842-7277
413 North Moss St.
Burbank, CA 91502
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Japan
0120 191014 or
+81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor China Ltd.
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