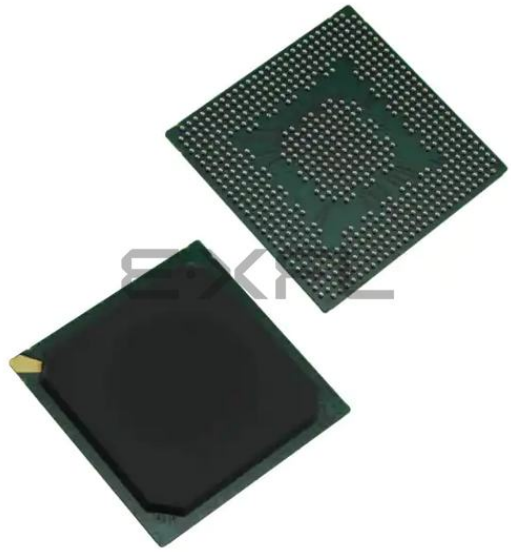

Welcome to E-XFL.COM

Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	PowerPC e300c3
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	333MHz
Co-Processors/DSP	Security; SEC 3.3
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 + PHY (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	Cryptography, Random Number Generator
Package / Case	620-BBGA Exposed Pad
Supplier Device Package	620-HBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mpc8314evrafda

  - Combines a True Random Number Generator (TRNG) and a NIST-approved Pseudo-Random Number Generator (PRNG) (as described in Annex C of FIPS140-2 and ANSI X9.62).
- Cyclical Redundancy Check Hardware Accelerator (CRCA)
  - Implements CRC32C as required for iSCSI header and payload checksums, CRC32 as required for IEEE 802 packets, as well as for programmable 32 bit CRC polynomials

2.4 DDR Memory Controller

The DDR1/DDR2 memory controller includes the following features:

- Single 16- or 32-bit interface supporting both DDR1 and DDR2 SDRAM
- Support for up to 266 MHz data rate
- Support for two physical banks (chip selects), each bank independently addressable
- 64-Mbit to 2-Gbit (for DDR1) and to 4-Gbit (for DDR2) devices with x8/x16 data ports (no direct x4 support)
- Support for one 16-bit device or two 8-bit devices on a 16-bit bus or two 16-bit devices on a 32-bit bus
- Support for up to 16 simultaneous open pages
- Supports auto refresh
- On-the-fly power management using CKE
- 1.8-/2.5-V SSTL2 compatible I/O

2.5 PCI Controller

The PCI controller includes the following features:

- Designed to comply with *PCI Local Bus Specification Revision 2.3*
- Single 32-bit data PCI interface operates at up to 66 MHz
- PCI 3.3-V compatible (not 5-V compatible)
- Support for host and agent modes
- On-chip arbitration, supporting three external masters on PCI
- Selectable hardware-enforced coherency

2.6 TDM Interface

The TDM interface includes the following features:

- Independent receive and transmit with dedicated data, clock and frame sync line
- Separate or shared RCK and TCK whose source can be either internal or external
- Glueless interface to E1/T1 frames and MVIP, SCAS, and H.110 buses
- Up to 128 time slots, where each slot can be programmed to be active or inactive
- 8- or 16-bit word widths
- The TDM Transmitter Sync Signal (TFS), Transmitter Clock Signal (TCK) and Receiver Clock

Table 24. RGMII/RTBI (When Operating at 2.5 V) DC Electrical Characteristics (continued)

Parameters	Symbol	Conditions	Min	Max	Unit

Note:
1. The symbol V_{IN}, in this case, represents the LV_{IN} symbol referenced in Table 1 and Table 2.

9.2 MII, RMII, RGMII, and RTBI AC Timing Specifications

The AC timing specifications for MII, RMII, RGMII, and RTBI are presented in this section.

9.2.1 MII AC Timing Specifications

This section describes the MII transmit and receive AC timing specifications.

9.2.1.1 MII Transmit AC Timing Specifications

This table provides the MII transmit AC timing specifications.

Table 25. MII Transmit AC Timing Specifications

At recommended operating conditions with LVDD of 3.3 V ± 300 mv.

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
TX_CLK clock period 10 Mbps	t_{MTX}	—	400	—	ns
TX_CLK clock period 100 Mbps	t_{MTX}	—	40	—	ns
TX_CLK duty cycle	t_{MTXH}/t_{MTX}	35	—	65	%
TX_CLK to MII data TXD[3:0], TX_ER, TX_EN delay	t_{MTKHDX}	1	5	15	ns
TX_CLK data clock rise V_{IL}(min) to V_{IH}(max)	t_{MTXR}	1.0	—	4.0	ns
TX_CLK data clock fall V_{IH}(max) to V_{IL}(min)	t_{MTXF}	1.0	—	4.0	ns

Note:
1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{MTKHDX} symbolizes MII transmit timing (MT) for the time t_{MTX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{MTX} represents the MII(M) transmit (TX) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure shows the MII transmit AC timing diagram.

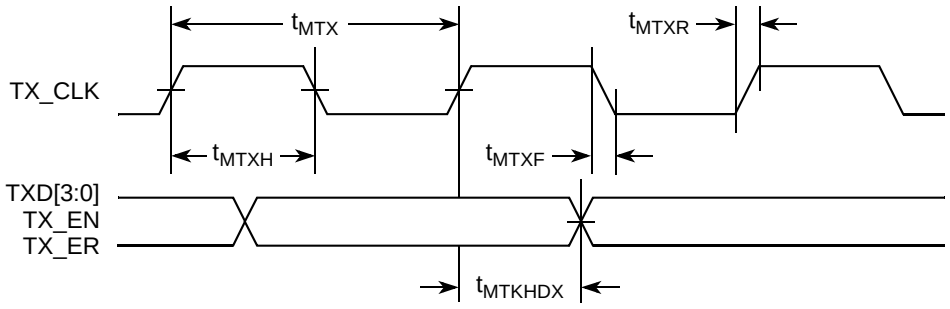

Figure 9. MII Transmit AC Timing Diagram

9.2.2 RMII AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications.

9.2.2.1 RMII Transmit AC Timing Specifications

This section describes the RMII transmit and receive AC timing specifications. This table provides the RMII transmit AC timing specifications.

Table 27. RMII Transmit AC Timing Specifications

At recommended operating conditions with LVDD of 3.3 V ± 300 mv

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
REF_CLK clock	t_{RMX}	—	20	—	ns
REF_CLK duty cycle	t_{RMXH}/t_{RMX}	35	—	65	%
REF_CLK to RMII data TXD[1:0], TX_EN delay	$t_{RMTKHDX}$	2	—	10	ns
REF_CLK data clock rise V_{IL}(min) to V_{IH}(max)	t_{RMXR}	1.0	—	4.0	ns
REF_CLK data clock fall V_{IH}(max) to V_{IL}(min)	t_{RMXF}	1.0	—	4.0	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first three letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{RMTKHDX}$ symbolizes RMII transmit timing (RMT) for the time t_{RMX} clock reference (K) going high (H) until data outputs (D) are invalid (X). Note that, in general, the clock reference symbol representation is based on two to three letters representing the clock of a particular functional. For example, the subscript of t_{RMX} represents the RMII(RM) reference (X) clock. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).

This figure shows the RMII transmit AC timing diagram.

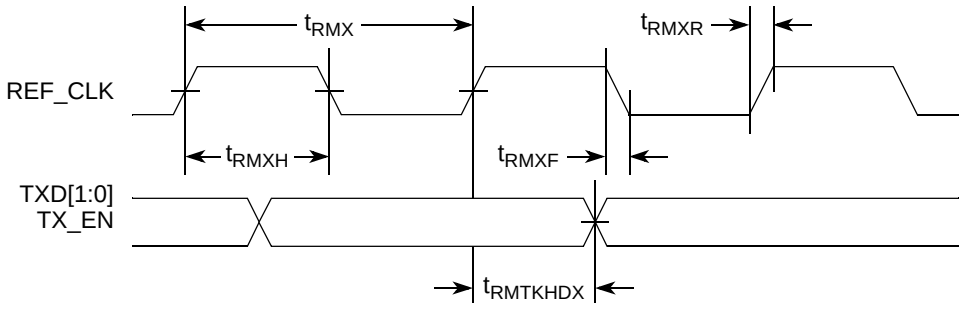

Figure 12. RMII Transmit AC Timing Diagram

9.2.2.2 RMII Receive AC Timing Specifications

This table provides the RMII receive AC timing specifications.

Table 28. RMII Receive AC Timing Specifications

At recommended operating conditions with LVDD of 3.3 V ± 300 mv

Parameter/Condition	Symbol [1]	Min	Typ	Max	Unit
REF_CLK clock period	t_{RMX}	—	20	—	ns
REF_CLK duty cycle	t_{RMXH}/t_{RMX}	35	—	65	%

This figure shows the MII management AC timing diagram.

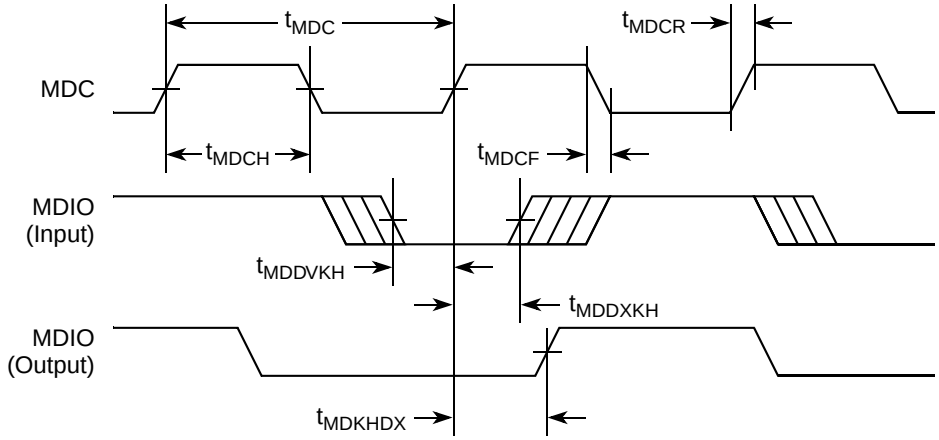

Figure 16. MII Management Interface Timing Diagram

9.4 1588 Timer Specifications

This section describes the DC and AC electrical specifications for the 1588 timer.

9.4.1 1588 Timer DC Specifications

This table provides the 1588 timer DC specifications.

Table 32. GPIO DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.0	NVDD + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	0 V ≤ V_{IN} ≤ NVDD	—	± 5	μA

9.4.2 1588 Timer AC Specifications

This table provides the 1588 timer AC specifications.

Table 33. 1588 Timer AC Specifications

Parameter	Symbol	Min	Max	Unit	Note
Timer clock cycle time	t_{TMRCK}	0	70	MHz	1
Input setup to timer clock	t_{TMRCKS}	—	—	—	2, 3
Input hold from timer clock	t_{TMRCKH}	—	—	—	2, 3
Output clock to output valid	t_{GCLKNV}	0	6	ns	
Timer alarm to output valid	t_{TMRAL}	—	—	—	2

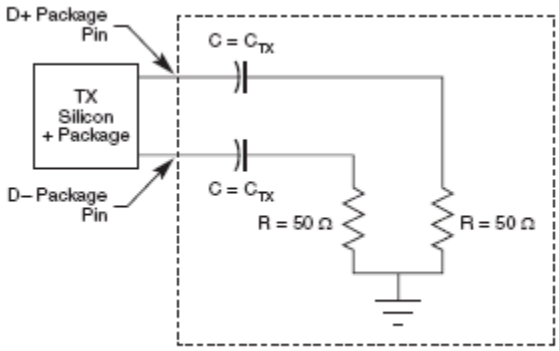

Figure 20. SGMII AC Test/Measurement Load

10 USB

10.1 USB Dual-Role Controllers

This section provides the AC and DC electrical specifications for the USB-ULPI interface.

10.1.1 USB DC Electrical Characteristics

This table lists the DC electrical characteristics for the USB interface.

Table 39. USB DC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
High-level input voltage	V_{IH}	2	LVDD + 0.3	V
Low-level input voltage	V_{IL}	–0.3	0.8	V
Input current	I_{IN}	—	±5	μA
High-level output voltage, I_{OH} = –100 μA	V_{OH}	LVDD – 0.2	—	V
Low-level output voltage, I_{OL} = 100 μA	V_{OL}	—	0.2	V

Note:
1. The symbol V_{IN}, in this case, represents the NV_{IN} symbol referenced in Table 1 and Table 2.

10.1.2 USB AC Electrical Specifications

This table lists the general timing parameters of the USB-ULPI interface.

Table 40. USB General Timing Parameters

Parameter	Symbol [1]	Min	Max	Unit	Note
USB clock cycle time	t_{USCK}	15	—	ns	1, 2
Input setup to USB clock—all inputs	t_{USIVKH}	4	—	ns	1, 4
Input hold to USB clock—all inputs	t_{USIXKH}	1	—	ns	1, 4

Table 40. USB General Timing Parameters (continued)

Parameter	Symbol [1]	Min	Max	Unit	Note
USB clock to output valid—all outputs	t_{USKHOV}	—	9	ns	1
Output hold from USB clock—all outputs	t_{USKHOX}	1	—	ns	1

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(First two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(First two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{USIXKH} symbolizes USB timing (US) for the input (I) to go invalid (X) with respect to the time the USB clock reference (K) goes high (H). Also, t_{USKHOX} symbolizes USB timing (US) for the us clock reference (K) to go high (H), with respect to the output (O) going invalid (X) or output hold time.
2. All timings are in reference to USB clock.
3. All signals are measured from NVDD/2 of the rising edge of USB clock to 0.4 × NVDD of the signal in question for 3.3-V signaling levels.
4. Input timings are measured at the pin.
5. For purposes of active/float timing measurements, the Hi-Z or off-state is defined to be when the total current delivered through the component pin is less than or equal to the leakage current specification.

Figure 21 and Figure 22 provide the AC test load and signals for the USB, respectively.

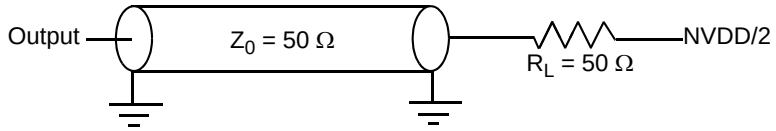

Figure 21. USB AC Test Load

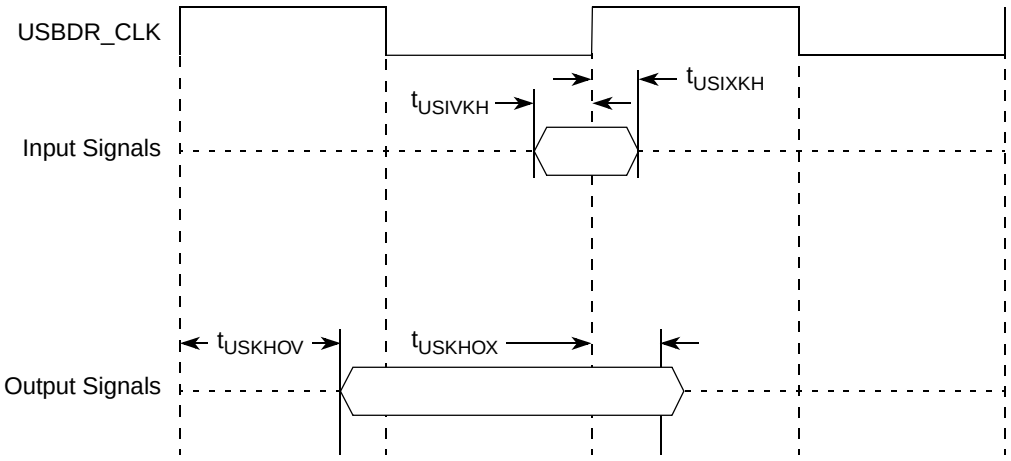

Figure 22. USB Signals

10.2 On-Chip USB PHY

This section provides the AC and DC electrical specifications for the USB PHY interface of the MPC8314E.

For details refer to Tables 7-7 through 7-10, and Table 7-14 in the *USB 2.0 Specifications document*, and the pull-up/down resistors ECN updates, all available at www.usb.org.

This table provides the USB clock input (USB_CLK_IN) DC timing specifications.

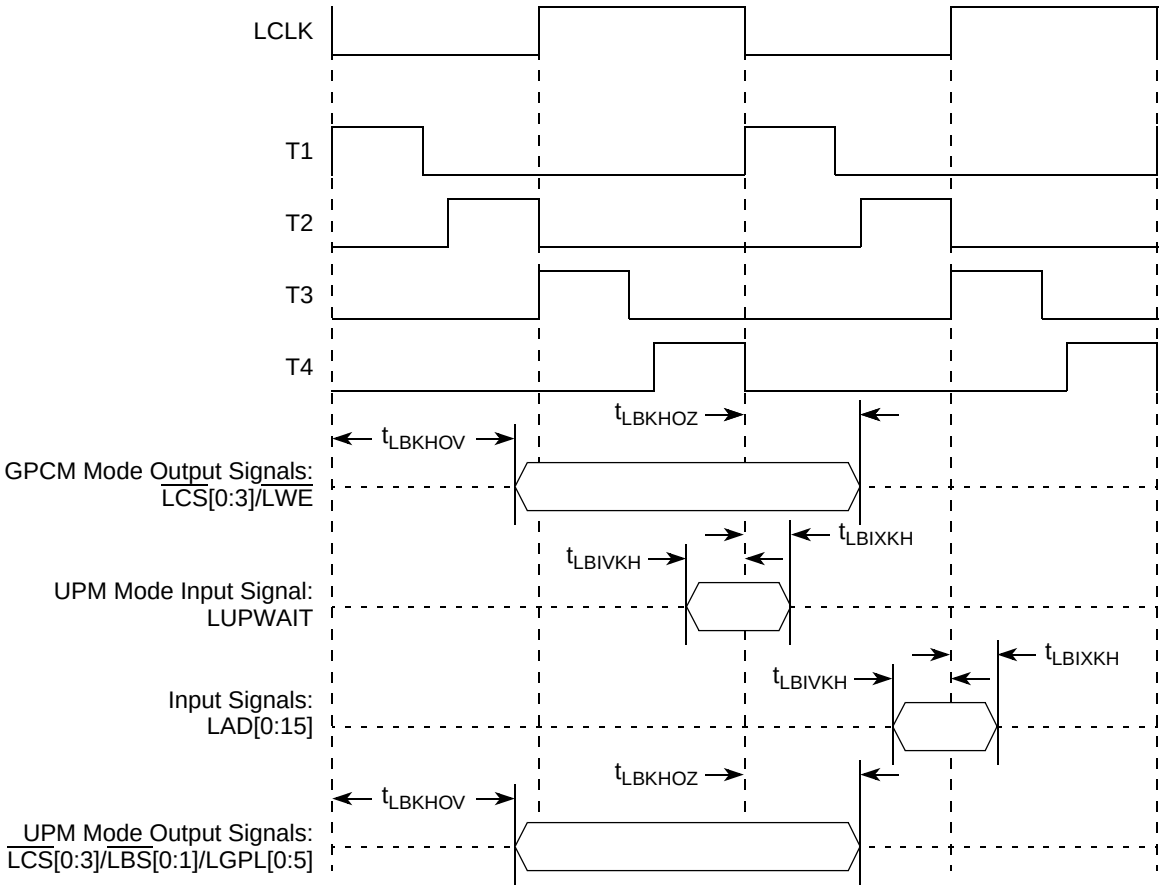

Figure 26. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 4

12 JTAG

This section describes the DC and AC electrical specifications for the IEEE Std 1149.1™ (JTAG) interface.

12.1 JTAG DC Electrical Characteristics

This table provides the DC electrical characteristics for the IEEE 1149.1 (JTAG) interface.

Table 45. JTAG Interface DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.1	NVDD + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	—	—	±5	μA
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

12.2 JTAG AC Timing Specifications

This section describes the AC electrical specifications for the IEEE 1149.1 (JTAG) interface. This table provides the JTAG AC timing specifications as defined in Figure 28 through Figure 31.

Table 46. JTAG AC Timing Specifications (Independent of SYS_CLK_IN) [1]

At recommended operating conditions (see Table 2)

Parameter	Symbol [2]	Min	Max	Unit	Note
JTAG external clock frequency of operation	f_{JTG}	0	33.3	MHz	—
JTAG external clock cycle time	t_{JTG}	30	—	ns	—
JTAG external clock pulse width measured at 1.4 V	t_{JTKHKL}	15	—	ns	—
JTAG external clock rise and fall times	t_{JTGR}, t_{JTGF}	0	2	ns	—
$\overline{\text{TRST}}$ assert time	t_{TRST}	25	—	ns	3
Input setup times: Boundary-scan data TMS, TDI	 t_{JTDVKH} t_{JTIVKH}	 4 4	 — —	ns	4
Input hold times: Boundary-scan data TMS, TDI	 t_{JTDXKH} t_{JTIXKH}	 10 10	 — —	ns	4
Valid times: Boundary-scan data TDO	 t_{JTKLDV} t_{JTKLOV}	 2 2	 11 11	ns	5
Output hold times: Boundary-scan data TDO	 t_{JTKLDX} t_{JTKLOX}	 2 2	 — —	ns	5
JTAG external clock to output high impedance: Boundary-scan data TDO	 t_{JTKLDZ} t_{JTKLOZ}	 2 2	 19 9	ns	5, 6

Note:

1. All outputs are measured from the midpoint voltage of the falling/rising edge of t_{TCLK} to the midpoint of the signal in question. The output timings are measured at the pins. All output timings assume a purely resistive 50-Ω load (see Table 27). Time-of-flight delays must be added for trace lengths, vias, and connectors in the system.
2. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{JTDVKH} symbolizes JTAG device timing (JT) with respect to the time data input signals (D) reaching the valid state (V) relative to the t_{JTG} clock reference (K) going to the high (H) state or setup time. Also, t_{JTDXKH} symbolizes JTAG timing (JT) with respect to the time data input signals (D) went invalid (X) relative to the t_{JTG} clock reference (K) going to the high (H) state. Note that, in general, the clock reference symbol representation is based on three letters representing the clock of a particular functional. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
3. $\overline{\text{TRST}}$ is an asynchronous level sensitive signal. The setup time is for test purposes only.
4. Non-JTAG signal input timing with respect to t_{TCLK}.
5. Non-JTAG signal output timing with respect to t_{TCLK}.
6. Guaranteed by design and characterization.

This figure provides the test access port timing diagram.

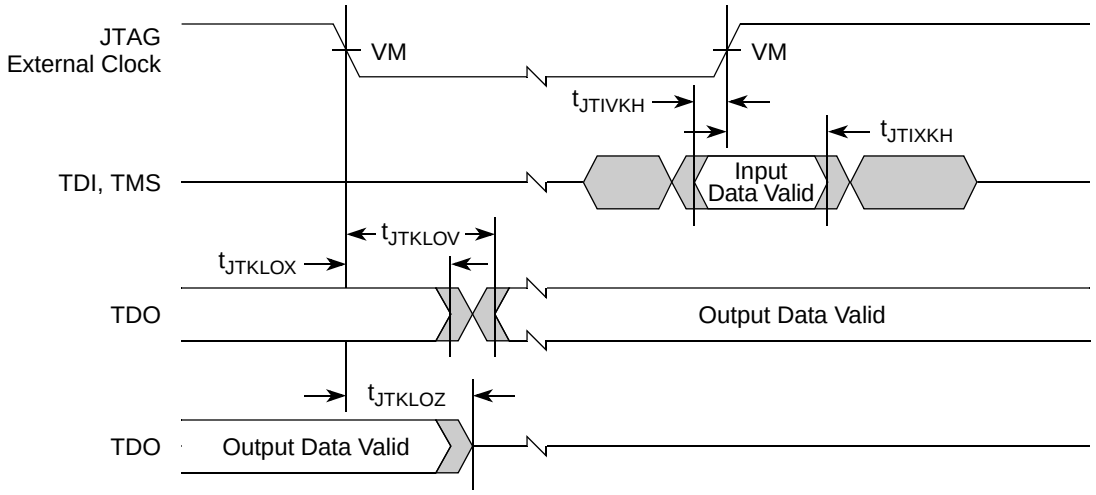

Figure 31. Test Access Port Timing Diagram

13 I²C

This section describes the DC and AC electrical characteristics for the I²C interface of the MPC8314E.

13.1 I²C DC Electrical Characteristics

This table provides the DC electrical characteristics for the I²C interface.

Table 47. I²C DC Electrical Characteristics

At recommended operating conditions with NVDD of 3.3 V ± 300 mv

Parameter	Symbol	Min	Max	Unit	Note
Input high voltage level	V_{IH}	0.7 × NVDD	NVDD + 0.3	V	—
Input low voltage level	V_{IL}	–0.3	0.3 × NVDD	V	—
Low level output voltage	V_{OL}	0	0.2 × NVDD	V	1
High level output voltage	V_{OH}	0.8 × NVDD	NVDD + 0.3	V	—
Output fall time from V_{IH}(min) to V_{IL}(max) with a bus capacitance from 10 to 400 pF	t_{I2KLKV}	20 + 0.1 × C_B	250	ns	2
Pulse width of spikes which must be suppressed by the input filter	t_{I2KHKL}	0	50	ns	3
Capacitance for each I/O pin	C_I	—	10	pF	—
Input current (0 V ≤V_{IN} ≤ NVDD)	I_{IN}	—	± 5	μA	4

Note:

1. Output voltage (open drain or open collector) condition = 3 mA sink current.
2. C_B = capacitance of one bus line in pF.
3. See the *MPC8315E PowerQUICC II Pro Integrated Host Processor Family Reference Manual* for information on the digital filter used.
4. I/O pins obstruct the SDA and SCL lines if NVDD is switched off.

13.2 I²C AC Electrical Specifications

This table provides the AC timing parameters for the I²C interface.

Table 48. I²C AC Electrical Specifications

All values refer to V_{IH} (min) and V_{IL} (max) levels (see Table 47)

Parameter	Symbol [1]	Min	Max	Unit
SCL clock frequency	f_{I2C}	0	400	kHz
Low period of the SCL clock	t_{I2CL}	1.3	—	μs
High period of the SCL clock	t_{I2CH}	0.6	—	μs
Setup time for a repeated START condition	t_{I2SVKH}	0.6	—	μs
Hold time (repeated) START condition (after this period, the first clock pulse is generated)	t_{I2SXKL}	0.6	—	μs
Data setup time	t_{I2DVKH}	100	—	ns
Data hold time: CBUS compatible masters I²C bus devices	t_{I2DXKL}	 — 0 [2]	 — 0.9 [3]	μs
Fall time of both SDA and SCL signals	t_{I2CF} [4]	—	300	ns
Setup time for STOP condition	t_{I2PVKH}	0.6	—	μs
Bus free time between a STOP and START condition	t_{I2KHDX}	1.3	—	μs
Noise margin at the LOW level for each connected device (including hysteresis)	V_{NL}	0.1 × NVDD	—	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{NH}	0.2 × NVDD	—	V

Note:

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state)(reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, t_{I2DVKH} symbolizes I²C timing (I2) with respect to the time data input signals (D) reach the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. Also, t_{I2SXKL} symbolizes I²C timing (I2) for the time that the data with respect to the start condition (S) went invalid (X) relative to the t_{I2C} clock reference (K) going to the low (L) state or hold time. Also, t_{I2PVKH} symbolizes I²C timing (I2) for the time that the data with respect to the stop condition (P) reaching the valid state (V) relative to the t_{I2C} clock reference (K) going to the high (H) state or setup time. For rise and fall times, the latter convention is used with the appropriate letter: R (rise) or F (fall).
2. MPC8314E provides a hold time of at least 300 ns for the SDA signal (referred to the V_{IHmin} of the SCL signal) to bridge the undefined region of the falling edge of SCL.
3. The maximum t_{I2DVKH} has to be met only if the device does not stretch the LOW period (t_{I2CL}) of the SCL signal.
4. MPC8314E does not follow the *I2C-BUS Specifications* version 2.1 regarding the tI2CF AC parameter.

This figure provides the AC test load for the I²C.

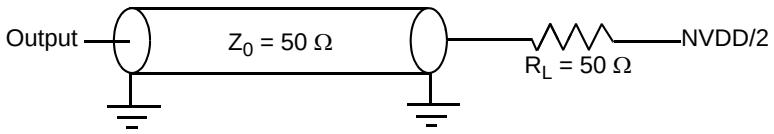

Figure 32. I²C AC Test Load

This figure shows the AC timing diagram for the I^2C bus.

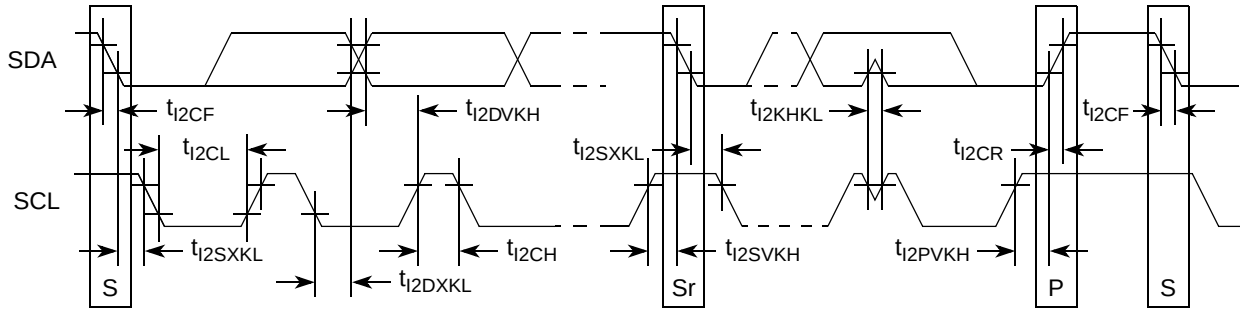

Figure 33. I^2C Bus AC Timing Diagram

14 PCI

This section describes the DC and AC electrical specifications for the PCI bus of the MPC8314E.

14.1 PCI DC Electrical Characteristics

This table provides the DC electrical characteristics for the PCI interface.

Table 49. PCI DC Electrical Characteristics [1]

Parameter	Symbol	Test Condition	Min	Max	Unit
High-level input voltage	V_{IH}	$V_{OUT} \geq V_{OH}$ (min) or	0.5 x NVDD	NVDD + 0.3	V
Low-level input voltage	V_{IL}	$V_{OUT} \leq V_{OL}$ (max)	–0.5	0.3 × NVDD	V
High-level output voltage	V_{OH}	NVDD = min, I_{OH} = –500 µA	0.9 x NVDD	—	V
Low-level output voltage	V_{OL}	NVDD = min, I_{OL} = 1500 µA	—	0.1 x NVDD	V
Input current	I_{IN}	0 V ≤ V_{IN} ≤ NVDD	—	± 10	µA

Note:
1. The symbol V_{IN}, in this case, represents the NV_{IN} symbol referenced in Table 1 and Table 2.

14.2 PCI AC Electrical Specifications

This section describes the general AC timing parameters of the PCI bus. Note that the PCI_CLK or PCI_SYNC_IN signal is used as the PCI input clock depending on whether the MPC8314E is configured as a host or agent device. This table shows the PCI AC timing specifications at 66 MHz.

Table 50. PCI AC Timing Specifications at 66 MHz

Parameter	Symbol [1]	Min	Max	Unit	Note
Clock to output valid	t_{PCKHOV}	—	6.0	ns	2
Output hold from clock	t_{PCKHOX}	1	—	ns	2
Clock to output high impedance	t_{PCKHOZ}	—	14	ns	2, 3
Input setup to clock	t_{PCIVKH}	3.3	—	ns	2, 4

Table 55. Differential Receiver (RX) Input Specifications (continued)

Parameter	Symbol	Comments	Min	Typical	Max	Unit	Note
Powered down DC input impedance	$Z_{RX-HIGH-IMP-DC}$	Required RX D+ as well as D- DC Impedance when the Receiver terminations do not have power.	200 k	—	—	Ω	6
Electrical idle detect threshold	$V_{RX-IDLE-DET-DIFFp-p}$	V_{PEEIDT} = 2*|V_{RX-D+} -V_{RX-D-}| Measured at the package pins of the Receiver	65	—	175	mV	—
Unexpected Electrical Idle Enter Detect Threshold Integration Time	$T_{RX-IDLE-DET-DIFF-ENTERTIME}$	An unexpected Electrical Idle (Vrx-diffp-p < Vrx-idle-det-diffp-p) must be recognized no longer than Trx-idle-det-diff-entertime to signal an unexpected idle condition.	—	—	10	ms	—
Total Skew	$L_{RX-SKEW}$	Skew across all lanes on a Link. This includes variation in the length of SKP ordered set (e.g. COM and one to five SKP Symbols) at the RX as well as any delay differences arising from the interconnect itself.	—	—	20	ns	—

Note:

1. No test load is necessarily associated with this value.
2. Specified at the measurement point and measured over any 250 consecutive UIs. The test load in Figure 51 should be used as the RX device when taking measurements (also refer to the receiver compliance eye diagram shown in Figure 50). If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as a reference for the eye diagram.
3. A T_{RX-EYE} = 0.40 UI provides for a total sum of 0.60 UI deterministic and random jitter budget for the transmitter and interconnect collected any 250 consecutive UIs. The $T_{RX-EYE-MEDIAN-to-MAX-JITTER}$ specification ensures a jitter distribution in which the median and the maximum deviation from the median is less than half of the total. UI jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value. If the clocks to the RX and TX are not derived from the same reference clock, the TX UI recovered from 3500 consecutive UI must be used as the reference for the eye diagram.
4. The receiver input impedance shall result in a differential return loss greater than or equal to 15 dB with the D+ line biased to 300 mV and the D– line biased to –300 mV and a common mode return loss greater than or equal to 6 dB (no bias required) over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements for is 50 Ω to ground for both the D+ and D– line (that is, as measured by a vector network analyzer with 50-Ω probes, see Figure 51). Note that the series capacitors, C_{TX}, is optional for the return loss measurement.
5. Impedance during all LTSSM states. When transitioning from a fundamental reset to detect (the initial state of the LTSSM) there is a 5 ms transition time before receiver termination values must be met on all unconfigured lanes of a port.
6. The RX DC common mode impedance that exists when no power is present or fundamental reset is asserted. This helps ensure that the receiver detect circuit does not falsely assume a receiver is powered on when it is not. This term must be measured at 300 mV above the RX ground.
7. It is recommended that the recovered TX UI is calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function. Least squares and median deviation fits have worked well with experimental and simulated data.

Table 66. MPC8314E TEPBGA II Pinout Listing

Signal	Package Pin Number	Pin Type	Power Supply	Note
DDR Memory Controller Interface				
MEMC_MDQ[0]	AF16	I/O	GVDD	—
MEMC_MDQ[1]	AE17	I/O	GVDD	—
MEMC_MDQ[2]	AH17	I/O	GVDD	—
MEMC_MDQ[3]	AG17	I/O	GVDD	—
MEMC_MDQ[4]	AG18	I/O	GVDD	—
MEMC_MDQ[5]	AH18	I/O	GVDD	—
MEMC_MDQ[6]	AD18	I/O	GVDD	—
MEMC_MDQ[7]	AF19	I/O	GVDD	—
MEMC_MDQ[8]	AH19	I/O	GVDD	—
MEMC_MDQ[9]	AD19	I/O	GVDD	—
MEMC_MDQ[10]	AG20	I/O	GVDD	—
MEMC_MDQ[11]	AH20	I/O	GVDD	—
MEMC_MDQ[12]	AH21	I/O	GVDD	—
MEMC_MDQ[13]	AE21	I/O	GVDD	—
MEMC_MDQ[14]	AH22	I/O	GVDD	—
MEMC_MDQ[15]	AD21	I/O	GVDD	—
MEMC_MDQ[16]	AG10	I/O	GVDD	—
MEMC_MDQ[17]	AH9	I/O	GVDD	—
MEMC_MDQ[18]	AH8	I/O	GVDD	—
MEMC_MDQ[19]	AD11	I/O	GVDD	—
MEMC_MDQ[20]	AH7	I/O	GVDD	—
MEMC_MDQ[21]	AG7	I/O	GVDD	—
MEMC_MDQ[22]	AF8	I/O	GVDD	—
MEMC_MDQ[23]	AD10	I/O	GVDD	—
MEMC_MDQ[24]	AE9	I/O	GVDD	—
MEMC_MDQ[25]	AH6	I/O	GVDD	—
MEMC_MDQ[26]	AH5	I/O	GVDD	—
MEMC_MDQ[27]	AG6	I/O	GVDD	—
MEMC_MDQ[28]	AH4	I/O	GVDD	—
MEMC_MDQ[29]	AE6	I/O	GVDD	—
MEMC_MDQ[30]	AD8	I/O	GVDD	—
MEMC_MDQ[31]	AF5	I/O	GVDD	—
MEMC_MDM0	AE18	O	GVDD	—
MEMC_MDM1	AE20	O	GVDD	—
MEMC_MDM2	AE10	O	GVDD	—

Table 66. MPC8314E TEPBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
MEMC_MDM3	AF6	O	GVDD	—
MEMC_MDQS[0]	AF17	I/O	GVDD	—
MEMC_MDQS[1]	AG21	I/O	GVDD	—
MEMC_MDQS[2]	AG9	I/O	GVDD	—
MEMC_MDQS[3]	AF7	I/O	GVDD	—
MEMC_MBA[0]	AH16	O	GVDD	—
MEMC_MBA[1]	AH15	O	GVDD	—
MEMC_MBA[2]	AG15	O	GVDD	—
MEMC_MA0	AD15	O	GVDD	—
MEMC_MA1	AE15	O	GVDD	—
MEMC_MA2	AH14	O	GVDD	—
MEMC_MA3	AG14	O	GVDD	—
MEMC_MA4	AF14	O	GVDD	—
MEMC_MA5	AE14	O	GVDD	—
MEMC_MA6	AH13	O	GVDD	—
MEMC_MA7	AH12	O	GVDD	—
MEMC_MA8	AF13	O	GVDD	—
MEMC_MA9	AD13	O	GVDD	—
MEMC_MA10	AG12	O	GVDD	—
MEMC_MA11	AH11	O	GVDD	—
MEMC_MA12	AH10	O	GVDD	—
MEMC_MA13	AE12	O	GVDD	—
MEMC_MA14	AF11	O	GVDD	—
$\overline{\text{MEMC\_MWE}}$	AE5	O	GVDD	—
$\overline{\text{MEMC\_MRAS}}$	AD7	O	GVDD	—
$\overline{\text{MEMC\_MCAS}}$	AG4	O	GVDD	—
$\overline{\text{MEMC\_MCS}}$[0]	AH3	O	GVDD	—
$\overline{\text{MEMC\_MCS}}$[1]	AD5	O	GVDD	—
MEMC_MCKE	AE4	O	GVDD	3
MEMC_MCK[0]	AF4	O	GVDD	—
$\overline{\text{MEMC\_MCK}}$[0]	AF3	O	GVDD	—
MEMC_MCK[1]	AF1	O	GVDD	—
$\overline{\text{MEMC\_MCK}}$[1]	AE1	O	GVDD	—
MEMC_MODT[0]	AE3	O	GVDD	—
MEMC_MODT[1]	AD4	O	GVDD	—
MEMC_MVREF	AD12	I	GVDD	—

Table 66. MPC8314E TEPBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
DMA_DREQ0/GPIO_12	AD1	I/O	$NVDD1_{OFF}$	—
DMA_DONE0/GPIO_14	AD2	I/O	$NVDD1_{OFF}$	—
NC, No Connect	A2	—	—	—
NC, No Connect	M25	—	—	—
NC, No Connect	P26	—	—	—
NC, No Connect	N25	—	—	—
NC, No Connect	U26	—	—	—
NC, No Connect	T25	—	—	—
NC, No Connect	R26	—	—	—
NC, No Connect	U25	—	—	—
PCI				
PCI_INTA	B18	O	$NVDD2_{OFF}$	—
PCI_RESET_OUT	A20	O	$NVDD2_{OFF}$	—
PCI_AD[0]	J25	I/O	$NVDD2_{OFF}$	—
PCI_AD[1]	J24	I/O	$NVDD2_{OFF}$	—
PCI_AD[2]	K24	I/O	$NVDD2_{OFF}$	—
PCI_AD[3]	H27	I/O	$NVDD2_{OFF}$	—
PCI_AD[4]	H28	I/O	$NVDD2_{OFF}$	—
PCI_AD[5]	H26	I/O	$NVDD2_{OFF}$	—
PCI_AD[6]	G27	I/O	$NVDD2_{OFF}$	—
PCI_AD[7]	G28	I/O	$NVDD2_{OFF}$	—
PCI_AD[8]	F26	I/O	$NVDD2_{OFF}$	—
PCI_AD[9]	F28	I/O	$NVDD2_{OFF}$	—
PCI_AD[10]	G25	I/O	$NVDD2_{OFF}$	—
PCI_AD[11]	F27	I/O	$NVDD2_{OFF}$	—
PCI_AD[12]	E27	I/O	$NVDD2_{OFF}$	—
PCI_AD[13]	E28	I/O	$NVDD2_{OFF}$	—
PCI_AD[14]	D28	I/O	$NVDD2_{OFF}$	—
PCI_AD[15]	D27	I/O	$NVDD2_{OFF}$	—
PCI_AD[16]	B25	I/O	$NVDD2_{OFF}$	—
PCI_AD[17]	D24	I/O	$NVDD2_{OFF}$	—
PCI_AD[18]	B26	I/O	$NVDD2_{OFF}$	—
PCI_AD[19]	C24	I/O	$NVDD2_{OFF}$	—
PCI_AD[20]	A26	I/O	$NVDD2_{OFF}$	—
PCI_AD[21]	E20	I/O	$NVDD2_{OFF}$	—
PCI_AD[22]	A23	I/O	$NVDD2_{OFF}$	—

Table 66. MPC8314E TEPBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
GPIO_1/DMA_DACK1/GTM1_TIN2/GTM2_TIN1	A4	I/O	$NVDD1_{ON}$	—
GPIO_2/DMA_DONE1/GTM1_TGATE2/GTM2_TGATE1	K3	I/O	$NVDD4_{OFF}$	—
GPIO_3/GTM1_TIN3/GTM2_TIN4	K1	I/O	$NVDD4_{OFF}$	—
GPIO_4/GTM1_TGATE3/GTM2_TGATE4	K2	I/O	$NVDD4_{OFF}$	—
GPIO_5/GTM1_TOUT3/GTM2_TOUT1	L5	I/O	$NVDD4_{OFF}$	—
GPIO_6/GTM1_TIN4/GTM2_TIN3	L3	I/O	$NVDD4_{OFF}$	—
GPIO_7/GTM1_TGATE4/GTM2_TGATE3	L1	I/O	$NVDD4_{OFF}$	—
GPIO_8/USBDR_DRIVE_VBUS/GTM1_TIN1/GTM2_TIN2	M1	I/O	$NVDD4_{OFF}$	—
GPIO_9/USBDR_PWRFAULT/GTM1_TGATE1/GTM2_TGATE2	M2	I/O	$NVDD4_{OFF}$	—
GPIO_10/USBDR_PCTL0/GTM1_TOUT2/GTM2_TOUT1	M5	I/O	$NVDD4_{OFF}$	—
GPIO_11/USBDR_PCTL1/GTM1_TOUT4/GTM2_TOUT3	M4	I/O	$NVDD4_{OFF}$	—
SPI				
SPIMOSI/GPIO_15	W3	I/O	$NVDD1_{OFF}$	—
SPIMISO/GPIO_16	W4	I/O	$NVDD1_{OFF}$	—
SPICLK	Y1	I/O	$NVDD1_{OFF}$	—
SPISEL/GPIO_17	W2	I/O	$NVDD1_{OFF}$	—
Power and Ground Supplies				
GVDD	Y11, Y12, Y14, Y15, Y17, AC8, AC11, AC14, AC17, AD6, AD9, AD17, AE8, AE13, AE19, AF10, AF15, AF21, AG2, AG3, AG8, AG13, AG19, AH2	I	—	—
$LVDD1_{OFF}$	H6, J3, L6, L9, M9	I	—	—
$LVDD2_{ON}$	C11, D9, E10, F11, J12	I	—	—
$NVDD1_{OFF}$	U9, V9, W10, Y4, Y6, AA3, AB4	I	—	—
$NVDD1_{ON}$	B1, B2, C1, D5, E7, F5, F9, J11, K10	I	—	—
$NVDD2_{OFF}$	B22, B27, C19, E16, F15, F18, F21, F25, H25, J17, J18, J23, L20, M20	I	—	—
$NVDD2_{ON}$	L26, N19	I	—	—
$NVDD3_{OFF}$	U20, V20, V23, V26, W19, Y18, Y26, AA23, AA25, AC20, AC25, AD23, AE25, AG25, AG27, T27, U27	I	—	—
$NVDD4_{OFF}$	K4, L2, M6, N10	I	—	—

Table 69. System PLL Multiplication Factors

RCWL[SPMF]	System PLL Multiplication Factor
0000	Reserved
0001	Reserved
0010	× 2
0011	× 3
0100	× 4
0101	× 5
0110–1111	Reserved

As described in Section 23, "Clocking," The LBCM, DDRCM, and SPMF parameters in the reset configuration word low and the $\overline{\text{CFG\_SYS\_CLKIN\_DIV}}$ configuration input signal select the ratio between the primary clock input (SYS_CLK_IN or PCI_CLK) and the internal coherent system bus clock (*csb_clk*). Table 70 and Table 71 shows the expected frequency values for the CSB frequency for select *csb_clk* to SYS_CLK_IN/PCI_SYNC_IN ratios.

Table 70. CSB Frequency Options for Host Mode

$\overline{\text{CFG\_SYS\_CLKIN\_DIV}}$ at Reset[1]	SPMF	csb_clk : Input Clock Ratio [2]	Input Clock Frequency (MHz)[2]		
			24	33.33	66.67
High/Low [3]	0010	2:1			133
High/Low	0011	3:1		100	—
High/Low	0100	4:1	96	133	—
High/Low	0101	5:1	120	—	—

1 $\overline{\text{CFG\_SYS\_CLKIN\_DIV}}$ select the ratio between SYS_CLK_IN and PCI_SYNC_OUT.
2 SYS_CLK_IN is the input clock in host mode; PCI_CLK is the input clock in agent mode.
3 In the Host mode it does not matter if the value is High or Low.

Table 71. CSB Frequency Options for Agent Mode

$\overline{\text{CFG\_SYS\_CLKIN\_DIV}}$ at Reset[1]	SPMF	*csb_clk* : Input Clock Ratio [2]	Input Clock frequency (MHz)[2]		
			25	33.33	66.67
High	0010	2: 1			133
High	0011	3: 1		100	—
High	0100	4: 1		133	—
High	0101	5: 1	120	—	—

1 $\overline{\text{CFG\_SYS\_CLKIN\_DIV}}$ doubles csb_clk if set low.
2 SYS_CLK_IN is the input clock in host mode; PCI_CLK is the input clock in agent mode.

Table 73. Suggested PLL Configurations

Conf. No.	SPMF	Core\PLL	Input Clock Frequency (MHz)	CSB Frequency (MHz)	Core Frequency (MHz)
6	0010	0000101	66.67	133.33	333.33
7	0101	0000110	25	125	375
8	0100	0000110	33.33	133.33	400
9	0010	0000110	66.67	133.33	400

24 Thermal

This section describes the thermal specifications of the MPC8314E.

24.1 Thermal Characteristics

This table provides the package thermal characteristics for the 620 29 × 29 mm TEPBGA II.

Table 74. Package Thermal Characteristics for TEPBGA II

Characteristic	Board type	Symbol	Value	Unit	Note
Junction to ambient natural convection	Single layer board (1s)	$R_{\theta JA}$	23	°C/W	1, 2
Junction to ambient natural convection	Four layer board (2s2p)	$R_{\theta JA}$	16	°C/W	1, 2, 3
Junction to ambient (@200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	18	°C/W	1, 3
Junction to ambient (@200 ft/min)	Four layer board (2s2p)	$R_{\theta JMA}$	13	°C/W	1, 3
Junction to board	—	$R_{\theta JB}$	8	°C/W	4
Junction to case	—	$R_{\theta JC}$	6	°C/W	5
Junction to package top	Natural convection	Ψ_{JT}	6	°C/W	6

Note:

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

This circuit is intended to filter noise in the PLLs resonant frequency range from a 500 kHz to 10 MHz range. It should be built with surface mount capacitors with minimum Effective Series Inductance (ESL). Consistent with the recommendations of Dr. Howard Johnson in *High Speed Digital Design: A Handbook of Black Magic* (Prentice Hall, 1993), multiple small capacitors of equal value are recommended over a single large value capacitor.

Each circuit should be placed as close as possible to the specific AV_{DD} pin being supplied to minimize noise coupled from nearby circuits. It should be possible to route directly from the capacitors to the AV_{DD} pin, which is on the periphery of package, without the inductance of vias. Note that the RC filter results in lower voltage level on AVDD. This does not imply that the DC specification can be relaxed.

This figure shows the PLL power supply filter circuit.

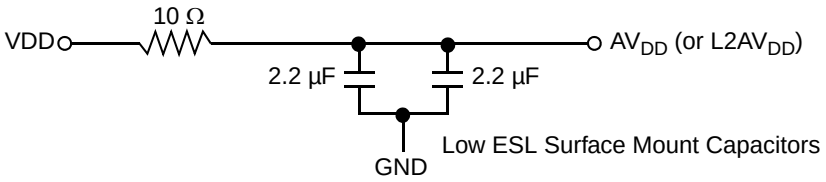

Figure 61. PLL Power Supply Filter Circuit

25.3 Decoupling Recommendations

Due to large address and data buses, and high operating frequencies, the device can generate transient power surges and high frequency noise in its power supply, especially while driving large capacitive loads. This noise must be prevented from reaching other components in the MPC8314E system, and the MPC8314E itself requires a clean, tightly regulated source of power. Therefore, it is recommended that the system designer place at least one decoupling capacitor at each VDD, NVDD, GVDD, and LVDD pins of the device. These decoupling capacitors should receive their power from separate VDD, NVDD, GVDD, LVDD, and GND power planes in the PCB, utilizing thick and short traces to minimize inductance. Capacitors may be placed directly under the device using a standard escape pattern. Others may surround the part.

These capacitors should have a value of 0.01 or 0.1 µF. Only ceramic SMT (surface mount technology) capacitors should be used to minimize lead inductance, preferably 0402 or 0603 sizes.

In addition, it is recommended that there be several bulk storage capacitors distributed around the PCB, feeding the VDD, NVDD, GVDD, and LVDD planes, to enable quick recharging of the smaller chip capacitors. These bulk capacitors should have a low ESR (equivalent series resistance) rating to ensure the quick response time necessary. They should also be connected to the power and ground planes through two vias to minimize inductance. Suggested bulk capacitors—100–330 µF (AVX TPS tantalum or Sanyo OSCON).

25.4 Connection Recommendations

To ensure reliable operation, it is highly recommended to connect unused inputs to an appropriate signal level. Unused active low inputs should be tied to NVDD, GVDD, or LVDD as required. Unused active high inputs should be connected to GND. All NC (no-connect) signals must remain unconnected.

also includes an application modifier which may specify special application conditions. Each part number also contains a revision code which refers to the die mask revision number.

Table 77. Part Numbering Nomenclature

MPC	8314	E	C	VR	AG	D	A
Product Code	**Part Identifier**	**Encryption Acceleration**	**Temperature Range [3]**	**Package [1]**	**e300 Core Frequency [2]**	**DDR Frequency**	**Revision Level**
MPC	8314	Blank = Not included E = included	Blank = 0 to 105°C C = –40 to 105°C	VR= Pb Free TEPBGA II	AD = 266 MHz AF = 333 MHz AG = 400 MHz	D = 266 MHz	Contact local Freescale sales office

Note:
1. See Section 22, “Package and Pin Listings,” for more information on available package types.
2. Processor core frequencies supported by parts addressed by this specification only. Not all parts described in this specification support all core frequencies. Additionally, parts addressed by electric may support other maximum core frequencies.
3. Contact your local Freescale field applications engineer (FAE).

This table shows the SVR settings by device and package type.

Table 78. SVR Settings

Device	Package	SVR (Rev 1.0)	SVR (Rev 1.1)	SVR (Rev 1.2)
MPC8314E	TEPBGA II	0x80B6_0010	0x80B6_0011	0x80B6_0012
MPC8314	TEPBGA II	0x80B7_0010	0x80B7_0011	0x80B7_0012

Note:
1. PVR = 8085_0020 for all devices and revisions in this table.