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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Active
Core Processor	PowerPC e300c3
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	333MHz
Co-Processors/DSP	-
RAM Controllers	DDR, DDR2
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100/1000Mbps (2)
SATA	-
USB	USB 2.0 + PHY (1)
Voltage - I/O	1.8V, 2.5V, 3.3V
Operating Temperature	0°C ~ 105°C (TA)
Security Features	-
Package / Case	620-BBGA Exposed Pad
Supplier Device Package	620-HBGA (29x29)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mpc8314vrafda

- One floating point unit and two integer units
- Software-compatible with the Freescale processor families implementing the PowerPC Architecture
- Performance monitor

2.2 Serial Interfaces

The following interfaces are supported in the MPC8314E.

- Two enhanced TSECs (eTSECs)
- Two Ethernet interfaces using one RGMII/MII/RMII/RTBI or SGMII (no GMII)
- Dual UART, one I^2C, and one SPI interface

2.3 Security Engine

The security engine is optimized to handle all the algorithms associated with IPSec, 802.11i, and iSCSI. The security engine contains one crypto-channel, a controller, and a set of crypto execution units (EUs). The execution units are:

- Public key execution unit (PKEU)
  - RSA and Diffie-Hellman (to 4096 bits)
  - Programmable field size up to 2048 bits
  - Elliptic curve cryptography (1023 bits)
  - F2m and F(p) modes
  - Programmable field size up to 511 bits
- Data encryption standard execution unit (DEU)
  - DES, 3DES
  - Two key (K1, K2) or three key (K1, K2, K3)
  - ECB, CBC, CFB-64 and OFB-64 modes for both DES and 3DES
- Advanced encryption standard unit (AESU)
  - Implements the Rinjdael symmetric key cipher
  - Key lengths of 128, 192, and 256 bits
  - ECB, CBC, CCM, CTR, GCM, CMAC, OFB, CFB, XCBC-MAC and LRW modes
  - XOR acceleration
- Message digest execution unit (MDEU)
  - SHA with 160-bit, 256-bit, 384-bit and 512-bit message digest
  - SHA-384/512
  - MD5 with 128-bit message digest
  - HMAC with either algorithm
- Random number generator (RNG)

Table 1. Absolute Maximum Ratings [1] (continued)

Characteristic		Symbol	Max Value	Unit	Note
DDR2 DRAM I/O supply voltage		GVDD	–0.3 to 1.9	V	—
PCI, local bus, DUART, system control and power management, I^2C, Ethernet management, 1588 timer and JTAG I/O voltage		NVDD	–0.3 to 3.6	V	7
USB, and eTSEC I/O voltage		LVDD	–0.3 to 2.75 or –0.3 to 3.6	V	6, 8
PHY voltage	USB PHY	USB_PLL_PWR1	–0.3 to 1.26	V	—
		USB_PLL_PWR3, USB_VDDA_BIAS, VDDA	–0.3 to 3.6	V	—
	SERDES PHY	XCOREVDD, XPADVDD, SDAVDD	–0.3 to 1.26	V	—
Input voltage	DDR DRAM signals	MV_{IN}	–0.3 to (GVDD + 0.3)	V	2, 4
	DDR DRAM reference	MVREF	–0.3 to (GVDD + 0.3)	V	2, 4
	eTSEC signals	LV_{IN}	–0.3 to (LVDD + 0.3)	V	3, 4
	Local bus, DUART, SYS_CLK_IN, system control and power management, I^2C, and JTAG signals	NV_{IN}	–0.3 to (NVDD + 0.3)	V	3, 4
	PCI	NV_{IN}	–0.3 to (NVDD + 0.3)	V	5
Storage temperature range		T_{STG}	–55 to150	°C	—

Note:

1. Functional and tested operating conditions are given in Table 2. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.
2. **Caution:** MV_{IN} must not exceed GVDD by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
3. **Caution:** (N,L)V_{IN} must not exceed (N,L)VDD by more than 0.3 V. This limit may be exceeded for a maximum of 20 ms during power-on reset and power-down sequences.
4. (M,N,L)V_{IN} and MVREF may overshoot/undershoot to a voltage and for a maximum duration as shown in Figure 2.
5. NV_{IN} on the PCI interface may overshoot/undershoot according to the PCI Electrical Specification for 3.3-V operation, as shown in Figure 2.
6. The max value of supply voltage should be selected based on the RGMII mode.
7. NVDD means NVDD1_OFF, NVDD1_ON, NVDD2_OFF, NVDD2_ON, NVDD3_OFF, NVDD4_OFF
8. LVDD means LVDD1_OFF and LVDD2_ON

Table 19. DDR SDRAM Input AC Timing Specifications

At recommended operating conditions with GVDD of (2.5V ± 200 mV)

Controller Skew for MDQS—MDQ 266 MHz 200 MHz	t_{CISKEW}	 –750 –1250	 750 1250	ps	1, 2

Note:

1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit to be captured with MDQS[n]. This should be subtracted from the total timing budget.
2. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}. This can be determined by the following equation: t_{DISKEW} =+/–(T/4 – abs(t_{CISKEW})) where T is the clock period and abs(t_{CISKEW}) is the absolute value of t_{CISKEW}.

This figure shows the DDR SDRAM input AC timing for the tolerated MDQS to MDQ skew (t_{DISKEW})

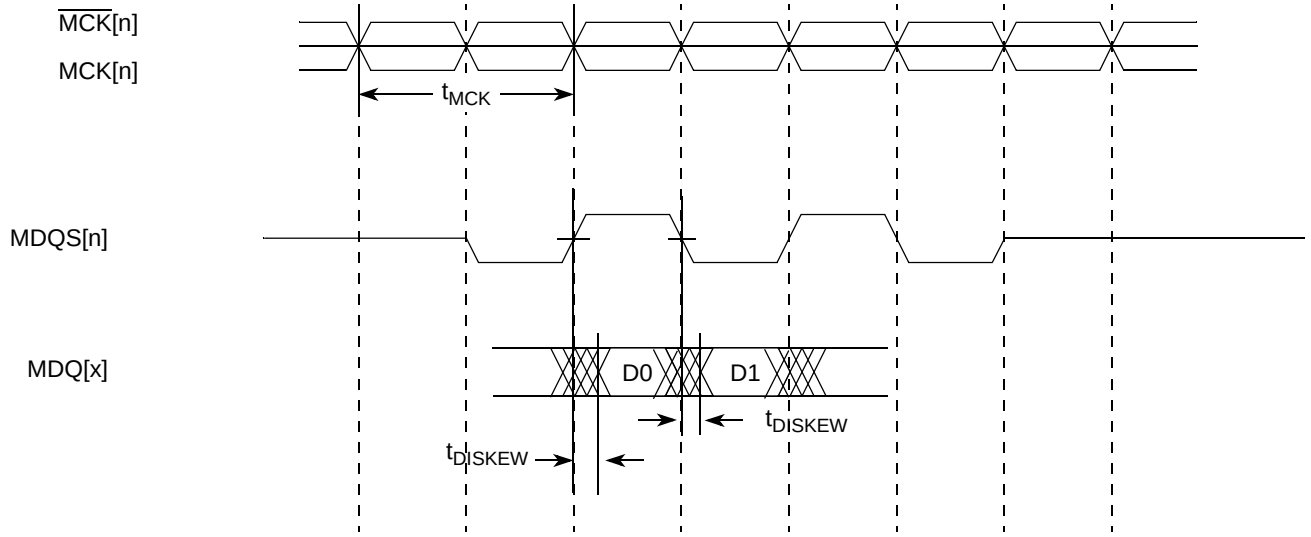


Figure 5. Timing Diagram for t_{DISKEW}

7.2.2 DDR and DDR2 SDRAM Output AC Timing Specifications

Table 20. DDR and DDR2 SDRAM Output AC Timing Specifications

At recommended operating conditions

Parameter	Symbol [1]	Min	Max	Unit	Note
MCK[n] cycle time at MCK[n]/MCK[n] crossing	t_{MCK}	7.5	10	ns	2
ADDR/CMD output setup with respect to MCK 266 MHz 200 MHz	t_{DDKHAS}	 2.9 3.5	 — —	ns	3
ADDR/CMD output hold with respect to MCK 266 MHz 200 MHz	t_{DDKHAX}	 3.15 4.20	 — —	ns	3
MCS[n] output setup with respect to MCK 266 MHz 200 MHz	t_{DDKHCS}	 3.15 4.20	 — —	ns	3

This figure shows the DDR SDRAM output timing for the MCK to MDQS skew measurement (t_{DDKHMH}).

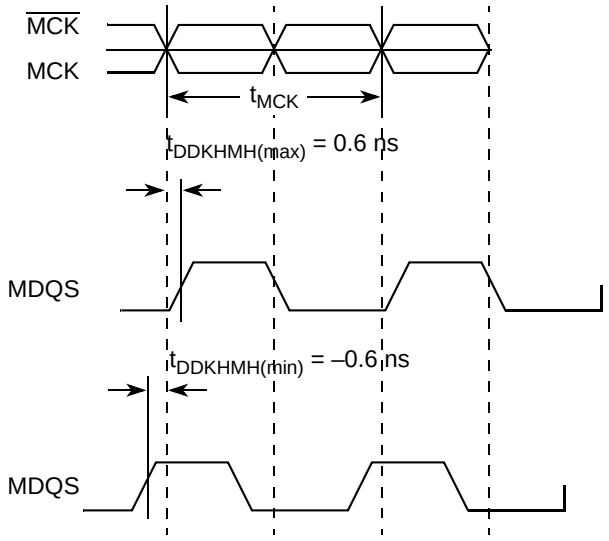


Figure 6. Timing Diagram for t_{DDKHMH}

This figure shows the DDR and DDR2 SDRAM output timing diagram.

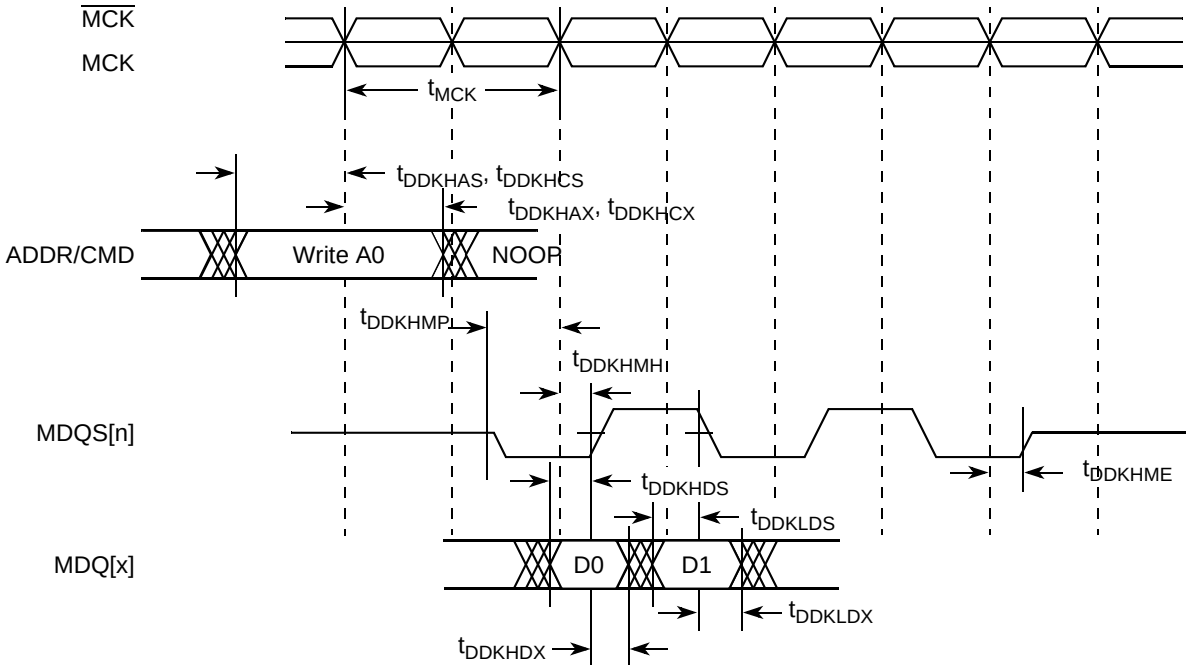


Figure 7. DDR and DDR2 SDRAM Output Timing Diagram

This figure shows the MII management AC timing diagram.

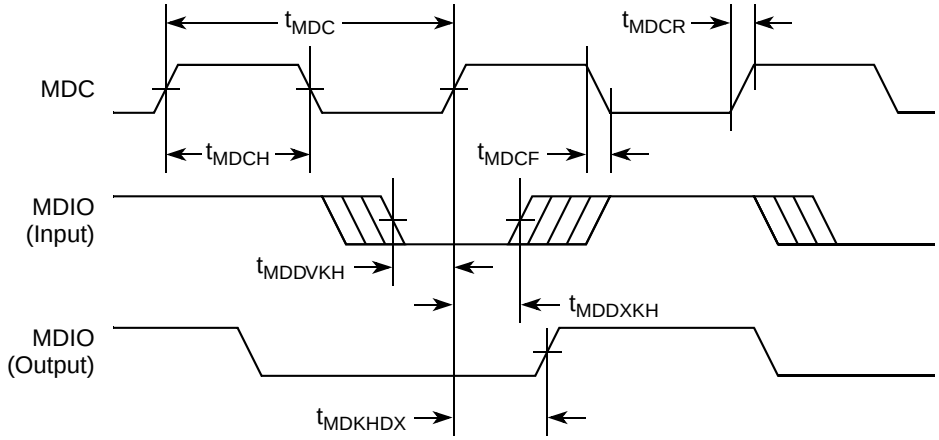


Figure 16. MII Management Interface Timing Diagram

9.4 1588 Timer Specifications

This section describes the DC and AC electrical specifications for the 1588 timer.

9.4.1 1588 Timer DC Specifications

This table provides the 1588 timer DC specifications.

Table 32. GPIO DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.0	NVDD + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	0 V ≤ V_{IN} ≤ NVDD	—	± 5	μA

9.4.2 1588 Timer AC Specifications

This table provides the 1588 timer AC specifications.

Table 33. 1588 Timer AC Specifications

Parameter	Symbol	Min	Max	Unit	Note
Timer clock cycle time	t_{TMRCK}	0	70	MHz	1
Input setup to timer clock	t_{TMRCKS}	—	—	—	2, 3
Input hold from timer clock	t_{TMRCKH}	—	—	—	2, 3
Output clock to output valid	t_{GCLKNV}	0	6	ns	
Timer alarm to output valid	t_{TMRAL}	—	—	—	2

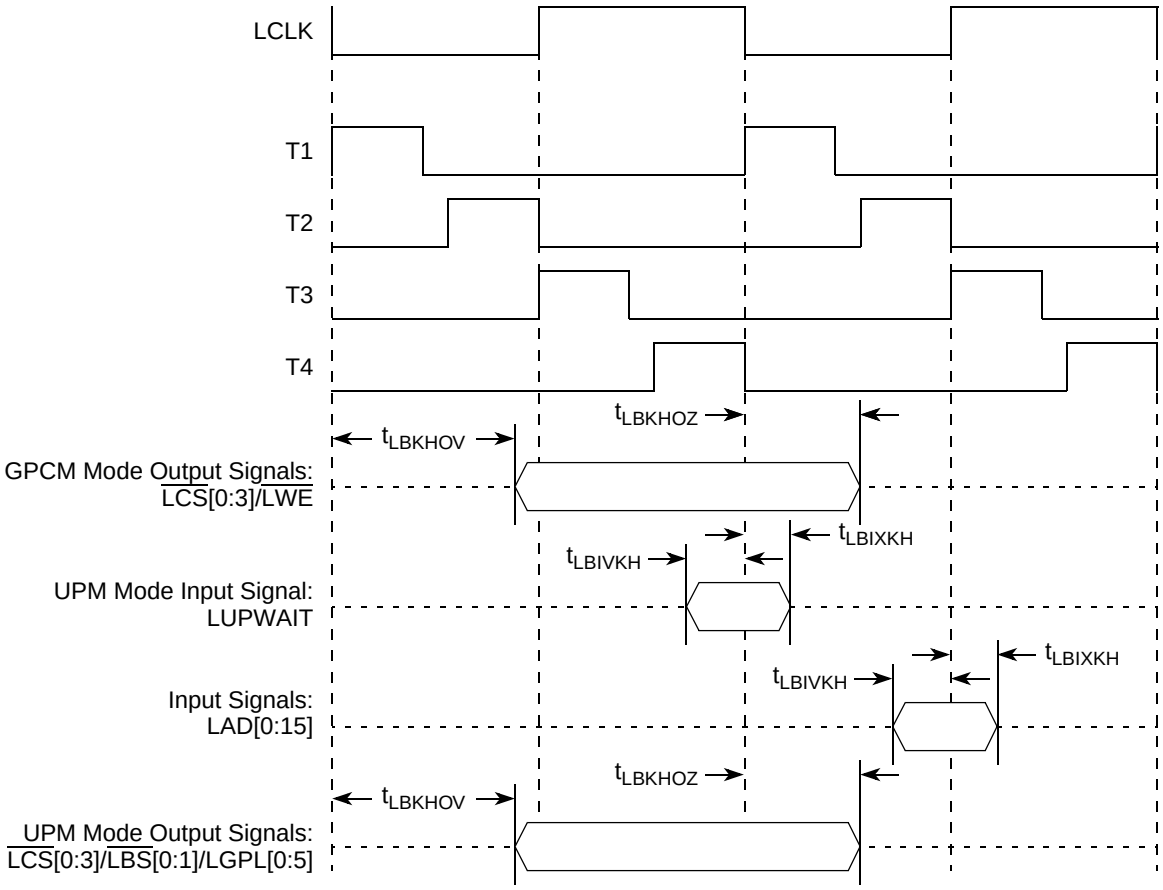


Figure 26. Local Bus Signals, GPCM/UPM Signals for LCRR[CLKDIV] = 4

12 JTAG

This section describes the DC and AC electrical specifications for the IEEE Std 1149.1™ (JTAG) interface.

12.1 JTAG DC Electrical Characteristics

This table provides the DC electrical characteristics for the IEEE 1149.1 (JTAG) interface.

Table 45. JTAG Interface DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Input high voltage	V_{IH}	—	2.1	NVDD + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	—	—	±5	μA
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V

The Differential Output Voltage (or Swing) of the transmitter, V_{OD}, is defined as the difference of the two complimentary output voltages: $V_{TXn} - V_{\overline{TXn}}$. The V_{OD} value can be either positive or negative.

3. **Differential Input Voltage, V_{ID}** (or **Differential Input Swing**):

   The Differential Input Voltage (or Swing) of the receiver, V_{ID}, is defined as the difference of the two complimentary input voltages: $V_{RXn} - V_{\overline{RXn}}$. The V_{ID} value can be either positive or negative.

4. **Differential Peak Voltage, V_{DIFFp}**

   The peak value of the differential transmitter output signal or the differential receiver input signal is defined as Differential Peak Voltage, $V_{DIFFp} = |A - B|$ Volts.

5. **Differential Peak-to-Peak, $V_{DIFFp-p}$**

   Because the differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to –(A – B) Volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as Differential Peak-to-Peak Voltage, $V_{DIFFp-p} = 2*V_{DIFFp} = 2 * |(A - B)|$ Volts, which is twice of differential swing in amplitude, or twice of the differential peak. For example, the output differential peak-peak voltage can also be calculated as $V_{TX-DIFFp-p} = 2*|V_{OD}|$.

6. **Differential Waveform**

   The differential waveform is constructed by subtracting the inverting signal ($\overline{TXn}$, for example) from the non-inverting signal (TXn, for example) within a differential pair. There is only one signal trace curve in a differential waveform. The voltage represented in the differential waveform is not referenced to ground. Refer to Figure 46 as an example for differential waveform.

7. **Common Mode Voltage, V_{cm}**

   The Common Mode Voltage is equal to one half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. In this example, for SerDes output, $V_{cm\_out} = (V_{TXn} + V_{\overline{TXn}})/2 = (A + B) / 2$, which is the arithmetic mean of the two complimentary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. Sometimes, it may be even different between the receiver input and driver output circuits within the same component. It's also referred as the DC offset in some occasion.

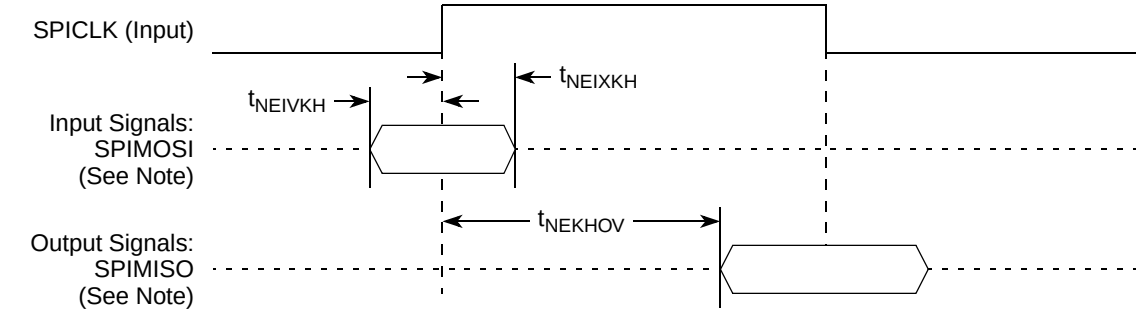
Table 54. Differential Transmitter (TX) Output Specifications (continued)

Parameter	Symbol	Comments	Min	Typical	Max	Unit	Note
Maximum time to transition to a valid electrical idle after sending an electrical idle ordered set	$T_{TX-IDLE-SET-TO-IDLE}$	After sending an Electrical Idle ordered set, the Transmitter must meet all Electrical Idle Specifications within this time. This is considered a debounce time for the Transmitter to meet Electrical Idle after transitioning from L0.	—	—	20	UI	—
Maximum time to transition to valid TX specifications after leaving an electrical idle condition	$T_{TX-IDLE-TO-DIFF-DATA}$	Maximum time to meet all TX specifications when transitioning from Electrical Idle to sending differential data. This is considered a debounce time for the TX to meet all TX specifications after leaving Electrical Idle	—	—	20	UI	—
Differential return loss	$RL_{TX-DIFF}$	Measured over 50 MHz to 1.25 GHz.	12	—	—	dB	4
Common mode return loss	RL_{TX-CM}	Measured over 50 MHz to 1.25 GHz.	6	—	—	dB	4
DC differential TX impedance	$Z_{TX-DIFF-DC}$	TX DC Differential mode Low Impedance	80	100	120	Ω	—
Transmitter DC impedance	Z_{TX-DC}	Required TX D+ as well as D- DC Impedance during all states	40	—	—	Ω	—
Lane-to-Lane output skew	$L_{TX-SKEW}$	Static skew between any two Transmitter Lanes within a single Link	—	—	500 + 2 UI	ps	—
AC coupling capacitor	C_{TX}	All Transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself.	75	—	200	nF	8
Crosslink random timeout	$T_{crosslink}$	This random timeout helps resolve conflicts in crosslink configuration by eventually resulting in only one Downstream and one Upstream Port.	0	—	1	ms	7

Note:

1. No test load is necessarily associated with this value.
2. Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 51 and measured over any 250 consecutive TX UIs. (Also refer to the transmitter compliance eye diagram shown in Figure 49.)
3. A T_{TX-EYE} = 0.70 UI provides for a total sum of deterministic and random jitter budget of $T_{TX-JITTER-MAX}$ = 0.30 UI for the transmitter collected over any 250 consecutive TX UIs. The $T_{TX-EYE-MEDIAN-to-MAX-JITTER}$ median is less than half of the total TX jitter budget collected over any 250 consecutive TX UIs. It should be noted that the median is not the same as the mean. The jitter median describes the point in time where the number of jitter points on either side is approximately equal as opposed to the averaged time value.
4. The transmitter input impedance shall result in a differential return loss greater than or equal to 12 dB and a common mode return loss greater than or equal to 6 dB over a frequency range of 50 MHz to 1.25 GHz. This input impedance requirement applies to all valid input levels. The reference impedance for return loss measurements is 50 Ω to ground for both the D+ and D– line (that is, as measured by a vector network analyzer with 50-Ω probes, see Figure 51). Note that the series capacitors, C_{TX}, is optional for the return loss measurement.
5. Measured between 20%–80% at transmitter package pins into a test load as shown in Figure 51 for both V_{TX-D+} and V_{TX-D-}.
6. See Section 4.3.1.8 of the *PCI Express Base Specifications*, Rev 1.0a.
7. See Section 4.2.6.3 of the *PCI Express Base Specifications*, Rev 1.0a.
8. MPC8315E SerDes transmitter does not have C_{TX} built-in. An external AC Coupling capacitor is required

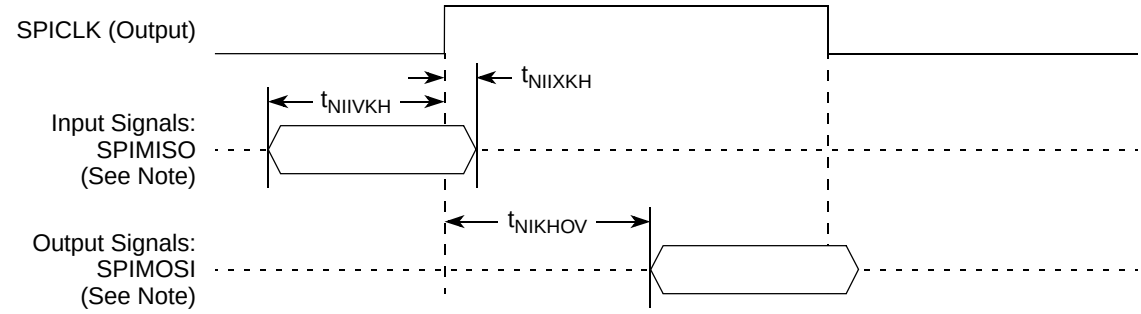
This figure shows the SPI timing in slave mode (external clock).



Note: The clock edge is selectable on SPI.

Figure 55. SPI AC Timing in Slave Mode (External Clock) Diagram

This figure shows the SPI timing in master mode (internal clock).



Note: The clock edge is selectable on SPI.

Figure 56. SPI AC Timing in Master Mode (Internal Clock) Diagram

21 TDM

This section describes the DC and AC electrical specifications for the TDM of the MPC8314E.

21.1 TDM DC Electrical Characteristics

This table provides the DC electrical characteristics TDM.

Table 64. TDM DC Electrical Characteristics

Characteristic	Symbol	Condition	Min	Max	Unit
Output high voltage	V_{OH}	I_{OH} = –8.0 mA	2.4	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0 mA	—	0.5	V
Output low voltage	V_{OL}	I_{OL} = 3.2 mA	—	0.4	V
Input high voltage	V_{IH}	—	2.1	NVDD + 0.3	V
Input low voltage	V_{IL}	—	–0.3	0.8	V
Input current	I_{IN}	0 V ≤ V_{IN} ≤ NVDD	—	± 5	μA

21.2 TDM AC Electrical Characteristics

This table provides the TDM AC timing specifications.

Table 65. TDM AC Timing specifications

Parameter/Condition	Symbol	Min	Max	Unit
TDMxRCK/TDMxTCK	t_{DM}	20.0	—	ns
TDMxRCK/TDMxTCK high pulse width	t_{DM_HIGH}	8.0	—	ns
TDMxRCK/TDMxTCK low pulse width	t_{DM_LOW}	8.0	—	ns
TDMxRCK/TDMxTCK rise time (20% to 80%)	t_{DMKH}	1.0	4.0	ns
TDMxRCK/TDMxTCK fall time (80% to 20%)	t_{DMKL}	1.0	4.0	ns
TDM all input setup time	t_{DMIVKH}	3.0	—	ns
TDMxRD hold time	$t_{DMRDIXKH}$	3.5	—	ns
TDMxTFS/TDMxRFS input hold time	$t_{DMFSIXKH}$	2.0	—	ns
TDMxTCK High to TDMxTD output active	t_{DM_OUTAC}	4.0	—	ns
TDMxTCK High to TDMxTD output valid	$t_{DMTKHOV}$	—	14.0	ns
TDMxTD hold time	$t_{DMTKHOX}$	2.0	—	ns
TDMxTCK High to TDMxTD output high impedance	t_{DM_OUTHI}	—	10.0	ns
TDMxTFS/TDMxRFS output valid	$t_{DMFSKHOV}$	—	13.5	ns
TDMxTFS/TDMxRFS output hold time	$t_{DMFSKHOX}$	2.5	—	ns

Note:

1. The symbols used for timing specifications herein follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. For example, $t_{TDMIVKH}$ symbolizes TDM timing (DM) with respect to the time the input signals (I) reach the valid state (V) relative to the TDM Clock, t_{TC}, reference (K) going to the high (H) state or setup time. Also, output signals (O), hold (X).
2. Output values are based on 30 pF capacitive load.
3. Inputs are referenced to the sampling that the TDM is programmed to use. Outputs are referenced to the programming edge they are programmed to use. Use of the rising edge or falling edge as a reference is programmable. TDMxTCK and TDMxRCK are shown using the rising edge.

This figure shows the TDM receive signal timing.

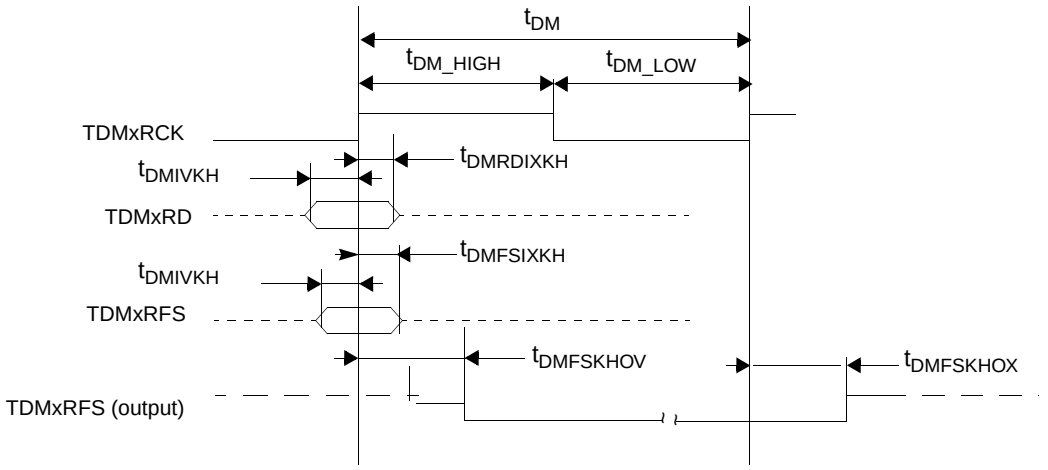


Figure 57. TDM Receive Signals

Table 66. MPC8314E TEPBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
TSEC2_TXD[1]/CFG_RESET_SOURCE[2]	E8	I/O	LVDD2_ON	—
TSEC2_TXD[0]/CFG_RESET_SOURCE[3]	B7	I/O	LVDD2_ON	—
TSEC2_TX_EN	D12	O	LVDD2_ON	—
TSEC2_TX_ER	B11	O	LVDD2_ON	—
SGMII / PCI Express PHY				
TXA	P4	O	XPADVDD	—
$\overline{\text{TXA}}$	N4	O	XPADVDD	—
RXA	R1	I	XCOREVDD	—
$\overline{\text{RXA}}$	P1	I	XCOREVDD	—
TXB	U4	O	XPADVDD	—
$\overline{\text{TXB}}$	V4	O	XPADVDD	—
RXB	U1	I	XCOREVDD	—
$\overline{\text{RXB}}$	V1	I	XCOREVDD	—
SD_IMP_CAL_RX	N3	I	XCOREVDD	—
$\overline{\text{SD\_REF\_CLK}}$	R4	I	XCOREVDD	—
SD_REF_CLK	R5	I	XCOREVDD	—
SD_PLL_TPD	T2	O	—	—
SD_IMP_CAL_TX	V5	I	XPADVDD	—
SDAVDD	T3	I	—	—
SD_PLL_TPA_ANA	T4	O	—	—
SDAVSS	T5	I	—	—
USB Phy				
USB_DP	A11	I/O	USB_VDDA	—
USB_DM	A12	I/O	USB_VDDA	—
USB_VBUS	C12	I	—	—
USB_TPA	A14	O	—	—
USB_RBIAS	D14	I	—	8
USB_PLL_PWR3	A13	I	—	—
USB_PLL_GND0 & USB_PLL_GND1	D13	I	—	—
USB_PLL_PWR1	B13	I	—	—
USB_VSSA_BIAS	E14	I	—	—
USB_VDDA_BIAS	C14	I	—	—
USB_VSSA	E13	I	—	—
USB_VDDA	E12	I	—	—
GPIO				
GPIO_0/$\overline{\text{DMA\_DREQ1}}$/$\overline{\text{GTM1\_TOUT1}}$	C5	I/O	NVDD1_ON	—

Table 66. MPC8314E TEPBGA II Pinout Listing (continued)

Signal	Package Pin Number	Pin Type	Power Supply	Note
GPIO_1/DMA_DACK1/GTM1_TIN2/GTM2_TIN1	A4	I/O	$NVDD1_{ON}$	—
GPIO_2/DMA_DONE1/GTM1_TGATE2/GTM2_TGATE1	K3	I/O	$NVDD4_{OFF}$	—
GPIO_3/GTM1_TIN3/GTM2_TIN4	K1	I/O	$NVDD4_{OFF}$	—
GPIO_4/GTM1_TGATE3/GTM2_TGATE4	K2	I/O	$NVDD4_{OFF}$	—
GPIO_5/GTM1_TOUT3/GTM2_TOUT1	L5	I/O	$NVDD4_{OFF}$	—
GPIO_6/GTM1_TIN4/GTM2_TIN3	L3	I/O	$NVDD4_{OFF}$	—
GPIO_7/GTM1_TGATE4/GTM2_TGATE3	L1	I/O	$NVDD4_{OFF}$	—
GPIO_8/USBDR_DRIVE_VBUS/GTM1_TIN1/GTM2_TIN2	M1	I/O	$NVDD4_{OFF}$	—
GPIO_9/USBDR_PWRFAULT/GTM1_TGATE1/GTM2_TGATE2	M2	I/O	$NVDD4_{OFF}$	—
GPIO_10/USBDR_PCTL0/GTM1_TOUT2/GTM2_TOUT1	M5	I/O	$NVDD4_{OFF}$	—
GPIO_11/USBDR_PCTL1/GTM1_TOUT4/GTM2_TOUT3	M4	I/O	$NVDD4_{OFF}$	—
SPI				
SPIMOSI/GPIO_15	W3	I/O	$NVDD1_{OFF}$	—
SPIMISO/GPIO_16	W4	I/O	$NVDD1_{OFF}$	—
SPICLK	Y1	I/O	$NVDD1_{OFF}$	—
SPISEL/GPIO_17	W2	I/O	$NVDD1_{OFF}$	—
Power and Ground Supplies				
GVDD	Y11, Y12, Y14, Y15, Y17, AC8, AC11, AC14, AC17, AD6, AD9, AD17, AE8, AE13, AE19, AF10, AF15, AF21, AG2, AG3, AG8, AG13, AG19, AH2	I	—	—
$LVDD1_{OFF}$	H6, J3, L6, L9, M9	I	—	—
$LVDD2_{ON}$	C11, D9, E10, F11, J12	I	—	—
$NVDD1_{OFF}$	U9, V9, W10, Y4, Y6, AA3, AB4	I	—	—
$NVDD1_{ON}$	B1, B2, C1, D5, E7, F5, F9, J11, K10	I	—	—
$NVDD2_{OFF}$	B22, B27, C19, E16, F15, F18, F21, F25, H25, J17, J18, J23, L20, M20	I	—	—
$NVDD2_{ON}$	L26, N19	I	—	—
$NVDD3_{OFF}$	U20, V20, V23, V26, W19, Y18, Y26, AA23, AA25, AC20, AC25, AD23, AE25, AG25, AG27, T27, U27	I	—	—
$NVDD4_{OFF}$	K4, L2, M6, N10	I	—	—

The primary clock source can be one of two inputs, SYS_CLK_IN or PCI_CLK, depending on whether the device is configured in PCI host or PCI agent mode. When the device is configured as a PCI host device, SYS_CLK_IN is its primary input clock. SYS_CLK_IN feeds the PCI clock divider (÷2) and the multiplexors for PCI_SYNC_OUT and PCI_CLK_OUT. The $\overline{\text{CFG\_SYS\_CLKIN\_DIV}}$ configuration input selects whether SYS_CLK_IN or SYS_CLK_IN/2 is driven out on the PCI_SYNC_OUT signal.

PCI_SYNC_OUT is connected externally to PCI_SYNC_IN to allow the internal clock subsystem to synchronize to the system PCI clocks. PCI_SYNC_OUT must be connected properly to PCI_SYNC_IN, with equal delay to all PCI agent devices in the system, to allow the device to function. When the device is configured as a PCI agent device, PCI_CLK is the primary input clock. When the device is configured as a PCI agent device the SYS_CLK_IN signal should be tied to GND.

As shown in Figure 60, the primary clock input (frequency) is multiplied up by the system phase-locked loop (PLL) and the clock unit to create the coherent system bus clock (*csb_clk*), the internal clock for the DDR controller (*ddr_clk*), and the internal clock for the local bus interface unit (*lbiu_clk*).

The *csb_clk* frequency is derived from a complex set of factors that can be simplified into the following equation:

$$csb\_clk = \{\text{PCI\_SYNC\_IN} \times (1 + \sim \overline{\text{CFG\_SYS\_CLKIN\_DIV}})\} \times \text{SPMF}$$

In PCI host mode, PCI_SYNC_IN × (1 + ~ $\overline{\text{CFG\_SYS\_CLKIN\_DIV}}$) is the SYS_CLK_IN frequency.

The *csb_clk* serves as the clock input to the e300 core. A second PLL inside the e300 core multiplies up the *csb_clk* frequency to create the internal clock for the e300 core (*core_clk*). The system and core PLL multipliers are selected by the SPMF and COREPLL fields in the reset configuration word low (RCWL) which is loaded at power-on reset or by one of the hard-coded reset options. See Chapter 4, “Reset, Clocking, and Initialization,” in the *MPC8315E PowerQUICC II Pro Integrated Host Processor Family Reference Manual* for more information on the clock subsystem.

The internal *ddr_clk* frequency is determined by the following equation:

$$ddr\_clk = csb\_clk \times (1 + \text{RCWL[DDRCM]})$$

Note that *ddr_clk* is not the external memory bus frequency; *ddr_clk* passes through the DDR clock divider (÷2) to create the differential DDR memory bus clock outputs (MCK and $\overline{\text{MCK}}$). However, the data rate is the same frequency as *ddr_clk*.

The internal *lbiu_clk* frequency is determined by the following equation:

$$lbiu\_clk = csb\_clk \times (1 + \text{RCWL[LBCM]})$$

Note that *lbiu_clk* is not the external local bus frequency; *lbiu_clk* passes through the LBIU clock divider to create the external local bus clock outputs (LCLK[0:1]). The LBIU clock divider ratio is controlled by LCRR[CLKDIV].

In addition, some of the internal units may be required to be shut off or operate at lower frequency than the *csb_clk* frequency. Those units have a default clock ratio that can be configured by a memory mapped register after the device comes out of reset. Table 67 specifies which units have a configurable clock frequency.

Table 67. Configurable Clock Units

Unit	Default Frequency	Options
eTSEC1	*csb_clk*	Off, *csb_clk, csb_clk/2, csb_clk/3*
eTSEC2	*csb_clk*	Off, *csb_clk, csb_clk/2, csb_clk/3*
Security Core, I2C, SAP, TPR	*csb_clk*	Off, *csb_clk, csb_clk/2, csb_clk/3*
USB DR	*csb_clk*	Off, *csb_clk, csb_clk/2, csb_clk/3*
PCI and DMA complex	*csb_clk*	Off, *csb_clk*
PCI Express	*csb_clk*	Off, *csb_clk*
Serial ATA	*csb_clk*	Off, *csb_clk, csb_clk/2, csb_clk/3*

This table provides the operating frequencies for the TEPBGA II under recommended operating conditions (see Table 2).

Table 68. Operating Frequencies for TEPBGA II

Characteristic[1]	Max Operating Frequency	Unit
e300 core frequency (*core_clk*)	400	MHz
Coherent system bus frequency (*csb_clk*)	133	MHz
DDR1/2 memory bus frequency (MCK)[2]	133	MHz
Local bus frequency (LCLK*n*)[3]	66	MHz
PCI input frequency (SYS_CLK_IN or PCI_CLK)	24-66	MHz

Note:
1. The SYS_CLK_IN frequency, RCWL[SPMF], and RCWL[COREPLL] settings must be chosen such that the resulting *csb_clk*, MCK, LCLK[0:1], and *core_clk* frequencies do not exceed their respective maximum or minimum operating frequencies.
2. The DDR data rate is 2x the DDR memory bus frequency.
3. The local bus frequency is 1/2, 1/4, or 1/8 of the *lbiu_clk* frequency (depending on LCRR[CLKDIV]) which is in turn 1x or 2x the *csb_clk* frequency (depending on RCWL[LBCM]).

23.1 System PLL Configuration

The system PLL is controlled by the RCWL[SPMF] parameter. Table 69 shows the multiplication factor encodings for the system PLL.

NOTE

If RCWL[DDRCM] and RCWL[LBCM] are both cleared, the system PLL VCO frequency = (CSB frequency) × (System PLL VCO Divider).

If either RCWL[DDRCM] or RCWL[LBCM] are set, the system PLL VCO frequency = 2 × (CSB frequency) × (System PLL VCO Divider).

The VCO divider needs to be set properly so that the System PLL VCO frequency is in the range of 450–750 MHz.

Table 73. Suggested PLL Configurations

Conf. No.	SPMF	Core\PLL	Input Clock Frequency (MHz)	CSB Frequency (MHz)	Core Frequency (MHz)
6	0010	0000101	66.67	133.33	333.33
7	0101	0000110	25	125	375
8	0100	0000110	33.33	133.33	400
9	0010	0000110	66.67	133.33	400

24 Thermal

This section describes the thermal specifications of the MPC8314E.

24.1 Thermal Characteristics

This table provides the package thermal characteristics for the 620 29 × 29 mm TEPBGA II.

Table 74. Package Thermal Characteristics for TEPBGA II

Characteristic	Board type	Symbol	Value	Unit	Note
Junction to ambient natural convection	Single layer board (1s)	$R_{\theta JA}$	23	°C/W	1, 2
Junction to ambient natural convection	Four layer board (2s2p)	$R_{\theta JA}$	16	°C/W	1, 2, 3
Junction to ambient (@200 ft/min)	Single layer board (1s)	$R_{\theta JMA}$	18	°C/W	1, 3
Junction to ambient (@200 ft/min)	Four layer board (2s2p)	$R_{\theta JMA}$	13	°C/W	1, 3
Junction to board	—	$R_{\theta JB}$	8	°C/W	4
Junction to case	—	$R_{\theta JC}$	6	°C/W	5
Junction to package top	Natural convection	Ψ_{JT}	6	°C/W	6

Note:

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with the single layer board horizontal. Board meets JESD51-9 specification.
3. Per JEDEC JESD51-6 with the board horizontal.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

24.2.3 Experimental Determination of Junction Temperature

To determine the junction temperature of the device in the application after prototypes are available, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using the following equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

T_J = junction temperature (°C)

T_T = thermocouple temperature on top of package (°C)

Ψ_{JT} = junction to ambient thermal resistance (°C/W)

P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

24.2.4 Heat Sinks and Junction-to-Case Thermal Resistance

In some application environments, a heat sink is required to provide the necessary thermal management of the device. When a heat sink is used, the thermal resistance is expressed as the sum of a junction to case thermal resistance and a case to ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

$R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)

$R_{\theta JC}$ = junction to case thermal resistance (°C/W)

$R_{\theta CA}$ = case to ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

To illustrate the thermal performance of the devices with heat sinks, the thermal performance has been simulated with a few commercially available heat sinks. The heat sink choice is determined by the application environment (temperature, air flow, adjacent component power dissipation) and the physical space available. Because there is not a standard application environment, a standard heat sink is not required.

Millennium Electronics (MEI) Loroco Sites 671 East Brokaw Road San Jose, CA 95112 Internet: www.mei-thermal.com	408-436-8770
Tyco Electronics Chip Coolers™ P.O. Box 3668 Harrisburg, PA 17105 Internet: www.tycoelectronics.com	800-522-6752
Wakefield Engineering 33 Bridge St. Pelham, NH 03076 Internet: www.wakefield.com	603-635-2800

Interface material vendors include the following:

Chomerics, Inc. 77 Dragon Ct. Woburn, MA 01801 Internet: www.chomerics.com	781-935-4850
Dow-Corning Corporation Corporate Center PO BOX 994 Midland, MI 48686-0994 Internet: www.dowcorning.com	800-248-2481
Shin-Etsu MicroSi, Inc. 10028 S. 51st St. Phoenix, AZ 85044 Internet: www.microsi.com	888-642-7674
The Bergquist Company 18930 West 78th St. Chanhassen, MN 55317 Internet: www.bergquistcompany.com	800-347-4572

24.3 Heat Sink Attachment

When attaching heat sinks to these devices, an interface material is required. The best method is to use thermal grease and a spring clip. The spring clip should connect to the printed circuit board, either to the board itself, to hooks soldered to the board, or to a plastic stiffener. Avoid attachment forces which would lift the edge of the package or peel the package from the board. Such peeling forces reduce the solder joint lifetime of the package. Recommended maximum force on the top of the package is 10 lb force (45 Newtons). If an adhesive attachment is planned, the adhesive should be intended for attachment to painted or plastic surfaces and its performance verified under the application requirements.

Power and ground connections must be made to all external VDD, GVDD, LVDD, NVDD, and GND pins of the device.

25.5 Output Buffer DC Impedance

The MPC8314E drivers are characterized over process, voltage, and temperature. For all buses, the driver is a push-pull single-ended driver type (open drain for I^2C).

To measure Z_0 for the single-ended drivers, an external resistor is connected from the chip pad to NVDD or GND. Then, the value of each resistor is varied until the pad voltage is NVDD/2 (see Figure 62). The output impedance is the average of two components, the resistances of the pull-up and pull-down devices. When data is held high, SW1 is closed (SW2 is open) and R_P is trimmed until the voltage at the pad equals NVDD/2. R_P then becomes the resistance of the pull-up devices. R_P and R_N are designed to be close to each other in value. Then, $Z_0 = (R_P + R_N)/2$.

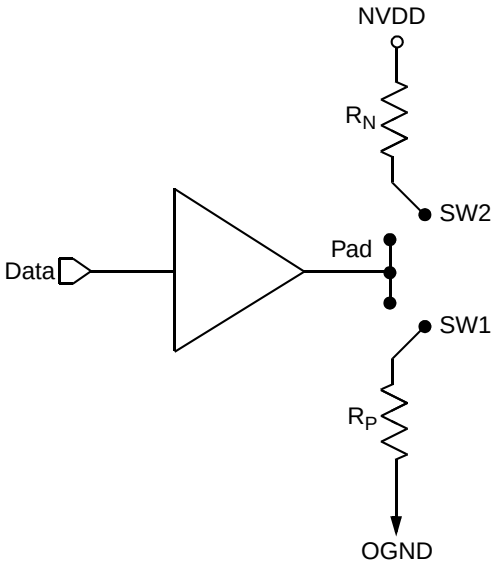


Figure 62. Driver Impedance Measurement

The value of this resistance and the strength of the driver's current source can be found by making two measurements. First, the output voltage is measured while driving logic 1 without an external differential termination resistor. The measured voltage is $V_1 = R_{source} \times I_{source}$. Second, the output voltage is measured while driving logic 1 with an external precision differential termination resistor of value R_{term}. The measured voltage is $V_2 = (1/(1/R_1 + 1/R_2)) \times I_{source}$. Solving for the output impedance gives $R_{source} = R_{term} \times (V_1/V_2 - 1)$. The drive current is then $I_{source} = V_1/R_{source}$.

This table summarizes the signal impedance targets. The driver impedance are targeted at minimum VDD, nominal NVDD, 105°C.

Table 76. Impedance Characteristics

Impedance	Local Bus, Ethernet, DUART, Control, Configuration, Power Management	PCI Signals (not including PCI Output Clocks)	PCI Output Clocks (including PCI_SYNC_OUT)	DDR DRAM	Symbol	Unit
R_N	42 Target	25 Target	42 Target	20 Target	Z_0	Ω
R_P	42 Target	25 Target	42 Target	20 Target	Z_0	Ω
Differential	NA	NA	NA	NA	Z_{DIFF}	Ω

Note: Nominal supply voltages. See Table 1, T_j = 105°C.

25.6 Configuration Pin Multiplexing

The MPC8314E provides the user with power-on configuration options that can be set through the use of external pull-up or pull-down resistors of 4.7 kΩ on certain output pins (see customer visible configuration pins). These pins are generally used as output only pins in normal operation.

While $\overline{\text{HRESET}}$ is asserted however, these pins are treated as inputs. The value presented on these pins while $\overline{\text{HRESET}}$ is asserted, is latched when $\overline{\text{PORESET}}$ deasserts, at which time the input receiver is disabled and the I/O circuit takes on its normal function. Careful board layout with stubless connections to these pull-up/pull-down resistors coupled with the large value of the pull-up/pull-down resistor should minimize the disruption of signal quality or speed for output pins thus configured.

25.7 Pull-Up Resistor Requirements

The MPC8314E requires high resistance pull-up resistors (10 kΩ is recommended) on open drain type pins including I^2C pins and EPIC interrupt pins.

For more information on required pull up resistors and the connections required for JTAG interface, see AN3438, MPC8315 Design Checklist

26 Ordering Information

Ordering information for the parts fully covered by this specification document is provided in Section 26.1, “Part Numbers Fully Addressed by this Document.”

26.1 Part Numbers Fully Addressed by this Document

This table provides the Freescale part numbering nomenclature for the MPC8314E. Note that the individual part numbers correspond to a maximum processor core frequency. For available frequencies, contact your local Freescale sales office. In addition to the processor frequency, the part numbering scheme

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