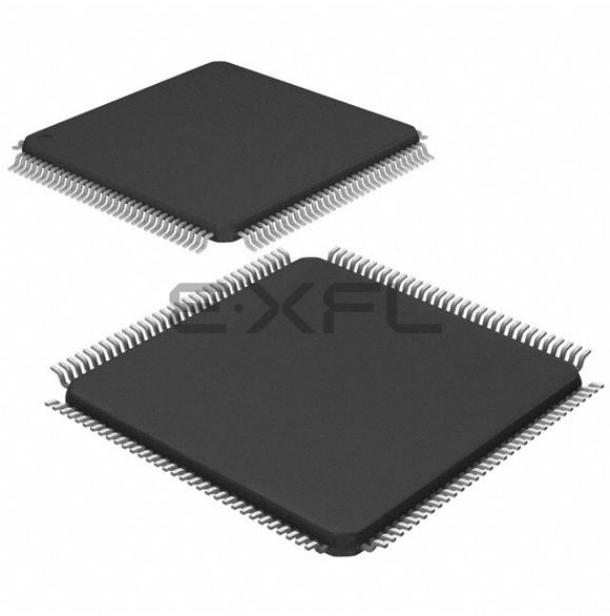
Rohm Semiconductor - ML610Q428-NNNTBZ03A7 Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	nX-U8/100
Core Size	8-Bit
Speed	4.2MHz
Connectivity	I²C, SSP, UART/USART
Peripherals	LCD, Melody Driver, POR, PWM, WDT
Number of I/O	14
Program Memory Size	48KB (24K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	1.1V ~ 3.6V
Data Converters	A/D 2x12b, 2x24b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	128-TQFP
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/rohm-semi/ml610q428-nnntbz03a7

- PWM
  - Resolution 16 bits × 3 channel

- Synchronous serial port
  - Master/slave selectable
  - LSB first/MSB first selectable
  - 8-bit length/16-bit length selectable
  - Timer interrupt is used as a serial clock and selection is possible

- UART
  - TXD/RXD × 1 channel
  - Bit length, parity/no parity, odd parity/even parity, 1 stop bit/2 stop bits
  - Positive logic/negative logic selectable
  - Built-in baud rate generator

- I^2C bus interface
  - Master function only
  - Fast mode (400 kbps@4MHz), standard mode (100 kbps@4MHz, 50kbps@500kHz)

- Melody driver
  - Scale: 29 types (Melody sound frequency: 508 Hz to 32.768 kHz)
  - Tone length: 63 types
  - Tempo: 15 types
  - Buzzer output mode (4 output modes, 8 frequencies, 16 duty levels)

- RC oscillation type A/D converter
  - 24-bit counter
  - Time division × 2 channels

- Successive approximation type A/D converter
  - 12-bit A/D converter
  - Input × 2 channels

- General-purpose ports
  - Non-maskable interrupt input port × 1 channel
  - Input-only port × 10 channels (including secondary functions)
  - Output-only port × 3 channels (including secondary functions)
  - Input/output port
    ML610Q428: 14 channels (including secondary functions)
    ML610Q429: 20 channels (including secondary functions)

- LCD driver
  - Dot matrix can be supported.
    ML610Q428: 1392 dots max. (58 seg × 24 com), 1/1 to 1/24 duty
    ML610Q429: 512 dots max. (64 seg × 8 com) , 1/1 to 1/8 duty
  - 1/3 or 1/4 bias (built-in bias generation circuit)
  - Frame frequency selecable (approx. 32Hz, 64 Hz, 73 Hz, 85 Hz, and 102 Hz)
  - Bias voltage multiplying clock selectable (8 types)
  - Contrast adjustment (1/3 bias: 32 steps, 1/4 bias: 20 steps)
  - LCD drive stop mode, LCD display mode, all LCDs on mode, and all LCDs off mode selectable
  - Programmable display allocation function (available only when 1/1~1/8 duty is selected)

- Reset
  - Reset through the RESET_N pin
  - Power-on reset generation when powered on
  - Reset when oscillation stop of the low-speed clock is detected
  - Reset by the watchdog timer (WDT) overflow

- Power supply voltage detect function
  - Judgment voltages: One of 16 levels
  - Judgment accuracy: ±2% (Typ.)

- Clock
  - Low-speed clock: (This LSI can not guarantee the operation withoug low-speed clock)
    Crystal oscillation (32.768 kHz)
  - High-speed clock:
    Built-in RC oscillation (2M/500kHz)
    Built-in PLL oscillation (8.192 MHz ±2.5%), crystal/ceramic oscillation (4.096 MHz), external clock
  - Selection of high-speed clock mode by software:
    Built-in RC oscillation, built-in PLL oscillation, crystal/ceramic oscillation, external clock

- Power management
  - HALT mode: Instruction execution by CPU is suspended (peripheral circuits are in operating states).
  - STOP mode: Stop of low-speed oscillation and high-speed oscillation (Operations of CPU and peripheral circuits are stopped.)
  - Clock gear: The frequency of high-speed system clock can be changed by software (1/1, 1/2, 1/4, or 1/8 of the oscillation clock)
  - Block Control Function: Power down (reset registers and stop clock supply) the circuits of unused peripherals.

- Guaranteed operating range
  - Operating temperature: –20°C to 70°C
  - Operating voltage: V_{DD} = 1.1V to 3.6V

- Product name – Supported Function
  The lien up to the ML610Q428and ML610Q429 is beiow.

- Chip (Die) -	ROM type	Operating temperature	Product availability
ML610Q428-xxxWA	Flash ROM	-20°C to +70°C	Yes
ML610Q429-xxxWA	Flash ROM	-20°C to +70°C	Yes

-128-pin plastic TQFP -	ROM type	Operating temperature	Product availability
ML610Q428-xxxTB	Flash ROM	-20°C to +70°C	Yes
ML610Q429-xxxTB	Flash ROM	-20°C to +70°C	Yes

xxx: ROM code number (xxx of the blank product is NNN)
Q:Flash ROM version
WA: Chip
TB: TQFP

BLOCK DIAGRAM

ML610Q428 Block Diagram

Figure 1 show the block diagram of the ML610Q428.
"*" indicates the secondary function of each port.

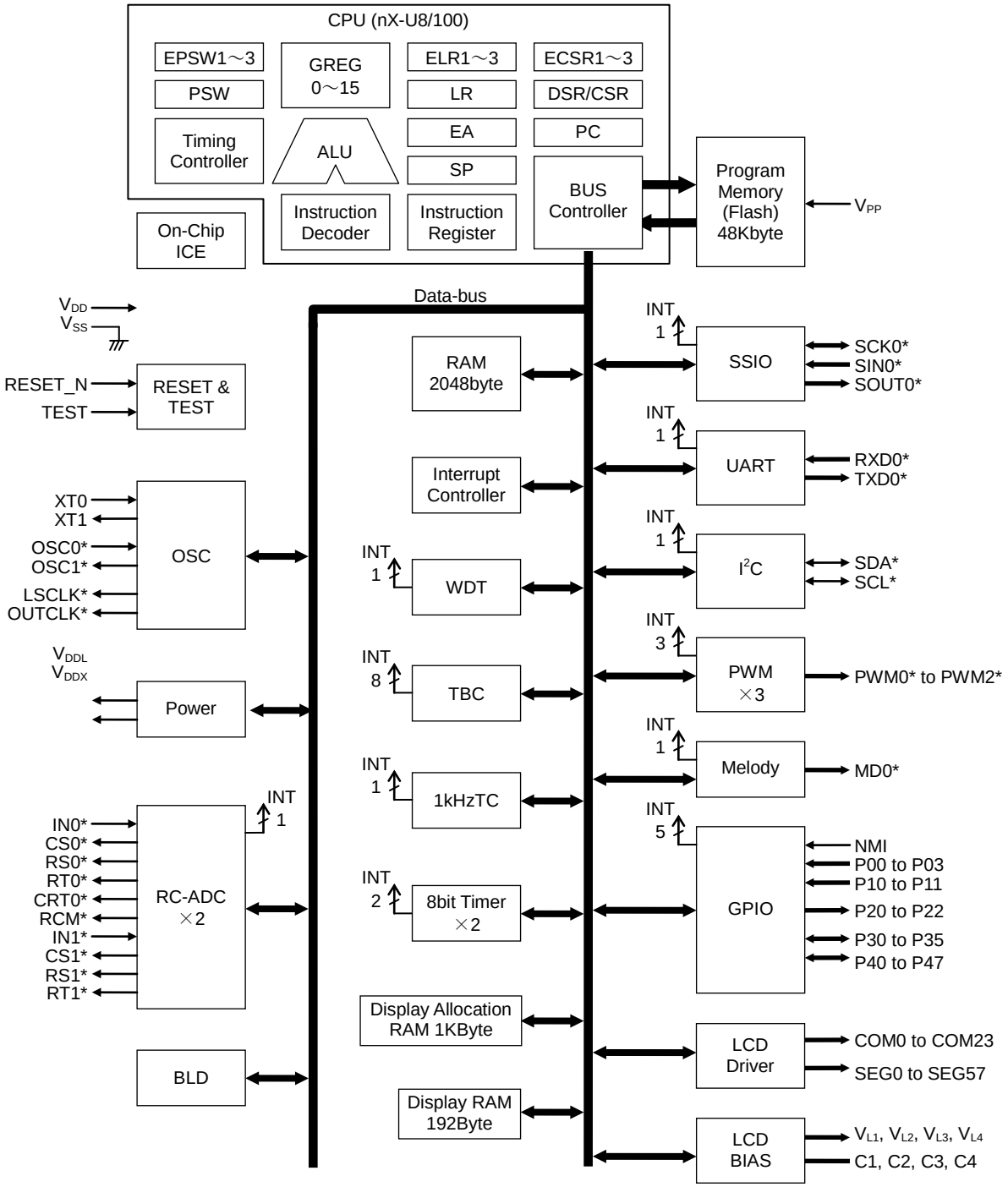
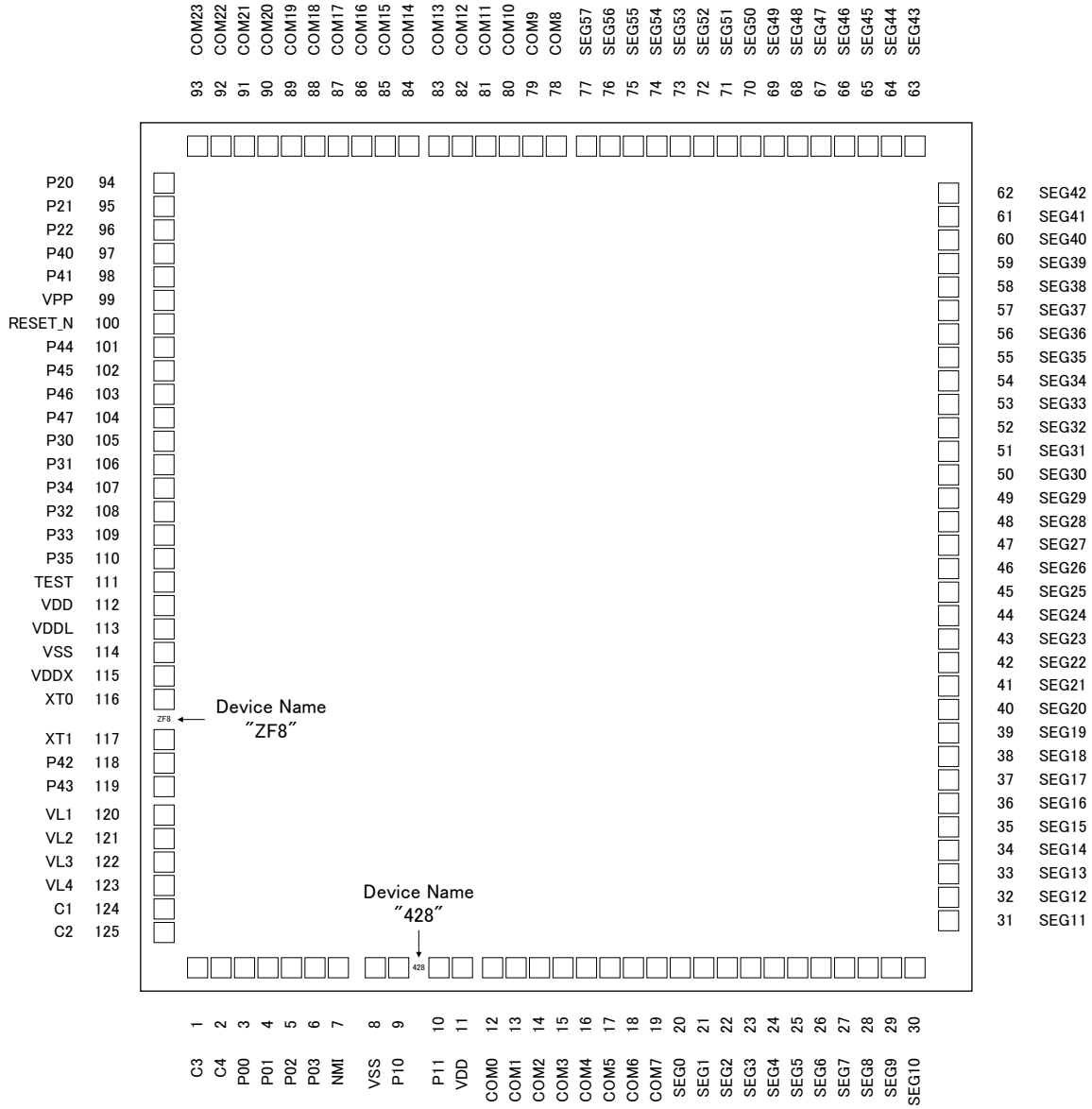


Figure 1 ML610Q428 Block Diagram

ML610Q428 Chip Dimension

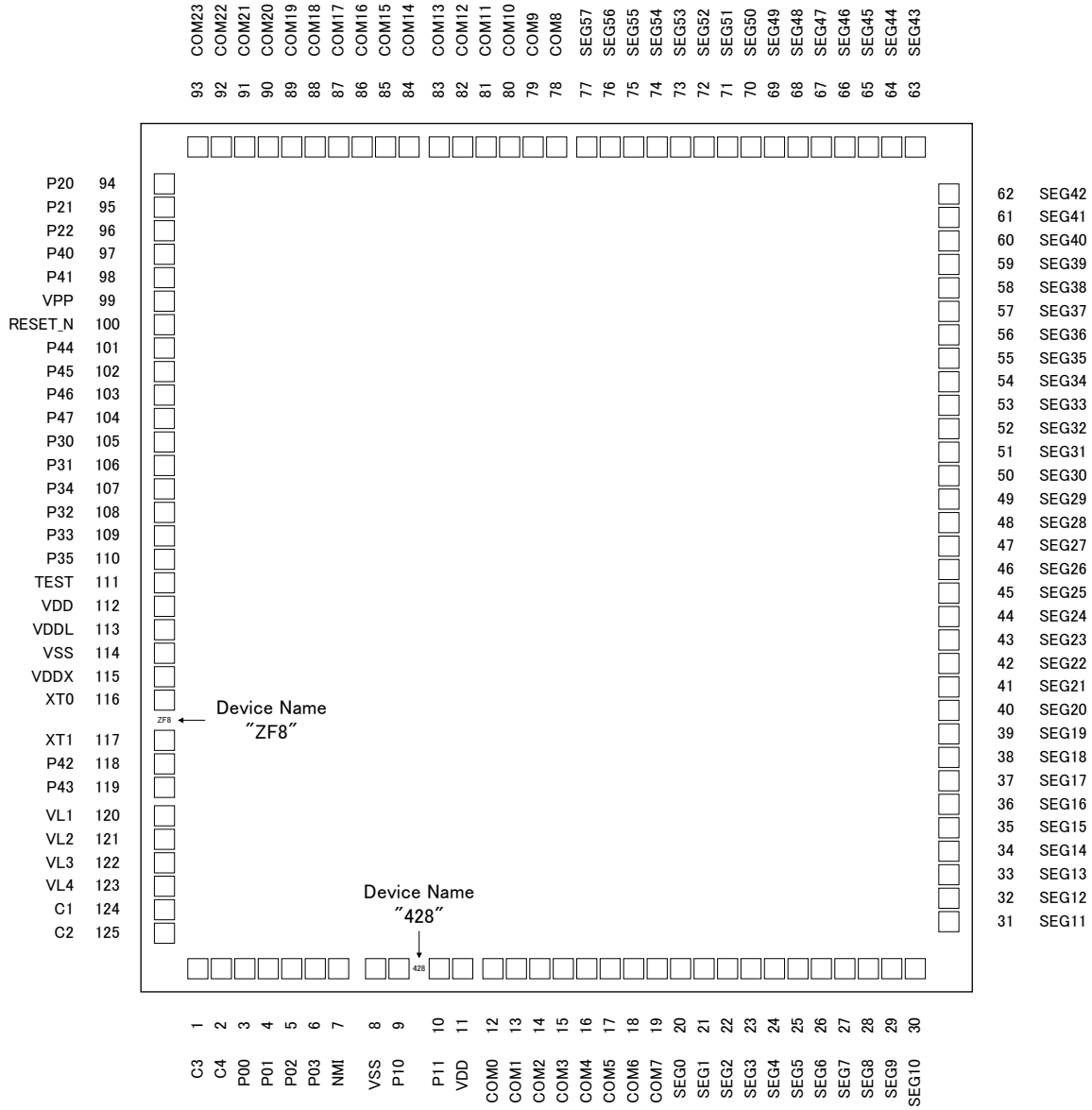


Chip size:	2.99 mm × 3.11 mm
PAD count:	125 pins
Minimum PAD pitch:	80 μm
PAD aperture:	70 μm × 70 μm
Chip thickness:	350 μm
Voltage of the rear side of chip:	V_{SS} level

Figure 5 ML610Q428 Chip Dimension

Note:
Figure 5 is an image figure of the order of PAD, and it differs from an actual image. Refer to the PAD coordinate for detailed arrangement.
A chip angle can be checked by the distinguishing mark of three figures.

ML610Q429 Chip Dimension



Chip size:	2.99 mm × 3.11 mm
PAD count:	125 pins
Minimum PAD pitch:	80 μm
PAD aperture:	70 μm × 70 μm
Chip thickness:	350 μm
Voltage of the rear side of chip:	V_{SS} level

Figure 6 ML610Q429 Chip Dimension

Note:
Figure 6 is an image figure of the order of PAD, and it differs from an actual image. Refer to the PAD coordinate for detailed arrangement.
A chip angle can be checked by the distinguishing mark of three figures.

PIN LIST

PAD No.		Primary function			Secondary function			Tertiary function		
Q429	Q428	Pin name	I/O	Function	Pin name	I/O	Function	Pin name	I/O	Function
8,114	8,114	Vss	—	Negative power supply pin	—	—	—	—	—	—
11,112	11,112	V_{DD}	—	Positive power supply pin	—	—	—	—	—	—
113	113	V_{DDL}	—	Power supply pin for internal logic (internally generated)	—	—	—	—	—	—
115	115	V_{DDX}	—	Power supply pin for low-speed oscillation (internally generated)	—	—	—	—	—	—
99	99	V_{PP}	—	Power supply pin for Flash ROM	—	—	—	—	—	—
120	120	V_{L1}	—	Power supply pin for LCD bias (internally generated)	—	—	—	—	—	—
121	121	V_{L2}	—	Power supply pin for LCD bias (internally generated)	—	—	—	—	—	—
122	122	V_{L3}	—	Power supply pin for LCD bias (internally generated)	—	—	—	—	—	—
123	123	V_{L4}	—	Power supply pin for LCD bias (internally generated)	—	—	—	—	—	—
124	124	C1	—	Capacitor connection pin for LCD bias generation	—	—	—	—	—	—
125	125	C2	—	Capacitor connection pin for LCD bias generation	—	—	—	—	—	—
1	1	C3	—	Capacitor connection pin for LCD bias generation	—	—	—	—	—	—
2	2	C4	—	Capacitor connection pin for LCD bias generation	—	—	—	—	—	—
111	111	TEST	I/O	Input/output pin for testing	—	—	—	—	—	—
100	100	RESET_N	I	Reset input pin	—	—	—	—	—	—
116	116	XT0	I	Low-speed clock oscillation pin	—	—	—	—	—	—
117	117	XT1	O	Low-speed clock oscillation pin	—	—	—	—	—	—
7	7	NMI	I	Non-maskable interrupt pin	—	—	—	—	—	—
3	3	P00/EXI0	I	Input port, External interrupt 0 input	—	—	—	—	—	—
4	4	P01/EXI1	I	Input port, External interrupt 1 input	—	—	—	—	—	—
5	5	P02/EXI2 /RXD0 /P2CK	I	Input port, External interrupt 2, UART0 receive, PWM2 external clock input	—	—	—	—	—	—
6	6	P03/EXI3	I	Input port, External interrupt 3	—	—	—	—	—	—
90	—	P04/EXI4	I/O	Input port, External interrupt 4	—	—	—	—	—	—
91	—	P05/EXI5	I/O	Input port, External interrupt 5	—	—	—	—	—	—
92	—	P06/EXI6	I/O	Input port, External interrupt 6	—	—	—	—	—	—
93	—	P07/EXI7	I/O	Input port, External	—	—	—	—	—	—

PAD No.		Primary function			Secondary function			Tertiary function		
Q429	Q428	Pin name	I/O	Function	Pin name	I/O	Function	Pin name	I/O	Function
				interrupt 7						
9	9	P10	I	Input port	OSC0	I	High-speed oscillation	—	—	—
10	10	P11	I	Input port	OSC1	O	High-speed oscillation	—	—	—
94	94	P20/LED0	O	Output port	LSCLK	O	Low-speed clock output	PWM2	O	PWM2 output
95	95	P21/LED1	O	Output port	OUTCLK	O	High-speed clock output	—	—	—
96	96	P22/LED2	O	Output port	MD0	O	Melody output	—	—	—
105	105	P30	I/O	Input/output port	IN0	I	RC type ADC0 oscillation input pin	PWM2	O	PWM2 output
106	106	P31	I/O	Input/output port	CS0	O	RC type ADC0 reference capacitor connection pin	—	—	—
108	108	P32	I/O	Input/output port	RS0	O	RC type ADC0 reference resistor connection pin	—	—	—
109	109	P33	I/O	Input/output port	RT0	O	RC type ADC0 resistor sensor connection pin	—	—	—
107	107	P34	I/O	Input/output port	RCT0	O	RC type ADC0 resistor/capacitor sensor connection pin	PWM0	O	PWM0 output
110	110	P35	I/O	Input/output port	RCM	O	RC type ADC oscillation monitor	PWM1	O	PWM1 output
97	97	P40	I/O	Input/output port	SDA	I/O	I^2C data input/output	SIN0	I	SSIO data input
98	98	P41	I/O	Input/output port	SCL	I/O	I^2C clock input/output	SCK0	I/O	SSIO synchronous clock
118	118	P42	I/O	Input/output port	RXD0	I	UART data input	SOUT0	O	SSIO data output
119	119	P43	I/O	Input/output port	TXD0	O	UART data output	PWM0	O	PWM0 output
101	101	P44/T02P0CK	I/O	Input/output port, Timer 0/Timer 2/PWM0 external clock input	IN1	I	RC type ADC1 oscillation input pin	SIN0	I	SSIO0 data input
102	102	P45/T13P1CK	I/O	Input/output port, Timer 1/Timer 3/PWM1 external clock input	CS1	O	RC type ADC1 reference capacitor connection pin	SCK0	I/O	SSIO0 synchronous clock
103	103	P46/T46P2CK	I/O	Input/output port, PWM2 external clock input	RS1	O	RC type ADC1 reference resistor connection pin	SOUT0	O	SSIO0 data output
104	1004	P47	I/O	Input/output port	RT1	O	RC type ADC1 resistor sensor connection pin	PWM1	O	PWM1 output
84	—	PA0	I/O	Input/output port	—	—	—	—	—	—
85	—	PA1	I/O	Input/output port	—	—	—	—	—	—
86	—	PA2	I/O	Input/output port	—	—	—	—	—	—
87	—	PA3	I/O	Input/output port	—	—	—	—	—	—
88	—	PA4	I/O	Input/output port	—	—	—	—	—	—
89	—	PA5	I/O	Input/output port	—	—	—	—	—	—
12	12	COM0	O	LCD common pin	—	—	—	—	—	—
13	13	COM1	O	LCD common pin	—	—	—	—	—	—
14	14	COM2	O	LCD common pin	—	—	—	—	—	—
15	15	COM3	O	LCD common pin	—	—	—	—	—	—
16	16	COM4	O	LCD common pin	—	—	—	—	—	—
17	17	COM5	O	LCD common pin	—	—	—	—	—	—
18	18	COM6	O	LCD common pin	—	—	—	—	—	—
19	19	COM7	O	LCD common pin	—	—	—	—	—	—
—	78	COM8	O	LCD common pin	—	—	—	—	—	—
—	79	COM9	O	LCD common pin	—	—	—	—	—	—
—	80	COM10	O	LCD common pin	—	—	—	—	—	—
—	81	COM11	O	LCD common pin	—	—	—	—	—	—
—	82	COM12	O	LCD common pin	—	—	—	—	—	—
—	83	COM13	O	LCD common pin	—	—	—	—	—	—
—	84	COM14	O	LCD common pin	—	—	—	—	—	—
—	85	COM15	O	LCD common pin	—	—	—	—	—	—

PIN DESCRIPTION

Pin name	I/O	Description	Primary/ Secondary/ Tertiary	Logic
System				
RESET_N	I	Reset input pin. When this pin is set to a “L” level, system reset mode is set and the internal section is initialized. When this pin is set to a “H” level subsequently, program execution starts. A pull-up resistor is internally connected.	—	Negative
XT0	I	Crystal connection pin for low-speed clock.	—	—
XT1	O	A 32.768 kHz crystal oscillator (see measuring circuit 1) is connected to this pin. Capacitors CDL and CGL are connected across this pin and V_{SS} as required.	—	—
OSC0	I	Crystal/ceramic connection pin for high-speed clock.	Secondary	—
OSC1	O	A crystal or ceramic is connected to this pin (4.1 MHz max.). Capacitors CDH and CGH (see measuring circuit 1) are connected across this pin and V_{SS}. This pin is used as the secondary function of the P10 pin(OSC0) and P11 pin(OSC1).	Secondary	—
LSCLK	O	Low-speed clock output pin. This pin is used as the secondary function of the P20 pin.	Secondary	—
OUTCLK	O	High-speed clock output pin. This pin is used as the secondary function of the P21 pin.	Secondary	—
General-purpose input port				
P00-P03	I	General-purpose input port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
P04-P07	I	General-purpose input port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used. These pins are for the ML610Q429, but are not provided in the ML610Q428.	Primary	Positive
P10-P11	I	General-purpose input port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
General-purpose output port				
P20-P22	O	General-purpose output port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
General-purpose input/output port				
P30-P35	I/O	General-purpose input/output port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
P40-P47	I/O	General-purpose input/output port. Since these pins have secondary functions, the pins cannot be used as a port when the secondary functions are used.	Primary	Positive
PA0-PA5	I/O	General-purpose input/output port. These pins are for the ML610Q429, but are not provided in the ML610Q428.	Primary	Positive

Pin name	I/O	Description	Primary/ Secondary/ Tertiary	Logic
UART				
TXD0	O	UART data output pin. This pin is used as the secondary function of the P43 pin.	Secondary	Positive
RXD0	I	UART data input pin. This pin is used as the secondary function of the P42 or the primary function of the P02 pin.	Primary/Secondary	Positive
I^2C bus interface				
SDA	I/O	I^2C data input/output pin. This pin is used as the secondary function of the P40 pin. This pin has an NMOS open drain output. When using this pin as a function of the I^2C, externally connect a pull-up resistor.	Secondary	Positive
SCL	O	I^2C clock output pin. This pin is used as the secondary function of the P41 pin. This pin has an NMOS open drain output. When using this pin as a function of the I^2C, externally connect a pull-up resistor.	Secondary	Positive
Synchronous serial (SSIO)				
SCK0	I/O	Synchronous serial clock input/output pin. This pin is used as the tertiary function of the P41 or P45 pin.	Tertiary	—
SIN0	I	Synchronous serial data input pin. This pin is used as the tertiary function of the P40 or P44 pin.	Tertiary	Positive
SOUT0	O	Synchronous serial data output pin. This pin is used as the tertiary function of the P42 or P46 pin.	Tertiary	Positive
PWM				
PWM0	O	PWM0 output pin. This pin is used as the tertiary function of the P43 or P34 pin.	Tertiary	Positive
T0P0CK	I	PWM0 external clock input pin. This pin is used as the primary function of the P44 pin.	Primary	—
PWM1	O	PWM1 output pin. This pin is used as the tertiary function of the P47 or P35 pin.	Tertiary	Positive
T1P1CK	I	PWM1 external clock input pin. This pin is used as the primary function of the P45 pin.	Primary	—
PWM2	O	PWM2 output pin. This pin is used as the tertiary function of the P20 or P30 pin.	Tertiary	Positive
P2CK	I	PWM2 external clock input pin. This pin is used as the primary function of the P02 pin.	Primary	—
External interrupt				
NMI	I	External non-maskable interrupt input pin. An interrupt is generated on both edges.	Primary	Positive/ negative
EXI0-7	I	External maskable interrupt input pins. Interrupt enable and edge selection can be performed for each bit by software. These pins are used as the primary functions of the P00-P07 pins.	Primary	Positive/ negative
Timer				
T0P0CK	I	External clock input pin used for Timer 0. This pin is used as the primary function of the P44 pin.	Primary	—
T1P1CK	I	External clock input pin used for Timer 1. This pin is used as the primary function of the P45 pin.	Primary	—
Melody				
MD0	O	Melody/buzzer signal output pin. This pin is used as the secondary function of the P22 pin.	Secondary	Positive/ negative
LED drive				
LED0-2	O	Nch open drain output pins to drive LED.	Primary	Positive/ negative

Pin name	I/O	Description	Primary/ Secondary/ Tertiary	Logic
RC oscillation type A/D converter				
IN0	I	Channel 0 oscillation input pin. This pin is used as the secondary function of the P30 pin.	Secondary	—
CS0	O	Channel 0 reference capacitor connection pin. This pin is used as the secondary function of the P31 pin.	Secondary	—
RS0	O	This pin is used as the secondary function of the P32 pin which is the reference resistor connection pin of Channel 0.	Secondary	—
RT0	O	Resistor sensor connection pin of Channel 0 for measurement. This pin is used as the secondary function of the P34 pin.	Secondary	—
CRT0	O	Resistor/capacitor sensor connection pin of Channel 0 for measurement. This pin is used as the secondary function of the P33 pin.	Secondary	—
RCM	O	RC oscillation monitor pin. This pin is used as the secondary function of the P35 pin.	Secondary	—
IN1	I	Oscillation input pin of Channel 1. This pin is used as the secondary function of the P44 pin.	Secondary	—
CS1	O	Reference capacitor connection pin of Channel 1. This pin is used as the secondary function of the P45 pin.	Secondary	—
RS1	O	Reference resistor connection pin of Channel 1. This pin is used as the secondary function of the P46 pin.	Secondary	—
RT1	O	Resistor sensor connection pin for measurement of Channel 1. This pin is used as the secondary function of the P47 pin.	Secondary	—
LCD drive signal				
COM0-7	O	Common output pins.	—	—
COM8-23	O	Common output pins. These pins are for the ML610Q428, but are not provided in the ML610Q429.	—	—
SEG0-57	O	Segment output pin.	—	—
SEG58-63	O	Segment output pins. These pins are for the ML610Q429, but are not provided in the ML610Q428.	—	—
LCD driver power supply				
V_{L1}	—	Power supply pins for LCD bias (internally generated). Capacitors Ca, Cb, Cc, and Cd (see measuring circuit 1) are connected between V_{SS} and V_{L1}, V_{L2}, V_{L3}, and V_{L4}, respectively.	—	—
V_{L2}	—		—	—
V_{L3}	—		—	—
V_{L4}	—		—	—
C1	—	Power supply pins for LCD bias (internally generated). Capacitors C12 and C34 (see measuring circuit 1) are connected between C1 and C2 and between C3 and C4, respectively.	—	—
C2	—		—	—
C3	—		—	—
C4	—		—	—
For testing				
TEST	I/O	Input/output pin for testing. A pull-down resistor is internally connected.	—	—
Power supply				
V_{SS}	—	Negative power supply pin.	—	—
V_{DD}	—	Positive power supply pin.	—	—
V_{DDL}	—	Positive power supply pin (internally generated) for internal logic. Capacitors CL0 and CL1 (see measuring circuit 1) are connected between this pin and V_{SS}.	—	—
V_{DDX}	—	Plus-side power supply pin (internally generated) for low-speed oscillation. Capacitor Cx (see measuring circuit 1) is connected between this pin and V_{SS}.	—	—
V_{PP}	—	Power supply pin for programming Flash ROM. A pull-up resistor is internally connected.	—	—

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

(V_{SS} = 0V)

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage 1	V_{DD}	Ta = 25°C	–0.3 to +4.6	V
Power supply voltage 2	V_{PP}	Ta = 25°C	–0.3 to +9.5	V
Power supply voltage 3	V_{DDL}	Ta = 25°C	–0.3 to +3.6	V
Power supply voltage 4	V_{DDX}	Ta = 25°C	–0.3 to +3.6	V
Power supply voltage 5	V_{L1}	Ta = 25°C	–0.3 to +1.75	V
Power supply voltage 6	V_{L2}	Ta = 25°C	–0.3 to +3.5	V
Power supply voltage 7	V_{L3}	Ta = 25°C	–0.3 to +5.25	V
Power supply voltage 8	V_{L4}	Ta = 25°C	–0.3 to +7.0	V
Input voltage	V_{IN}	Ta = 25°C	–0.3 to V_{DD}+0.3	V
Output voltage	V_{OUT}	Ta = 25°C	–0.3 to V_{DD}+0.3	V
Output current 1	I_{OUT1}	Port3–A, Ta = 25°C	–12 to +11	mA
Output current 2	I_{OUT2}	Port2, Ta = 25°C	–12 to +20	mA
Power dissipation	PD	Ta = 25°C	122	mW
Storage temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

(V_{SS} = 0V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature	T_{OP}	—	–20 to +70	°C
Operating voltage	V_{DD}	—	1.1 to 3.6	V
Operating frequency (CPU)	f_{OP}	V_{DD} = 1.1 to 3.6V	30k to 36k	Hz
		V_{DD} = 1.3 to 3.6V	30k to 650k	
		V_{DD} = 1.8 to 3.6V	30k to 4.2M	
Capacitor externally connected to V_{DDL} pin	C_{L0}	—	1.0±30%	µF
	C_{L1}	—	0.1±30%	
Capacitor externally connected to V_{DDX} pin	C_X	—	0.1±30%	µF
Capacitors externally connected to $V_{L1, 2, 3, 4}$ pins	$C_{a, b, c, d}$	—	1.0±30%	µF
Capacitors externally connected across C1 and C2 pins and across C3 and C4 pins	C_{12}, C_{34}	—	1.0±30%	µF

CLOCK GENERATION CIRCUIT OPERATING CONDITIONS

(V_{SS} = 0V)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Low-speed crystal oscillation frequency	f_{XTL}	—	—	32.768k	—	Hz
Recommended equivalent series resistance value of low-speed crystal oscillation	R_L	—	—	—	40k	Ω
Low-speed crystal oscillation external capacitor *1	C_{DL}/C_{GL}	C_L=6pF of crystal oscillation *2	—	0	—	pF
		C_L=9pF of crystal oscillation	—	6	—	
		C_L=12pF of crystal oscillation	—	12	—	
High-speed crystal/ceramic oscillation frequency	f_{XTH}	—	—	4.0M / 4.096M	—	Hz
High-speed crystal oscillation external capacitor	C_{DH}	—	—	24	—	pF
	C_{GH}	—	—	24	—	

*1: The external C_{DL} and C_{GL} need to be adjusted in consideration of variation of internal loading capacitance C_D and C_G, and other additional capacitance such as PCB layout.

*2: When using a crystal oscillator C_L = 6pF, there is a possibility that can not be adjusted by external C_{DL} and C_{GL}.

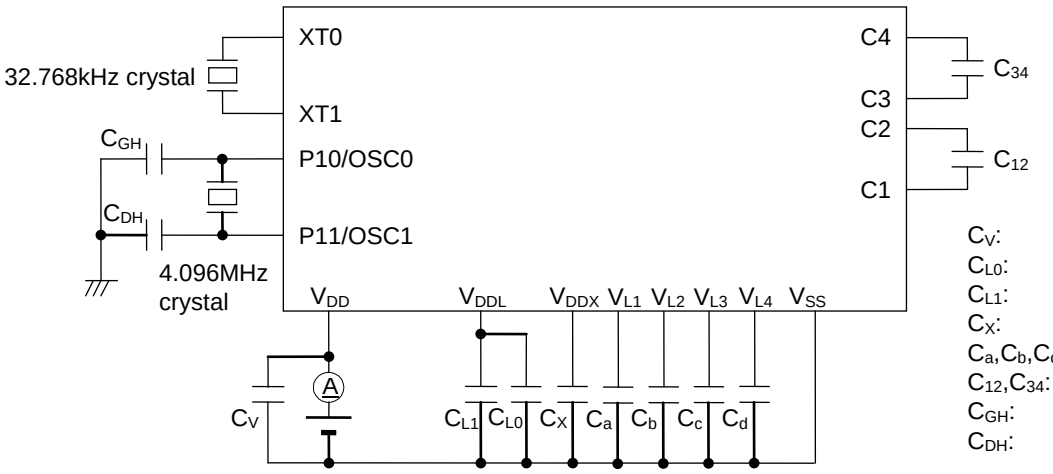
DC CHARACTERISTICS (4/5)

(V_{DD} = 1.1 to 3.6V, V_{SS} = 0V, Ta = –20 to +70°C, unless otherwise specified) (4/5)

Parameter	Symbol	Condition		Rating Min.	Rating Typ.	Rating Max.	Unit	Measuring circuit
Output voltage 1 (P20–P22/2nd function is selected) (P30–P36) (P40–P47) (PA0–PA5)*1	VOH1	IOH1 = –0.5mA, V_{DD} = 1.8 to 3.6V		V_{DD} –0.5	—	—	V	2
		IOH1 = -0.1mA, V_{DD} = 1.3 to 3.6V		V_{DD} –0.3	—	—		
		IOH1 = -0.03mA, V_{DD} = 1.1 to 3.6V		V_{DD} –0.3	—	—		
	VOL1	IOL1 = +0.5mA, V_{DD} = 1.8 to 3.6V		—	—	0.5		
		IOL1 = +0.1mA, V_{DD} = 1.3 to 3.6V		—	—	0.5		
		IOL1 = +0.03mA, V_{DD} = 1.1 to 3.6V		—	—	0.3		
Output voltage 2 (P20–P22/2nd function is Not selected)	VOH2	IOH1 = –0.5mA, V_{DD} = 1.8 to 3.6V		V_{DD} –0.5	—	—		
		IOH1 = -0.1mA, V_{DD} = 1.3 to 3.6V		V_{DD} –0.3	—	—		
		IOH1 = -0.03mA, V_{DD} = 1.1 to 3.6V		V_{DD} –0.3	—	—		
	VOL2	IOL2 = +5mA, V_{DD} = 1.8 to 3.6V		—	—	0.5		
Output voltage 3 (P40–P41)	VOL3	IOL3 = +3mA, V_{DD} = 2.0 to 3.6V (when I^2C mode is selected)		—	—	0.4		
Output voltage 4 (COM0–23) (SEG0–63)	VOH4	IOH4 = –0.2mA, VL1=1.2V		V_{L4} –0.2	—	—		
	VOMH4	IOMH4 = +0.2mA, VL1=1.2V		—	—	V_{L3} +0.2		
	VOMH4S	IOMH4S = –0.2mA, VL1=1.2V		V_{L3} –0.2	—	—		
	VOM4	IOM4 = +0.2mA, VL1=1.2V		—	—	V_{L2} +0.2		
	VOM4S	IOM4S = –0.2mA, VL1=1.2V		V_{L2} –0.2	—	—		
	VOML4	IOML4 = +0.2mA, VL1=1.2V		—	—	V_{L1} +0.2		
	VOML4S	IOML4S = –0.2mA, VL1=1.2V		V_{L1} –0.2	—	—		
	VOL4	IOL4 = +0.2mA, VL1=1.2V		—	—	0.2		
Output leakage (P20–P22) (P30–P35) (P40–P47) (PA0–PA5)*1	IOOH	VOH = V_{DD} (in high-impedance state)		—	—	1	μA	3
	IOOL	VOL = V_{SS} (in high-impedance state)		–1	—	—		
Input current 1 (RESET_N)	IIH1	VIH1 = V_{DD}		0	—	1	μA	4
	IIL1	VIL1 = V_{SS}	V_{DD} = 1.8 to 3.6V	–600	–300	–20		
			V_{DD} = 1.3 to 3.6V	–600	–300	-10		
			V_{DD} = 1.1 to 3.6V	–600	–300	-2		
Input current 1 (TEST)	IIH1	VIH1 = V_{DD}	V_{DD} = 1.8 to 3.6V	20	300	600		
			V_{DD} = 1.3 to 3.6V	10	300	600		
			V_{DD} = 1.1 to 3.6V	2	300	600		
	IIL1	VIL1 = V_{ss}		-1	—	—		
Input current 2 (NMI) (P00–P03) (P04–P07) *1 (P10–P11)	IIH2	VIH2 = V_{DD} (when pulled-down)	V_{DD} = 1.8 to 3.6V	2	30	200		
			V_{DD} = 1.3 to 3.6V	0.2	30	200		
			V_{DD} = 1.1 to 3.6V	0.01	30	200		
	IIL2	VIL2 = V_{SS} (when pulled-up)	V_{DD} = 1.8 to 3.6V	–200	–30	–2		
			V_{DD} = 1.3 to 3.6V	–200	–30	-0.2		

MEASURING CIRCUITS

MEASURING CIRCUIT 1

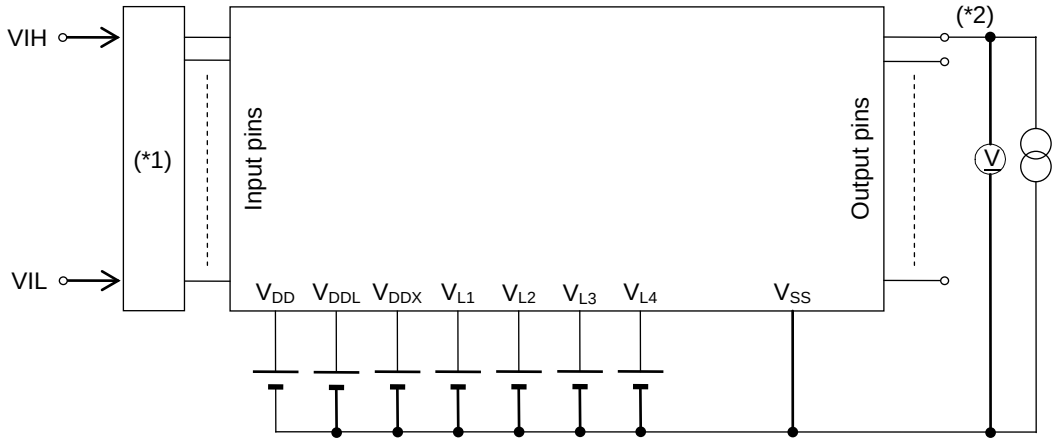


C_V:	1µF
C_{L0}:	1µF
C_{L1}:	0.1µF
C_X:	0.1µF
C_a,C_b,C_c,C_d:	1µF
C_{12},C_{34}:	1µF
C_{GH}:	24pF
C_{DH}:	24pF

32.768kHz crystal resonator
DT-26 (Load capacitance 6pF)
(Made by KDS:DAISHINKU CORP.)

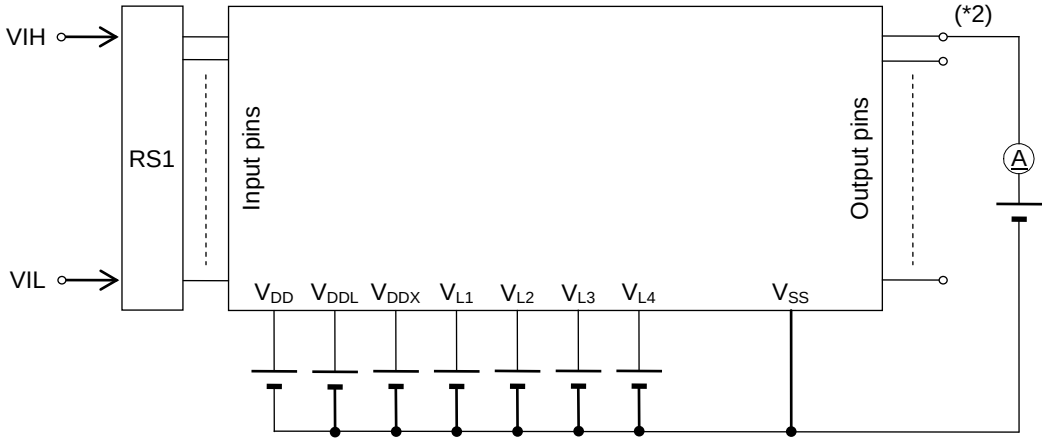
4.096MHz crystal:
HC49SFWB (Kyocera)

MEASURING CIRCUIT 2



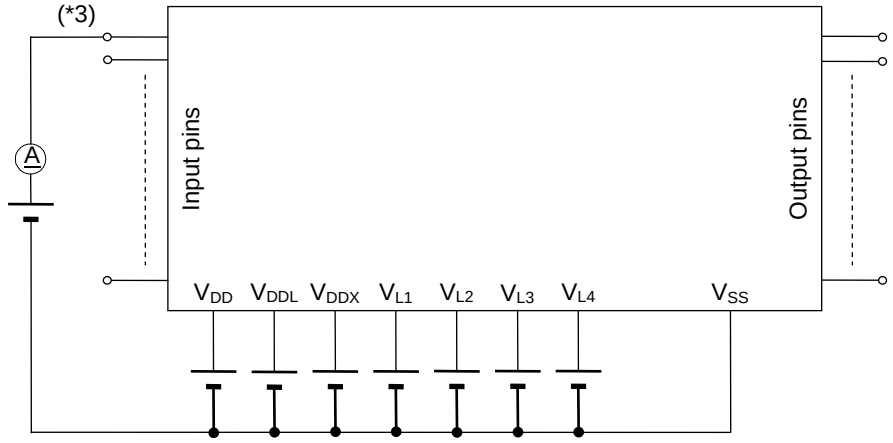
(*1) Input logic circuit to determine the specified measuring conditions.
(*2) Measured at the specified output pins.

MEASURING CIRCUIT 3



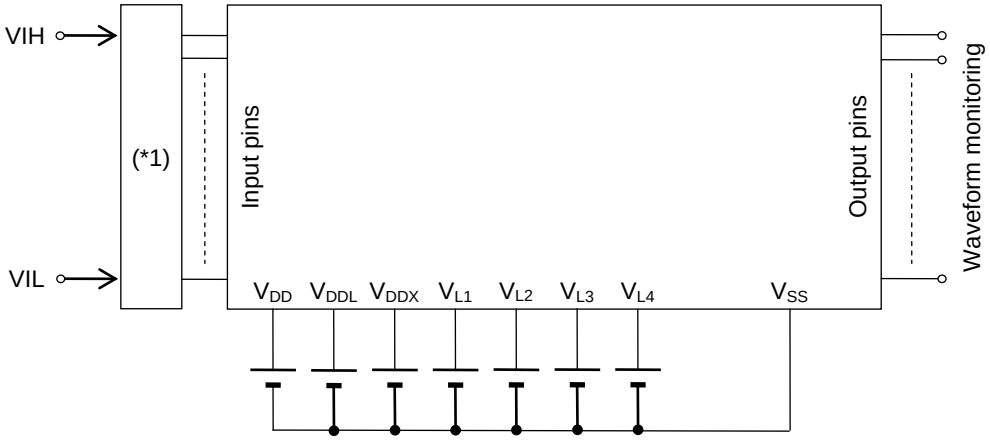
*1: Input logic circuit to determine the specified measuring conditions.
*2: Measured at the specified output pins.

MEASURING CIRCUIT 4



*3: Measured at the specified output pins.

MEASURING CIRCUIT 5

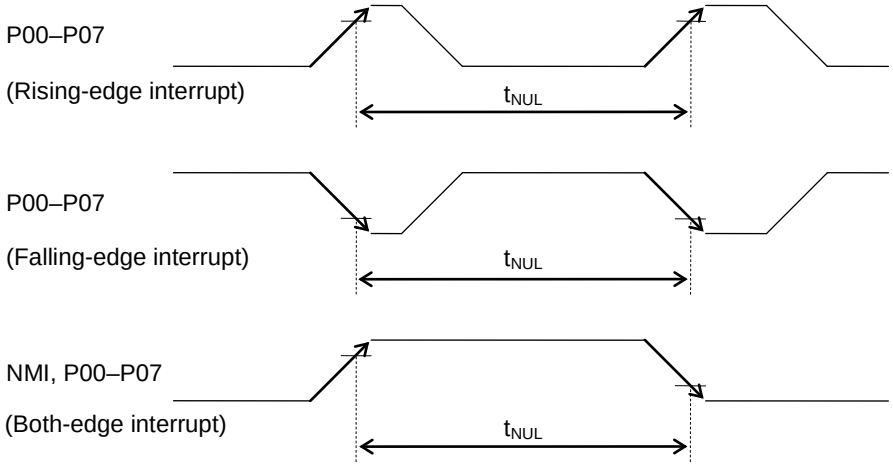


*1: Input logic circuit to determine the specified measuring conditions.

AC CHARACTERISTICS (External Interrupt)

(V_{DD} = 1.1 to 3.6V, V_{SS} = 0V, Ta = –20 to +70°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
External interrupt disable period	T_{NUL}	Interrupt: Enabled (MIE = 1), CPU: NOP operation System clock: 32.768kHz	76.8	—	106.8	μs

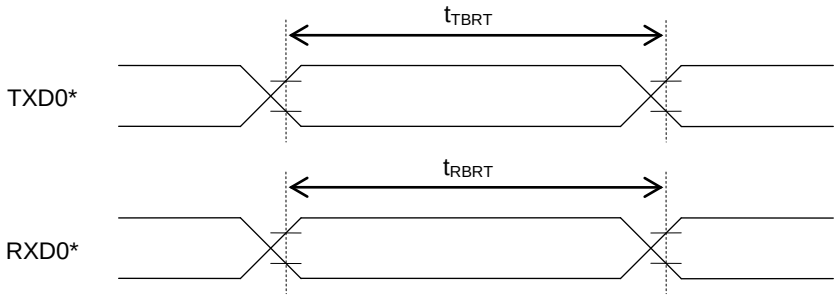


AC CHARACTERISTICS (UART)

(V_{DD} = 1.3 to 3.6V, V_{SS} = 0V, Ta = –20 to +70°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Transmit baud rate	t_{TBRT}	—	—	BRT*1	—	s
Receive baud rate	t_{RBRT}	—	BRT*1 –3%	BRT*1	BRT*1 +3%	s

*1: Baud rate period (including the error of the clock frequency selected) set with the UART baud rate register (UA0BRTL,H) and the UART mode register 0 (UA0MOD0).



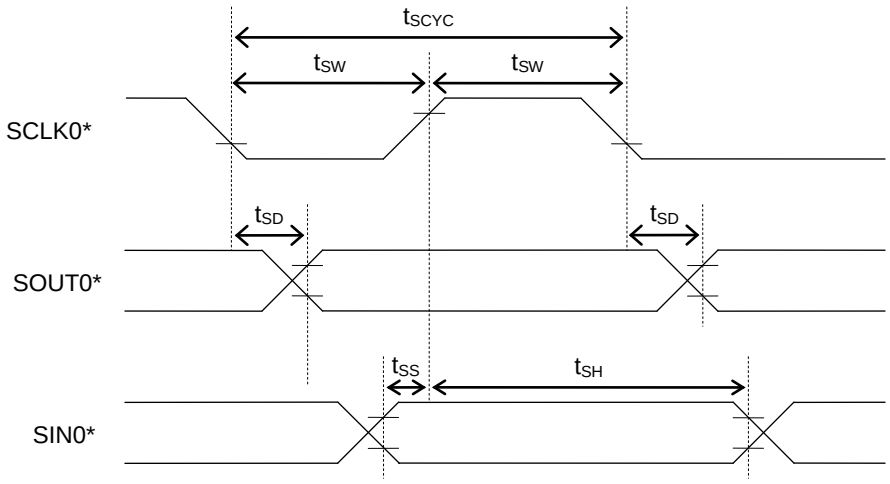
*: Indicates the secondary function of the port.

AC CHARACTERISTICS (Synchronous Serial Port)

(V_{DD} = 1.3 to 3.6V, V_{SS} = 0V, Ta = –20 to +70°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCLK input cycle (slave mode)	t_{SCYC}	When high-speed oscillation is not active	10	—	—	µs
		When high-speed oscillation is active (V_{DD} = 1.8 to 3.6V)	1	—	—	µs
SCLK output cycle (master mode)	t_{SCYC}	—	—	SCLK*1	—	s
SCLK input pulse width (slave mode)	t_{SW}	When high-speed oscillation is not active	4	—	—	µs
		When high-speed oscillation is active (V_{DD} = 1.8 to 3.6V)	0.4	—	—	µs
SCLK output pulse width (master mode)	t_{SW}	—	SCLK*1 ×0.4	SCLK*1 ×0.5	SCLK*1 ×0.6	s
SOUT output delay time (slave mode)	t_{SD}	—	—	—	180	ns
SOUT output delay time (master mode)	t_{SD}	—	—	—	80	ns
SIN input setup time (slave mode)	t_{SS}	—	80	—	—	ns
SIN input setup time (master mode)	t_{SS}	—	180	—	—	ns
SIN input hold time	t_{SH}	—	80	—	—	ns

*1: Clock period selected with S0CK3–0 of the serial port 0 mode register (SIO0MOD1)



*: Indicates the secondary function of the port.

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEDL610Q428-01	Feb.7.2011	–	–	Formally edition 1.0
FEDL610Q428-02	Jun 7.2011	3	3	Add the P version
FEDL610Q428-03	July.25.2014	All	All	Change header and footer
		3,18,19, 20,21,22, 23,26,27, 28,29	3,18,20, 21,22,23, 24,27,28, 29,30	Delete the P version
		3,7	4	Delete package products
		2,7	2	Delete the metal option of only ML610Q429's LCD driver
		3	4	Change from "Shipment" to " Product name – Supported Function "
		-	19	Add CLOCK GENERATION CIRCUIT OPERATING CONDITIONS
		19	20	Change "RESET" to "Reset pulse width (P_{RST})" and " Power-on reset activation power rise time (T_{POR})".
		21	22	Correct the C_{GL}'s value and the C_{DL}'s value of DC CHARACTERISTICS (3/5)'s note No.3
		30	31	Update Package Dimensions
FEDL610Q428-04	May.15,2015	2	2	Corrected a typo. "100kbps@1MHz HSCLK" is corrected to 100kbps@4MHz HSCLK.
		-	4,8	Add the ML610Q429 package product

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