# Rohm Semiconductor - ML610Q429-NNNTBZ03A7 Datasheet

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | nX-U8/100 |
| Core Size | 8-Bit |
| Speed | 4.2MHz |
| Connectivity | I²C, SSP, UART/USART |
| Peripherals | LCD, Melody Driver, POR, PWM, WDT |
| Number of I/O | 20 |
| Program Memory Size | 48KB (24K x 16) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 4K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.1V ~ 3.6V |
| Data Converters | A/D 2x12b, 2x24b |
| Oscillator Type | Internal |
| Operating Temperature | -20°C ~ 70°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 128-TQFP |
| Supplier Device Package | - |
| Purchase URL | https://www.e-xfl.com/product-detail/rohm-semi/ml610q429-nnntbz03a7 |

- PWM
  - Resolution 16 bits × 3 channel

- Synchronous serial port
  - Master/slave selectable
  - LSB first/MSB first selectable
  - 8-bit length/16-bit length selectable
  - Timer interrupt is used as a serial clock and selection is possible

- UART
  - TXD/RXD × 1 channel
  - Bit length, parity/no parity, odd parity/even parity, 1 stop bit/2 stop bits
  - Positive logic/negative logic selectable
  - Built-in baud rate generator

- $I^2C$ bus interface
  - Master function only
  - Fast mode (400 kbps@4MHz), standard mode (100 kbps@4MHz, 50kbps@500kHz)

- Melody driver
  - Scale: 29 types (Melody sound frequency: 508 Hz to 32.768 kHz)
  - Tone length: 63 types
  - Tempo: 15 types
  - Buzzer output mode (4 output modes, 8 frequencies, 16 duty levels)

- RC oscillation type A/D converter
  - 24-bit counter
  - Time division × 2 channels

- Successive approximation type A/D converter
  - 12-bit A/D converter
  - Input × 2 channels

- General-purpose ports
  - Non-maskable interrupt input port × 1 channel
  - Input-only port × 10 channels (including secondary functions)
  - Output-only port × 3 channels (including secondary functions)
  - Input/output port
    ML610Q428: 14 channels (including secondary functions)
    ML610Q429: 20 channels (including secondary functions)

- LCD driver
  - Dot matrix can be supported.
    ML610Q428: 1392 dots max. (58 seg × 24 com), 1/1 to 1/24 duty
    ML610Q429: 512 dots max. (64 seg × 8 com) , 1/1 to 1/8 duty
  - 1/3 or 1/4 bias (built-in bias generation circuit)
  - Frame frequency selecable (approx. 32Hz, 64 Hz, 73 Hz, 85 Hz, and 102 Hz)
  - Bias voltage multiplying clock selectable (8 types)
  - Contrast adjustment (1/3 bias: 32 steps, 1/4 bias: 20 steps)
  - LCD drive stop mode, LCD display mode, all LCDs on mode, and all LCDs off mode selectable
  - Programmable display allocation function (available only when 1/1~1/8 duty is selected)

- Reset
  - Reset through the RESET_N pin
  - Power-on reset generation when powered on
  - Reset when oscillation stop of the low-speed clock is detected
  - Reset by the watchdog timer (WDT) overflow

- Power supply voltage detect function
  - Judgment voltages: One of 16 levels
  - Judgment accuracy: ±2% (Typ.)

- Clock
  - Low-speed clock: (This LSI can not guarantee the operation withoug low-speed clock)
    Crystal oscillation (32.768 kHz)
  - High-speed clock:
    Built-in RC oscillation (2M/500kHz)
    Built-in PLL oscillation (8.192 MHz ±2.5%), crystal/ceramic oscillation (4.096 MHz), external clock
  - Selection of high-speed clock mode by software:
    Built-in RC oscillation, built-in PLL oscillation, crystal/ceramic oscillation, external clock

- Power management
  - HALT mode: Instruction execution by CPU is suspended (peripheral circuits are in operating states).
  - STOP mode: Stop of low-speed oscillation and high-speed oscillation (Operations of CPU and peripheral circuits are stopped.)
  - Clock gear: The frequency of high-speed system clock can be changed by software (1/1, 1/2, 1/4, or 1/8 of the oscillation clock)
  - Block Control Function: Power down (reset registers and stop clock supply) the circuits of unused peripherals.

- Guaranteed operating range
  - Operating temperature: –20°C to 70°C
  - Operating voltage: $V_{DD}$ = 1.1V to 3.6V

## BLOCK DIAGRAM

### ML610Q428 Block Diagram

Figure 1 show the block diagram of the ML610Q428.
"*" indicates the secondary function of each port.

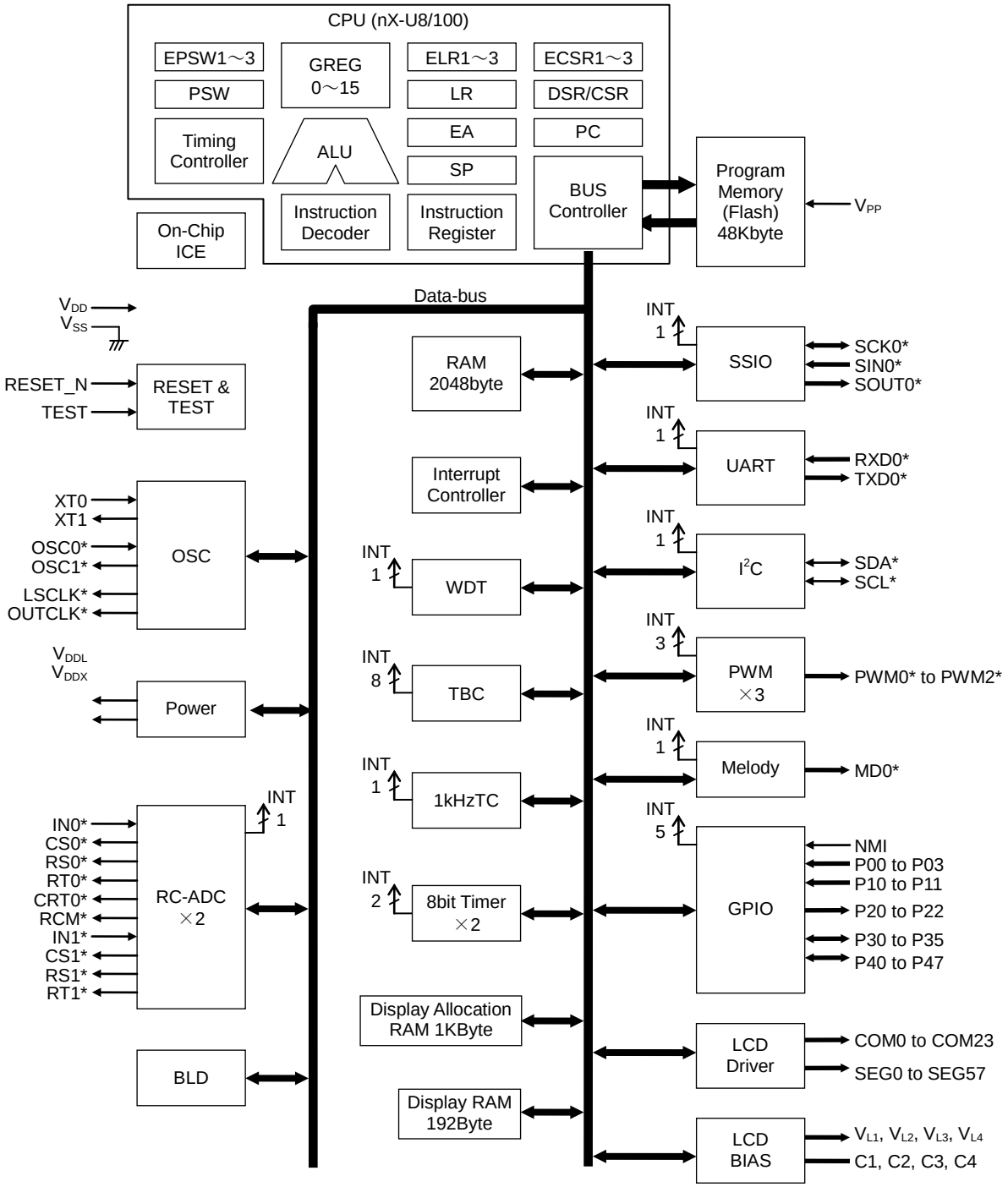



**Figure 1 ML610Q428 Block Diagram**

### ML610Q429 Block Diagram

Figure 2 show the block diagram of the ML610Q429.
"*" indicates the secondary function of each port.

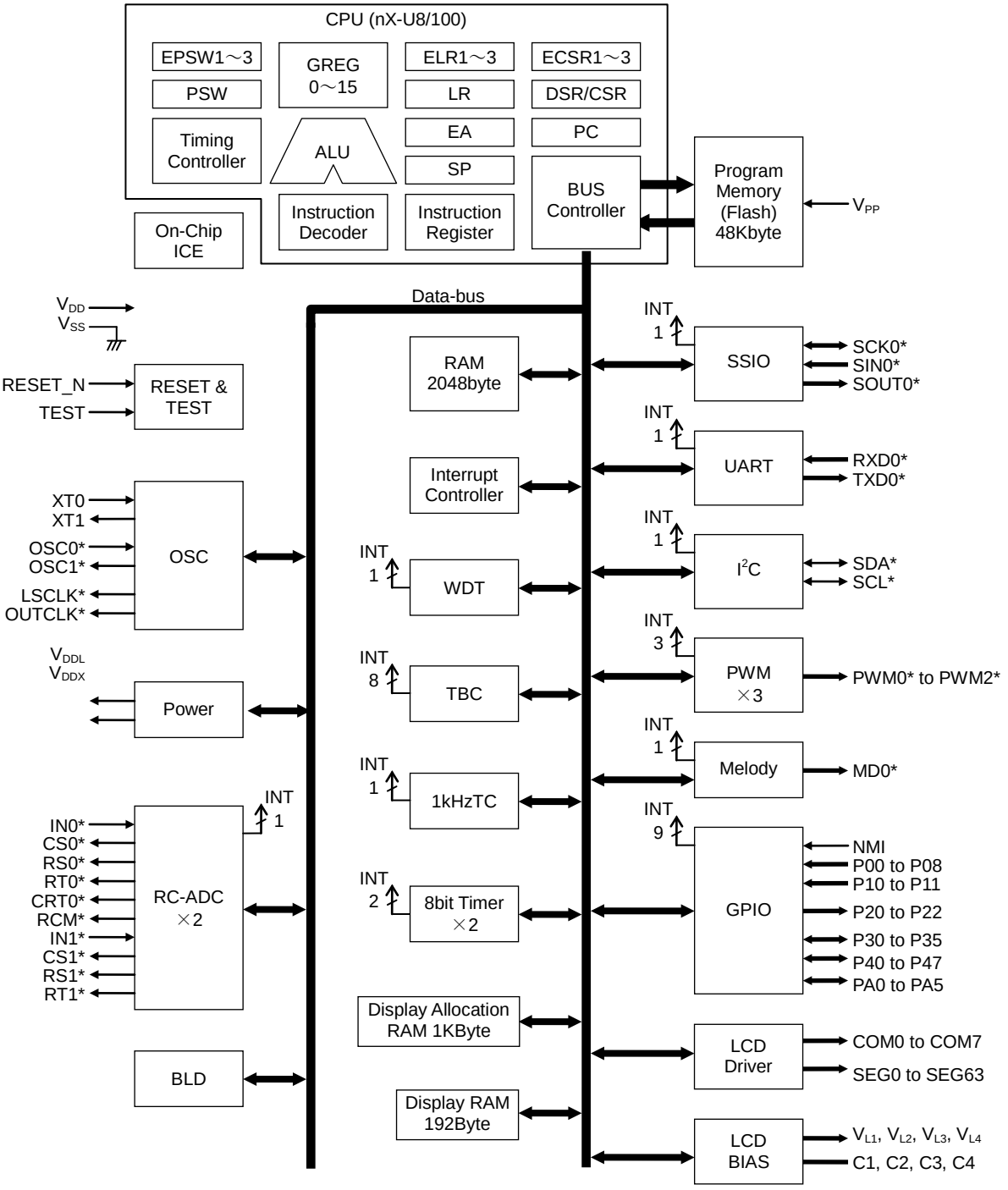
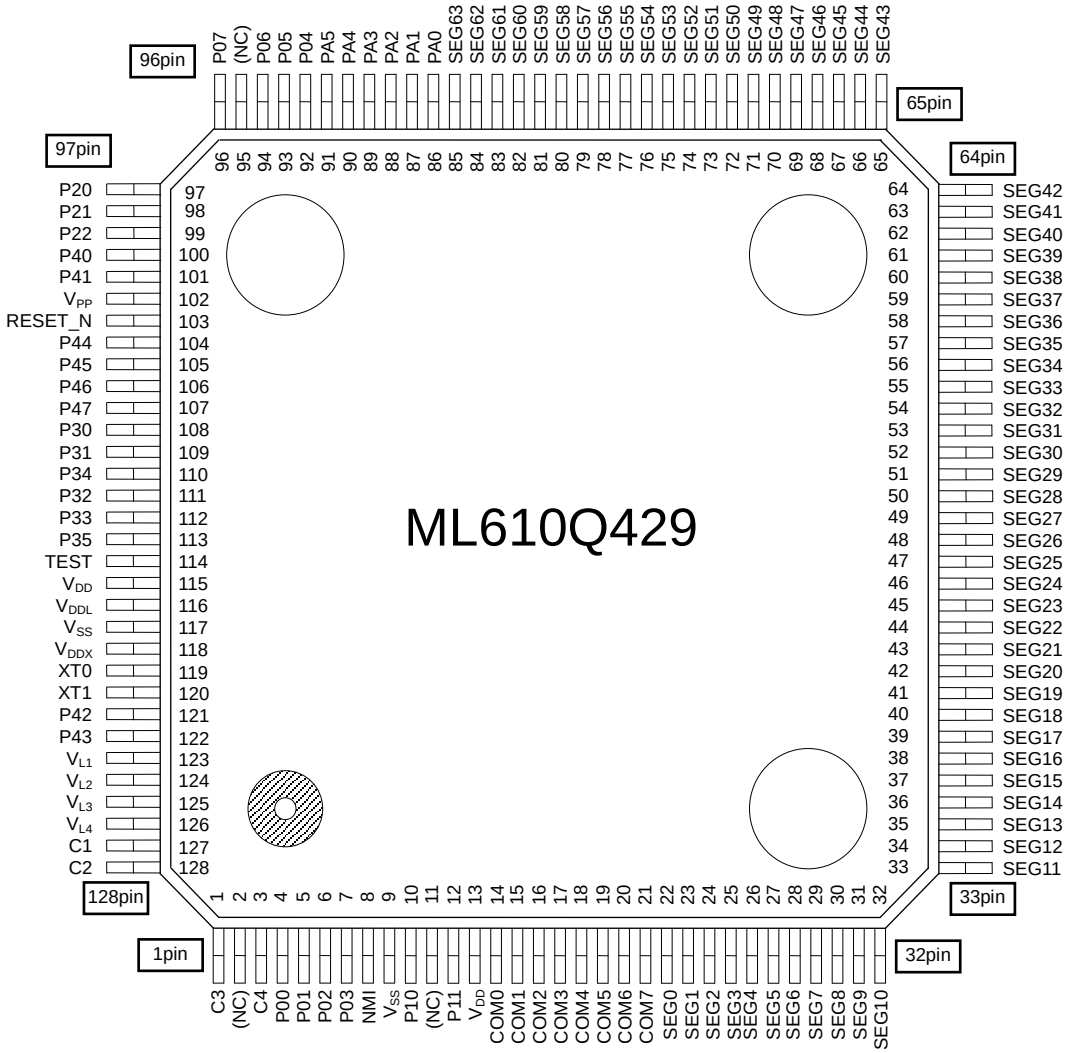



**Figure 2 ML610Q429 Block Diagram**

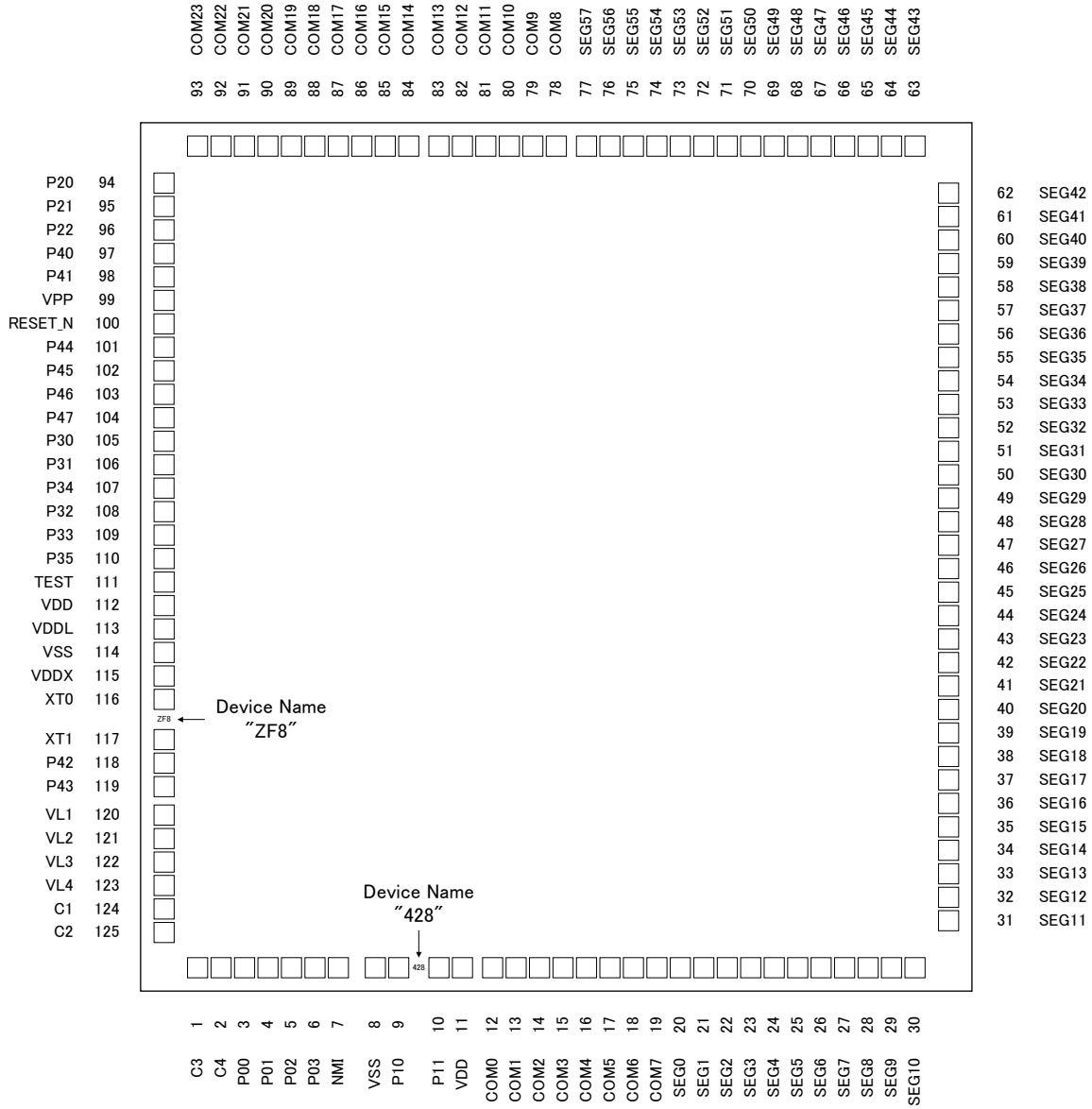
**ML610Q429 TQFP128 Pin Layout**




(NC): No Connection

**Figure 4 ML610Q429 TQFP128 Pin Configuration**

**ML610Q428 Chip Dimension**




| | |
|---|---|
| Chip size: | 2.99 mm × 3.11 mm |
| PAD count: | 125 pins |
| Minimum PAD pitch: | 80 μm |
| PAD aperture: | 70 μm × 70 μm |
| Chip thickness: | 350 μm |
| Voltage of the rear side of chip: | $V_{SS}$ level |

**Figure 5 ML610Q428 Chip Dimension**

Note:
Figure 5 is an image figure of the order of PAD, and it differs from an actual image. Refer to the PAD coordinate for detailed arrangement.
A chip angle can be checked by the distinguishing mark of three figures.

## PIN LIST

| PAD No. | | Primary function | | | Secondary function | | | Tertiary function | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Q429 | Q428 | Pin name | I/O | Function | Pin name | I/O | Function | Pin name | I/O | Function |
| 8,114 | 8,114 | Vss | — | Negative power supply pin | — | — | — | — | — | — |
| 11,112 | 11,112 | $V_{DD}$ | — | Positive power supply pin | — | — | — | — | — | — |
| 113 | 113 | $V_{DDL}$ | — | Power supply pin for internal logic (internally generated) | — | — | — | — | — | — |
| 115 | 115 | $V_{DDX}$ | — | Power supply pin for low-speed oscillation (internally generated) | — | — | — | — | — | — |
| 99 | 99 | $V_{PP}$ | — | Power supply pin for Flash ROM | — | — | — | — | — | — |
| 120 | 120 | $V_{L1}$ | — | Power supply pin for LCD bias (internally generated) | — | — | — | — | — | — |
| 121 | 121 | $V_{L2}$ | — | Power supply pin for LCD bias (internally generated) | — | — | — | — | — | — |
| 122 | 122 | $V_{L3}$ | — | Power supply pin for LCD bias (internally generated) | — | — | — | — | — | — |
| 123 | 123 | $V_{L4}$ | — | Power supply pin for LCD bias (internally generated) | — | — | — | — | — | — |
| 124 | 124 | C1 | — | Capacitor connection pin for LCD bias generation | — | — | — | — | — | — |
| 125 | 125 | C2 | — | Capacitor connection pin for LCD bias generation | — | — | — | — | — | — |
| 1 | 1 | C3 | — | Capacitor connection pin for LCD bias generation | — | — | — | — | — | — |
| 2 | 2 | C4 | — | Capacitor connection pin for LCD bias generation | — | — | — | — | — | — |
| 111 | 111 | TEST | I/O | Input/output pin for testing | — | — | — | — | — | — |
| 100 | 100 | RESET_N | I | Reset input pin | — | — | — | — | — | — |
| 116 | 116 | XT0 | I | Low-speed clock oscillation pin | — | — | — | — | — | — |
| 117 | 117 | XT1 | O | Low-speed clock oscillation pin | — | — | — | — | — | — |
| 7 | 7 | NMI | I | Non-maskable interrupt pin | — | — | — | — | — | — |
| 3 | 3 | P00/EXI0 | I | Input port, External interrupt 0 input | — | — | — | — | — | — |
| 4 | 4 | P01/EXI1 | I | Input port, External interrupt 1 input | — | — | — | — | — | — |
| 5 | 5 | P02/EXI2 /RXD0 /P2CK | I | Input port, External interrupt 2, UART0 receive, PWM2 external clock input | — | — | — | — | — | — |
| 6 | 6 | P03/EXI3 | I | Input port, External interrupt 3 | — | — | — | — | — | — |
| 90 | — | P04/EXI4 | I/O | Input port, External interrupt 4 | — | — | — | — | — | — |
| 91 | — | P05/EXI5 | I/O | Input port, External interrupt 5 | — | — | — | — | — | — |
| 92 | — | P06/EXI6 | I/O | Input port, External interrupt 6 | — | — | — | — | — | — |
| 93 | — | P07/EXI7 | I/O | Input port, External | — | — | — | — | — | — |

| PAD No. | | Primary function | | | Secondary function | | | Tertiary function | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Q429 | Q428 | Pin name | I/O | Function | Pin name | I/O | Function | Pin name | I/O | Function |
| | | | | interrupt 7 | | | | | | |
| 9 | 9 | P10 | I | Input port | OSC0 | I | High-speed oscillation | — | — | — |
| 10 | 10 | P11 | I | Input port | OSC1 | O | High-speed oscillation | — | — | — |
| 94 | 94 | P20/LED0 | O | Output port | LSCLK | O | Low-speed clock output | PWM2 | O | PWM2 output |
| 95 | 95 | P21/LED1 | O | Output port | OUTCLK | O | High-speed clock output | — | — | — |
| 96 | 96 | P22/LED2 | O | Output port | MD0 | O | Melody output | — | — | — |
| 105 | 105 | P30 | I/O | Input/output port | IN0 | I | RC type ADC0 oscillation input pin | PWM2 | O | PWM2 output |
| 106 | 106 | P31 | I/O | Input/output port | CS0 | O | RC type ADC0 reference capacitor connection pin | — | — | — |
| 108 | 108 | P32 | I/O | Input/output port | RS0 | O | RC type ADC0 reference resistor connection pin | — | — | — |
| 109 | 109 | P33 | I/O | Input/output port | RT0 | O | RC type ADC0 resistor sensor connection pin | — | — | — |
| 107 | 107 | P34 | I/O | Input/output port | RCT0 | O | RC type ADC0 resistor/capacitor sensor connection pin | PWM0 | O | PWM0 output |
| 110 | 110 | P35 | I/O | Input/output port | RCM | O | RC type ADC oscillation monitor | PWM1 | O | PWM1 output |
| 97 | 97 | P40 | I/O | Input/output port | SDA | I/O | $I^2C$ data input/output | SIN0 | I | SSIO data input |
| 98 | 98 | P41 | I/O | Input/output port | SCL | I/O | $I^2C$ clock input/output | SCK0 | I/O | SSIO synchronous clock |
| 118 | 118 | P42 | I/O | Input/output port | RXD0 | I | UART data input | SOUT0 | O | SSIO data output |
| 119 | 119 | P43 | I/O | Input/output port | TXD0 | O | UART data output | PWM0 | O | PWM0 output |
| 101 | 101 | P44/T02P0CK | I/O | Input/output port, Timer 0/Timer 2/PWM0 external clock input | IN1 | I | RC type ADC1 oscillation input pin | SIN0 | I | SSIO0 data input |
| 102 | 102 | P45/T13P1CK | I/O | Input/output port, Timer 1/Timer 3/PWM1 external clock input | CS1 | O | RC type ADC1 reference capacitor connection pin | SCK0 | I/O | SSIO0 synchronous clock |
| 103 | 103 | P46/T46P2CK | I/O | Input/output port, PWM2 external clock input | RS1 | O | RC type ADC1 reference resistor connection pin | SOUT0 | O | SSIO0 data output |
| 104 | 1004 | P47 | I/O | Input/output port | RT1 | O | RC type ADC1 resistor sensor connection pin | PWM1 | O | PWM1 output |
| 84 | — | PA0 | I/O | Input/output port | — | — | — | — | — | — |
| 85 | — | PA1 | I/O | Input/output port | — | — | — | — | — | — |
| 86 | — | PA2 | I/O | Input/output port | — | — | — | — | — | — |
| 87 | — | PA3 | I/O | Input/output port | — | — | — | — | — | — |
| 88 | — | PA4 | I/O | Input/output port | — | — | — | — | — | — |
| 89 | — | PA5 | I/O | Input/output port | — | — | — | — | — | — |
| 12 | 12 | COM0 | O | LCD common pin | — | — | — | — | — | — |
| 13 | 13 | COM1 | O | LCD common pin | — | — | — | — | — | — |
| 14 | 14 | COM2 | O | LCD common pin | — | — | — | — | — | — |
| 15 | 15 | COM3 | O | LCD common pin | — | — | — | — | — | — |
| 16 | 16 | COM4 | O | LCD common pin | — | — | — | — | — | — |
| 17 | 17 | COM5 | O | LCD common pin | — | — | — | — | — | — |
| 18 | 18 | COM6 | O | LCD common pin | — | — | — | — | — | — |
| 19 | 19 | COM7 | O | LCD common pin | — | — | — | — | — | — |
| — | 78 | COM8 | O | LCD common pin | — | — | — | — | — | — |
| — | 79 | COM9 | O | LCD common pin | — | — | — | — | — | — |
| — | 80 | COM10 | O | LCD common pin | — | — | — | — | — | — |
| — | 81 | COM11 | O | LCD common pin | — | — | — | — | — | — |
| — | 82 | COM12 | O | LCD common pin | — | — | — | — | — | — |
| — | 83 | COM13 | O | LCD common pin | — | — | — | — | — | — |
| — | 84 | COM14 | O | LCD common pin | — | — | — | — | — | — |
| — | 85 | COM15 | O | LCD common pin | — | — | — | — | — | — |

| PAD No. | | Primary function | | | Secondary function | | | Tertiary function | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Q429 | Q428 | Pin name | I/O | Function | Pin name | I/O | Function | Pin name | I/O | Function |
| 65 | 65 | SEG45 | O | LCD segment pin | — | — | — | — | — | — |
| 66 | 66 | SEG46 | O | LCD segment pin | — | — | — | — | — | — |
| 67 | 67 | SEG47 | O | LCD segment pin | — | — | — | — | — | — |
| 68 | 68 | SEG48 | O | LCD segment pin | — | — | — | — | — | — |
| 69 | 69 | SEG49 | O | LCD segment pin | — | — | — | — | — | — |
| 70 | 70 | SEG50 | O | LCD segment pin | — | — | — | — | — | — |
| 71 | 71 | SEG51 | O | LCD segment pin | — | — | — | — | — | — |
| 72 | 72 | SEG52 | O | LCD segment pin | — | — | — | — | — | — |
| 73 | 73 | SEG53 | O | LCD segment pin | — | — | — | — | — | — |
| 74 | 74 | SEG54 | O | LCD segment pin | — | — | — | — | — | — |
| 75 | 75 | SEG55 | O | LCD segment pin | — | — | — | — | — | — |
| 76 | 76 | SEG56 | O | LCD segment pin | — | — | — | — | — | — |
| 77 | 77 | SEG57 | O | LCD segment pin | — | — | — | — | — | — |
| 78 | — | SEG58 | O | LCD segment pin | — | — | — | — | — | — |
| 79 | — | SEG59 | O | LCD segment pin | — | — | — | — | — | — |
| 80 | — | SEG60 | O | LCD segment pin | — | — | — | — | — | — |
| 81 | — | SEG61 | O | LCD segment pin | — | — | — | — | — | — |
| 82 | — | SEG62 | O | LCD segment pin | — | — | — | — | — | — |
| 83 | — | SEG63 | O | LCD segment pin | — | — | — | — | — | — |

## TERMINATION OF UNUSED PINS

Table 3 shows methods of terminating the unused pins.

**Table 3 Termination of Unused Pins**

| Pin | Recommended pin termination |
|---|---|
| $V_{PP}$ | Open |
| $V_{L1}$, $V_{L2}$, $V_{L3}$, $V_{L4}$ | Open |
| C1, C2, C3, C4 | Open |
| RESET_N | Open |
| TEST | Open |
| NMI | Open |
| P00 to P07 | $V_{DD}$ or $V_{SS}$ |
| P10 to P11 | $V_{DD}$ |
| P20 to P22 | Open |
| P30 to P35 | Open |
| P40 to P47 | Open |
| PA0 to PA5 | Open |
| COM0 to 23 | Open |
| SEG0 to 63 | Open |

Note:
It is recommended to set the unused input ports and input/output ports to the inputs with pull-down resistors/pull-up resistors or the output mode since the supply current may become excessively large if the pins are left open in the high impedance input setting.

The main difference points of ML610Q428 and ML610Q429

**Table 4 The main difference points of ML610Q428 and ML610Q429.**

| Function | ML610Q428 | ML610Q429 |
|---|---|---|
| PORT0 | P03 to P00 | P07 to P00 |
| PORTA | Nothing | PA5 to PA0 |
| LCD COM | COM23 to COM0 | COM7 to COM0 |
| LCD SEG | SEG57 to SEG0 | SEG63 to SEG0 |

## ELECTRICAL CHARACTERISTICS

### ABSOLUTE MAXIMUM RATINGS

($V_{SS}$ = 0V)

| Parameter | Symbol | Condition | Rating | Unit |
|---|---|---|---|---|
| Power supply voltage 1 | $V_{DD}$ | Ta = 25°C | –0.3 to +4.6 | V |
| Power supply voltage 2 | $V_{PP}$ | Ta = 25°C | –0.3 to +9.5 | V |
| Power supply voltage 3 | $V_{DDL}$ | Ta = 25°C | –0.3 to +3.6 | V |
| Power supply voltage 4 | $V_{DDX}$ | Ta = 25°C | –0.3 to +3.6 | V |
| Power supply voltage 5 | $V_{L1}$ | Ta = 25°C | –0.3 to +1.75 | V |
| Power supply voltage 6 | $V_{L2}$ | Ta = 25°C | –0.3 to +3.5 | V |
| Power supply voltage 7 | $V_{L3}$ | Ta = 25°C | –0.3 to +5.25 | V |
| Power supply voltage 8 | $V_{L4}$ | Ta = 25°C | –0.3 to +7.0 | V |
| Input voltage | $V_{IN}$ | Ta = 25°C | –0.3 to $V_{DD}$+0.3 | V |
| Output voltage | $V_{OUT}$ | Ta = 25°C | –0.3 to $V_{DD}$+0.3 | V |
| Output current 1 | $I_{OUT1}$ | Port3–A, Ta = 25°C | –12 to +11 | mA |
| Output current 2 | $I_{OUT2}$ | Port2, Ta = 25°C | –12 to +20 | mA |
| Power dissipation | PD | Ta = 25°C | 122 | mW |
| Storage temperature | $T_{STG}$ | — | –55 to +150 | °C |

### RECOMMENDED OPERATING CONDITIONS

($V_{SS}$ = 0V)

| Parameter | Symbol | Condition | Range | Unit |
|---|---|---|---|---|
| Operating temperature | $T_{OP}$ | — | –20 to +70 | °C |
| Operating voltage | $V_{DD}$ | — | 1.1 to 3.6 | V |
| Operating frequency (CPU) | $f_{OP}$ | $V_{DD}$ = 1.1 to 3.6V | 30k to 36k | Hz |
| | | $V_{DD}$ = 1.3 to 3.6V | 30k to 650k | |
| | | $V_{DD}$ = 1.8 to 3.6V | 30k to 4.2M | |
| Capacitor externally connected to $V_{DDL}$ pin | $C_{L0}$ | — | 1.0±30% | µF |
| | $C_{L1}$ | — | 0.1±30% | |
| Capacitor externally connected to $V_{DDX}$ pin | $C_X$ | — | 0.1±30% | µF |
| Capacitors externally connected to $V_{L1, 2, 3, 4}$ pins | $C_{a, b, c, d}$ | — | 1.0±30% | µF |
| Capacitors externally connected across C1 and C2 pins and across C3 and C4 pins | $C_{12}$, $C_{34}$ | — | 1.0±30% | µF |

## OPERATING CONDITIONS OF FLASH ROM

($V_{SS}$ = 0V)

| Parameter | Symbol | Condition | Range | Unit |
|---|---|---|---|---|
| Operating temperature | $T_{OP}$ | At write/erase | 0 to +40 | °C |
| Operating voltage | $V_{DD}$ | At write/erase*1 | 2.75 to 3.6 | V |
| | $V_{DDL}$ | At write/erase*1 | 2.5 to 2.75 | |
| | $V_{PP}$ | At write/erase*1 | 7.7 to 8.3 | |
| Write cycles | $C_{EP}$ | — | 80 | cycles |
| Data retention | $Y_{DR}$ | — | 10 | years |

*1: In addition the power supply to VDD pin and VPP pin, within the range 2.5V to 2.75V has to be supplied to VDDL pin when programming and eraseing Flash ROM.

## DC CHARACTERISTICS (1/5)

($V_{DD}$ = 1.1 to 3.6V, $V_{SS}$ = 0V, Ta = −20 to +70°C, unless otherwise specified) (1/5)

| Parameter | Symbol | Condition | | Rating Min. | Rating Typ. | Rating Max. | Unit | Measuring circuit |
|---|---|---|---|---|---|---|---|---|
| 500kHz RC oscillation frequency | $f_{RC}$ | $V_{DD}$ = 1.3 to 3.6V | Ta = 25°C | Typ. −10% | 500 | Typ. +10% | kHz | 1 |
| | | | Ta = −20 to +70°C | Typ. −25% | 500 | Typ. +25% | kHz | |
| PLL oscillation frequency*4 | $f_{PLL}$ | LSCLK = 32.768kHz $V_{DD}$ = 1.8 to 3.6V | | -2.5% | 8.192 | +2.5% | MHz | |
| Low-speed crystal oscillation start time*2 | $T_{XTL}$ | — | | — | 0.3 | 2 | s | |
| 500kHz RC oscillation start time | $T_{RC}$ | — | | — | 50 | 500 | µs | |
| High-speed crystal oscillation start time*3 | $T_{XTH}$ | $V_{DD}$ = 1.8 to 3.6V | | — | 2 | 20 | ms | |
| PLL oscillation start time | $T_{PLL}$ | $V_{DD}$ = 1.8 to 3.6V | | — | 1 | 10 | | |
| Low-speed oscillation stop detect time*1 | $T_{STOP}$ | — | | 0.2 | 3 | 20 | | |
| Reset pulse width | $P_{RST}$ | — | | 200 | — | — | µs | |
| Reset noise elimination pulse width | $P_{NRST}$ | — | | — | — | 0.3 | | |
| Power-on reset activation power rise time | $T_{POR}$ | — | | — | — | 10 | ms | |

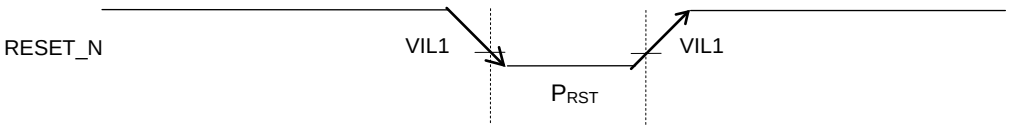
*1: When low-speed crystal oscillation stops for a duration more than the low-speed oscillation stop detect time, the system is reset to shift to system reset mode.

*2 : Use 32.768kHz crystal resonator DT-26 (Load capacitance 6pF) (made by KDS:DAISHINKU CORP.) is used ($C_{GL}$=$C_{DL}$=12pF).

*3 : Use 4.096MHz Crystal Oscillator CHC49SFWB (Kyocera).

*4: 1024 clock average.

[Reset pulse width]




**Reset pulse width ($P_{RST}$)**

[Power-on reset activation power rise time]


**Power-on reset activation power rise time ($T_{POR}$)**

**DC CHARACTERISTICS (2/5)**

($V_{DD}$ = 1.1 to 3.6V, $V_{SS}$ = 0V, Ta = −20 to +70°C, unless otherwise specified) (2/5)

| Parameter | Symbol | Condition | | Rating Min. | Rating Typ. | Rating Max. | Unit | Measuring circuit |
|---|---|---|---|---|---|---|---|---|
| $V_{L1}$ voltage | $V_{L1}$ | $V_{DD}$ = 3.0V, Tj = 25°C | CN4–0 = 00H | 0.89 | 0.94 | 0.99 | V | 1 |
| | | | CN4–0 = 01H | 0.91 | 0.96 | 1.01 | | |
| | | | CN4–0 = 02H | 0.93 | 0.98 | 1.03 | | |
| | | | CN4–0 = 03H | 0.95 | 1.00 | 1.05 | | |
| | | | CN4–0 = 04H | 0.97 | 1.02 | 1.07 | | |
| | | | CN4–0 = 05H | 0.99 | 1.04 | 1.09 | | |
| | | | CN4–0 = 06H | 1.01 | 1.06 | 1.11 | | |
| | | | CN4–0 = 07H | 1.03 | 1.08 | 1.13 | | |
| | | | CN4–0 = 08H | 1.05 | 1.10 | 1.15 | | |
| | | | CN4–0 = 09H | 1.07 | 1.12 | 1.17 | | |
| | | | CN4–0 = 0AH | 1.09 | 1.14 | 1.19 | | |
| | | | CN4–0 = 0BH | 1.11 | 1.16 | 1.21 | | |
| | | | CN4–0 = 0CH | 1.13 | 1.18 | 1.23 | | |
| | | | CN4–0 = 0DH | 1.15 | 1.20 | 1.25 | | |
| | | | CN4–0 = 0EH | 1.17 | 1.22 | 1.27 | | |
| | | | CN4–0 = 0FH | 1.19 | 1.24 | 1.29 | | |
| | | | CN4–0 = 10H | 1.21 | 1.26 | 1.31 | | |
| | | | CN4–0 = 11H | 1.23 | 1.28 | 1.33 | | |
| | | | CN4–0 = 12H | 1.25 | 1.30 | 1.35 | | |
| | | | CN4–0 = 13H | 1.27 | 1.32 | 1.37 | | |
| | | | CN4–0 = 14H *1 | 1.29 | 1.34 | 1.39 | | |
| | | | CN4–0 = 15H *1 | 1.31 | 1.36 | 1.41 | | |
| | | | CN4–0 = 16H *1 | 1.33 | 1.38 | 1.43 | | |
| | | | CN4–0 = 17H *1 | 1.35 | 1.40 | 1.45 | | |
| | | | CN4–0 = 18H *1 | 1.37 | 1.42 | 1.47 | | |
| | | | CN4–0 = 19H *1 | 1.39 | 1.44 | 1.49 | | |
| | | | CN4–0 = 1AH *1 | 1.41 | 1.46 | 1.51 | | |
| | | | CN4–0 = 1BH *1 | 1.43 | 1.48 | 1.53 | | |
| | | | CN4–0 = 1CH *1 | 1.45 | 1.50 | 1.55 | | |
| | | | CN4–0 = 1DH *1 | 1.47 | 1.52 | 1.57 | | |
| | | | CN4–0 = 1EH *1 | 1.49 | 1.54 | 1.59 | | |
| | | | CN4–0 = 1FH *1 | 1.51 | 1.56 | 1.61 | | |
| $V_{L1}$ temperature deviation | $\Delta V_{L1}$ | $V_{DD}$ = 3.0V | | — | −1.5 | — | mV/°C | |
| $V_{L1}$ voltage dependency | $\Delta V_{L1}$ | $V_{DD}$ = 1.3 to 3.6V | | — | 5 | 20 | mV/V | |
| $V_{L2}$ voltage | $V_{L2}$ | $V_{DD}$ = 3.0V, Tj = 25°C, 300kΩ load ($V_{L4}$–$V_{SS}$) | | Typ. −10% | $V_{L1}$×2 | Typ. +4% | V | |
| $V_{L3}$ voltage | $V_{L3}$ | $V_{DD}$ = 3.0V, Tj = 25°C, 300kΩ load ($V_{L4}$–$V_{SS}$) | 1/3 bias | Typ. −10% | $V_{L1}$×2 | Typ. +4% | V | |
| | | | 1/4 bias | | $V_{L1}$×3 | | | |
| $V_{L4}$ voltage | $V_{L4}$ | | 1/3 bias | Typ. −10% | $V_{L1}$×3 | Typ. +5% | | |
| | | | 1/4 bias | | $V_{L1}$×4 | | | |
| LCD bias voltage generation time | $T_{BIAS}$ | — | | — | — | 600 | ms | |

*1: When using 1/4 bias, the $V_{L1}$ voltage is set to typ. 1.32 V (same voltage as in CN4–0 = 13H).

**DC CHARACTERISTICS (3/5)**

($V_{DD}$ = 1.1 to 3.6V, $V_{SS}$ = 0V, Ta = –20 to +70°C, unless otherwise specified) (3/5)

| Parameter | Symbol | Condition | | Rating Min. | Rating Typ. | Rating Max. | Unit | Measuring circuit |
|---|---|---|---|---|---|---|---|---|
| BLD threshold voltage | $V_{BLD}$ | $V_{DD}$ = 1.35 to 3.6V | LD2–0 = 0H | Typ. –2% | 1.35 | Typ. +2% | V | 1 |
| | | | LD2–0 = 1H | | 1.4 | | | |
| | | | LD2–0 = 2H | | 1.45 | | | |
| | | | LD2–0 = 3H | | 1.5 | | | |
| | | | LD2–0 = 4H | | 1.6 | | | |
| | | | LD2–0 = 5H | | 1.7 | | | |
| | | | LD2–0 = 6H | | 1.8 | | | |
| | | | LD2–0 = 7H | | 1.9 | | | |
| | | | LD2–0 = 8H | | 2.0 | | | |
| | | | LD2–0 = 9H | | 2.1 | | | |
| | | | LD2–0 = 0AH | | 2.2 | | | |
| | | | LD2–0 = 0BH | | 2.3 | | | |
| | | | LD2–0 = 0CH | | 2.4 | | | |
| | | | LD2–0 = 0DH | | 2.5 | | | |
| | | | LD2–0 = 0EH | | 2.7 | | | |
| | | | LD2–0 = 0FH | | 2.9 | | | |
| BLD threshold voltage temperature deviation | $\Delta V_{BLD}$ | $V_{DD}$ = 1.35 to 3.6V | | — | 0 | — | %/°C | |
| Supply current 1 | IDD1 | CPU: In STOP state. Low-speed/high-speed oscillation: stopped. | Ta = 25°C | — | 0.15 | 0.50 | μA | |
| | | | Ta = -20 to +70°C | — | — | 2.50 | | |
| Supply current 2 | IDD2 | CPU: In HALT state (LTBC, RTC: Operating*3*5). High-speed oscillation: Stopped. LCD/BIAS circuits: Stopped. | Ta = 25°C | — | 0.5 | 1.3 | μA | |
| | | | Ta = -20 to +70°C | — | — | 3.5 | | |
| Supply current 3 | IDD3 | CPU: In 32.768kHz operating state.*1*3 High-speed oscillation: Stopped. LCD/BIAS circuits: Operating.*2 | Ta = 25°C | — | 5 | 7 | μA | |
| | | | Ta = -20 to +70°C | — | — | 12 | | |
| Supply current 4 | IDD4 | CPU: In 500kHz CR operating state. LCD/BIAS circuits: Operating.*2*3 | Ta = 25°C | — | 70 | 85 | μA | |
| | | | Ta = -20 to +70°C | — | — | 100 | | |
| Supply current 5 | IDD5 | CPU: In 2MHz CR operating state. LCD/BIAS circuits: Operating.*2*3 | Ta = 25°C | — | 0.4 | 0.5 | mA | |
| | | | Ta = -20 to +70°C | — | — | 0.6 | | |
| Supply current 6 | IDD6 | CPU: In 4.096MHz operating state. PLL: In oscillating state. LCD/BIAS circuits: Operating. *2*3 $V_{DD}$ = 1.8 to 3.6V | Ta = 25°C | — | 0.8 | 1.0 | mA | |
| | | | Ta = -20 to +70°C | — | — | 1.2 | | |

*1 : CPU operating rate is 100% (No HALT state).
*2 : All SEGs: off waveform, No LCD panel load, 1/3 bias, 1/3 duty, Frame frequency: Approx. 64 Hz, Bias voltage multiplying clock: 1/128 LSCLK (256Hz)
*3 : Use 32.768kHz crystal resonator DT-26 (Load capacitance 6pF) (made by KDS:DAISHINKU CORP.) is used ($C_{GL}$=$C_{DL}$=12pF).
*4 : Use 4.096MHz Crystal Oscillator CHC49SFWB (Kyocera).
*5 : Significant bits of BLKCON0~BLKCON4 registers are all “1”.

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| (P30–P35)<br>(P40–P47)<br>(PA0–PA5)*1 | | | $V_{DD}$ = 1.1 to 3.6V | –200 | –30 | -0.01 | | |
| | IIH2Z | VIH2 = $V_{DD}$ (in high-impedance state) | | — | — | 1 | | |
| | IIL2Z | VIL2 = $V_{SS}$ (in high-impedance state) | | –1 | — | — | | |

*1: ML610Q429 only

**DC CHARACTERISTICS (5/5)**

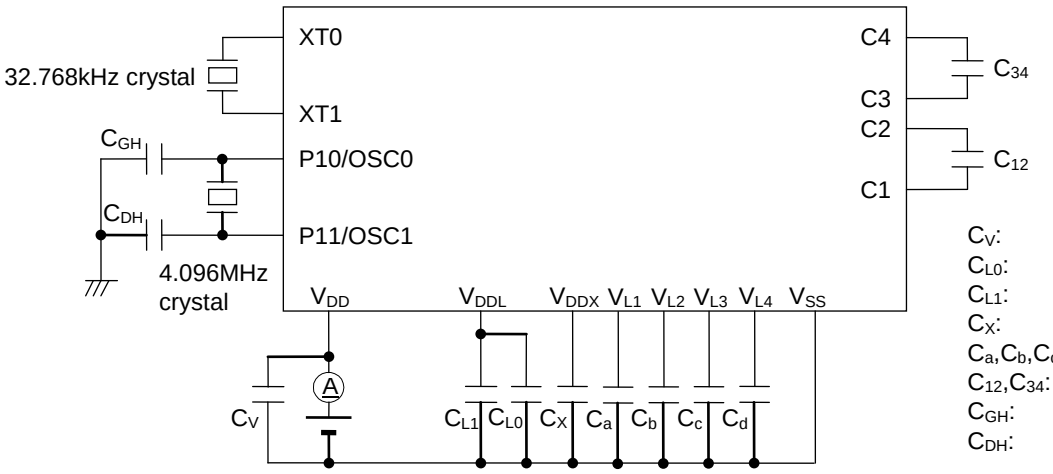
($V_{DD}$ = 1.1 to 3.6V, $V_{SS}$ = 0V, Ta = -20 to +70°C, unless otherwise specified) (5/5)

| Parameter | Symbol | Condition | Rating | | | Unit | Measuring circuit |
|---|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | | |
| Input voltage 1<br>(RESET_N)<br>(TEST)<br>(NMI)<br>(P00–P03)<br>(P04–P07)*1<br>(P10–P11)<br>(P31–P35)<br>(P40–P43)<br>(P45–P47)<br>(PA0–PA5)*1 | VIH1 | $V_{DD}$ = 1.3 to 3.6V | 0.7 ×$V_{DD}$ | — | $V_{DD}$ | V | 5 |
| | | $V_{DD}$ = 1.1 to 3.6V | 0.7 ×$V_{DD}$ | — | $V_{DD}$ | | |
| | VIL1 | $V_{DD}$ = 1.3 to 3.6V | 0 | — | 0.3 ×$V_{DD}$ | | |
| | | $V_{DD}$ = 1.1 to 3.6V | 0 | — | 0.2 ×$V_{DD}$ | | |
| Input voltage 2<br>(P30, P44) | VIH2 | — | 0.7 ×$V_{DD}$ | — | $V_{DD}$ | | |
| | VIL2 | — | 0 | — | 0.3 ×$V_{DD}$ | | |
| Input pin capacitance<br>(NMI)<br>(P00–P03)<br>(P04–P07)*1<br>(P10–P11)<br>(P30–P35)<br>(P40–P47)<br>(PA0–PA5)*1 | CIN | f = 10kHz<br>$V_{rms}$ = 50mV<br>Ta = 25°C | — | — | 5 | pF | — |

*1: ML610Q429 only

## MEASURING CIRCUITS

### MEASURING CIRCUIT 1

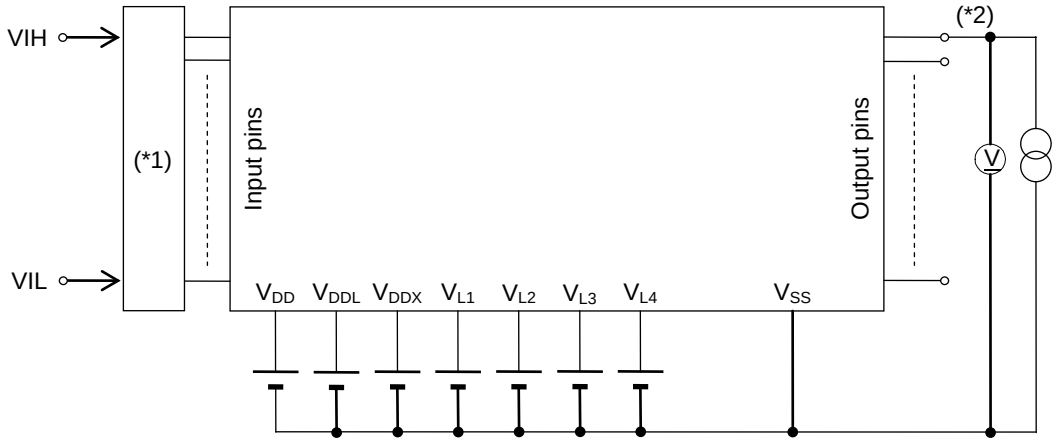



| | |
|---|---|
| $C_V$: | 1µF |
| $C_{L0}$: | 1µF |
| $C_{L1}$: | 0.1µF |
| $C_X$: | 0.1µF |
| $C_a$,$C_b$,$C_c$,$C_d$: | 1µF |
| $C_{12}$,$C_{34}$: | 1µF |
| $C_{GH}$: | 24pF |
| $C_{DH}$: | 24pF |

32.768kHz crystal resonator
DT-26 (Load capacitance 6pF)
(Made by KDS:DAISHINKU CORP.)

4.096MHz crystal:
HC49SFWB (Kyocera)

### MEASURING CIRCUIT 2



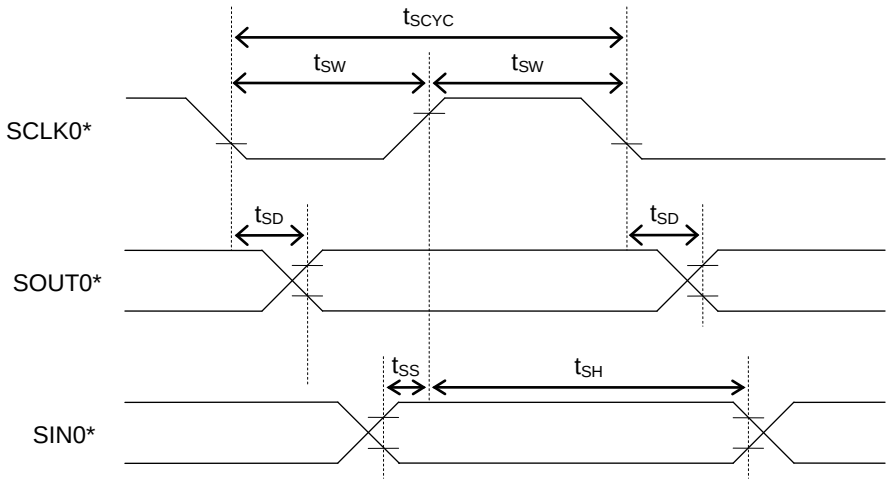

(*1) Input logic circuit to determine the specified measuring conditions.
(*2) Measured at the specified output pins.

**AC CHARACTERISTICS (Synchronous Serial Port)**

($V_{DD}$ = 1.3 to 3.6V, $V_{SS}$ = 0V, Ta = –20 to +70°C, unless otherwise specified)

| Parameter | Symbol | Condition | Rating | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| SCLK input cycle (slave mode) | $t_{SCYC}$ | When high-speed oscillation is not active | 10 | — | — | µs |
| | | When high-speed oscillation is active ($V_{DD}$ = 1.8 to 3.6V) | 1 | — | — | µs |
| SCLK output cycle (master mode) | $t_{SCYC}$ | — | — | SCLK*1 | — | s |
| SCLK input pulse width (slave mode) | $t_{SW}$ | When high-speed oscillation is not active | 4 | — | — | µs |
| | | When high-speed oscillation is active ($V_{DD}$ = 1.8 to 3.6V) | 0.4 | — | — | µs |
| SCLK output pulse width (master mode) | $t_{SW}$ | — | SCLK*1 ×0.4 | SCLK*1 ×0.5 | SCLK*1 ×0.6 | s |
| SOUT output delay time (slave mode) | $t_{SD}$ | — | — | — | 180 | ns |
| SOUT output delay time (master mode) | $t_{SD}$ | — | — | — | 80 | ns |
| SIN input setup time (slave mode) | $t_{SS}$ | — | 80 | — | — | ns |
| SIN input setup time (master mode) | $t_{SS}$ | — | 180 | — | — | ns |
| SIN input hold time | $t_{SH}$ | — | 80 | — | — | ns |

*1: Clock period selected with S0CK3–0 of the serial port 0 mode register (SIO0MOD1)




*: Indicates the secondary function of the port.

### AC CHARACTERISTICS ($I^2C$ Bus Interface: Standard Mode 100kHz)

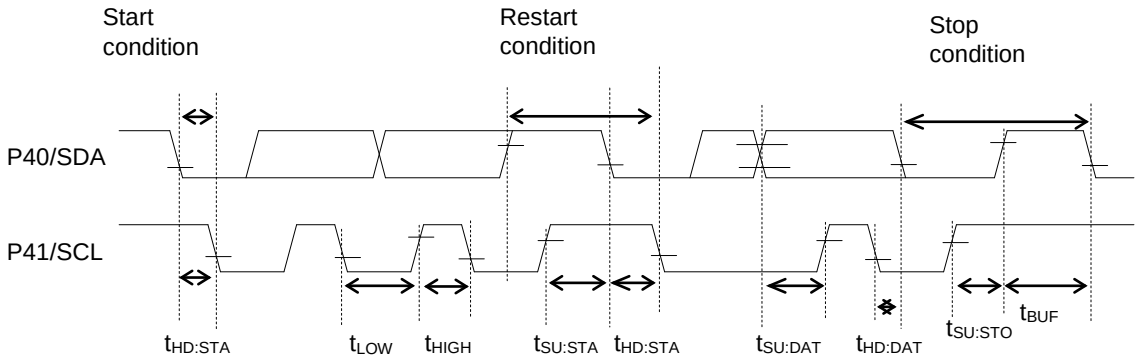
($V_{DD}$ = 1.8 to 3.6V, $V_{SS}$ = 0V, Ta = –20 to +70°C, unless otherwise specified)

| Parameter | Symbol | Condition | Rating | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| SCL clock frequency | $f_{SCL}$ | — | 0 | — | 100 | kHz |
| SCL hold time (start/restart condition) | $t_{HD:STA}$ | — | 4.0 | — | — | µs |
| SCL "L" level time | $t_{LOW}$ | — | 4.7 | — | — | µs |
| SCL "H" level time | $t_{HIGH}$ | — | 4.0 | — | — | µs |
| SCL setup time (restart condition) | $t_{SU:STA}$ | — | 4.7 | — | — | µs |
| SDA hold time | $t_{HD:DAT}$ | — | 0 | — | 3.45 | µs |
| SDA setup time | $t_{SU:DAT}$ | — | 0.25 | — | — | µs |
| SDA setup time (stop condition) | $t_{SU:STO}$ | — | 4.0 | — | — | µs |
| Bus-free time | $t_{BUF}$ | — | 4.7 | — | — | µs |

### AC CHARACTERISTICS ($I^2C$ Bus Interface: Fast Mode 400kHz)

($V_{DD}$ = 1.8 to 3.6V, $V_{SS}$ = 0V, Ta = –20 to +70°C, unless otherwise specified)

| Parameter | Symbol | Condition | Rating | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| SCL clock frequency | $f_{SCL}$ | — | 0 | — | 400 | kHz |
| SCL hold time (start/restart condition) | $t_{HD:STA}$ | — | 0.6 | — | — | µs |
| SCL "L" level time | $t_{LOW}$ | — | 1.3 | — | — | µs |
| SCL "H" level time | $t_{HIGH}$ | — | 0.6 | — | — | µs |
| SCL setup time (restart condition) | $t_{SU:STA}$ | — | 0.6 | — | — | µs |
| SDA hold time | $t_{HD:DAT}$ | — | 0 | — | 0.9 | µs |
| SDA setup time | $t_{SU:DAT}$ | — | 0.1 | — | — | µs |
| SDA setup time (stop condition) | $t_{SU:STO}$ | — | 0.6 | — | — | µs |
| Bus-free time | $t_{BUF}$ | — | 1.3 | — | — | µs |



## REVISION HISTORY

| Document No. | Date | Page | | Description |
|---|---|---|---|---|
| | | Previous Edition | Current Edition | |
| FEDL610Q428-01 | Feb.7.2011 | – | – | Formally edition 1.0 |
| FEDL610Q428-02 | Jun 7.2011 | 3 | 3 | Add the P version |
| FEDL610Q428-03 | July.25.2014 | All | All | Change header and footer |
| | | 3,18,19, 20,21,22, 23,26,27, 28,29 | 3,18,20, 21,22,23, 24,27,28, 29,30 | Delete the P version |
| | | 3,7 | 4 | Delete package products |
| | | 2,7 | 2 | Delete the metal option of only ML610Q429's LCD driver |
| | | 3 | 4 | Change from "Shipment" to " Product name – Supported Function " |
| | | - | 19 | Add CLOCK GENERATION CIRCUIT OPERATING CONDITIONS |
| | | 19 | 20 | Change "RESET" to "Reset pulse width ($P_{RST}$)" and " Power-on reset activation power rise time ($T_{POR}$ )". |
| | | 21 | 22 | Correct the $C_{GL}$'s value and the $C_{DL}$'s value of DC CHARACTERISTICS (3/5)'s note No.3 |
| | | 30 | 31 | Update Package Dimensions |
| FEDL610Q428-04 | May.15,2015 | 2 | 2 | Corrected a typo. "100kbps@1MHz HSCLK" is corrected to 100kbps@4MHz HSCLK. |
| | | - | 4,8 | Add the ML610Q429 package product |

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