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What Are [Embedded - Microcontrollers - Application Specific](#)?

Application specific microcontrollers are engineered to

Details

Product Status	Obsolete
Applications	Capacitive Sensing
Core Processor	M8C
Program Memory Type	FLASH (8kB)
Controller Series	CY8C20xx6A
RAM Size	1K x 8
Interface	I ² C, SPI
Number of I/O	28
Voltage - Supply	1.71V ~ 5.5V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	32-UFQFN Exposed Pad
Supplier Device Package	32-QFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c20436an-24lqxi

Analog Multiplexer System

The Analog Mux Bus can connect to every GPIO pin. Pins are connected to the bus individually or in any combination. The bus also connects to the analog system for analysis with the CapSense block comparator.

Switch control logic enables selected pins to precharge continuously under hardware control. This enables capacitive measurement for applications such as touch sensing. Other multiplexer applications include:

- Complex capacitive sensing interfaces, such as sliders and touchpads.
- Chip-wide mux that allows analog input from any I/O pin.
- Crosspoint connection between any I/O pin combinations.

Additional System Resources

System resources provide additional capability, such as configurable USB and I²C slave, SPI master/slave communication interface, three 16-bit programmable timers, and various system resets supported by the M8C.

These system resources provide additional capability useful to complete systems. Additional resources include low voltage detection and power on reset. The merits of each system resource are listed here:

- The I²C slave/SPI master-slave module provides 50/100/400 kHz communication over two wires. SPI communication over three or four wires runs at speeds of 46.9 kHz to 3 MHz (lower for a slower system clock).
- Low-voltage detection (LVD) interrupts can signal the application of falling voltage levels, while the advanced power-on-reset (POR) circuit eliminates the need for a system supervisor.
- An internal reference provides an absolute reference for capacitive sensing.
- A register-controlled bypass mode allows the user to disable the LDO regulator.

Getting Started

The quickest way to understand PSoC silicon is to read this datasheet and then use the PSoC Designer Integrated Development Environment (IDE). This datasheet is an overview of the PSoC integrated circuit and presents specific pin, register, and electrical specifications.

For in depth information, along with detailed programming details, see the [Technical Reference Manual](#) for the CY8C20XX6A/S PSoC devices.

For up-to-date ordering, packaging, and electrical specification information, see the latest PSoC device datasheets on the web at www.cypress.com/psoc.

CapSense Design Guides

Design Guides are an excellent introduction to the wide variety of possible CapSense designs. They are located at www.cypress.com/go/CapSenseDesignGuides.

Refer Getting Started with CapSense design guide for information on CapSense design and CY8C20XX6A/H/AS CapSense® Design Guide for specific information on CY8C20XX6A/AS CapSense controllers.

Silicon Errata

Errata documents known issues with silicon including errata trigger conditions, scope of impact, available workarounds and silicon revision applicability. Refer to Silicon Errata for the PSoC® CY8C20x36A/46A/66A/96A/46AS/66AS/36H/46H families available at <http://www.cypress.com/?rID=56239> for errata information on CY8C20xx6A/AS/H family of device. Compare errata document with datasheet for a complete functional description of device.

Development Kits

[PSoC Development Kits](#) are available online from and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

Training

[Free PSoC technical training](#) (on demand, webinars, and workshops), which is available online via www.cypress.com, covers a wide variety of topics and skill levels to assist you in your designs.

CYPros Consultants

Certified PSoC consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC consultant go to the [CYPros Consultants](#) web site.

Solutions Library

Visit our growing [library of solution focused designs](#). Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

Technical Support

[Technical support](#) – including a searchable Knowledge Base articles and technical forums – is also available online. If you cannot find an answer to your question, call our Technical Support hotline at 1-800-541-4736.

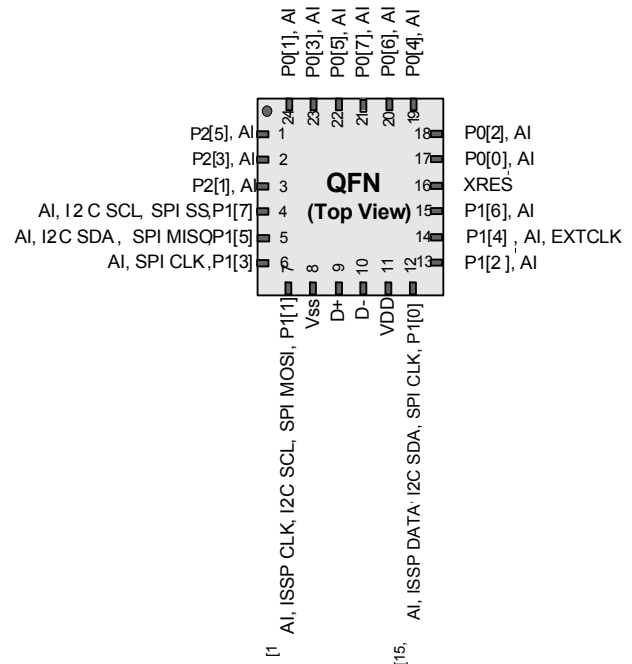
24-pin QFN (15 Sensing Inputs (With USB)) ^[13]

Table 3. Pin Definitions – CY8C20396A ^[14]

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I	P2[5]	
2	I/O	I	P2[3]	
3	I/O	I	P2[1]	
4	IOHR	I	P1[7]	I ² C SCL, SPI SS
5	IOHR	I	P1[5]	I ² C SDA, SPI MISO
6	IOHR	I	P1[3]	SPI CLK
7	IOHR	I	P1[1]	ISSP CLK ^[15] , I ² C SCL, SPI MOSI
8	Power		V _{SS}	Ground ^[17]
9	I/O	I	D+	USB D+
10	I/O	I	D-	USB D-
11	Power		V _{DD}	Supply
12	IOHR	I	P1[0]	ISSP DATA ^[15] , I ² C SDA, SPI CLK ^[16]
13	IOHR	I	P1[2]	
14	IOHR	I	P1[4]	Optional external clock input (EXTCLK)
15	IOHR	I	P1[6]	
16	RESET INPUT		XRES	Active high external reset with internal pull-down
17	IOH	I	P0[0]	
18	IOH	I	P0[2]	
19	IOH	I	P0[4]	
20	IOH	I	P0[6]	
21	IOH	I	P0[7]	
22	IOH	I	P0[5]	
23	IOH	I	P0[3]	Integrating input
24	IOH	I	P0[1]	Integrating input
CP	Power		V _{SS}	Center pad must be connected to Ground

LEGEND I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output

Figure 5. CY8C20396A



Notes

13. 20 GPIOs = 15 pins for capacitive sensing + 2 pins for I²C + 2 pins for USB + 1 pin for modulation capacitor.
14. The center pad (CP) on the QFN package must be connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.
15. On power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to high impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the I²C bus. Use alternate pins if you encounter issues.
16. Alternate SPI clock.
17. All VSS pins should be brought out to one common GND plane.



48-pin QFN (OCD) (33 Sensing Inputs) ^[46]

The 48-pin QFN part is for the CY8C20066A On-Chip Debug (OCD). Note that this part is only used for in-circuit debugging.

Table 10. Pin Definitions – CY8C20066A ^[47, 48]

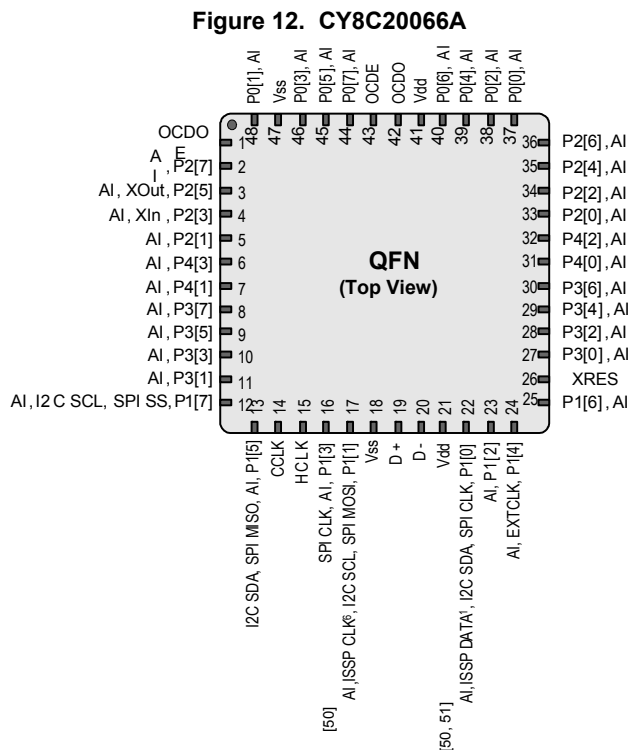
Pin No.	Digital	Analog	Name	Description
1 ^[49]			OCDOE	OCD mode direction pin
2	I/O	I	P2[7]	
3	I/O	I	P2[5]	Crystal output (XOut)
4	I/O	I	P2[3]	Crystal input (XIn)
5	I/O	I	P2[1]	
6	I/O	I	P4[3]	
7	I/O	I	P4[1]	
8	I/O	I	P3[7]	
9	I/O	I	P3[5]	
10	I/O	I	P3[3]	
11	I/O	I	P3[1]	
12	IOHR	I	P1[7]	I ² C SCL, SPI SS
13	IOHR	I	P1[5]	I ² C SDA, SPI MISO
14 ^[49]			CCLK	OCD CPU clock output
15 ^[49]			HCLK	OCD high speed clock output
16	IOHR	I	P1[3]	SPI CLK.
17	IOHR	I	P1[1]	ISSP CLK ^[50] , I ² C SCL, SPI MOSI
18	Power		V _{SS}	Ground connection ^[52]
19	I/O		D+	USB D+
20	I/O		D-	USB D-
21	Power		V _{DD}	Supply voltage
22	IOHR	I	P1[0]	ISSP DATA ^[50] , I ² C SDA, SPI CLK ^[51]
23	IOHR	I	P1[2]	
24	IOHR	I	P1[4]	Optional external clock input (EXTCLK)
25	IOHR	I	P1[6]	
26	Input		XRES	Active high external reset with internal pull-down
27	I/O	I	P3[0]	
28	I/O	I	P3[2]	
29	I/O	I	P3[4]	
30	I/O	I	P3[6]	
31	I/O	I	P4[0]	
32	I/O	I	P4[2]	
33	I/O	I	P2[0]	
34	I/O	I	P2[2]	
35	I/O	I	P2[4]	
36	I/O	I	P2[6]	

Pin No.	Digital	Analog	Name	Description
37	IOH	I	P0[0]	
38	IOH	I	P0[2]	
39	IOH	I	P0[4]	
40	IOH	I	P0[6]	
41	Power		V _{DD}	Supply voltage
42 ^[49]			OCDO	OCD even data I/O
43 ^[49]			OCDE	OCD odd data output
44	IOH	I	P0[7]	
45	IOH	I	P0[5]	
46	IOH	I	P0[3]	Integrating input
47	Power		V _{SS}	Ground connection ^[52]
48	IOH	I	P0[1]	
CP	Power		V _{SS}	Center pad must be connected to ground

LEGEND A = Analog, I = Input, O = Output, NC = No Connection H = 5 mA High Output Drive, R = Regulated Output.

Notes

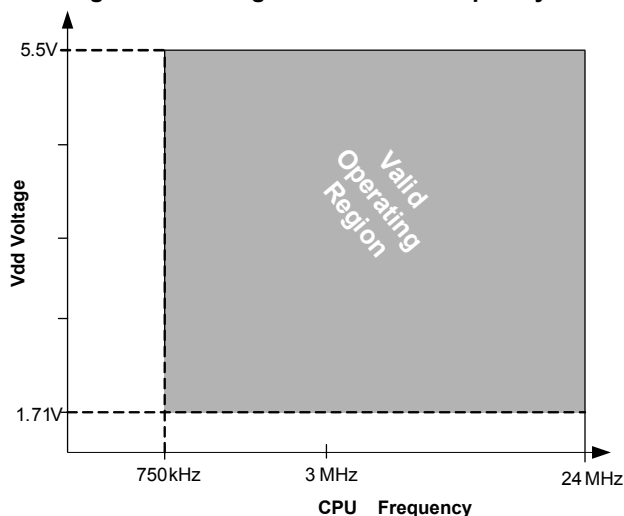
46. 38 GPIOs = 33 pins for capacitive sensing + 2 pins for I2C + 2 pins for USB + 1 pin for modulation capacitor.
47. This part is available in limited quantities for In-Circuit Debugging during prototype development. It is not available in production volumes.
48. The center pad (CP) on the QFN package must be connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.
49. This pin (associated with OCD part only) is required for connecting the device to ICE-Cube In-Circuit Emulator for firmware debugging purpose. To know more about the usage of ICE-Cube, refer to [CY3215-DK PSoC® IN-CIRCUIT EMULATOR KIT GUIDE](#).
50. On Power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to High impedance state. On reset, after XRES de- asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. In both cases, a pull-up resistance on these lines combines with the pull-down resistance (5.6K ohm) and form a potential divider. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the I2C bus. Use alternate pins if you encounter issues.
51. Alternate SPI clock.
52. All VSS pins should be brought out to one common GND plane.



Electrical Specifications

This section presents the DC and AC electrical specifications of the CY8C20XX6A/S PSoC devices. For the latest electrical specifications, confirm that you have the most recent datasheet by visiting the web at <http://www.cypress.com/psoc>.

Figure 13. Voltage versus CPU Frequency



Absolute Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Table 11. Absolute Maximum Ratings

Symbol	Description	Conditions	Min	Typ	Max	Units
T _{STG}	Storage temperature	Higher storage temperatures reduce data retention time. Recommended Storage Temperature is +25 °C ± 25 °C. Extended duration storage temperatures above 85 °C degrades reliability.	-55	+25	+125	°C
V _{DD}	Supply voltage relative to V _{SS}	—	-0.5	—	+6.0	V
V _{IO}	DC input voltage	—	V _{SS} - 0.5	—	V _{DD} + 0.5	V
V _{IOZ} ^[53]	DC voltage applied to tristate	—	V _{SS} - 0.5	—	V _{DD} + 0.5	V
I _{MIO}	Maximum current into any port pin	—	-25	—	+50	mA
ESD	Electrostatic discharge voltage	Human body model ESD	2000	—	—	V
LU	Latch-up current	In accordance with JEDEC78 standard	—	—	200	mA

Operating Temperature

Table 12. Operating Temperature

Symbol	Description	Conditions	Min	Typ	Max	Units
T _A	Ambient temperature	—	-40	—	+85	°C
T _C	Commercial temperature range	—	0	—	70	°C
T _J	Operational die temperature	The temperature rise from ambient to junction is package specific. Refer the Thermal Impedances on page 38 . The user must limit the power consumption to comply with this requirement.	-40	—	+100	°C

Note

53. Port1 pins are hot-swap capable with I/O configured in High-Z mode, and pin input voltage above V_{DD}.

DC GPIO Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 5.5 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, 2.4 V to 3.0 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, or 1.71 V to 2.4 V and $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 14. 3.0 V to 5.5 V DC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R _{PU}	Pull-up resistor	–	4	5.60	8	kΩ
V _{OH1}	High output voltage Port 2 or 3 or 4 pins	I _{OH} ≤ 10 μA, maximum of 10 mA source current in all I/Os	V _{DD} – 0.20	–	–	V
V _{OH2}	High output voltage Port 2 or 3 or 4 pins	I _{OH} = 1 mA, maximum of 20 mA source current in all I/Os	V _{DD} – 0.90	–	–	V
V _{OH3}	High output voltage Port 0 or 1 pins with LDO regulator Disabled for port 1	I _{OH} < 10 μA, maximum of 10 mA source current in all I/Os	V _{DD} – 0.20	–	–	V
V _{OH4}	High output voltage Port 0 or 1 pins with LDO regulator Disabled for port 1	I _{OH} = 5 mA, maximum of 20 mA source current in all I/Os	V _{DD} – 0.90	–	–	V
V _{OH5}	High output voltage Port 1 Pins with LDO Regulator Enabled for 3 V out	I _{OH} < 10 μA, V _{DD} > 3.1 V, maximum of 4 I/Os all sourcing 5 mA	2.85	3.00	3.30	V
V _{OH6}	High output voltage Port 1 pins with LDO regulator enabled for 3 V out	I _{OH} = 5 mA, V _{DD} > 3.1 V, maximum of 20 mA source current in all I/Os	2.20	–	–	V
V _{OH7}	High output voltage Port 1 pins with LDO enabled for 2.5 V out	I _{OH} < 10 μA, V _{DD} > 2.7 V, maximum of 20 mA source current in all I/Os	2.35	2.50	2.75	V
V _{OH8}	High output voltage Port 1 pins with LDO enabled for 2.5 V out	I _{OH} = 2 mA, V _{DD} > 2.7 V, maximum of 20 mA source current in all I/Os	1.90	–	–	V
V _{OH9}	High output voltage Port 1 pins with LDO enabled for 1.8 V out	I _{OH} < 10 μA, V _{DD} > 2.7 V, maximum of 20 mA source current in all I/Os	1.60	1.80	2.10	V
V _{OH10}	High output voltage Port 1 pins with LDO enabled for 1.8 V out	I _{OH} = 1 mA, V _{DD} > 2.7 V, maximum of 20 mA source current in all I/Os	1.20	–	–	V
V _{OL}	Low output voltage	I _{OL} = 25 mA, V _{DD} > 3.3 V, maximum of 60 mA sink current on even port pins (for example, P0[2] and P1[4]) and 60 mA sink current on odd port pins (for example, P0[3] and P1[5])	–	–	0.75	V
V _{IL}	Input low voltage	–	–	–	0.80	V
V _{IH}	Input high voltage	–	2.00	–	–	V
V _H	Input hysteresis voltage	–	–	80	–	mV
I _{IL}	Input leakage (Absolute Value)	–	–	0.001	1	μA
C _{PIN}	Pin capacitance	Package and pin dependent Temp = 25 °C	0.50	1.70	7	pF
V _{ILLVT3.3}	Input Low Voltage with low threshold enable set, Enable for Port1	Bit3 of IO_CFG1 set to enable low threshold voltage of Port1 input	0.8	V	–	–
V _{IHLVT3.3}	Input High Voltage with low threshold enable set, Enable for Port1	Bit3 of IO_CFG1 set to enable low threshold voltage of Port1 input	1.4	–	–	V
V _{ILLVT5.5}	Input Low Voltage with low threshold enable set, Enable for Port1	Bit3 of IO_CFG1 set to enable low threshold voltage of Port1 input	0.8	V	–	–
V _{IHLVT5.5}	Input High Voltage with low threshold enable set, Enable for Port1	Bit3 of IO_CFG1 set to enable low threshold voltage of Port1 input	1.7	–	–	V

Table 16. 1.71 V to 2.4 V DC GPIO Specifications (continued)

Symbol	Description	Conditions	Min	Typ	Max	Units
V _{IH}	Input high voltage	–	0.65 × V _{DD}	–	–	V
V _H	Input hysteresis voltage	–	–	80	–	mV
I _{IL}	Input leakage (absolute value)	–	–	1	1000	nA
C _{PIN}	Capacitive load on pins	Package and pin dependent temp = 25 °C	0.50	1.70	7	pF

Table 17. DC Characteristics – USB Interface

Symbol	Description	Conditions	Min	Typ	Max	Units
R _{USBI}	USB D+ pull-up resistance	With idle bus	900	–	1575	Ω
R _{USBA}	USB D+ pull-up resistance	While receiving traffic	1425	–	3090	Ω
V _{OHUSB}	Static output high	–	2.8	–	3.6	V
V _{OLUSB}	Static output low	–	–	–	0.3	V
V _{DI}	Differential input sensitivity	–	0.2	–	–	V
V _{CM}	Differential input common mode range	–	0.8	–	2.5	V
V _{SE}	Single ended receiver threshold	–	0.8	–	2.0	V
C _{IN}	Transceiver capacitance	–	–	–	50	pF
I _{IO}	High Z state data line leakage	On D+ or D- line	–10	–	+10	μA
R _{PS2}	PS/2 pull-up resistance	–	3000	5000	7000	Ω
R _{EXT}	External USB series resistor	In series with each USB pin	21.78	22.0	22.22	Ω

DC Analog Mux Bus Specifications

Table 18 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 18. DC Analog Mux Bus Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R _{SW}	Switch resistance to common analog bus	–	–	–	800	Ω
R _{GND}	Resistance of initialization switch to V _{SS}	–	–	–	800	Ω

The maximum pin voltage for measuring R_{SW} and R_{GND} is 1.8 V

DC Low Power Comparator Specifications

Table 19 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 19. DC Comparator Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V _{LPC}	Low power comparator (LPC) common mode	Maximum voltage limited to V _{DD}	0.0	–	1.8	V
I _{LPC}	LPC supply current	–	–	10	40	μA
V _{OSLPC}	LPC voltage offset	–	–	3	30	mV

Comparator User Module Electrical Specifications

Table 20 lists the guaranteed maximum and minimum specifications. Unless stated otherwise, the specifications are for the entire device voltage and temperature operating range: $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$, $1.71\text{ V} \leq V_{DD} \leq 5.5\text{ V}$.

Table 20. Comparator User Module Electrical Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
t_{COMP}	Comparator response time	50 mV overdrive	–	70	100	ns
Offset		Valid from 0.2 V to $V_{DD} - 0.2\text{ V}$	–	2.5	30	mV
Current		Average DC current, 50 mV overdrive	–	20	80	μA
PSRR	Supply voltage > 2 V	Power supply rejection ratio	–	80	–	dB
	Supply voltage < 2 V	Power supply rejection ratio	–	40	–	dB
Input range		–	0		1.5	V

ADC Electrical Specifications

Table 21. ADC User Module Electrical Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
Input						
V_{IN}	Input voltage range	–	0	–	V_{REFADC}	V
C_{IIN}	Input capacitance	–	–	–	5	pF
R_{IN}	Input resistance	Equivalent switched cap input resistance for 8-, 9-, or 10-bit resolution	$1/(500\text{fF} \times \text{data clock})$	$1/(400\text{fF} \times \text{data clock})$	$1/(300\text{fF} \times \text{data clock})$	Ω
Reference						
V_{REFADC}	ADC reference voltage	–	1.14	–	1.26	V
Conversion Rate						
F_{CLK}	Data clock	Source is chip's internal main oscillator. See AC Chip-Level Specifications for accuracy	2.25	–	6	MHz
S8	8-bit sample rate	Data clock set to 6 MHz. sample rate = $0.001 / (2^{\text{Resolution}} / \text{Data Clock})$	–	23.43	–	ksps
S10	10-bit sample rate	Data clock set to 6 MHz. sample rate = $0.001 / (2^{\text{resolution}} / \text{data clock})$	–	5.85	–	ksps
DC Accuracy						
RES	Resolution	Can be set to 8-, 9-, or 10-bit	8	–	10	bits
DNL	Differential nonlinearity	–	–1	–	+2	LSB
INL	Integral nonlinearity	–	–2	–	+2	LSB
E_{OFFSET}	Offset error	8-bit resolution	0	3.20	19.20	LSB
		10-bit resolution	0	12.80	76.80	LSB
E_{GAIN}	Gain error	For any resolution	–5	–	+5	%FSR
Power						
I_{ADC}	Operating current	–	–	2.10	2.60	mA
PSRR	Power supply rejection ratio	PSRR ($V_{DD} > 3.0\text{ V}$)	–	24	–	dB
		PSRR ($V_{DD} < 3.0\text{ V}$)	–	30	–	dB

Table 29. AC Characteristics – USB Data Timings

Symbol	Description	Conditions	Min	Typ	Max	Units
t_{DRATE}	Full speed data rate	Average bit rate	12 – 0.25%	12	12 + 0.25%	MHz
t_{JR1}	Receiver jitter tolerance	To next transition	–18.5	–	18.5	ns
t_{JR2}	Receiver jitter tolerance	To pair transition	–9.0	–	9	ns
t_{DJ1}	FS Driver jitter	To next transition	–3.5	–	3.5	ns
t_{DJ2}	FS Driver jitter	To pair transition	–4.0	–	4.0	ns
t_{FDEOP}	Source jitter for differential transition	To SE0 transition	–2.0	–	5	ns
t_{FEOPT}	Source SE0 interval of EOP	–	160.0	–	175	ns
t_{FEOPR}	Receiver SE0 interval of EOP	–	82.0	–	–	ns
t_{FST}	Width of SE0 interval during differential transition	–	–	–	14	ns

Table 30. AC Characteristics – USB Driver

Symbol	Description	Conditions	Min	Typ	Max	Units
t_{FR}	Transition rise time	50 pF	4	–	20	ns
t_{FF}	Transition fall time	50 pF	4	–	20	ns
$t_{FRFM}^{[70]}$	Rise/fall time matching	–	90	–	111	%
V_{CRS}	Output signal crossover voltage	–	1.30	–	2.00	V

AC Comparator Specifications

Table 31 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 31. AC Low Power Comparator Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
t_{LPC}	Comparator response time, 50 mV overdrive	50 mV overdrive does not include offset voltage	–	–	100	ns

AC External Clock Specifications

Table 32 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 32. AC External Clock Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{OSCEXT}	Frequency (external oscillator frequency)	–	0.75	–	25.20	MHz
	High period	–	20.60	–	5300	ns
	Low period	–	20.60	–	–	ns
	Power-up IMO to switch	–	150	–	–	μs

Note

70. T_{FRFM} is not met under all conditions. There is a corner case at lower supply voltages, such as those under 3.3 V. This condition does not affect USB communications. Signal integrity tests show an excellent eye diagram at 3.15 V.

AC Programming Specifications

Figure 15. AC Waveform

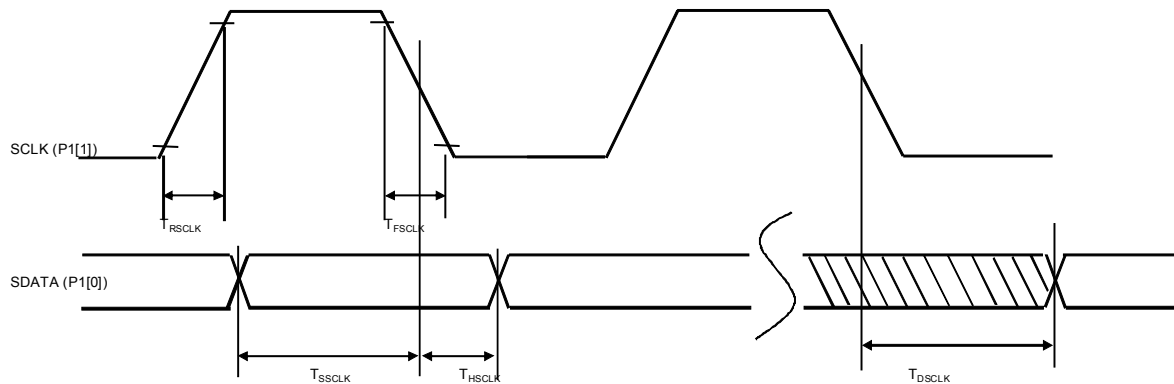


Table 33 lists the guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 33. AC Programming Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
t_{RSCLK}	Rise time of SCLK	—	1	—	20	ns
t_{FSCLK}	Fall time of SCLK	—	1	—	20	ns
t_{SSCLK}	Data setup time to falling edge of SCLK	—	40	—	—	ns
t_{HSCLK}	Data hold time from falling edge of SCLK	—	40	—	—	ns
F_{SCLK}	Frequency of SCLK	—	0	—	8	MHz
t_{ERASEB}	Flash erase time (block)	—	—	—	18	ms
t_{WRITE}	Flash block write time	—	—	—	25	ms
t_{DSCLK}	Data out delay from falling edge of SCLK	$3.6 < V_{DD}$	—	—	60	ns
t_{DSCLK3}	Data out delay from falling edge of SCLK	$3.0 \leq V_{DD} \leq 3.6$	—	—	85	ns
t_{DSCLK2}	Data out delay from falling edge of SCLK	$1.71 \leq V_{DD} \leq 3.0$	—	—	130	ns
t_{XRST3}	External reset pulse width after power-up	Required to enter programming mode when coming out of sleep	300	—	—	μ s
t_{XRES}	XRES pulse length	—	300	—	—	μ s
$t_{VDDWAIT}^{[71]}$	V_{DD} stable to wait-and-poll hold off	—	0.1	—	1	ms
$t_{VDDXRES}^{[71]}$	V_{DD} stable to XRES assertion delay	—	14.27	—	—	ms
t_{POLL}	SDATA high pulse time	—	0.01	—	200	ms
$t_{ACQ}^{[71]}$	"Key window" time after a V_{DD} ramp acquire event, based on 256 ILO clocks.	—	3.20	—	19.60	ms
$t_{XRESINI}^{[71]}$	"Key window" time after an XRES event, based on 8 ILO clocks	—	98	—	615	μ s

Note

71. Valid from 5 to 50 °C. See the spec, CY8C20X66, CY8C20X46, CY8C20X36, CY7C643XX, CY7C604XX, CY8CTST2XX, CY8CTMG2XX, CY8C20X67, CY8C20X47, CY8C20X37, Programming Spec for more details.

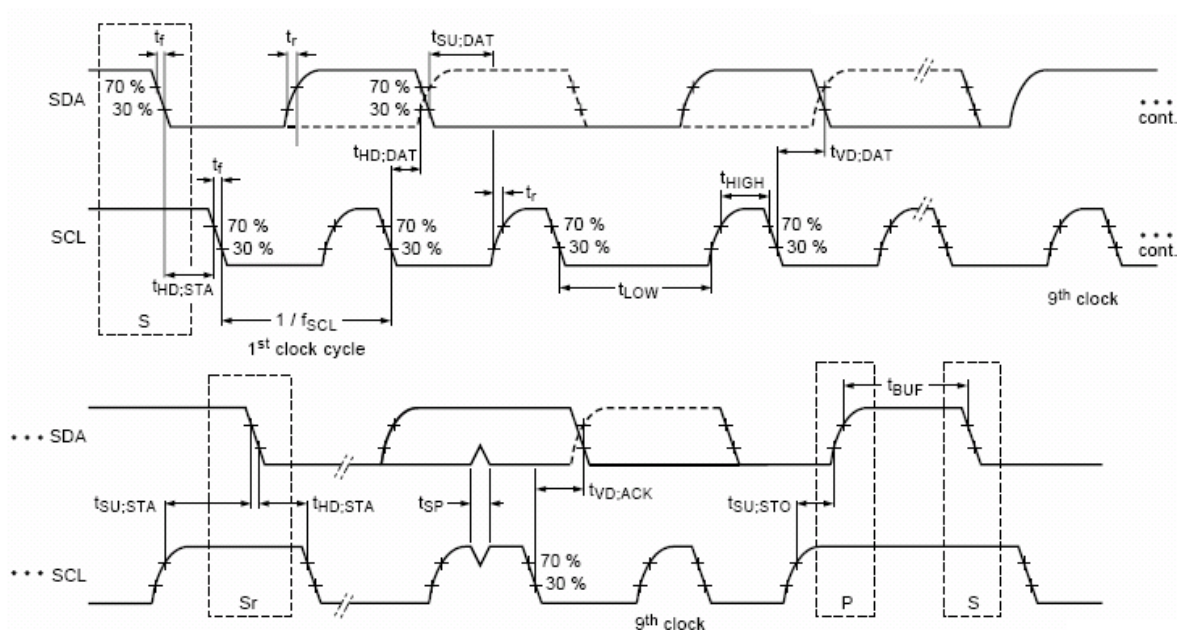
AC I²C Specifications

Table 34 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 34. AC Characteristics of the I²C SDA and SCL Pins

Symbol	Description	Standard Mode		Fast Mode		Units
		Min	Max	Min	Max	
f _{SCL}	SCL clock frequency	0	100	0	400	kHz
t _{HD;STA}	Hold time (repeated) START condition. After this period, the first clock pulse is generated	4.0	–	0.6	–	μs
t _{LOW}	LOW period of the SCL clock	4.7	–	1.3	–	μs
t _{HIGH}	HIGH Period of the SCL clock	4.0	–	0.6	–	μs
t _{SU;STA}	Setup time for a repeated START condition	4.7	–	0.6	–	μs
t _{HD;DAT}	Data hold time	0	3.45	0	0.90	μs
t _{SU;DAT}	Data setup time	250	–	100 ^[72]	–	ns
t _{SU;STO}	Setup time for STOP condition	4.0	–	0.6	–	μs
t _{BUF}	Bus free time between a STOP and START condition	4.7	–	1.3	–	μs
t _{SP}	Pulse width of spikes are suppressed by the input filter	–	–	0	50	ns

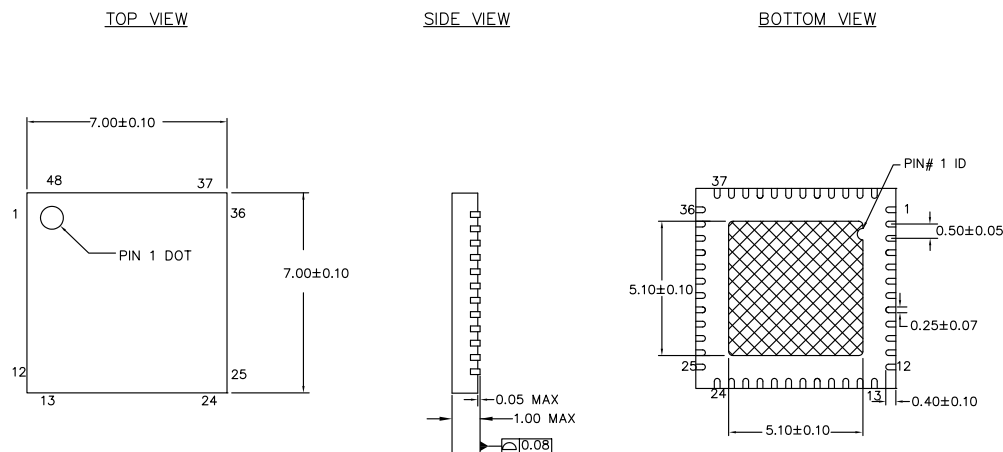
Figure 16. Definition for Timing for Fast/Standard Mode on the I²C Bus




Note

72. A Fast-Mode I²C-bus device can be used in a standard mode I²C-bus system, but the requirement t_{SU;DAT} ≥ 250 ns must then be met. This automatically be the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line t_{rmax} + t_{SU;DAT} = 1000 + 250 = 1250 ns (according to the Standard-Mode I²C-bus specification) before the SCL line is released.

Figure 25. 48-pin QFN (7 × 7 × 1.0 mm) LT48A 5.1 × 5.1 E-Pad (Sawn) Package Outline, 001-13191

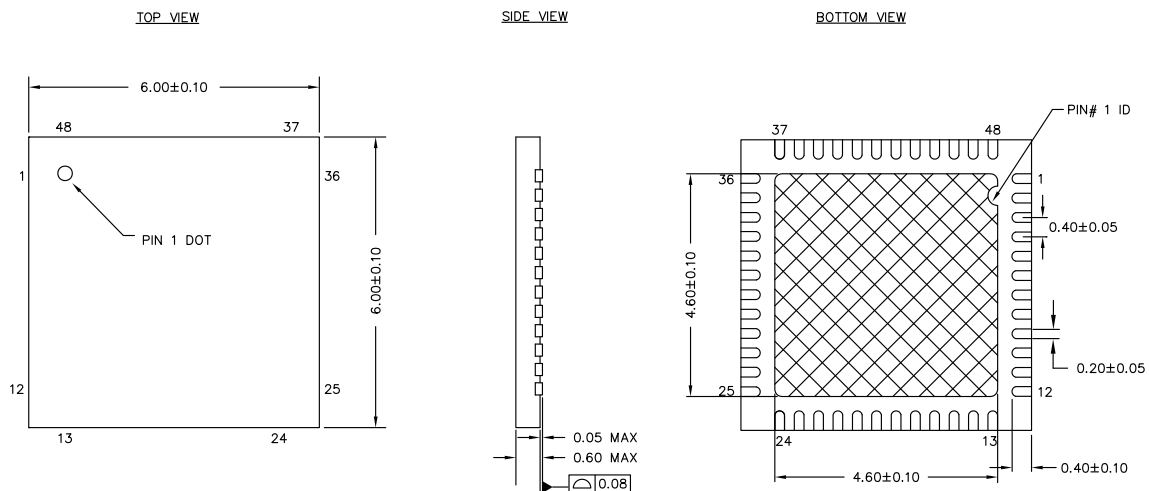


NOTES:


1.  HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO-220
3. PACKAGE WEIGHT: 13 ± 1 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-13191 *H

Figure 26. 48-pin QFN (6 × 6 × 0.6 mm) LQ48A 4.6 × 4.6 E-Pad (Sawn) Package Outline, 001-57280



NOTES:

1.  HATCH AREA IS SOLDERABLE EXPOSED PAD
2. REFERENCE JEDEC # MO-248
3. PACKAGE WEIGHT: 68 ± 7 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-57280 *E

Important Notes

- For information on the preferred dimensions for mounting QFN packages, see the following Application Note at http://www.amkor.com/products/notes_papers/MLFAppNote.pdf.
- Pinned vias for thermal conduction are not required for the low power PSoC device.

CY3207ISSP In-System Serial Programmer (ISSP)

The CY3207ISSP is a production programmer. It includes protection circuitry and an industrial case that is more robust than the MiniProg in a production programming environment.

Note that CY3207ISSP needs special software and is not compatible with PSoC Programmer. The kit includes:

- CY3207 Programmer Unit
- PSoC ISSP Software CD
- 110 ~ 240 V Power Supply, Euro-Plug Adapter
- USB 2.0 Cable

Accessories (Emulation and Programming)

Table 40. Emulation and Programming Accessories

Part Number	Pin Package	Flex-Pod Kit ^[75]	Foot Kit ^[76]	Adapter ^[77]
CY8C20236A-24LKXI	16-pin QFN (No E-Pad)	CY3250-20246QFN	CY3250-20246QFN-POD	See note 74
CY8C20246A-24LKXI	16-pin QFN (No E-Pad)	CY3250-20246QFN	CY3250-20246QFN-POD	See note 77
CY8C20246AS-24LKXI	16-pin QFN (No E-Pad)	Not Supported		
CY8C20336A-24LQXI	24-pin QFN	CY3250-20346QFN	CY3250-20346QFN-POD	See note 74
CY8C20346A-24LQXI	24-pin QFN	CY3250-20346QFN	CY3250-20346QFN-POD	See note 77
CY8C20346AS-24LQXI	24-pin QFN	Not Supported		
CY8C20396A-24LQXI	24-pin QFN	Not Supported		
CY8C20436A-24LQXI	32-pin QFN	CY3250-20466QFN	CY3250-20466QFN-POD	See note 74
CY8C20446A-24LQXI	32-pin QFN	CY3250-20466QFN	CY3250-20466QFN-POD	See note 77
CY8C20446AS-24LQXI	32-pin QFN	Not Supported		
CY8C20466A-24LQXI	32-pin QFN	CY3250-20466QFN	CY3250-20466QFN-POD	See note 77
CY8C20466AS-24LQXI	32-pin QFN	Not Supported		
CY8C20496A-24LQXI	32-pin QFN	Not Supported		
CY8C20536A-24PVXI	48-pin SSOP	CY3250-20566	CY3250-20566-POD	See note 77
CY8C20546A-24PVXI	48-pin SSOP	CY3250-20566	CY3250-20566-POD	See note 77
CY8C20566A-24PVXI	48-pin SSOP	CY3250-20566	CY3250-20566-POD	See note 77

Third Party Tools

Several tools have been specially designed by third-party vendors to accompany PSoC devices during development and production. Specific details for each of these tools can be found at <http://www.cypress.com> under Documentation > Evaluation Boards.

Build a PSoC Emulator into Your Board

For details on how to emulate your circuit before going to volume production using an on-chip debug (OCD) non-production PSoC device, refer Application Note [Debugging - Build a PSoC Emulator into Your Board – AN2323](#).

Notes

75. Flex-Pod kit includes a practice flex-pod and a practice PCB, in addition to two flex-pods.

76. Foot kit includes surface mount feet that can be soldered to the target PCB.

77. Programming adapter converts non-DIP package to DIP footprint. Specific details and ordering information for each of the adapters can be found at <http://www.emulation.com>.

Ordering Information

Table 41 lists the CY8C20XX6A/S PSoC devices' key package features and ordering codes.

Table 41. PSoC Device Key Features and Ordering Information

Package	Ordering Code	Flash (Bytes)	SRAM (Bytes)	CapSense Blocks	Digital I/O Pins	Analog Inputs ^[78]	XRES Pin	USB	ADC
16-pin (3 × 3 × 0.6 mm) QFN (no E-Pad)	CY8C20236A-24LKXI	8 K	1 K	1	13	13	Yes	No	Yes
16-pin (3 × 3 × 0.6 mm) QFN (no E-Pad) (Tape and Reel)	CY8C20236A-24LKXIT	8 K	1 K	1	13	13	Yes	No	Yes
16-pin (3 × 3 × 0.6 mm) QFN (no E-Pad)	CY8C20246A-24LKXI	16 K	2 K	1	13	13	Yes	No	Yes
16-pin (3 × 3 × 0.6 mm) QFN (no E-Pad)	CY8C20246AS-24LKXI	16 K	2 K	1	13	13	Yes	No	Yes
16-pin (3 × 3 × 0.6 mm) QFN (no E-Pad) (Tape and Reel)	CY8C20246A-24LKXIT	16 K	2 K	1	13	13	Yes	No	Yes
16-pin (3 × 3 × 0.6 mm) QFN (no E-Pad) (Tape and Reel)	CY8C20246AS-24LKXIT	16 K	2 K	1	13	13	Yes	No	Yes
24-pin (4 × 4 × 0.6 mm) QFN	CY8C20336A-24LQXI	8 K	1 K	1	20	20	Yes	No	Yes
24-pin (4 × 4 × 0.6 mm) QFN (Tape and Reel)	CY8C20336A-24LQXIT	8 K	1 K	1	20	20	Yes	No	Yes
24-pin (4 × 4 × 0.6 mm) QFN	CY8C20346A-24LQXI	16 K	2 K	1	20	20	Yes	No	Yes
24-pin (4 × 4 × 0.6 mm) QFN	CY8C20346AS-24LQXI	16 K	2 K	1	20	20	Yes	No	Yes
24-pin (4 × 4 × 0.6 mm) QFN (Tape and Reel)	CY8C20346A-24LQXIT	16 K	2 K	1	20	20	Yes	No	Yes
24-pin (4 × 4 × 0.6 mm) QFN (Tape and Reel)	CY8C20346AS-24LQXIT	16 K	2 K	1	20	20	Yes	No	Yes
24-pin (4 × 4 × 0.6 mm) QFN	CY8C20396A-24LQXI	16 K	2 K	1	19	19	Yes	Yes	Yes
24-pin (4 × 4 × 0.6 mm) QFN (Tape and Reel)	CY8C20396A-24LQXIT	16 K	2 K	1	19	19	Yes	Yes	Yes
32-pin (5 × 5 × 0.6 mm) QFN	CY8C20436A-24LQXI	8 K	1 K	1	28	28	Yes	No	Yes
32-pin (5 × 5 × 0.6 mm) QFN (Tape and Reel)	CY8C20436A-24LQXIT	8 K	1 K	1	28	28	Yes	No	Yes
32-pin (5 × 5 × 0.6 mm) QFN	CY8C20446A-24LQXI	16 K	2 K	1	28	28	Yes	No	Yes
32-pin (5 × 5 × 0.6 mm) QFN	CY8C20446AS-24LQXI	16 K	2 K	1	28	28	Yes	No	Yes
32-pin (5 × 5 × 0.6 mm) QFN (Tape and Reel)	CY8C20446A-24LQXIT	16 K	2 K	1	28	28	Yes	No	Yes
32-pin (5 × 5 × 0.6 mm) QFN (Tape and Reel)	CY8C20446AS-24LQXIT	16 K	2 K	1	28	28	Yes	No	Yes
32-pin (5 × 5 × 0.6 mm) QFN	CY8C20466A-24LQXI	32 K	2 K	1	28	28	Yes	No	Yes
32-pin (5 × 5 × 0.6 mm) QFN	CY8C20466AS-24LQXI	32 K	2 K	1	28	28	Yes	No	Yes
32-pin (5 × 5 × 0.6 mm) QFN (Tape and Reel)	CY8C20466A-24LQXIT	32 K	2 K	1	28	28	Yes	No	Yes
32-pin (5 × 5 × 0.6 mm) QFN (Tape and Reel)	CY8C20466AS-24LQXIT	32 K	2 K	1	28	28	Yes	No	Yes
32-pin (5 × 5 × 0.6 mm) QFN	CY8C20496A-24LQXI	16 K	2 K	1	25	25	Yes	Yes	Yes
32-pin (5 × 5 × 0.6 mm) QFN (Tape and Reel)	CY8C20496A-24LQXIT	16 K	2 K	1	25	25	Yes	Yes	Yes

Notes

78. Dual-function Digital I/O Pins also connect to the common analog mux.

79. Not Recommended for New Designs.

Table 41. PSoC Device Key Features and Ordering Information (continued)

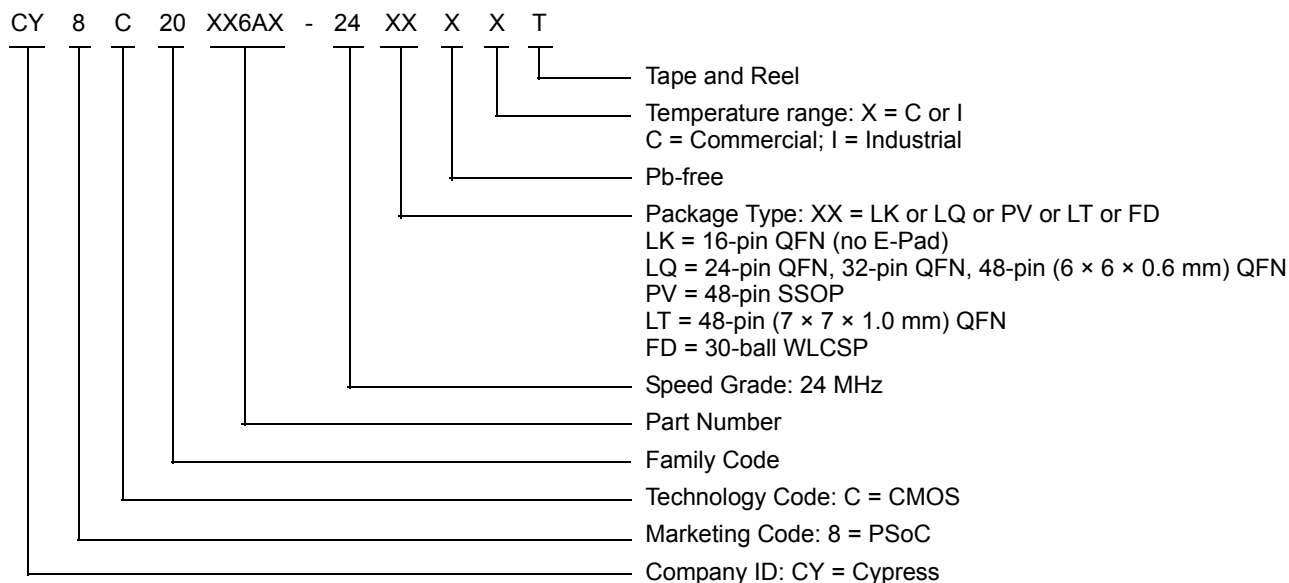
Package	Ordering Code	Flash (Bytes)	SRAM (Bytes)	CapSense Blocks	Digital I/O Pins	Analog Inputs ^[78]	XRES Pin	USB	ADC
24-pin (4 × 4 × 0.6 mm) QFN	CY8C20346AS-24LQXI	16 K	2 K	1	20	20	Yes	No	Yes
24-pin (4 × 4 × 0.6 mm) QFN (Tape and Reel)	CY8C20346AS-24LQXIT	16 K	2 K	1	20	20	Yes	No	Yes
32-pin (5 × 5 × 0.6 mm) QFN	CY8C20446AS-24LQXI	16 K	2 K	1	28	28	Yes	No	Yes
32-pin (5 × 5 × 0.6 mm) QFN (Tape and Reel)	CY8C20446AS-24LQXIT	16 K	2 K	1	28	28	Yes	No	Yes
32-pin (5 × 5 × 0.6 mm) QFN	CY8C20466AS-24LQXI	32 K	2 K	1	28	28	Yes	No	Yes
32-pin (5 × 5 × 0.6 mm) QFN (Tape and Reel)	CY8C20466AS-24LQXIT	32 K	2 K	1	28	28	Yes	No	Yes
48-pin (6 × 6 × 0.6 mm) QFN	CY8C20666AS-24LQXI	32 K	2 K	1	36	36	Yes	Yes	Yes
48-pin (6 × 6 × 0.6 mm) QFN (Tape and Reel)	CY8C20666AS-24LQXIT	32 K	2 K	1	36	36	Yes	Yes	Yes
48-pin (7 × 7 × 1.0 mm) QFN ^[79]	CY8C20666AS-24LTXI ^[79]	32 K	2 K	1	36	36	Yes	Yes	Yes
48-pin (7 × 7 × 1.0 mm) QFN (Tape and Reel) ^[79]	CY8C20666AS-24LTXIT ^[79]	32 K	2 K	1	36	36	Yes	Yes	Yes
48-pin (6 × 6 × 0.6 mm) QFN	CY8C20646AS-24LQXI	16 K	2 K	1	36	36	Yes	Yes	Yes
48-pin (6 × 6 × 0.6 mm) QFN (Tape and Reel)	CY8C20646AS-24LQXIT	16 K	2 K	1	36	36	Yes	Yes	Yes
48-pin (7 × 7 × 1.0 mm) QFN ^[79]	CY8C20646AS-24LTXI ^[79]	16 K	2 K	1	36	36	Yes	Yes	Yes
48-pin (7 × 7 × 1.0 mm) QFN (Tape and Reel) ^[79]	CY8C20646AS-24LTXIT ^[79]	16 K	2 K	1	36	36	Yes	Yes	Yes

Notes

78. Dual-function Digital I/O Pins also connect to the common analog mux.

79. Not Recommended for New Designs.

Ordering Code Definitions



3. DoubleTimer0 ISR

■ Problem Definition

When programmable timer 0 is used in “one-shot” mode by setting bit 1 of register 0,B0h (PT0_CFG), and the timer interrupt is used to wake the device from sleep, the interrupt service routine (ISR) may be executed twice.

■ Parameters Affected

No datasheet parameters are affected.

■ Trigger Condition(S)

Triggered by enabling one-shot mode in the timer, and using the timer to wake from sleep mode.

■ Scope of Impact

The ISR may be executed twice.

■ Workaround

In the ISR, firmware should clear the one-shot bit with a statement such as “`and reg[B0h], FDh`”

■ Fix Status

Will not be fixed

■ Changes

None

4. Missed GPIO Interrupt

■ Problem Definition

When in sleep mode, if a GPIO interrupt happens simultaneously with a Timer0 or Sleep Timer interrupt, the GPIO interrupt may be missed, and the corresponding GPIO ISR not run.

■ Parameters Affected

No datasheet parameters are affected.

■ Trigger Condition(S)

Triggered by enabling sleep mode, then having GPIO interrupt occur simultaneously with a Timer 0 or Sleep Timer interrupt.

■ Scope of Impact

The GPIO interrupt service routine will not be run.

■ Workaround

The system should be architected such that a missed GPIO interrupt may be detected. For example, if a GPIO is used to wake the system to perform some function, the system should detect if the function is not performed, and re-issue the GPIO interrupt.

Alternatively, if a GPIO interrupt is required to wake the system, then firmware should disable the Sleep Timer and Timer0.

Alternatively, the ISR's for Sleep Timer and Timer0 should manually check the state of the GPIO to determine if the host system has attempted to generate a GPIO interrupt.

■ Fix Status

Will not be fixed

■ Changes

None

Document History Page

Document Title: CY8C20XX6A/S, 1.8 V Programmable CapSense® Controller with SmartSense™ Auto-tuning 1–33 Buttons, 0–6 Sliders Document Number: 001-54459				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	2737924	SNV	07/14/2009	New silicon and document
*A	2764528	MATT	09/16/2009	Updated AC Chip Level Specifications Updated ADC User Module Electrical Specifications table Added Note 5. Added SR _{POWER_UP} parameter. Updated Ordering information. Updated Capacitance on Crystal Pins
*B	2803229	VZD	11/10/2009	Added “ Contents ” on page 4. Added Note 6 on page 20. Edited Features section to include reference to Incremental ADC.
*C	2846083	DST / KEJO	01/12/2010	Updated “ AC Programming Specifications ” on page 31 per CDT 56531. Updated Idd typical values in “ DC Chip-Level Specifications ” on page 21. Added 30-pin WLCSP pin and package details. Added Contents on page 2.
*D	2935141	KEJO/ISW / SSHH	03/05/2010	Updated “ Features ” on page 1. Added “ SmartSense ” on page 5. Updated “ PSoC® Functional Overview ” on page 5. Removed SNR statement regarding on page 4 (Analog Multiplexer section). Updated Additional System Resources on page 6 with the I2C enhanced slave interface point. Removed references to “system level” in “ Designing with PSoC Designer ” on page 9. Changed TC CLK and TC DATA to ISSP CLK and ISSP DATA respectively in all the pinouts. Modified notes in Pinouts. Updated 30-ball pin diagram. Removed IMO frequency trim options diagram in “ Electrical Specifications ” on page 20. Updated and formatted values in DC and AC specifications. Updated Ordering information table. Updated 48-pin SSOP package diagram. Added 30-Ball WLCSP package spec 001-50669. Removed AC Analog Mux Bus Specifications section. Added SPI Master and Slave mode diagrams. Modified Definition for Timing for Fast/Standard Mode on the I2C Bus on page 28 . Updated “ Thermal Impedances ” on page 38. Combined Development Tools with “ Development Tool Selection ” on page 39. Removed references to “system level”. Updated “ Evaluation Tools ” on page 39. Added “ Ordering Code Definitions ” on page 43. Updated “ Acronyms ” on page 44. Added Glossary and “ Reference Documents ” on page 44. Changed datasheet status from Preliminary to Final
*E	3043291	SAAC	09/30/2010	Change: Added the line “Supports SmartSense” in the “Low power CapSense® block” bullet in the Features section. Impact: Helps to know that this part has the feature of Auto Tuning. Change: Replaced pod MPNs. Areas affected: Foot kit column of table 37. Change: Template and Styles update. Areas affected: Entire datasheet. Impact: Datasheet adheres to Cypress standards.
*F	3071632	JPX	10/26/2010	In Table 36 on page 34 , modified t _{LOW} and t _{HIGH} min values to 42. Updated t _{SS_HIGH} min value to 50; removed max value.

Document History Page (continued)

Document Title: CY8C20XX6A/S, 1.8 V Programmable CapSense® Controller with SmartSense™ Auto-tuning 1–33 Buttons, 0–6 Sliders Document Number: 001-54459				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
*G	3247491	TTO / JPM / ARVM / BVI	06/16/2011	Add 4 new parameters to Table 14 on page 22 , and 2 new parameters to Table 15 on page 23 . Changed Typ values for the following parameters: I_{DD24} , I_{DD12} , I_{DD6} , V_{OSLPC} . Added footnote # 49 and referred it to pin numbers 1, 14, 15, 42, and 43 under Table 10 on page 19 . Added footnote # 53 and referred it to parameter V_{IOZ} under Table 11 on page 20 . Added “ t_{JIT_IMO} ” parameter to Table 27 on page 28 . Included footnote # 69 and added reference to t_{JIT_IMO} specification under Table 27 on page 28 . Updated Solder Reflow Specifications on page 38 as per specs 25-00090 and 25-00103. I_{SB0} Max value changed from 0.5 μA to 1.1 μA in Table 13 on page 21 . Added Table 26 on page 27 . Updated part numbers for “SmartSense_EMC” enabled CapSense controller.
*H	3367332	BTK / SSHH / JPM / TTO / VMAD	09/09/2011	Added parameter “ t_{OS} ” to Table 27 on page 28 . Added parameter “ I_{SBI2C} ” to Table 13 on page 21 . Added Table 24 on page 27 . Added Table 25 on page 27 . Replaced text “Port 2 or 3 pins” with “Port 2 or 3 or 4 pins” in Table 14 , Table 15 , Table 16 , and Table 28 .
*I	3371807	MATT	09/30/2011	Updated Packaging Information (Updated the next revision package outline for Figure 21 , Figure 24 and included a new package outline Figure 26). Updated Ordering Information (Added new part numbers CY8C20636A-24LQXI, CY8C20636A-24LQXIT, CY8C20646A-24LQXI, CY8C20646A-24LQXIT, CY8C20666A-24LQXI, CY8C20666A-24LQXIT, CY8C20666AS-24LQXI, CY8C20666AS-24LQXIT, CY8C20646AS-24LQXI and CY8C20646AS-24LQXIT). Updated to new template.
*J	3401666	MATT	10/11/2011	No technical updates.
*K	3414479	KPOL	10/19/2011	Removed clock stretching feature on page 1. Removed I ² C enhanced slave interface point from Additional System Resources .
*L	3452591	BVI / UDYG	12/01/2011	Changed document title. Updated DC Chip-Level Specifications table. Updated Solder Reflow Specifications section. Updated Getting Started and Designing with PSoC Designer sections. Included Development Tools section. Updated Software under Development Tool Selection section.
*M	3473330	ANBA	12/22/2011	Updated DC Chip-Level Specifications under Electrical Specifications (updated maximum value of I_{SB0} parameter from 1.1 μA to 1.05 μA).
*N	3587003	DST	04/16/2012	Added note for WLCSP package on page 1. Added Sensing inputs to pin table captions. Updated Conditions for DC Reference Buffer Specifications . Updated t_{JIT_IMO} description in AC Chip-Level Specifications . Added note for $t_{VDDWAIT}$, $t_{VDDXRES}$, t_{ACQ} , and $t_{XRESINI}$ specs. Removed WLCSP package outline.
*O	3638569	BVI	06/06/2012	Updated F_{SCLK} parameter in the Table 36 , “ SPI Slave AC Specifications ,” on page 34. Changed t_{OUT_HIGH} to t_{OUT_H} in Table 35 , “ SPI Master AC Specifications ,” on page 33. Updated package diagram 001-57280 to *C revision.