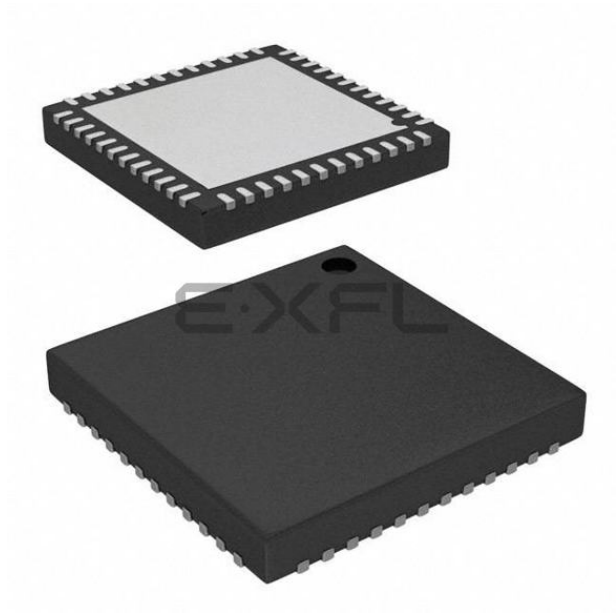

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What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Active
Applications	Capacitive Sensing
Core Processor	M8C
Program Memory Type	FLASH (8kB)
Controller Series	CY8C20xx6A
RAM Size	1K x 8
Interface	I²C, SPI
Number of I/O	36
Voltage - Supply	1.71V ~ 5.5V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	48-UFQFN Exposed Pad
Supplier Device Package	48-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c20636a-24lqxi

More Information

Cypress provides a wealth of data at www.cypress.com to help you to select the right PSoC device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the knowledge base article KBA92181, Resources Available for CapSense® Controllers. Following is an abbreviated list for CapSense devices:

- Overview: CapSense Portfolio, CapSense Roadmap
- Product Selectors: CapSense, CapSense Plus, CapSense Express, PSoC3 with CapSense, PSoC5 with CapSense, PSoC4. In addition, PSoC Designer offers a device selection tool at the time of creating a new project.
- Application notes: Cypress offers CapSense application notes covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with CapSense are:
  - AN64846: Getting Started With CapSense
  - AN73034: CY8C20xx6A/H/AS CapSense® Design Guide
  - AN2397: CapSense® Data Viewing Tools
- Technical Reference Manual (TRM):
  - PSoC® CY8C20xx6A/AS/L Family Technical Reference Manual
- Development Kits:
  - CY3280-20x66 Universal CapSense Controller Kit features a predefined control circuitry and plug-in hardware to make prototyping and debugging easy. Programming and I2C-to-USB Bridge hardware are included for tuning and data acquisition.
  - CY3280-BMM Matrix Button Module Kit consists of eight CapSense sensors organized in a 4x4 matrix format to form 16 physical buttons and eight LEDs. This module connects to any CY3280 Universal CapSense Controller Board, including CY3280-20x66 Universal CapSense Controller.
  - CY3280-BSM Simple Button Module Kit consists of ten CapSense buttons and ten LEDs. This module connects to any CY3280 Universal CapSense Controller Board, including CY3280-20x66 Universal CapSense Controller.

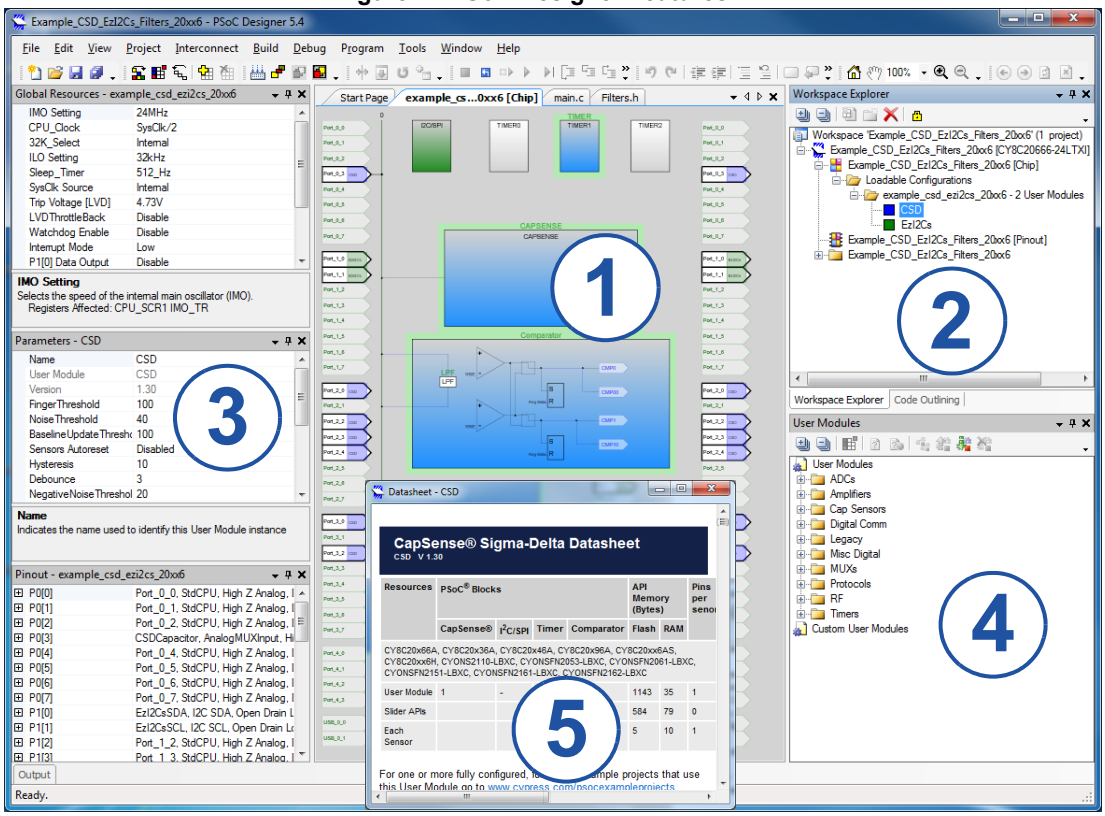
The CY3217-MiniProg1 and CY8CKIT-002 PSoC® MiniProg3 device provides an interface for flash programming.

PSoC Designer

PSoC Designer is a free Windows-based Integrated Design Environment (IDE). It enables concurrent hardware and firmware design of systems based on CapSense (see Figure 1). With PSoC Designer, you can:

1. Drag and drop User Modules to build your hardware system design in the main design workspace
2. Codesign your application firmware with the PSoC hardware, using the PSoC Designer IDE C compiler
3. Configure User Module
4. Explore the library of user modules
5. Review user module datasheets

Figure 1. PSoC Designer Features



PSoC® Functional Overview

The PSoC family consists of on-chip controller devices, which are designed to replace multiple traditional microcontroller unit (MCU)-based components with one, low cost single-chip programmable component. A PSoC device includes configurable analog and digital blocks, and programmable interconnect. This architecture allows the user to create customized peripheral configurations, to match the requirements of each individual application. Additionally, a fast CPU, Flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts.

The architecture for this device family, as shown in the Logic Block Diagram on page 2, consists of three main areas:

- The Core
- CapSense Analog System
- System Resources (including a full-speed USB port).

A common, versatile bus allows connection between I/O and the analog system.

Each CY8C20XX6A/S PSoC device includes a dedicated CapSense block that provides sensing and scanning control circuitry for capacitive sensing applications. Depending on the PSoC package, up to 36 GPIO are also included. The GPIO provides access to the MCU and analog mux.

PSoC Core

The PSoC Core is a powerful engine that supports a rich instruction set. It encompasses SRAM for data storage, an interrupt controller, sleep and watchdog timers, and IMO and ILO. The CPU core, called the M8C, is a powerful processor with speeds up to 24 MHz. The M8C is a 4-MIPS, 8-bit Harvard-architecture microprocessor.

CapSense System

The analog system contains the capacitive sensing hardware. Several hardware algorithms are supported. This hardware performs capacitive sensing and scanning without requiring external components. The analog system is composed of the CapSense PSoC block and an internal 1 V or 1.2 V analog reference, which together support capacitive sensing of up to 33 inputs [2]. Capacitive sensing is configurable on each GPIO pin. Scanning of enabled CapSense pins are completed quickly and easily across multiple ports.

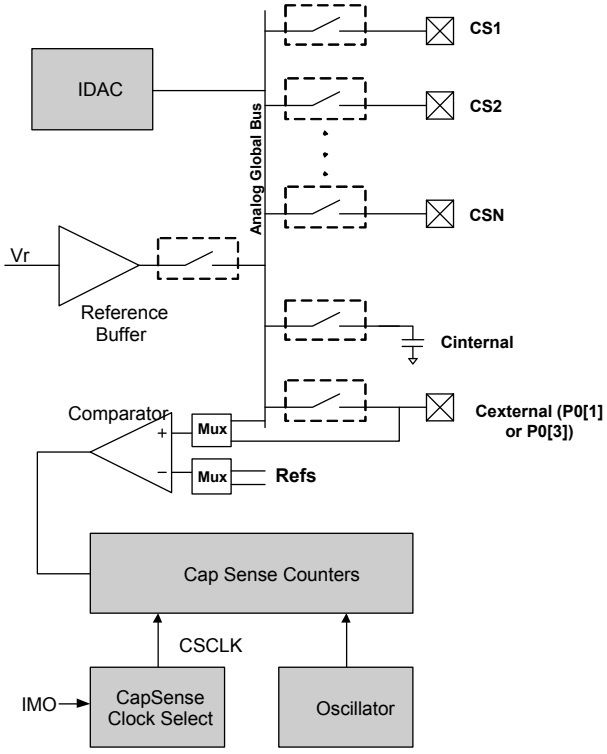
SmartSense

SmartSense is an innovative solution from Cypress that removes manual tuning of CapSense applications. This solution is easy to use and provides a robust noise immunity. It is the only auto-tuning solution that establishes, monitors, and maintains all required tuning parameters. SmartSense allows engineers to go from prototyping to mass production without re-tuning for manufacturing variations in PCB and/or overlay material properties.

SmartSense_EMC

In addition to the SmartSense auto tuning algorithm to remove manual tuning of CapSense applications, SmartSense_EMC user module incorporates a unique algorithm to improve robustness of capacitive sensing algorithm/circuit against high frequency conducted and radiated noise. Every electronic device must comply with specific limits for radiated and conducted external noise and these limits are specified by regulatory bodies (for example, FCC, CE, U/L and so on). A very good PCB layout design, power supply design and system design is a mandatory for a product to pass the conducted and radiated noise tests. An ideal PCB layout, power supply design or system design is not often possible because of cost and form factor limitations of the product. SmartSense_EMC with superior noise immunity is well suited and handy for such applications to pass radiated and conducted noise test.

Figure 2. CapSense System Block Diagram



Note
2. 36 GPIOs = 33 pins for capacitive sensing + 2 pins for I^2C + 1 pin for modulator capacitor.

Getting Started

The quickest way to understand PSoC silicon is to read this datasheet and then use the PSoC Designer Integrated Development Environment (IDE). This datasheet is an overview of the PSoC integrated circuit and presents specific pin, register, and electrical specifications.

For in depth information, along with detailed programming details, see the Technical Reference Manual for the CY8C20XX6A/S PSoC devices.

For up-to-date ordering, packaging, and electrical specification information, see the latest PSoC device datasheets on the web at www.cypress.com/psoc.

CapSense Design Guides

Design Guides are an excellent introduction to the wide variety of possible CapSense designs. They are located at www.cypress.com/go/CapSenseDesignGuides.

Refer Getting Started with CapSense design guide for information on CapSense design and CY8C20XX6A/H/AS CapSense® Design Guide for specific information on CY8C20XX6A/AS CapSense controllers.

Silicon Errata

Errata documents known issues with silicon including errata trigger conditions, scope of impact, available workarounds and silicon revision applicability. Refer to Silicon Errata for the PSoC® CY8C20x36A/46A/66A/96A/46AS/66AS/36H/46H families available at http://www.cypress.com/?rID=56239 for errata information on CY8C20xx6A/AS/H family of device. Compare errata document with datasheet for a complete functional description of device.

Development Kits

PSoC Development Kits are available online from and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

Training

Free PSoC technical training (on demand, webinars, and workshops), which is available online via www.cypress.com, covers a wide variety of topics and skill levels to assist you in your designs.

CYPros Consultants

Certified PSoC consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC consultant go to the CYPros Consultants web site.

Solutions Library

Visit our growing library of solution focused designs. Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

Technical Support

Technical support – including a searchable Knowledge Base articles and technical forums – is also available online. If you cannot find an answer to your question, call our Technical Support hotline at 1-800-541-4736.

Pinouts

The CY8C20XX6A/S PSoC device is available in a variety of packages, which are listed and illustrated in the following tables. Every port pin (labeled with a “P”) is capable of Digital I/O and connection to the common analog bus. However, V_{SS}, V_{DD}, and XRES are not capable of Digital I/O.

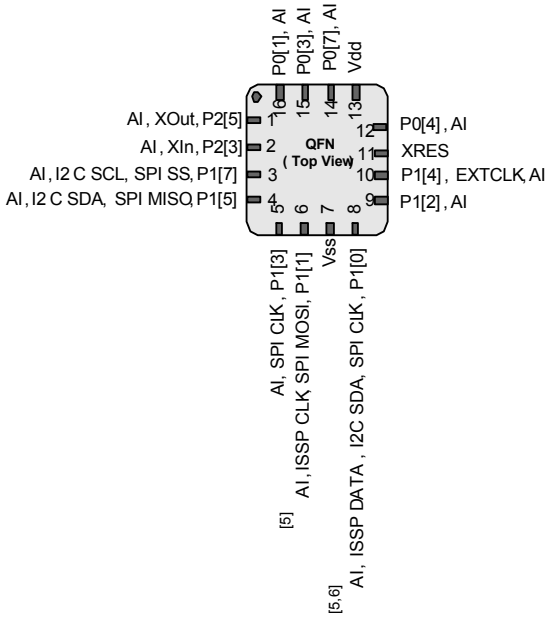
16-pin QFN (10 Sensing Inputs)[3, 4]

Table 1. Pin Definitions – CY8C20236A, CY8C20246A, CY8C20246AS PSoC Device

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I	P2[5]	Crystal output (XOut)
2	I/O	I	P2[3]	Crystal input (XIn)
3	IOHR	I	P1[7]	I^2C SCL, SPI SS
4	IOHR	I	P1[5]	I^2C SDA, SPI MISO
5	IOHR	I	P1[3]	SPI CLK
6	IOHR	I	P1[1]	ISSP CLK[5], I^2C SCL, SPI MOSI
7	Power		V_{SS}	Ground connection[7]
8	IOHR	I	P1[0]	ISSP DATA[5], I^2C SDA, SPI CLK[6]
9	IOHR	I	P1[2]	
10	IOHR	I	P1[4]	Optional external clock (EXTCLK)
11	Input		XRES	Active high external reset with internal pull-down
12	IOH	I	P0[4]	
13	Power		V_{DD}	Supply voltage
14	IOH	I	P0[7]	
15	IOH	I	P0[3]	Integrating input
16	IOH	I	P0[1]	Integrating input

LEGEND A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output.

Figure 3. CY8C20236A, CY8C20246A, CY8C20246AS



Notes
3. 13 GPIOs = 10 pins for capacitive sensing + 2 pins for I2C + 1 pin for modulation capacitor.
4. No Center Pad.
5. On power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to high impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the I2C bus. Use alternate pins if you encounter issues.
6. Alternate SPI clock.
7. All VSS pins should be brought out to one common GND plane.

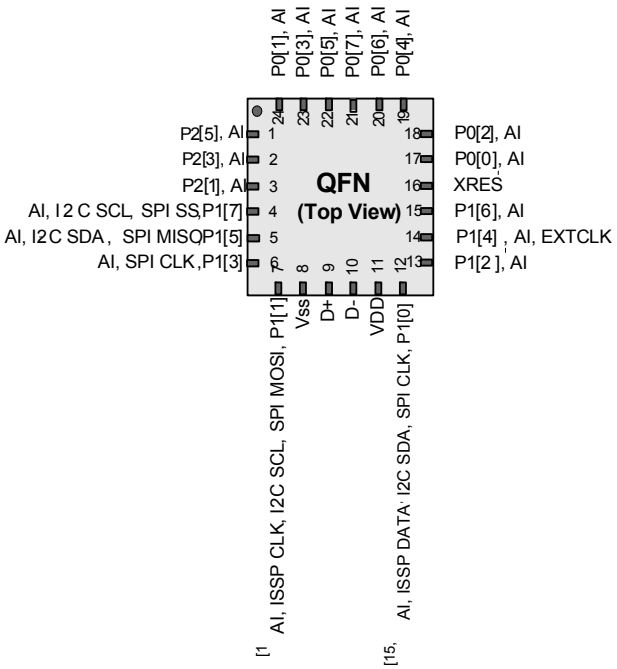
24-pin QFN (15 Sensing Inputs (With USB)) [13]

Table 3. Pin Definitions – CY8C20396A [14]

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I	P2[5]	
2	I/O	I	P2[3]	
3	I/O	I	P2[1]	
4	IOHR	I	P1[7]	I^2C SCL, SPI SS
5	IOHR	I	P1[5]	I^2C SDA, SPI MISO
6	IOHR	I	P1[3]	SPI CLK
7	IOHR	I	P1[1]	ISSP CLK[15], I^2C SCL, SPI MOSI
8	Power		V_{SS}	Ground[17]
9	I/O	I	D+	USB D+
10	I/O	I	D-	USB D-
11	Power		V_{DD}	Supply
12	IOHR	I	P1[0]	ISSP DATA[15], I^2C SDA, SPI CLK[16]
13	IOHR	I	P1[2]	
14	IOHR	I	P1[4]	Optional external clock input (EXTCLK)
15	IOHR	I	P1[6]	
16	RESET INPUT		XRES	Active high external reset with internal pull-down
17	IOH	I	P0[0]	
18	IOH	I	P0[2]	
19	IOH	I	P0[4]	
20	IOH	I	P0[6]	
21	IOH	I	P0[7]	
22	IOH	I	P0[5]	
23	IOH	I	P0[3]	Integrating input
24	IOH	I	P0[1]	Integrating input
CP	Power		V_{SS}	Center pad must be connected to Ground

LEGEND I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output

Figure 5. CY8C20396A



Notes
13. 20 GPIOs = 15 pins for capacitive sensing + 2 pins for I2C + 2 pins for USB + 1 pin for modulation capacitor.
14. The center pad (CP) on the QFN package must be connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.
15. On power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to high impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the I2C bus. Use alternate pins if you encounter issues.
16. Alternate SPI clock.
17. All VSS pins should be brought out to one common GND plane.

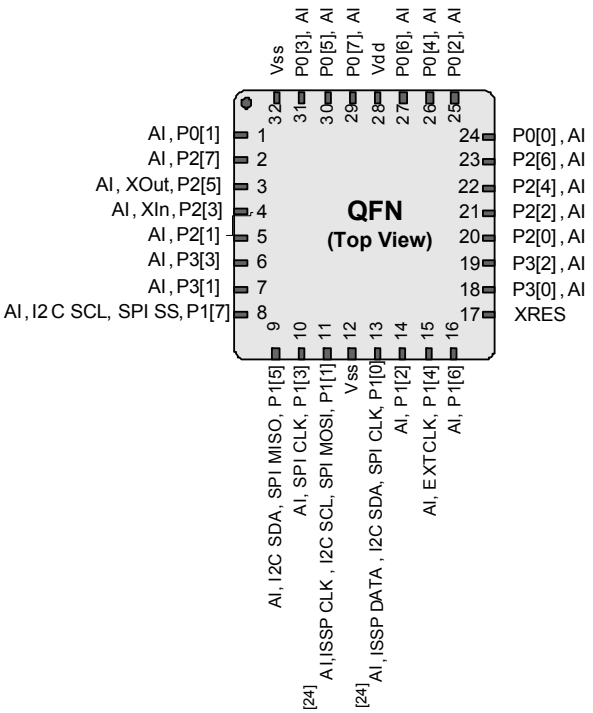
32-pin QFN (25 Sensing Inputs) [22]

Table 5. Pin Definitions – CY8C20436A, CY8C20446A, CY8C20446AS, CY8C20466A, CY8C20466AS[23]

Pin No.	Type		Name	Description
	Digital	Analog		
1	IOH	I	P0[1]	Integrating input
2	I/O	I	P2[7]	
3	I/O	I	P2[5]	Crystal output (XOut)
4	I/O	I	P2[3]	Crystal input (XIn)
5	I/O	I	P2[1]	
6	I/O	I	P3[3]	
7	I/O	I	P3[1]	
8	IOHR	I	P1[7]	I^2C SCL, SPI SS
9	IOHR	I	P1[5]	I^2C SDA, SPI MISO
10	IOHR	I	P1[3]	SPI CLK.
11	IOHR	I	P1[1]	ISSP CLK[24], I^2C SCL, SPI MOSI.
12	Power		V_{SS}	Ground connection[26]
13	IOHR	I	P1[0]	ISSP DATA[24], I^2C SDA, SPI CLK[25]
14	IOHR	I	P1[2]	
15	IOHR	I	P1[4]	Optional external clock input (EXTCLK)
16	IOHR	I	P1[6]	
17	Input		XRES	Active high external reset with internal pull-down
18	I/O	I	P3[0]	
19	I/O	I	P3[2]	
20	I/O	I	P2[0]	
21	I/O	I	P2[2]	
22	I/O	I	P2[4]	
23	I/O	I	P2[6]	
24	IOH	I	P0[0]	
25	IOH	I	P0[2]	
26	IOH	I	P0[4]	
27	IOH	I	P0[6]	
28	Power		V_{DD}	Supply voltage
29	IOH	I	P0[7]	
30	IOH	I	P0[5]	
31	IOH	I	P0[3]	Integrating input
32	Power		V_{SS}	Ground connection[26]
CP	Power		V_{SS}	Center pad must be connected to ground

LEGEND A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output.

Figure 7. CY8C20436A, CY8C20446A, CY8C20446AS, CY8C20466A, CY8C20466AS



Notes

22. 28 GPIOs = 25 pins for capacitive sensing + 2 pins for I2C + 1 pin for modulation capacitor.
23. The center pad (CP) on the QFN package must be connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.
24. On power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to high impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the I2C bus. Use alternate pins if you encounter issues.
25. Alternate SPI clock.
26. All VSS pins should be brought out to one common GND plane.

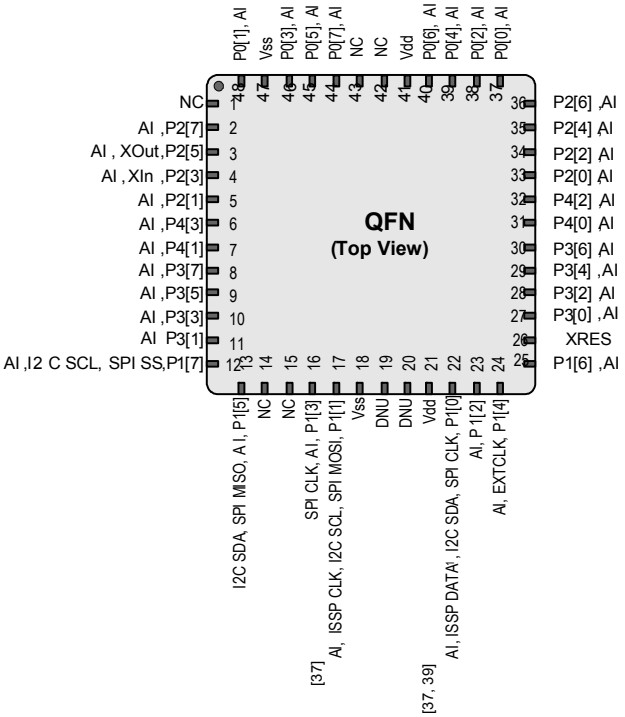
48-pin QFN (33 Sensing Inputs) [36]

Table 8. Pin Definitions – CY8C20636A[37, 38]

Pin No.	Digital	Analog	Name	Description
1			NC	No connection
2	I/O	I	P2[7]	
3	I/O	I	P2[5]	Crystal output (XOut)
4	I/O	I	P2[3]	Crystal input (XIn)
5	I/O	I	P2[1]	
6	I/O	I	P4[3]	
7	I/O	I	P4[1]	
8	I/O	I	P3[7]	
9	I/O	I	P3[5]	
10	I/O	I	P3[3]	
11	I/O	I	P3[1]	
12	IOHR	I	P1[7]	I^2C SCL, SPI SS
13	IOHR	I	P1[5]	I^2C SDA, SPI MISO
14			NC	No connection
15			NC	No connection
16	IOHR	I	P1[3]	SPI CLK
17	IOHR	I	P1[1]	ISSP CLK[37], I^2C SCL, SPI MOSI
18	Power		V_{SS}	Ground connection[40]
19			DNU	
20			DNU	
21	Power		V_{DD}	Supply voltage
22	IOHR	I	P1[0]	ISSP DATA[37], I^2C SDA, SPI CLK[39]
23	IOHR	I	P1[2]	
24	IOHR	I	P1[4]	Optional external clock input (EXTCLK)
25	IOHR	I	P1[6]	
26	Input		XRES	Active high external reset with internal pull-down
27	I/O	I	P3[0]	
28	I/O	I	P3[2]	
29	I/O	I	P3[4]	
30	I/O	I	P3[6]	
31	I/O	I	P4[0]	
32	I/O	I	P4[2]	
33	I/O	I	P2[0]	
34	I/O	I	P2[2]	
35	I/O	I	P2[4]	
36	I/O	I	P2[6]	
37	IOH	I	P0[0]	
38	IOH	I	P0[2]	
39	IOH	I	P0[4]	
40	IOH	I	P0[6]	
41	Power		V_{DD}	Supply voltage
42			NC	No connection
43			NC	No connection
44	IOH	I	P0[7]	
45	IOH	I	P0[5]	
46	IOH	I	P0[3]	Integrating input
47	Power		V_{SS}	Ground connection[40]
48	IOH	I	P0[1]	
CP	Power		V_{SS}	Center pad must be connected to ground

LEGEND A = Analog, I = Input, O = Output, NC = No Connection H = 5 mA High Output Drive, R = Regulated Output.

Figure 10. CY8C20636A



Notes

36. 36 GPIOs = 33 pins for capacitive sensing + 2 pins for I2C + 1 pin for modulation capacitor.
37. On power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to high impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the I2C bus. Use alternate pins if you encounter issues.
38. The center pad (CP) on the QFN package must be connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal
39. Alternate SPI clock.
40. All VSS pins should be brought out to one common GND plane.

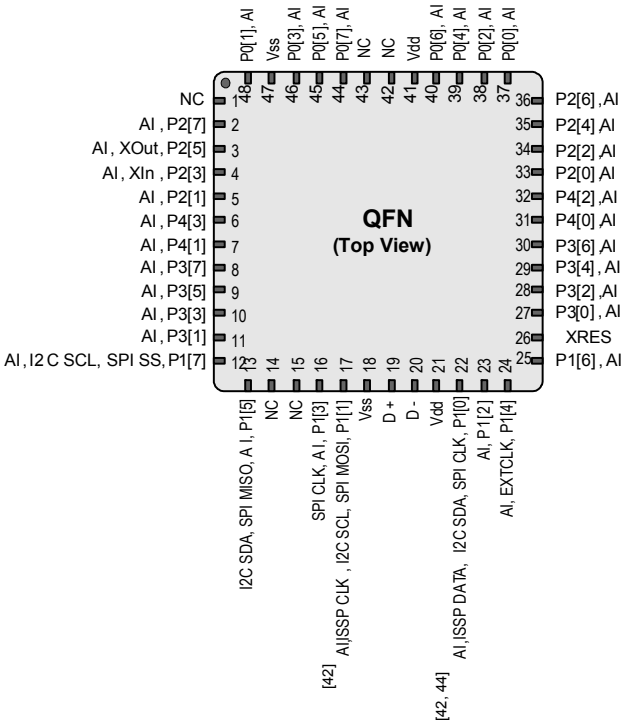
48-pin QFN (33 Sensing Inputs (With USB)) [41]

Table 9. Pin Definitions – CY8C20646A, CY8C20646AS, CY8C20666A, CY8C20666AS [42, 43]

Pin No.	Digital	Analog	Name	Description
1			NC	No connection
2	I/O	I	P2[7]	
3	I/O	I	P2[5]	Crystal output (XOut)
4	I/O	I	P2[3]	Crystal input (XIn)
5	I/O	I	P2[1]	
6	I/O	I	P4[3]	
7	I/O	I	P4[1]	
8	I/O	I	P3[7]	
9	I/O	I	P3[5]	
10	I/O	I	P3[3]	
11	I/O	I	P3[1]	
12	IOHR	I	P1[7]	I^2C SCL, SPI SS
13	IOHR	I	P1[5]	I^2C SDA, SPI MISO
14			NC	No connection
15			NC	No connection
16	IOHR	I	P1[3]	SPI CLK
17	IOHR	I	P1[1]	ISSP CLK[42], I^2C SCL, SPI MOSI
18	Power		V_{SS}	Ground connection[45]
19	I/O		D+	USB D+
20	I/O		D-	USB D-
21	Power		V_{DD}	Supply voltage
22	IOHR	I	P1[0]	ISSP DATA[42], I^2C SDA, SPI CLK[44]
23	IOHR	I	P1[2]	
24	IOHR	I	P1[4]	Optional external clock input (EXTCLK)
25	IOHR	I	P1[6]	
26	Input		XRES	Active high external reset with internal pull-down
27	I/O	I	P3[0]	
28	I/O	I	P3[2]	
29	I/O	I	P3[4]	
30	I/O	I	P3[6]	
31	I/O	I	P4[0]	
32	I/O	I	P4[2]	
33	I/O	I	P2[0]	
34	I/O	I	P2[2]	
35	I/O	I	P2[4]	
36	I/O	I	P2[6]	
37	IOH	I	P0[0]	
38	IOH	I	P0[2]	
39	IOH	I	P0[4]	
40	IOH	I	P0[6]	
41	Power		V_{DD}	Supply voltage
42			NC	No connection
43			NC	No connection
44	IOH	I	P0[7]	
45	IOH	I	P0[5]	
46	IOH	I	P0[3]	Integrating input
47	Power		V_{SS}	Ground connection[45]
48	IOH	I	P0[1]	
CP	Power		V_{SS}	Center pad must be connected to ground

LEGEND A = Analog, I = Input, O = Output, NC = No Connection H = 5 mA High Output Drive, R = Regulated Output.

Figure 11. CY8C20646A, CY8C20646AS, CY8C20666A, CY8C20666AS



Notes

41. 38 GPIOs = 33 pins for capacitive sensing + 2 pins for I2C + 2 pins for USB + 1 pin for modulation capacitor.
42. On Power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to High impedance state. On reset, after XRES de- asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. In both cases, a pull-up resistance on these lines combines with the pull-down resistance (5.6K ohm) and form a potential divider. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the I2C bus. Use alternate pins if you encounter issues.
43. The center pad (CP) on the QFN package must be connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.
44. Alternate SPI clock.
45. All VSS pins should be brought out to one common GND plane.

DC GPIO Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 5.5 V and –40 °C ≤ T_A ≤ 85 °C, 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, or 1.71 V to 2.4 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 C and are for design guidance only.

Table 14. 3.0 V to 5.5 V DC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{PU}	Pull-up resistor	–	4	5.60	8	kΩ
V_{OH1}	High output voltage Port 2 or 3 or 4 pins	I_{OH} ≤ 10 µA, maximum of 10 mA source current in all I/Os	V_{DD} – 0.20	–	–	V
V_{OH2}	High output voltage Port 2 or 3 or 4 pins	I_{OH} = 1 mA, maximum of 20 mA source current in all I/Os	V_{DD} – 0.90	–	–	V
V_{OH3}	High output voltage Port 0 or 1 pins with LDO regulator Disabled for port 1	I_{OH} < 10 µA, maximum of 10 mA source current in all I/Os	V_{DD} – 0.20	–	–	V
V_{OH4}	High output voltage Port 0 or 1 pins with LDO regulator Disabled for port 1	I_{OH} = 5 mA, maximum of 20 mA source current in all I/Os	V_{DD} – 0.90	–	–	V
V_{OH5}	High output voltage Port 1 Pins with LDO Regulator Enabled for 3 V out	I_{OH} < 10 µA, V_{DD} > 3.1 V, maximum of 4 I/Os all sourcing 5 mA	2.85	3.00	3.30	V
V_{OH6}	High output voltage Port 1 pins with LDO regulator enabled for 3 V out	I_{OH} = 5 mA, V_{DD} > 3.1 V, maximum of 20 mA source current in all I/Os	2.20	–	–	V
V_{OH7}	High output voltage Port 1 pins with LDO enabled for 2.5 V out	I_{OH} < 10 µA, V_{DD} > 2.7 V, maximum of 20 mA source current in all I/Os	2.35	2.50	2.75	V
V_{OH8}	High output voltage Port 1 pins with LDO enabled for 2.5 V out	I_{OH} = 2 mA, V_{DD} > 2.7 V, maximum of 20 mA source current in all I/Os	1.90	–	–	V
V_{OH9}	High output voltage Port 1 pins with LDO enabled for 1.8 V out	I_{OH} < 10 µA, V_{DD} > 2.7 V, maximum of 20 mA source current in all I/Os	1.60	1.80	2.10	V
V_{OH10}	High output voltage Port 1 pins with LDO enabled for 1.8 V out	I_{OH} = 1 mA, V_{DD} > 2.7 V, maximum of 20 mA source current in all I/Os	1.20	–	–	V
V_{OL}	Low output voltage	I_{OL} = 25 mA, V_{DD} > 3.3 V, maximum of 60 mA sink current on even port pins (for example, P0[2] and P1[4]) and 60 mA sink current on odd port pins (for example, P0[3] and P1[5])	–	–	0.75	V
V_{IL}	Input low voltage	–	–	–	0.80	V
V_{IH}	Input high voltage	–	2.00	–	–	V
V_H	Input hysteresis voltage	–	–	80	–	mV
I_{IL}	Input leakage (Absolute Value)	–	–	0.001	1	µA
C_{PIN}	Pin capacitance	Package and pin dependent Temp = 25 °C	0.50	1.70	7	pF
$V_{ILLVT3.3}$	Input Low Voltage with low threshold enable set, Enable for Port1	Bit3 of IO_CFG1 set to enable low threshold voltage of Port1 input	0.8	V	–	–
$V_{IHLVT3.3}$	Input High Voltage with low threshold enable set, Enable for Port1	Bit3 of IO_CFG1 set to enable low threshold voltage of Port1 input	1.4	–	–	V
$V_{ILLVT5.5}$	Input Low Voltage with low threshold enable set, Enable for Port1	Bit3 of IO_CFG1 set to enable low threshold voltage of Port1 input	0.8	V	–	–
$V_{IHLVT5.5}$	Input High Voltage with low threshold enable set, Enable for Port1	Bit3 of IO_CFG1 set to enable low threshold voltage of Port1 input	1.7	–	–	V

Table 16. 1.71 V to 2.4 V DC GPIO Specifications *(continued)*

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{IH}	Input high voltage	–	0.65 × V_{DD}	–	–	V
V_H	Input hysteresis voltage	–	–	80	–	mV
I_{IL}	Input leakage (absolute value)	–	–	1	1000	nA
C_{PIN}	Capacitive load on pins	Package and pin dependent temp = 25 °C	0.50	1.70	7	pF

Table 17. DC Characteristics – USB Interface

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{USBI}	USB D+ pull-up resistance	With idle bus	900	–	1575	Ω
R_{USBA}	USB D+ pull-up resistance	While receiving traffic	1425	–	3090	Ω
V_{OHUSB}	Static output high	–	2.8	–	3.6	V
V_{OLUSB}	Static output low	–	–	–	0.3	V
V_{DI}	Differential input sensitivity	–	0.2	–		V
V_{CM}	Differential input common mode range	–	0.8	–	2.5	V
V_{SE}	Single ended receiver threshold	–	0.8	–	2.0	V
C_{IN}	Transceiver capacitance	–	–	–	50	pF
I_{IO}	High Z state data line leakage	On D+ or D- line	–10	–	+10	µA
R_{PS2}	PS/2 pull-up resistance	–	3000	5000	7000	Ω
R_{EXT}	External USB series resistor	In series with each USB pin	21.78	22.0	22.22	Ω

DC Analog Mux Bus Specifications

Table 18 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 18. DC Analog Mux Bus Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{SW}	Switch resistance to common analog bus	–	–	–	800	Ω
R_{GND}	Resistance of initialization switch to V_{SS}	–	–	–	800	Ω

The maximum pin voltage for measuring R_{SW} and R_{GND} is 1.8 V

DC Low Power Comparator Specifications

Table 19 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 19. DC Comparator Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{LPC}	Low power comparator (LPC) common mode	Maximum voltage limited to V_{DD}	0.0	–	1.8	V
I_{LPC}	LPC supply current	–	–	10	40	µA
V_{OSLPC}	LPC voltage offset	–	–	3	30	mV

Table 29. AC Characteristics – USB Data Timings

Symbol	Description	Conditions	Min	Typ	Max	Units
t_{DRATE}	Full speed data rate	Average bit rate	12 – 0.25%	12	12 + 0.25%	MHz
t_{JR1}	Receiver jitter tolerance	To next transition	–18.5	–	18.5	ns
t_{JR2}	Receiver jitter tolerance	To pair transition	–9.0	–	9	ns
t_{DJ1}	FS Driver jitter	To next transition	–3.5	–	3.5	ns
t_{DJ2}	FS Driver jitter	To pair transition	–4.0	–	4.0	ns
t_{FDEOP}	Source jitter for differential transition	To SE0 transition	–2.0	–	5	ns
t_{FEOPT}	Source SE0 interval of EOP	–	160.0	–	175	ns
t_{FEOPR}	Receiver SE0 interval of EOP	–	82.0	–	–	ns
t_{FST}	Width of SE0 interval during differential transition	–	–	–	14	ns

Table 30. AC Characteristics – USB Driver

Symbol	Description	Conditions	Min	Typ	Max	Units
t_{FR}	Transition rise time	50 pF	4	–	20	ns
t_{FF}	Transition fall time	50 pF	4	–	20	ns
t_{FRFM}[70]	Rise/fall time matching	–	90	–	111	%
V_{CRS}	Output signal crossover voltage	–	1.30	–	2.00	V

AC Comparator Specifications

Table 31 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 31. AC Low Power Comparator Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
t_{LPC}	Comparator response time, 50 mV overdrive	50 mV overdrive does not include offset voltage	–	–	100	ns

AC External Clock Specifications

Table 32 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 32. AC External Clock Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{OSCEXT}	Frequency (external oscillator frequency)	–	0.75	–	25.20	MHz
	High period	–	20.60	–	5300	ns
	Low period	–	20.60	–	–	ns
	Power-up IMO to switch	–	150	–	–	µs

Note

70. T_{FRFM} is not met under all conditions. There is a corner case at lower supply voltages, such as those under 3.3 V. This condition does not affect USB communications. Signal integrity tests show an excellent eye diagram at 3.15 V.

Table 36. SPI Slave AC Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{SCLK}	SCLK clock frequency	–	–	–	4	MHz
t_{LOW}	SCLK low time	–	42	–	–	ns
t_{HIGH}	SCLK high time	–	42	–	–	ns
t_{SETUP}	MOSI to SCLK setup time	–	30	–	–	ns
t_{HOLD}	SCLK to MOSI hold time	–	50	–	–	ns
t_{SS_MISO}	SS high to MISO valid	–	–	–	153	ns
t_{SCLK_MISO}	SCLK to MISO valid	–	–	–	125	ns
t_{SS_HIGH}	SS high time	–	50	–	–	ns
t_{SS_CLK}	Time from SS low to first SCLK	–	2/SCLK	–	–	ns
t_{CLK_SS}	Time from last SCLK to SS high	–	2/SCLK	–	–	ns

Figure 19. SPI Slave Mode 0 and 2

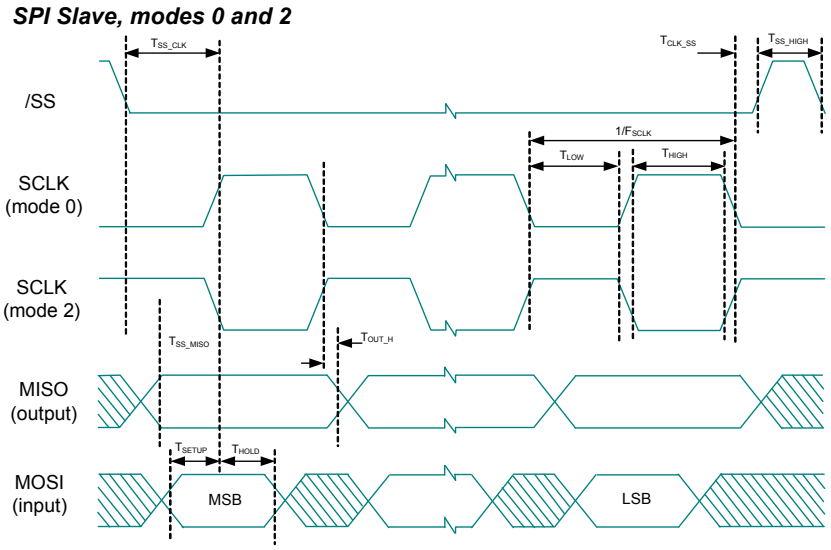


Figure 20. SPI Slave Mode 1 and 3

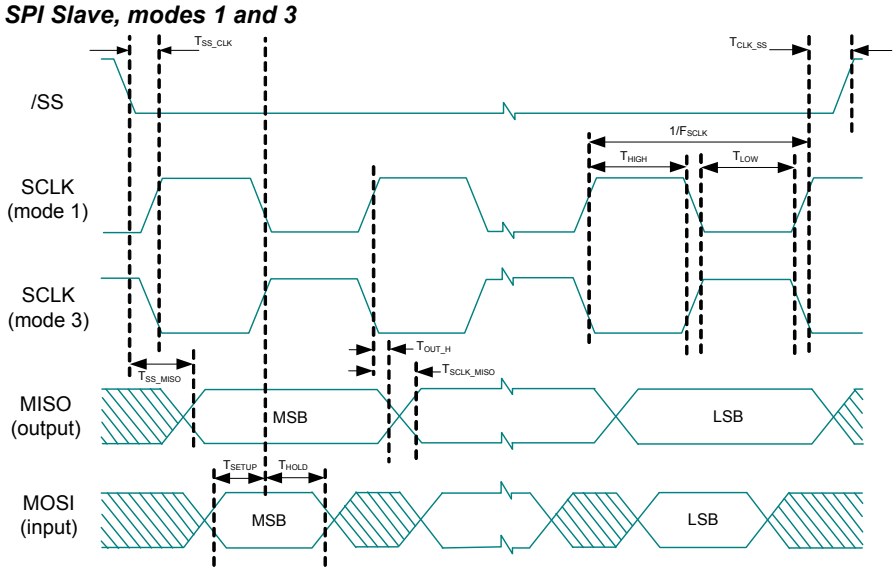


Figure 23. 32-pin QFN (5 × 5 × 0.55 mm) LQ32 3.5 × 3.5 E-Pad (Sawn) Package Outline, 001-42168

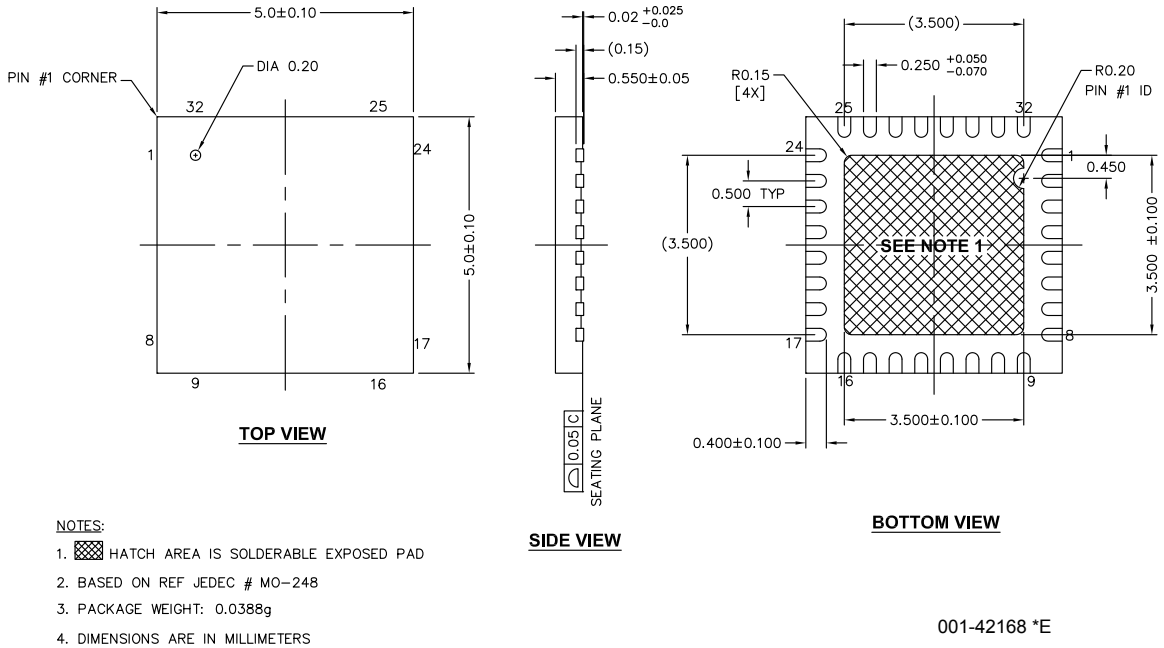


Figure 24. 48-pin SSOP (300 Mils) O483 Package Outline, 51-85061

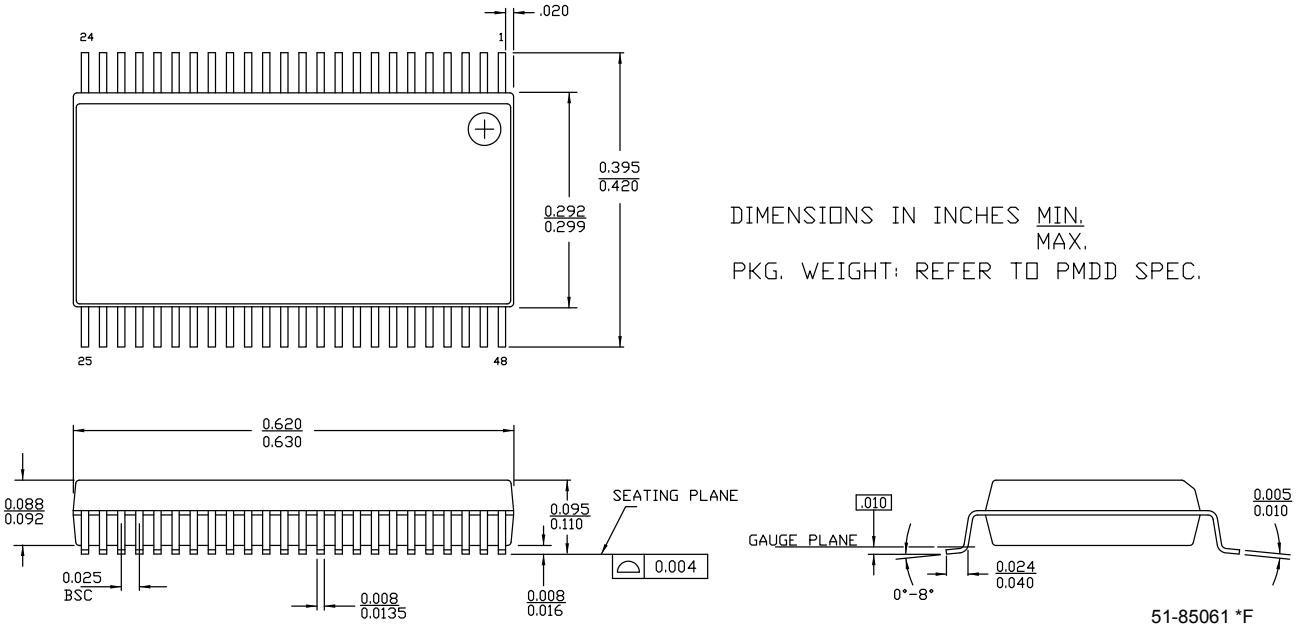
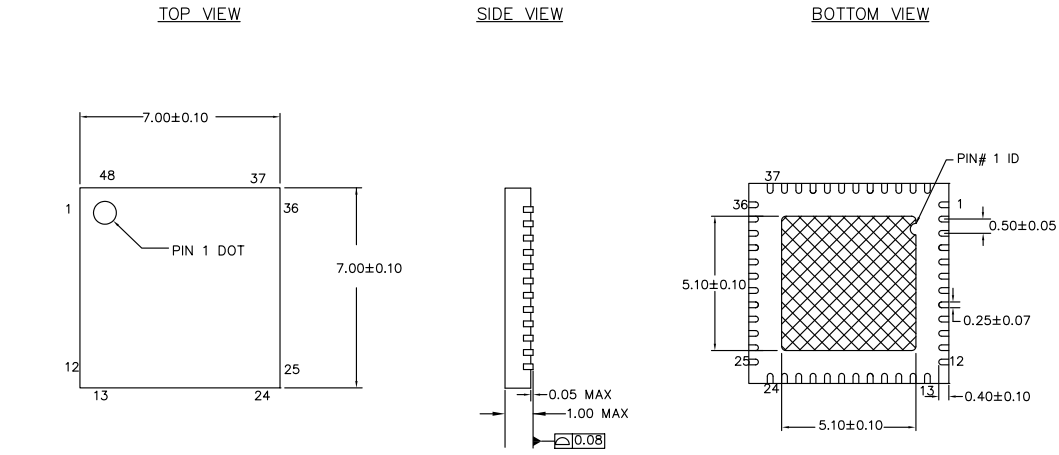


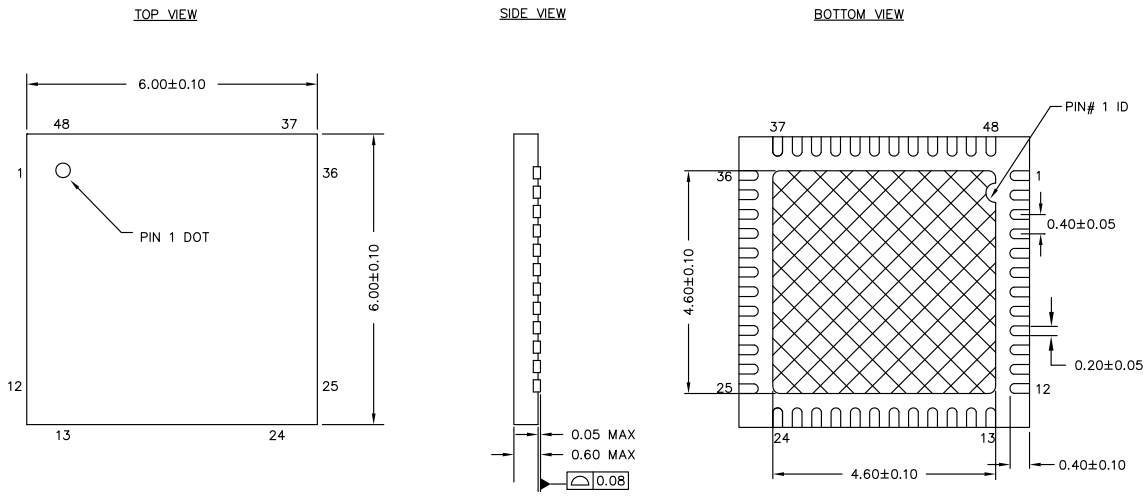
Figure 25. 48-pin QFN (7 × 7 × 1.0 mm) LT48A 5.1 × 5.1 E-Pad (Sawn) Package Outline, 001-13191



NOTES:
1. HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO−220
3. PACKAGE WEIGHT: 13 ± 1 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-13191 *H

Figure 26. 48-pin QFN (6 × 6 × 0.6 mm) LQ48A 4.6 × 4.6 E-Pad (Sawn) Package Outline, 001-57280



NOTES:
1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. REFERENCE JEDEC # MO−248
3. PACKAGE WEIGHT: 68 ±7 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-57280 *E

Important Notes

- For information on the preferred dimensions for mounting QFN packages, see the following Application Note at http://www.amkor.com/products/notes_papers/MLFAppNote.pdf.
- Pinned vias for thermal conduction are not required for the low power PSoC device.

Thermal Impedances

Table 37. Thermal Impedances per Package

Package	Typical θ_{JA} [73]	Typical θ_{JC}
16-pin QFN (No Center Pad)	33 °C/W	–
24-pin QFN [74]	21 °C/W	–
32-pin QFN [74]	20 °C/W	–
48-pin SSOP	69 °C/W	–
48-pin QFN (6 × 6 × 0.6 mm) [74]	25.20 °C/W	3.04 °C/W
48-pin QFN (7 × 7 × 1.0 mm) [74]	18 °C/W	–
30-ball WLCSP	54 °C/W	–

Capacitance on Crystal Pins

Table 38. Typical Package Capacitance on Crystal Pins

Package	Package Capacitance
32-pin QFN	3.2 pF
48-pin QFN	3.3 pF

Solder Reflow Specifications

Table 39 shows the solder reflow temperature limits that must not be exceeded.

Table 39. Solder Reflow Specifications

Package	Maximum Peak Temperature (T_C)	Maximum Time above T_C – 5 °C
16-pin QFN	260 °C	30 seconds
24-pin QFN	260 °C	30 seconds
32-pin QFN	260 °C	30 seconds
48-pin SSOP	260 °C	30 seconds
48-pin QFN (6 × 6 × 0.6 mm)	260 °C	30 seconds
48-pin QFN (7 × 7 × 1.0 mm)	260 °C	30 seconds
30-ball WLCSP	260 °C	30 seconds

Notes
73. $T_J = T_A + \text{Power} \times \theta_{JA}$.
74. To achieve the thermal impedance specified for the QFN package, the center thermal pad must be soldered to the PCB ground plane.

Table 41. PSoC Device Key Features and Ordering Information *(continued)*

Package	Ordering Code	Flash (Bytes)	SRAM (Bytes)	CapSense Blocks	Digital I/O Pins	Analog Inputs [78]	XRES Pin	USB	ADC
48-pin SSOP [79]	CY8C20536A-24PVXI [79]	8 K	1 K	1	34	34	Yes	No	Yes
48-pin SSOP (Tape and Reel) [79]	CY8C20536A-24PVXIT [79]	8 K	1 K	1	34	34	Yes	No	Yes
48-pin SSOP [79]	CY8C20546A-24PVXI [79]	16 K	2 K	1	34	34	Yes	No	Yes
48-pin SSOP (Tape and Reel) [79]	CY8C20546A-24PVXIT [79]	16 K	2 K	1	34	34	Yes	No	Yes
48-pin SSOP [79]	CY8C20566A-24PVXI [79]	32 K	2 K	1	34	34	Yes	No	Yes
48-pin SSOP (Tape and Reel) [79]	CY8C20566A-24PVXIT [79]	32 K	2 K	1	34	34	Yes	No	Yes
48-pin (6 × 6 × 0.6 mm) QFN	CY8C20636A-24LQXI	8 K	1 K	1	36	36	Yes	No	Yes
48-pin (6 × 6 × 0.6 mm) QFN (Tape and Reel)	CY8C20636A-24LQXIT	8 K	1 K	1	36	36	Yes	No	Yes
48-pin (7 × 7 × 1.0 mm) QFN [79]	CY8C20636A-24LTXI [79]	8 K	1 K	1	36	36	Yes	No	Yes
48-pin (7 × 7 × 1.0 mm) QFN (Tape and Reel) [79]	CY8C20636A-24LTXIT [79]	8 K	1 K	1	36	36	Yes	No	Yes
48-pin (6 × 6 × 0.6 mm) QFN	CY8C20646A-24LQXI	16 K	2 K	1	36	36	Yes	Yes	Yes
48-pin (6 × 6 × 0.6 mm) QFN (Tape and Reel)	CY8C20646A-24LQXIT	16 K	2 K	1	36	36	Yes	Yes	Yes
48-pin (7 × 7 × 1.0 mm) QFN [79]	CY8C20646A-24LTXI [79]	16 K	2 K	1	36	36	Yes	Yes	Yes
48-pin (7 × 7 × 1.0 mm) QFN (Tape and Reel) [79]	CY8C20646A-24LTXIT [79]	16 K	2 K	1	36	36	Yes	Yes	Yes
48-pin (6 × 6 × 0.6 mm) QFN	CY8C20666A-24LQXI	32 K	2 K	1	36	36	Yes	Yes	Yes
48-pin (6 × 6 × 0.6 mm) QFN (Tape and Reel)	CY8C20666A-24LQXIT	32 K	2 K	1	36	36	Yes	Yes	Yes
48-pin (7 × 7 × 1.0 mm) QFN [79]	CY8C20666A-24LTXI [79]	32 K	2 K	1	36	36	Yes	Yes	Yes
48-pin (7 × 7 × 1.0 mm) QFN [79]	CY8C20666AS-24LTXI [79]	32 K	2 K	1	36	36	Yes	Yes	Yes
48-pin (7 × 7 × 1.0 mm) QFN (Tape and Reel) [79]	CY8C20666A-24LTXIT [79]	32 K	2 K	1	36	36	Yes	Yes	Yes
48-pin (7 × 7 × 1.0 mm) QFN (Tape and Reel) [79]	CY8C20666AS-24LTXIT [79]	32 K	2 K	1	36	36	Yes	Yes	Yes
48-pin (7 × 7 × 1.0 mm) QFN (OCD) [78]	CY8C20066A-24LTXI [78]	32 K	2 K	1	36	36	Yes	Yes	Yes
30-ball WLCSP	CY8C20746A-24FDXC	16 K	1 K	1	27	27	Yes	No	Yes
30-ball WLCSP (Tape and Reel)	CY8C20746A-24FDXCT	16 K	1 K	1	27	27	Yes	No	Yes
30-ball WLCSP	CY8C20766A-24FDXC	32 K	2 K	1	27	27	Yes	No	Yes
30-ball WLCSP (Tape and Reel)	CY8C20766A-24FDXCT	32 K	2 K	1	27	27	Yes	No	Yes
24-pin (4 × 4 × 0.6 mm) QFN	CY8C20336AN-24LQXI	8 K	1 K	1	20	20	Yes	No	No
24-pin (4 × 4 × 0.6 mm) QFN (Tape and Reel)	CY8C20336AN-24LQXIT	8 K	1 K	1	20	20	Yes	No	No
32-pin (5 × 5 × 0.6 mm) QFN	CY8C20436AN-24LQXI	8 K	1 K	1	28	28	Yes	No	No
32-pin (5 × 5 × 0.6 mm) QFN (Tape and Reel)	CY8C20436AN-24LQXIT	8 K	1 K	1	28	28	Yes	No	No
16-pin (3 × 3 × 0.6 mm) QFN (no E-Pad)	CY8C20246AS-24LKXI	16 K	2 K	1	13	13	Yes	No	Yes
16-pin (3 × 3 × 0.6 mm) QFN (no E-Pad, Tape and Reel)	CY8C20246AS-24LKXIT	16 K	2 K	1	13	13	Yes	No	Yes

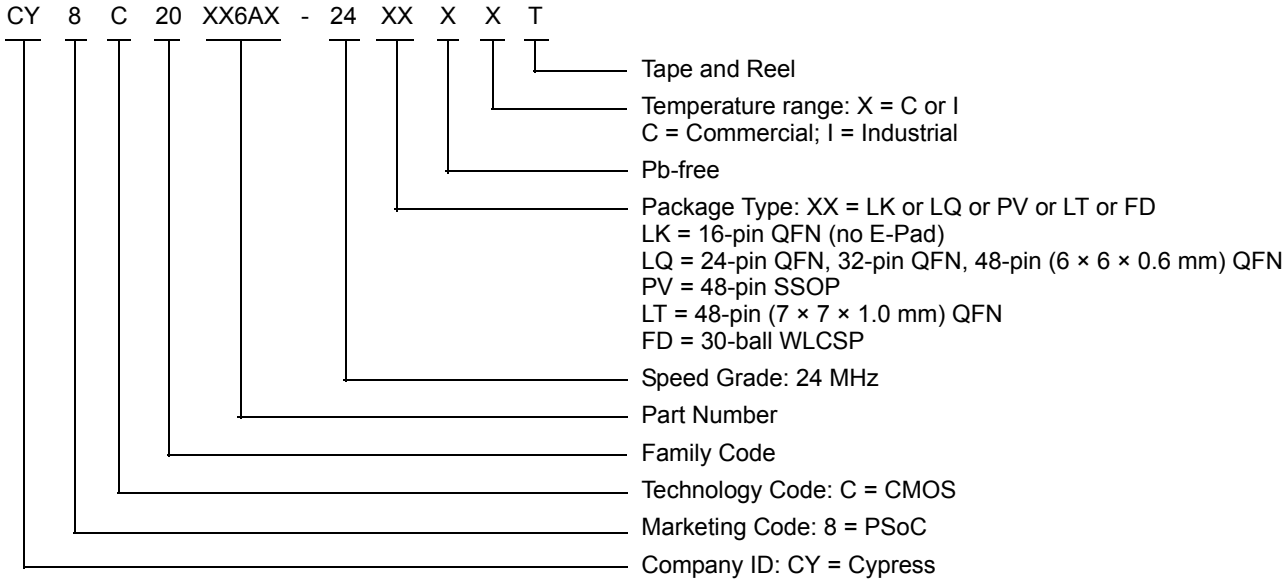
Notes
78. Dual-function Digital I/O Pins also connect to the common analog mux.
79. Not Recommended for New Designs.

Table 41. PSoC Device Key Features and Ordering Information *(continued)*

Package	Ordering Code	Flash (Bytes)	SRAM (Bytes)	CapSense Blocks	Digital I/O Pins	Analog Inputs [78]	XRES Pin	USB	ADC
24-pin (4 × 4 × 0.6 mm) QFN	CY8C20346AS-24LQXI	16 K	2 K	1	20	20	Yes	No	Yes
24-pin (4 × 4 × 0.6 mm) QFN (Tape and Reel)	CY8C20346AS-24LQXIT	16 K	2 K	1	20	20	Yes	No	Yes
32-pin (5 × 5 × 0.6 mm) QFN	CY8C20446AS-24LQXI	16 K	2 K	1	28	28	Yes	No	Yes
32-pin (5 × 5 × 0.6 mm) QFN (Tape and Reel)	CY8C20446AS-24LQXIT	16 K	2 K	1	28	28	Yes	No	Yes
32-pin (5 × 5 × 0.6 mm) QFN	CY8C20466AS-24LQXI	32 K	2 K	1	28	28	Yes	No	Yes
32-pin (5 × 5 × 0.6 mm) QFN (Tape and Reel)	CY8C20466AS-24LQXIT	32 K	2 K	1	28	28	Yes	No	Yes
48-pin (6 × 6 × 0.6 mm) QFN	CY8C20666AS-24LQXI	32 K	2 K	1	36	36	Yes	Yes	Yes
48-pin (6 × 6 × 0.6 mm) QFN (Tape and Reel)	CY8C20666AS-24LQXIT	32 K	2 K	1	36	36	Yes	Yes	Yes
48-pin (7 × 7 × 1.0 mm) QFN [79]	CY8C20666AS-24LTXI [79]	32 K	2 K	1	36	36	Yes	Yes	Yes
48-pin (7 × 7 × 1.0 mm) QFN (Tape and Reel) [79]	CY8C20666AS-24LTXIT [79]	32 K	2 K	1	36	36	Yes	Yes	Yes
48-pin (6 × 6 × 0.6 mm) QFN	CY8C20646AS-24LQXI	16 K	2 K	1	36	36	Yes	Yes	Yes
48-pin (6 × 6 × 0.6 mm) QFN (Tape and Reel)	CY8C20646AS-24LQXIT	16 K	2 K	1	36	36	Yes	Yes	Yes
48-pin (7 × 7 × 1.0 mm) QFN [79]	CY8C20646AS-24LTXI [79]	16 K	2 K	1	36	36	Yes	Yes	Yes
48-pin (7 × 7 × 1.0 mm) QFN (Tape and Reel) [79]	CY8C20646AS-24LTXIT [79]	16 K	2 K	1	36	36	Yes	Yes	Yes

Notes
78. Dual-function Digital I/O Pins also connect to the common analog mux.
79. Not Recommended for New Designs.

Ordering Code Definitions



3. DoubleTimer0 ISR

■ **Problem Definition**

When programmable timer 0 is used in “one-shot” mode by setting bit 1 of register 0,B0h (PT0_CFG), and the timer interrupt is used to wake the device from sleep, the interrupt service routine (ISR) may be executed twice.

■ **Parameters Affected**

No datasheet parameters are affected.

■ **Trigger Condition(S)**

Triggered by enabling one-shot mode in the timer, and using the timer to wake from sleep mode.

■ **Scope of Impact**

The ISR may be executed twice.

■ **Workaround**

In the ISR, firmware should clear the one-shot bit with a statement such as “`and reg[B0h], FDh`”

■ **Fix Status**

Will not be fixed

■ **Changes**

None

4. Missed GPIO Interrupt

■ **Problem Definition**

When in sleep mode, if a GPIO interrupt happens simultaneously with a Timer0 or Sleep Timer interrupt, the GPIO interrupt may be missed, and the corresponding GPIO ISR not run.

■ **Parameters Affected**

No datasheet parameters are affected.

■ **Trigger Condition(S)**

Triggered by enabling sleep mode, then having GPIO interrupt occur simultaneously with a Timer 0 or Sleep Timer interrupt.

■ **Scope of Impact**

The GPIO interrupt service routine will not be run.

■ **Workaround**

The system should be architected such that a missed GPIO interrupt may be detected. For example, if a GPIO is used to wake the system to perform some function, the system should detect if the function is not performed, and re-issue the GPIO interrupt.

Alternatively, if a GPIO interrupt is required to wake the system, then firmware should disable the Sleep Timer and Timer0.

Alternatively, the ISR’s for Sleep Timer and Timer0 should manually check the state of the GPIO to determine if the host system has attempted to generate a GPIO interrupt.

■ **Fix Status**

Will not be fixed

■ **Changes**

None

Document History Page *(continued)*

Document Title: CY8C20XX6A/S, 1.8 V Programmable CapSense® Controller with SmartSense™ Auto-tuning 1–33 Buttons, 0–6 Sliders Document Number: 001-54459				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*P	3774062	UBU	10/11/2012	Updated Electrical Specifications: Updated AC Chip-Level Specifications: Updated Table 27: Changed minimum value of F_{32K1} parameter from 19 kHz to 15 kHz. Updated Packaging Information: spec 001-09116 – Changed revision from *F to *G. spec 001-13937 – Changed revision from *D to *E. spec 51-85061 – Changed revision from *E to *F. spec 001-13191 – Changed revision from *F to *G. spec 001-57280 – Changed revision from *C to *D.
*Q	3807186	PKS	15/11/2012	No content update; appended to EROS document.
*R	3836626	SRLI	01/03/2013	Updated Document Title to read as “CY8C20XX6A/S, 1.8 V Programmable CapSense® Controller with SmartSense™ Auto-tuning 1–33 Buttons, 0–6 Sliders”. Updated Features. Updated PSoC® Functional Overview: Replaced “CY8C20X36A/46A/66A/96A/46AS/66AS” with “CY8C20XX6A/S”. Updated Getting Started: Replaced “CY8C20X36A/46A/66A/96A/46AS/66AS” with “CY8C20XX6A/S”. Updated Pinouts: Updated 16-pin QFN (10 Sensing Inputs)[3, 4]: Replaced “12 Sensing Inputs” with “10 Sensing Inputs” in heading, added Note 3 only. Updated 24-pin QFN (17 Sensing Inputs) [8]: Replaced “12 Sensing Inputs” with “17 Sensing Inputs” in heading, added Note 8 only. Updated 24-pin QFN (15 Sensing Inputs (With USB)) [13]: Replaced “18 Sensing Inputs” with “15 Sensing Inputs” in heading, added Note 13 only. Updated 30-ball WLCSP (24 Sensing Inputs) [18]: Replaced “26 Sensing Inputs” with “24 Sensing Inputs” in heading, added Note 18 only. Updated 32-pin QFN (25 Sensing Inputs) [22]: Replaced “27 Sensing Inputs” with “25 Sensing Inputs” in heading, added Note 22 only. updated 32-pin QFN (22 Sensing Inputs (With USB)) [27]: Replaced “24 Sensing Inputs” with “22 Sensing Inputs” in heading, added Note 27 only. Updated 48-pin SSOP (31 Sensing Inputs) [32]: Replaced “33 Sensing Inputs” with “31 Sensing Inputs” in heading, added Note 32 only. Updated 48-pin QFN (33 Sensing Inputs) [36]: Replaced “35 Sensing Inputs” with “33 Sensing Inputs” in heading, added Note 36 only. Updated 48-pin QFN (33 Sensing Inputs (With USB)) [41]: Replaced “35 Sensing Inputs” with “33 Sensing Inputs” in heading, added Note 41 only. Updated 48-pin QFN (OCD) (33 Sensing Inputs) [46]: Added “33 Sensing Inputs” in heading, added Note 46 only. Updated Packaging Information: spec 001-42168 – Changed revision from *D to *E. spec 001-57280 – Changed revision from *D to *E.
*S	3997568	BVI	05/11/2013	Added Errata.
*T	4044148	BVI	06/28/2013	Added Errata Footnotes. Updated Packaging Information: spec 001-09116 – Changed revision from *G to *H. Updated to new template.

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Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*U	4185313	BVI	11/07/2013	Updated Features. Updated Packaging Information: spec 001-09116 – Changed revision from *H to *I.
*V	4622119	SSHH	01/13/2015	Added More Information.
*W	4825924	SSHH	07/07/2015	Updated Pinouts: Updated 16-pin QFN (10 Sensing Inputs)[3, 4]: Updated Table 1: Added Note 7 and referred the same note in description of V_{SS} pin. Updated 24-pin QFN (17 Sensing Inputs) [8]: Updated Table 2: Added Note 12 and referred the same note in description of V_{SS} pin. Updated 24-pin QFN (15 Sensing Inputs (With USB)) [13]: Updated Table 3: Added Note 17 and referred the same note in description of V_{SS} pin. Updated 30-ball WLCSP (24 Sensing Inputs) [18]: Updated Table 4: Added Note 21 and referred the same note in description of V_{SS} pin. Updated 32-pin QFN (25 Sensing Inputs) [22]: Updated Table 5: Added Note 26 and referred the same note in description of V_{SS} pin. Updated 32-pin QFN (22 Sensing Inputs (With USB)) [27]: Updated Table 6: Added Note 31 and referred the same note in description of V_{SS} pin. Updated 48-pin SSOP (31 Sensing Inputs) [32]: Updated Table 7: Added Note 35 and referred the same note in description of V_{SS} pin. Updated 48-pin QFN (33 Sensing Inputs) [36]: Updated Table 8: Added Note 40 and referred the same note in description of V_{SS} pin. Updated 48-pin QFN (33 Sensing Inputs (With USB)) [41]: Updated Table 9: Added Note 45 and referred the same note in description of V_{SS} pin. Updated 48-pin QFN (OCD) (33 Sensing Inputs) [46]: Updated Table 10: Added Note 52 and referred the same note in description of V_{SS} pin. Updated Ordering Information: Removed prune part numbers (CY8C20636AN-24LTXI and CY8C20636AN-24LTXIT). Updated Packaging Information: spec 001-13937 – Changed revision from *E to *F. spec 001-13191 – Changed revision from *G to *H.
*X	5394582	SSHH	08/08/2016	Updated to new template. Completing Sunset Review.