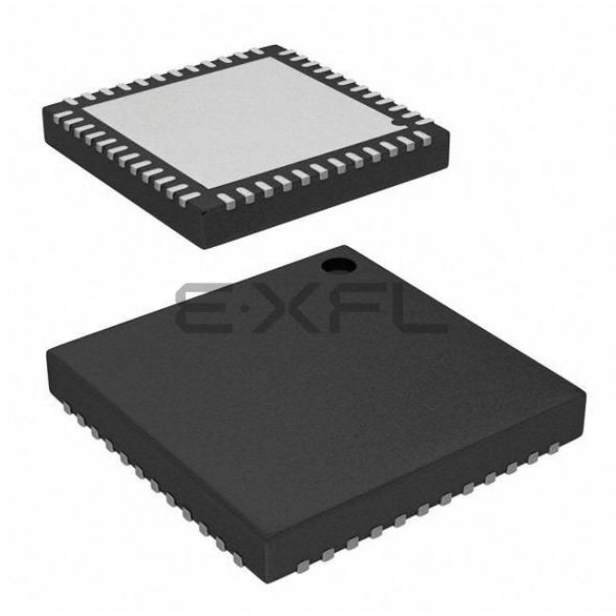

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Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

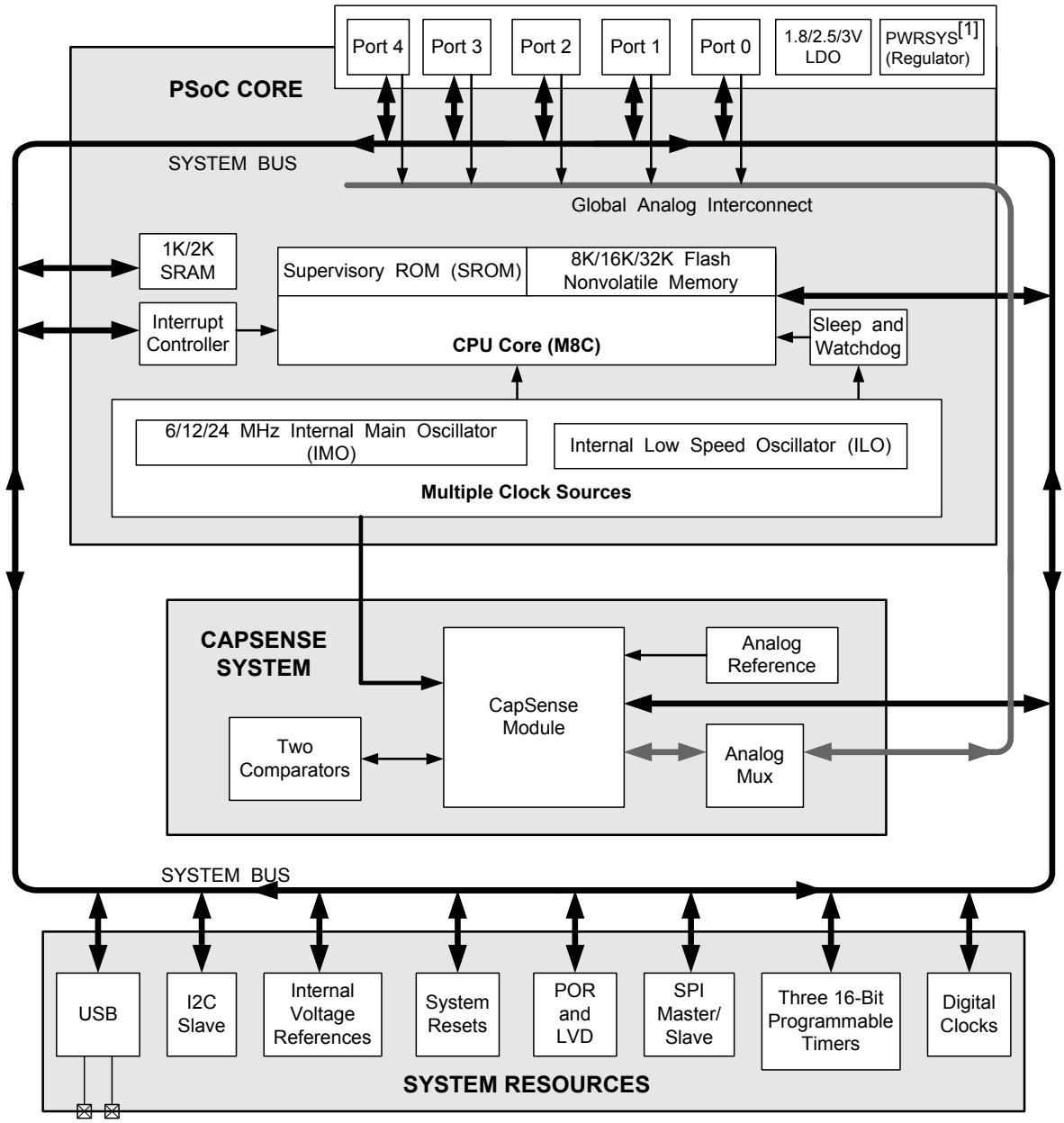
Embedded - Microcontrollers - Application Specific represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	Capacitive Sensing
Core Processor	M8C
Program Memory Type	FLASH (32kB)
Controller Series	CY8C20xx6A
RAM Size	2K x 8
Interface	I²C, SPI, USB
Number of I/O	36
Voltage - Supply	1.71V ~ 5.5V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c20666a-24lqxi

Logic Block Diagram



Note
1. Internal voltage regulator for internal circuitry

PSoC® Functional Overview

The PSoC family consists of on-chip controller devices, which are designed to replace multiple traditional microcontroller unit (MCU)-based components with one, low cost single-chip programmable component. A PSoC device includes configurable analog and digital blocks, and programmable interconnect. This architecture allows the user to create customized peripheral configurations, to match the requirements of each individual application. Additionally, a fast CPU, Flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts.

The architecture for this device family, as shown in the Logic Block Diagram on page 2, consists of three main areas:

- The Core
- CapSense Analog System
- System Resources (including a full-speed USB port).

A common, versatile bus allows connection between I/O and the analog system.

Each CY8C20XX6A/S PSoC device includes a dedicated CapSense block that provides sensing and scanning control circuitry for capacitive sensing applications. Depending on the PSoC package, up to 36 GPIO are also included. The GPIO provides access to the MCU and analog mux.

PSoC Core

The PSoC Core is a powerful engine that supports a rich instruction set. It encompasses SRAM for data storage, an interrupt controller, sleep and watchdog timers, and IMO and ILO. The CPU core, called the M8C, is a powerful processor with speeds up to 24 MHz. The M8C is a 4-MIPS, 8-bit Harvard-architecture microprocessor.

CapSense System

The analog system contains the capacitive sensing hardware. Several hardware algorithms are supported. This hardware performs capacitive sensing and scanning without requiring external components. The analog system is composed of the CapSense PSoC block and an internal 1 V or 1.2 V analog reference, which together support capacitive sensing of up to 33 inputs [2]. Capacitive sensing is configurable on each GPIO pin. Scanning of enabled CapSense pins are completed quickly and easily across multiple ports.

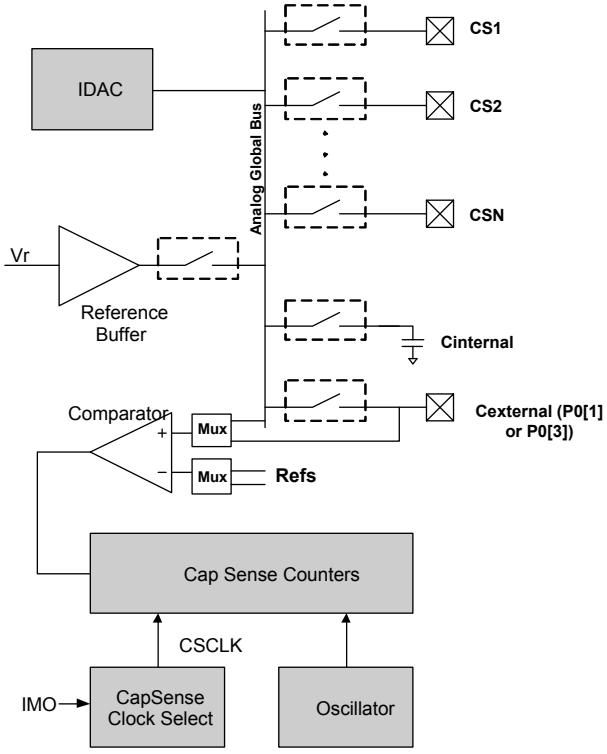
SmartSense

SmartSense is an innovative solution from Cypress that removes manual tuning of CapSense applications. This solution is easy to use and provides a robust noise immunity. It is the only auto-tuning solution that establishes, monitors, and maintains all required tuning parameters. SmartSense allows engineers to go from prototyping to mass production without re-tuning for manufacturing variations in PCB and/or overlay material properties.

SmartSense_EMC

In addition to the SmartSense auto tuning algorithm to remove manual tuning of CapSense applications, SmartSense_EMC user module incorporates a unique algorithm to improve robustness of capacitive sensing algorithm/circuit against high frequency conducted and radiated noise. Every electronic device must comply with specific limits for radiated and conducted external noise and these limits are specified by regulatory bodies (for example, FCC, CE, U/L and so on). A very good PCB layout design, power supply design and system design is a mandatory for a product to pass the conducted and radiated noise tests. An ideal PCB layout, power supply design or system design is not often possible because of cost and form factor limitations of the product. SmartSense_EMC with superior noise immunity is well suited and handy for such applications to pass radiated and conducted noise test.

Figure 2. CapSense System Block Diagram



Note
2. 36 GPIOs = 33 pins for capacitive sensing + 2 pins for I^2C + 1 pin for modulator capacitor.

Getting Started

The quickest way to understand PSoC silicon is to read this datasheet and then use the PSoC Designer Integrated Development Environment (IDE). This datasheet is an overview of the PSoC integrated circuit and presents specific pin, register, and electrical specifications.

For in depth information, along with detailed programming details, see the Technical Reference Manual for the CY8C20XX6A/S PSoC devices.

For up-to-date ordering, packaging, and electrical specification information, see the latest PSoC device datasheets on the web at www.cypress.com/psoc.

CapSense Design Guides

Design Guides are an excellent introduction to the wide variety of possible CapSense designs. They are located at www.cypress.com/go/CapSenseDesignGuides.

Refer Getting Started with CapSense design guide for information on CapSense design and CY8C20XX6A/H/AS CapSense® Design Guide for specific information on CY8C20XX6A/AS CapSense controllers.

Silicon Errata

Errata documents known issues with silicon including errata trigger conditions, scope of impact, available workarounds and silicon revision applicability. Refer to Silicon Errata for the PSoC® CY8C20x36A/46A/66A/96A/46AS/66AS/36H/46H families available at http://www.cypress.com/?rID=56239 for errata information on CY8C20xx6A/AS/H family of device. Compare errata document with datasheet for a complete functional description of device.

Development Kits

PSoC Development Kits are available online from and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

Training

Free PSoC technical training (on demand, webinars, and workshops), which is available online via www.cypress.com, covers a wide variety of topics and skill levels to assist you in your designs.

CYPros Consultants

Certified PSoC consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC consultant go to the CYPros Consultants web site.

Solutions Library

Visit our growing library of solution focused designs. Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

Technical Support

Technical support – including a searchable Knowledge Base articles and technical forums – is also available online. If you cannot find an answer to your question, call our Technical Support hotline at 1-800-541-4736.

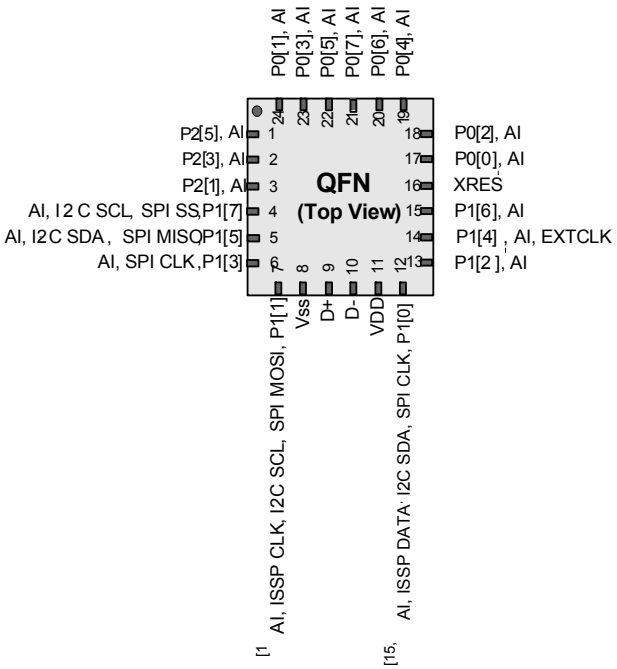
24-pin QFN (15 Sensing Inputs (With USB)) [13]

Table 3. Pin Definitions – CY8C20396A [14]

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I	P2[5]	
2	I/O	I	P2[3]	
3	I/O	I	P2[1]	
4	IOHR	I	P1[7]	I^2C SCL, SPI SS
5	IOHR	I	P1[5]	I^2C SDA, SPI MISO
6	IOHR	I	P1[3]	SPI CLK
7	IOHR	I	P1[1]	ISSP CLK[15], I^2C SCL, SPI MOSI
8	Power		V_{SS}	Ground[17]
9	I/O	I	D+	USB D+
10	I/O	I	D-	USB D-
11	Power		V_{DD}	Supply
12	IOHR	I	P1[0]	ISSP DATA[15], I^2C SDA, SPI CLK[16]
13	IOHR	I	P1[2]	
14	IOHR	I	P1[4]	Optional external clock input (EXTCLK)
15	IOHR	I	P1[6]	
16	RESET INPUT		XRES	Active high external reset with internal pull-down
17	IOH	I	P0[0]	
18	IOH	I	P0[2]	
19	IOH	I	P0[4]	
20	IOH	I	P0[6]	
21	IOH	I	P0[7]	
22	IOH	I	P0[5]	
23	IOH	I	P0[3]	Integrating input
24	IOH	I	P0[1]	Integrating input
CP	Power		V_{SS}	Center pad must be connected to Ground

LEGEND I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output

Figure 5. CY8C20396A



Notes
13. 20 GPIOs = 15 pins for capacitive sensing + 2 pins for I2C + 2 pins for USB + 1 pin for modulation capacitor.
14. The center pad (CP) on the QFN package must be connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.
15. On power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to high impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the I2C bus. Use alternate pins if you encounter issues.
16. Alternate SPI clock.
17. All VSS pins should be brought out to one common GND plane.

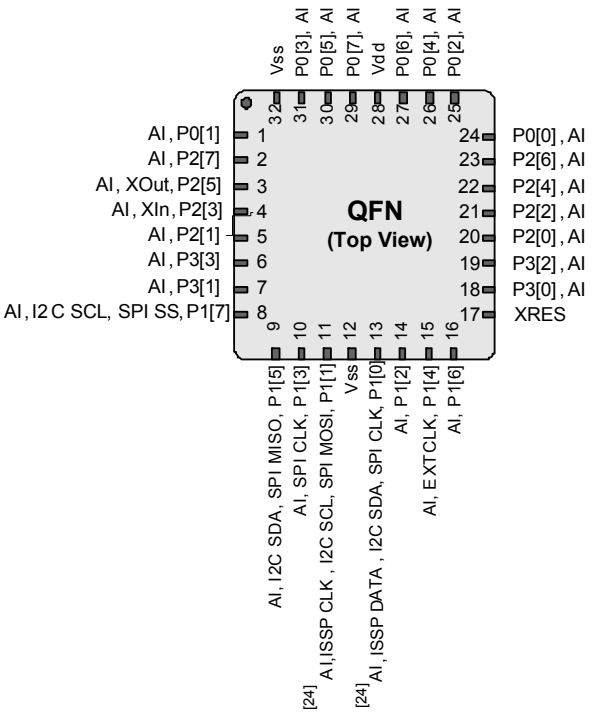
32-pin QFN (25 Sensing Inputs) [22]

Table 5. Pin Definitions – CY8C20436A, CY8C20446A, CY8C20446AS, CY8C20466A, CY8C20466AS[23]

Pin No.	Type		Name	Description
	Digital	Analog		
1	IOH	I	P0[1]	Integrating input
2	I/O	I	P2[7]	
3	I/O	I	P2[5]	Crystal output (XOut)
4	I/O	I	P2[3]	Crystal input (XIn)
5	I/O	I	P2[1]	
6	I/O	I	P3[3]	
7	I/O	I	P3[1]	
8	IOHR	I	P1[7]	I^2C SCL, SPI SS
9	IOHR	I	P1[5]	I^2C SDA, SPI MISO
10	IOHR	I	P1[3]	SPI CLK.
11	IOHR	I	P1[1]	ISSP CLK[24], I^2C SCL, SPI MOSI.
12	Power		V_{SS}	Ground connection[26]
13	IOHR	I	P1[0]	ISSP DATA[24], I^2C SDA, SPI CLK[25]
14	IOHR	I	P1[2]	
15	IOHR	I	P1[4]	Optional external clock input (EXTCLK)
16	IOHR	I	P1[6]	
17	Input		XRES	Active high external reset with internal pull-down
18	I/O	I	P3[0]	
19	I/O	I	P3[2]	
20	I/O	I	P2[0]	
21	I/O	I	P2[2]	
22	I/O	I	P2[4]	
23	I/O	I	P2[6]	
24	IOH	I	P0[0]	
25	IOH	I	P0[2]	
26	IOH	I	P0[4]	
27	IOH	I	P0[6]	
28	Power		V_{DD}	Supply voltage
29	IOH	I	P0[7]	
30	IOH	I	P0[5]	
31	IOH	I	P0[3]	Integrating input
32	Power		V_{SS}	Ground connection[26]
CP	Power		V_{SS}	Center pad must be connected to ground

LEGEND A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output.

Figure 7. CY8C20436A, CY8C20446A, CY8C20446AS, CY8C20466A, CY8C20466AS



Notes

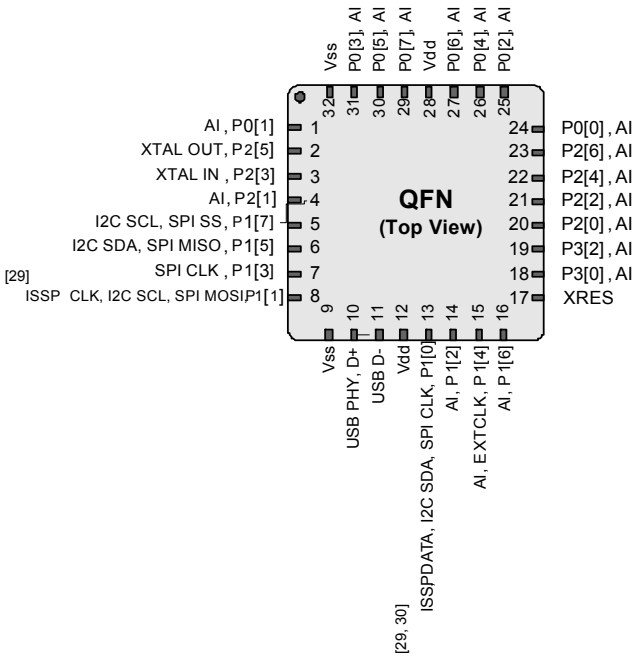
22. 28 GPIOs = 25 pins for capacitive sensing + 2 pins for I2C + 1 pin for modulation capacitor.
23. The center pad (CP) on the QFN package must be connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.
24. On power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to high impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the I2C bus. Use alternate pins if you encounter issues.
25. Alternate SPI clock.
26. All VSS pins should be brought out to one common GND plane.

32-pin QFN (22 Sensing Inputs (With USB)) [27]

Table 6. Pin Definitions – CY8C20496A[28]

Pin No.	Type		Name	Description
	Digital	Analog		
1	IOH	I	P0[1]	Integrating Input
2	I/O	I	P2[5]	XTAL Out
3	I/O	I	P2[3]	XTAL In
4	I/O	I	P2[1]	
5	IOHR	I	P1[7]	I^2C SCL, SPI SS
6	IOHR	I	P1[5]	I^2C SDA, SPI MISO
7	IOHR	I	P1[3]	SPI CLK
8	IOHR	I	P1[1]	ISSP CLK[29], I^2C SCL, SPI MOSI
9	Power		V_{SS}	Ground Pin[31]
10	I		D+	USB D+
11	I		D-	USB D-
12	Power		V_{DD}	Power pin
13	IOHR	I	P1[0]	ISSP DATA[29], I^2C SDA, SPI CLKI[30]
14	IOHR	I	P1[2]	
15	IOHR	I	P1[4]	Optional external clock input (EXTCLK)
16	IOHR	I	P1[6]	
17	Input		XRES	Active high external reset with internal pull-down
18	I/O	I	P3[0]	
19	I/O	I	P3[2]	
20	I/O	I	P2[0]	
21	I/O	I	P2[2]	
22	I/O	I	P2[4]	
23	I/O	I	P2[6]	
24	IOH	I	P0[0]	
25	IOH	I	P0[2]	
26	IOH	I	P0[4]	
27	IOH	I	P0[6]	
28	Power		V_{DD}	Power Pin
29	IOH	I	P0[7]	
30	IOH	I	P0[5]	
31	IOH	I	P0[3]	Integrating Input
32	Power		V_{SS}	Ground Pin[31]

Figure 8. CY8C20496A



LEGEND A = Analog, I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output.

Notes
27. 27 GPIOs = 22 pins for capacitive sensing + 2 pins for I2C + 2 pins for USB + 1 pin for modulation capacitor.
28. The center pad (CP) on the QFN package must be connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.
29. On power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to high impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the I2C bus. Use alternate pins if you encounter issues.
30. Alternate SPI clock.
31. All VSS pins should be brought out to one common GND plane.

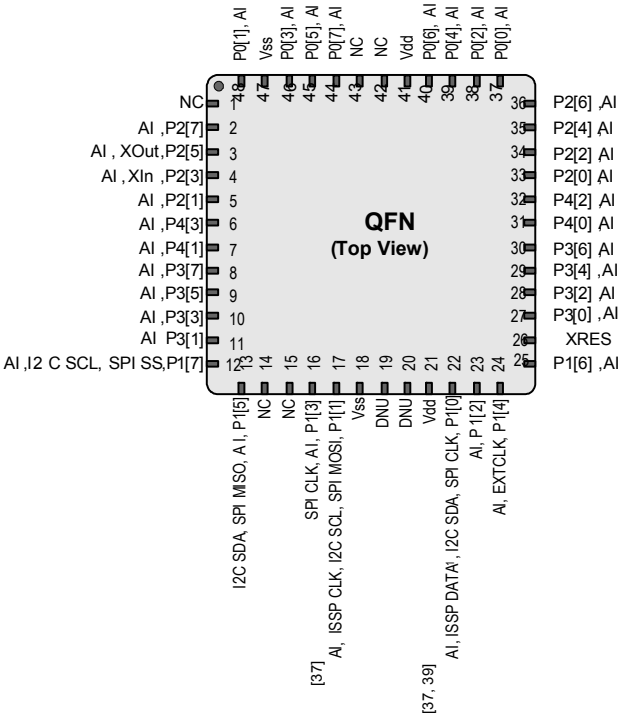
48-pin QFN (33 Sensing Inputs) [36]

Table 8. Pin Definitions – CY8C20636A[37, 38]

Pin No.	Digital	Analog	Name	Description
1			NC	No connection
2	I/O	I	P2[7]	
3	I/O	I	P2[5]	Crystal output (XOut)
4	I/O	I	P2[3]	Crystal input (XIn)
5	I/O	I	P2[1]	
6	I/O	I	P4[3]	
7	I/O	I	P4[1]	
8	I/O	I	P3[7]	
9	I/O	I	P3[5]	
10	I/O	I	P3[3]	
11	I/O	I	P3[1]	
12	IOHR	I	P1[7]	I^2C SCL, SPI SS
13	IOHR	I	P1[5]	I^2C SDA, SPI MISO
14			NC	No connection
15			NC	No connection
16	IOHR	I	P1[3]	SPI CLK
17	IOHR	I	P1[1]	ISSP CLK[37], I^2C SCL, SPI MOSI
18	Power		V_{SS}	Ground connection[40]
19			DNU	
20			DNU	
21	Power		V_{DD}	Supply voltage
22	IOHR	I	P1[0]	ISSP DATA[37], I^2C SDA, SPI CLK[39]
23	IOHR	I	P1[2]	
24	IOHR	I	P1[4]	Optional external clock input (EXTCLK)
25	IOHR	I	P1[6]	
26	Input		XRES	Active high external reset with internal pull-down
27	I/O	I	P3[0]	
28	I/O	I	P3[2]	
29	I/O	I	P3[4]	
30	I/O	I	P3[6]	
31	I/O	I	P4[0]	
32	I/O	I	P4[2]	
33	I/O	I	P2[0]	
34	I/O	I	P2[2]	
35	I/O	I	P2[4]	
36	I/O	I	P2[6]	
37	IOH	I	P0[0]	
38	IOH	I	P0[2]	
39	IOH	I	P0[4]	
40	IOH	I	P0[6]	
41	Power		V_{DD}	Supply voltage
42			NC	No connection
43			NC	No connection
44	IOH	I	P0[7]	
45	IOH	I	P0[5]	
46	IOH	I	P0[3]	Integrating input
47	Power		V_{SS}	Ground connection[40]
48	IOH	I	P0[1]	
CP	Power		V_{SS}	Center pad must be connected to ground

LEGEND A = Analog, I = Input, O = Output, NC = No Connection H = 5 mA High Output Drive, R = Regulated Output.

Figure 10. CY8C20636A



Notes

36. 36 GPIOs = 33 pins for capacitive sensing + 2 pins for I2C + 1 pin for modulation capacitor.
37. On power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to high impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the I2C bus. Use alternate pins if you encounter issues.
38. The center pad (CP) on the QFN package must be connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal
39. Alternate SPI clock.
40. All VSS pins should be brought out to one common GND plane.

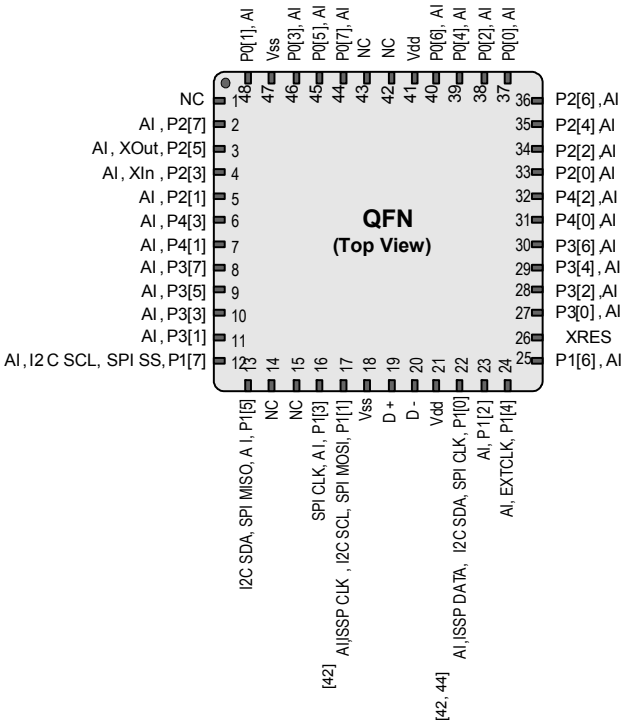
48-pin QFN (33 Sensing Inputs (With USB)) [41]

Table 9. Pin Definitions – CY8C20646A, CY8C20646AS, CY8C20666A, CY8C20666AS [42, 43]

Pin No.	Digital	Analog	Name	Description
1			NC	No connection
2	I/O	I	P2[7]	
3	I/O	I	P2[5]	Crystal output (XOut)
4	I/O	I	P2[3]	Crystal input (XIn)
5	I/O	I	P2[1]	
6	I/O	I	P4[3]	
7	I/O	I	P4[1]	
8	I/O	I	P3[7]	
9	I/O	I	P3[5]	
10	I/O	I	P3[3]	
11	I/O	I	P3[1]	
12	IOHR	I	P1[7]	I^2C SCL, SPI SS
13	IOHR	I	P1[5]	I^2C SDA, SPI MISO
14			NC	No connection
15			NC	No connection
16	IOHR	I	P1[3]	SPI CLK
17	IOHR	I	P1[1]	ISSP CLK[42], I^2C SCL, SPI MOSI
18	Power		V_{SS}	Ground connection[45]
19	I/O		D+	USB D+
20	I/O		D-	USB D-
21	Power		V_{DD}	Supply voltage
22	IOHR	I	P1[0]	ISSP DATA[42], I^2C SDA, SPI CLK[44]
23	IOHR	I	P1[2]	
24	IOHR	I	P1[4]	Optional external clock input (EXTCLK)
25	IOHR	I	P1[6]	
26	Input		XRES	Active high external reset with internal pull-down
27	I/O	I	P3[0]	
28	I/O	I	P3[2]	
29	I/O	I	P3[4]	
30	I/O	I	P3[6]	
31	I/O	I	P4[0]	
32	I/O	I	P4[2]	
33	I/O	I	P2[0]	
34	I/O	I	P2[2]	
35	I/O	I	P2[4]	
36	I/O	I	P2[6]	
37	IOH	I	P0[0]	
38	IOH	I	P0[2]	
39	IOH	I	P0[4]	
40	IOH	I	P0[6]	
41	Power		V_{DD}	Supply voltage
42			NC	No connection
43			NC	No connection
44	IOH	I	P0[7]	
45	IOH	I	P0[5]	
46	IOH	I	P0[3]	Integrating input
47	Power		V_{SS}	Ground connection[45]
48	IOH	I	P0[1]	
CP	Power		V_{SS}	Center pad must be connected to ground

LEGEND A = Analog, I = Input, O = Output, NC = No Connection H = 5 mA High Output Drive, R = Regulated Output.

Figure 11. CY8C20646A, CY8C20646AS, CY8C20666A, CY8C20666AS



Notes

41. 38 GPIOs = 33 pins for capacitive sensing + 2 pins for I2C + 2 pins for USB + 1 pin for modulation capacitor.
42. On Power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to High impedance state. On reset, after XRES de- asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. In both cases, a pull-up resistance on these lines combines with the pull-down resistance (5.6K ohm) and form a potential divider. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the I2C bus. Use alternate pins if you encounter issues.
43. The center pad (CP) on the QFN package must be connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.
44. Alternate SPI clock.
45. All VSS pins should be brought out to one common GND plane.

DC Chip-Level Specifications

Table 13 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 13. DC Chip-Level Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{DD}[54, 55, 56, 57]	Supply voltage	No USB activity. Refer the table "DC POR and LVD Specifications" on page 26	1.71	–	5.50	V
V_{DDUSB}[54, 55, 56, 57]	Operating voltage	USB activity, USB regulator enabled	4.35	–	5.25	V
		USB activity, USB regulator bypassed	3.15	3.3	3.60	V
I_{DD24}	Supply current, IMO = 24 MHz	Conditions are $V_{DD} \leq 3.0$ V, $T_A = 25$ °C, CPU = 24 MHz. CapSense running at 12 MHz, no I/O sourcing current	–	2.88	4.00	mA
I_{DD12}	Supply current, IMO = 12 MHz	Conditions are $V_{DD} \leq 3.0$ V, $T_A = 25$ °C, CPU = 12 MHz. CapSense running at 12 MHz, no I/O sourcing current	–	1.71	2.60	mA
I_{DD6}	Supply current, IMO = 6 MHz	Conditions are $V_{DD} \leq 3.0$ V, $T_A = 25$ °C, CPU = 6 MHz. CapSense running at 6 MHz, no I/O sourcing current	–	1.16	1.80	mA
$I_{DDAVG10}$	Average supply current per sensor	One sensor scanned at 10 mS rate	–	250	–	µA
$I_{DDAVG100}$	Average supply current per sensor	One sensor scanned at 100 mS rate	–	25	–	µA
$I_{DDAVG500}$	Average supply current per sensor	One sensor scanned at 500 mS rate	–	7	–	µA
I_{SB0}[58, 59, 60, 61, 62, 63]	Deep sleep current	$V_{DD} \leq 3.0$ V, $T_A = 25$ °C, I/O regulator turned off	–	0.10	1.05	µA
I_{SB1}[58, 59, 60, 61, 62, 63]	Standby current with POR, LVD and sleep timer	$V_{DD} \leq 3.0$ V, $T_A = 25$ °C, I/O regulator turned off	–	1.07	1.50	µA
I_{SBI2C}[58, 59, 60, 61, 62, 63]	Standby current with I^2C enabled	Conditions are $V_{DD} = 3.3$ V, $T_A = 25$ °C and CPU = 24 MHz	–	1.64	–	µA

Notes

54. When V_{DD} remains in the range from 1.71 V to 1.9 V for more than 50 µs, the slew rate when moving from the 1.71 V to 1.9 V range to greater than 2 V must be slower than 1 V/500 µs to avoid triggering POR. The only other restriction on slew rates for any other voltage range or transition is the SR_{POWER_UP} parameter.
55. If powering down in standby sleep mode, to properly detect and recover from a V_{DD} brown out condition any of the following actions must be taken:
    a. Bring the device out of sleep before powering down.
    b. Assure that V_{DD} falls below 100 mV before powering back up.
    c. Set the No Buzz bit in the OSC_CR0 register to keep the voltage monitoring circuit powered during sleep.
    d. Increase the buzz rate to assure that the falling edge of V_{DD} is captured. The rate is configured through the PSSDC bits in the SLP_CFG register.
    For the referenced registers, refer to the *CY8C20X36 Technical Reference Manual*. In deep sleep mode, additional low power voltage monitoring circuitry allows V_{DD} brown out conditions to be detected for edge rates slower than 1V/ms.
56. For USB mode, the V_{DD} supply for bus-powered application should be limited to 4.35 V–5.35 V. For self-powered application, V_{DD} should be 3.15 V–3.45 V.
57. For proper CapSense block functionality, if the drop in V_{DD} exceeds 5% of the base V_{DD}, the rate at which V_{DD} drops should not exceed 200 mV/s. Base V_{DD} can be between 1.8 V and 5.5 V.
58. Errata: When the device is put to sleep in Standby or I2C_USB Mode and the bandgap circuit is refreshed less frequently than every 8 ms (default), the device may not come out of sleep when a sleep-ending input is received. For more information, see the "Errata" on page 46.
59. Errata: The I2C block exhibits occasional data and bus corruption errors when the I2C master initiates transactions while the device is in or out of transition of sleep mode. For more information, see the "Errata" on page 46.
60. Errata: When programmable timer 0 is used in "one-shot" mode by setting bit 1 of register 0,B0h (PT0_CFG), and the timer interrupt is used to wake the device from sleep, the interrupt service routine (ISR) may be executed twice. For more information, see the "Errata" on page 47.
61. Errata: When in sleep mode, if a GPIO interrupt happens simultaneously with a Timer0 or Sleep Timer interrupt, the GPIO interrupt may be missed, and the corresponding GPIO ISR not run. For more information, see the "Errata" on page 47.
62. Errata: If an interrupt is posted a short time (within 2.5 CPU cycles) before firmware commands the device to sleep, the interrupt will be missed. For more information, see the "Errata" on page 48.
63. Errata: Device wakes up from sleep when an analog interrupt is trigger. For more information, see the "Errata" on page 48.

DC POR and LVD Specifications

Table 22 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 22. DC POR and LVD Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{POR0}	1.66 V selected in PSoC Designer	V_{DD} must be greater than or equal to 1.71 V during startup, reset from the XRES pin, or reset from watchdog.	1.61	1.66	1.71	V
V_{POR1}	2.36 V selected in PSoC Designer		–	2.36	2.41	V
V_{POR2}	2.60 V selected in PSoC Designer		–	2.60	2.66	V
V_{POR3}	2.82 V selected in PSoC Designer		–	2.82	2.95	V
V_{LVD0}	2.45 V selected in PSoC Designer	–	2.40	2.45	2.51	V
V_{LVD1}	2.71 V selected in PSoC Designer		2.64[64]	2.71	2.78	V
V_{LVD2}	2.92 V selected in PSoC Designer		2.85[65]	2.92	2.99	V
V_{LVD3}	3.02 V selected in PSoC Designer		2.95[66]	3.02	3.09	V
V_{LVD4}	3.13 V selected in PSoC Designer		3.06	3.13	3.20	V
V_{LVD5}	1.90 V selected in PSoC Designer		1.84	1.90	2.32	V
V_{LVD6}	1.80 V selected in PSoC Designer		1.75[67]	1.80	1.84	V
V_{LVD7}	4.73 V selected in PSoC Designer		4.62	4.73	4.83	V

DC Programming Specifications

Table 23 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 23. DC Programming Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
$V_{DDIWRITE}$	Supply voltage for flash write operations	–	1.71	–	5.25	V
I_{DDP}	Supply current during programming or verify	–	–	5	25	mA
V_{ILP}	Input low voltage during programming or verify	See the appropriate DC GPIO Specifications on page 22	–	–	V_{IL}	V
V_{IHP}	Input high voltage during programming or verify	See the appropriate "DC GPIO Specifications" on page 22	V_{IH}	–	–	V
I_{ILP}	Input current when Applying V_{ILP} to P1[0] or P1[1] during programming or verify	Driving internal pull-down resistor	–	–	0.2	mA
I_{IHP}	Input current when applying V_{IHP} to P1[0] or P1[1] during programming or verify	Driving internal pull-down resistor	–	–	1.5	mA
V_{OLP}	Output low voltage during programming or verify	–	–	–	V_{SS} + 0.75	V
V_{OHP}	Output high voltage during programming or verify	See appropriate DC GPIO Specifications on page 22. For V_{DD} > 3 V use V_{OH4} in Table 12 on page 20.	V_{OH}	–	V_{DD}	V
$Flash_{ENPB}$	Flash write endurance	Erase/write cycles per block	50,000	–	–	–
$Flash_{DR}$	Flash data retention	Following maximum Flash write cycles; ambient temperature of 55 °C	20	–	–	Years

Notes
64. Always greater than 50 mV above V_{PPOR1} voltage for falling supply.
65. Always greater than 50 mV above V_{PPOR2} voltage for falling supply.
66. Always greater than 50 mV above V_{PPOR3} voltage for falling supply.
67. Always greater than 50 mV above V_{PPOR0} voltage for falling supply.

DC I²C Specifications

Table 24 list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 5.5 V and –40 °C ≤ T_A ≤ 85 °C, 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, or 1.71 V to 2.4 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 24. DC I²C Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{ILI2C}	Input low level	3.1 V ≤ V_{DD} ≤ 5.5 V	–	–	0.25 × V_{DD}	V
		2.5 V ≤ V_{DD} ≤ 3.0 V	–	–	0.3 × V_{DD}	V
		1.71 V ≤ V_{DD} ≤ 2.4 V	–	–	0.3 × V_{DD}	V
V_{IHI2C}	Input high level	1.71 V ≤ V_{DD} ≤ 5.5 V	0.65 × V_{DD}	–	–	V

DC Reference Buffer Specifications

Table 25 list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 5.5 V and –40 °C ≤ T_A ≤ 85 °C, 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, or 1.71 V to 2.4 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 25. DC Reference Buffer Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{Ref}	Reference buffer output	1.7 V ≤ V_{DD} ≤ 5.5 V	1	–	1.05	V
V_{RefHi}	Reference buffer output	1.7 V ≤ V_{DD} ≤ 5.5 V	1.2	–	1.25	V

DC IDAC Specifications

Table 26 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 26. DC IDAC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
IDAC_DNL	Differential nonlinearity	–4.5	–	+4.5	LSB	–
IDAC_INL	Integral nonlinearity	–5	–	+5	LSB	–
IDAC_Gain (Source)	Range = 0.5x	6.64	–	22.46	µA	DAC setting = 128 dec. Not recommended for CapSense applications.
	Range = 1x	14.5	–	47.8	µA	
	Range = 2x	42.7	–	92.3	µA	
	Range = 4x	91.1	–	170	µA	DAC setting = 128 dec
	Range = 8x	184.5	–	426.9	µA	DAC setting = 128 dec

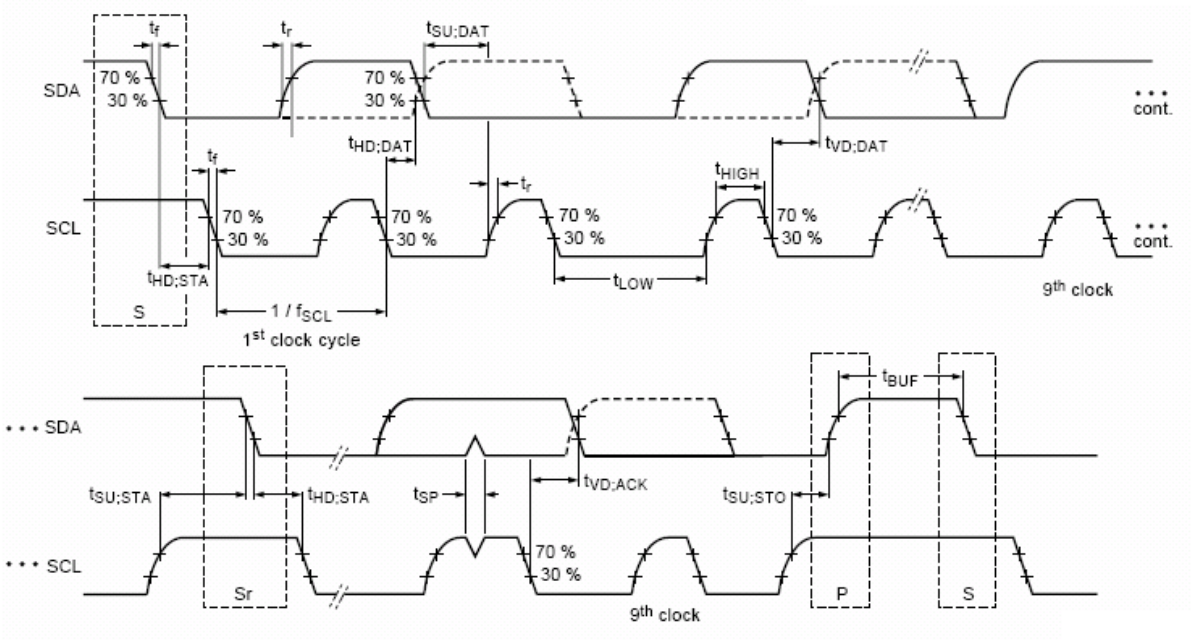
AC I²C Specifications

Table 34 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 34. AC Characteristics of the I²C SDA and SCL Pins

Symbol	Description	Standard Mode		Fast Mode		Units
		Min	Max	Min	Max	
f_{SCL}	SCL clock frequency	0	100	0	400	kHz
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated	4.0	–	0.6	–	µs
t_{LOW}	LOW period of the SCL clock	4.7	–	1.3	–	µs
t_{HIGH}	HIGH Period of the SCL clock	4.0	–	0.6	–	µs
$t_{SU;STA}$	Setup time for a repeated START condition	4.7	–	0.6	–	µs
$t_{HD;DAT}$	Data hold time	0	3.45	0	0.90	µs
$t_{SU;DAT}$	Data setup time	250	–	100[72]	–	ns
$t_{SU;STO}$	Setup time for STOP condition	4.0	–	0.6	–	µs
t_{BUF}	Bus free time between a STOP and START condition	4.7	–	1.3	–	µs
t_{SP}	Pulse width of spikes are suppressed by the input filter	–	–	0	50	ns

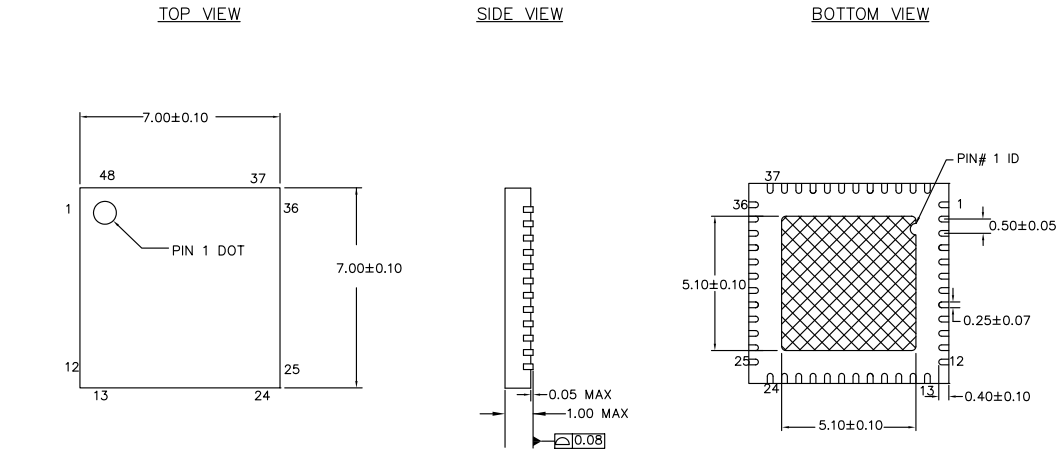
Figure 16. Definition for Timing for Fast/Standard Mode on the I²C Bus



Note

72. A Fast-Mode I²C-bus device can be used in a standard mode I²C-bus system, but the requirement $t_{SU;DAT} \geq 250$ ns must then be met. This automatically be the case if the device does not stretch the LOW period of the SCL signal. If such device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line $t_{rmax} + t_{SU;DAT} = 1000 + 250 = 1250$ ns (according to the Standard-Mode I²C-bus specification) before the SCL line is released.

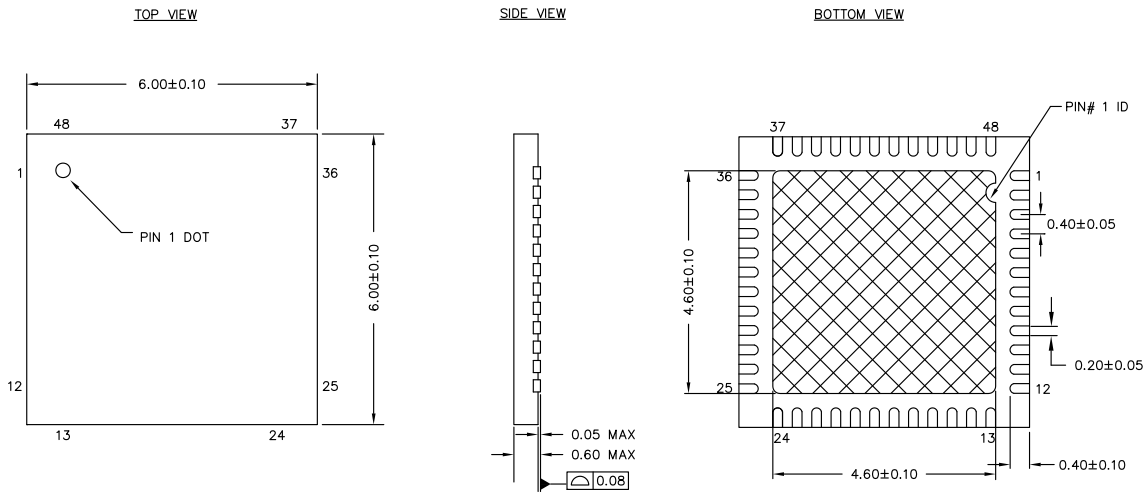
Figure 25. 48-pin QFN (7 × 7 × 1.0 mm) LT48A 5.1 × 5.1 E-Pad (Sawn) Package Outline, 001-13191



NOTES:
1. HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO−220
3. PACKAGE WEIGHT: 13 ± 1 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-13191 *H

Figure 26. 48-pin QFN (6 × 6 × 0.6 mm) LQ48A 4.6 × 4.6 E-Pad (Sawn) Package Outline, 001-57280



NOTES:
1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. REFERENCE JEDEC # MO−248
3. PACKAGE WEIGHT: 68 ±7 mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-57280 *E

Important Notes

- For information on the preferred dimensions for mounting QFN packages, see the following Application Note at http://www.amkor.com/products/notes_papers/MLFAppNote.pdf.
- Pinned vias for thermal conduction are not required for the low power PSoC device.

Thermal Impedances

Table 37. Thermal Impedances per Package

Package	Typical θ_{JA} [73]	Typical θ_{JC}
16-pin QFN (No Center Pad)	33 °C/W	–
24-pin QFN [74]	21 °C/W	–
32-pin QFN [74]	20 °C/W	–
48-pin SSOP	69 °C/W	–
48-pin QFN (6 × 6 × 0.6 mm) [74]	25.20 °C/W	3.04 °C/W
48-pin QFN (7 × 7 × 1.0 mm) [74]	18 °C/W	–
30-ball WLCSP	54 °C/W	–

Capacitance on Crystal Pins

Table 38. Typical Package Capacitance on Crystal Pins

Package	Package Capacitance
32-pin QFN	3.2 pF
48-pin QFN	3.3 pF

Solder Reflow Specifications

Table 39 shows the solder reflow temperature limits that must not be exceeded.

Table 39. Solder Reflow Specifications

Package	Maximum Peak Temperature (T_C)	Maximum Time above T_C – 5 °C
16-pin QFN	260 °C	30 seconds
24-pin QFN	260 °C	30 seconds
32-pin QFN	260 °C	30 seconds
48-pin SSOP	260 °C	30 seconds
48-pin QFN (6 × 6 × 0.6 mm)	260 °C	30 seconds
48-pin QFN (7 × 7 × 1.0 mm)	260 °C	30 seconds
30-ball WLCSP	260 °C	30 seconds

Notes
73. $T_J = T_A + \text{Power} \times \theta_{JA}$.
74. To achieve the thermal impedance specified for the QFN package, the center thermal pad must be soldered to the PCB ground plane.

CY3207ISSP In-System Serial Programmer (ISSP)

The CY3207ISSP is a production programmer. It includes protection circuitry and an industrial case that is more robust than the MiniProg in a production programming environment.
Note that CY3207ISSP needs special software and is not compatible with PSoC Programmer. The kit includes:

- CY3207 Programmer Unit
- PSoC ISSP Software CD
- 110 ~ 240 V Power Supply, Euro-Plug Adapter
- USB 2.0 Cable

Accessories (Emulation and Programming)

Table 40. Emulation and Programming Accessories

Part Number	Pin Package	Flex-Pod Kit[75]	Foot Kit[76]	Adapter[77]
CY8C20236A-24LKXI	16-pin QFN (No E-Pad)	CY3250-20246QFN	CY3250-20246QFN-POD	See note 74
CY8C20246A-24LKXI	16-pin QFN (No E-Pad)	CY3250-20246QFN	CY3250-20246QFN-POD	See note 77
CY8C20246AS-24LKXI	16-pin QFN (No E-Pad)	Not Supported		
CY8C20336A-24LQXI	24-pin QFN	CY3250-20346QFN	CY3250-20346QFN-POD	See note 74
CY8C20346A-24LQXI	24-pin QFN	CY3250-20346QFN	CY3250-20346QFN-POD	See note 77
CY8C20346AS-24LQXI	24-pin QFN	Not Supported		
CY8C20396A-24LQXI	24-pin QFN	Not Supported		
CY8C20436A-24LQXI	32-pin QFN	CY3250-20466QFN	CY3250-20466QFN-POD	See note 74
CY8C20446A-24LQXI	32-pin QFN	CY3250-20466QFN	CY3250-20466QFN-POD	See note 77
CY8C20446AS-24LQXI	32-pin QFN	Not Supported		
CY8C20466A-24LQXI	32-pin QFN	CY3250-20466QFN	CY3250-20466QFN-POD	See note 77
CY8C20466AS-24LQXI	32-pin QFN	Not Supported		
CY8C20496A-24LQXI	32-pin QFN	Not Supported		
CY8C20536A-24PVXI	48-pin SSOP	CY3250-20566	CY3250-20566-POD	See note 77
CY8C20546A-24PVXI	48-pin SSOP	CY3250-20566	CY3250-20566-POD	See note 77
CY8C20566A-24PVXI	48-pin SSOP	CY3250-20566	CY3250-20566-POD	See note 77

Third Party Tools

Several tools have been specially designed by third-party vendors to accompany PSoC devices during development and production. Specific details for each of these tools can be found at http://www.cypress.com under Documentation > Evaluation Boards.

Build a PSoC Emulator into Your Board

For details on how to emulate your circuit before going to volume production using an on-chip debug (OCD) non-production PSoC device, refer Application Note Debugging - Build a PSoC Emulator into Your Board – AN2323.

Notes
75. Flex-Pod kit includes a practice flex-pod and a practice PCB, in addition to two flex-pods.
76. Foot kit includes surface mount feet that can be soldered to the target PCB.
77. Programming adapter converts non-DIP package to DIP footprint. Specific details and ordering information for each of the adapters can be found at http://www.emulation.com.

Ordering Information

Table 41 lists the CY8C20XX6A/S PSoC devices' key package features and ordering codes.

Table 41. PSoC Device Key Features and Ordering Information

Package	Ordering Code	Flash (Bytes)	SRAM (Bytes)	CapSense Blocks	Digital I/O Pins	Analog Inputs [78]	XRES Pin	USB	ADC
16-pin (3 × 3 × 0.6 mm) QFN (no E-Pad)	CY8C20236A-24LKXI	8 K	1 K	1	13	13	Yes	No	Yes
16-pin (3 × 3 × 0.6 mm) QFN (no E-Pad) (Tape and Reel)	CY8C20236A-24LKXIT	8 K	1 K	1	13	13	Yes	No	Yes
16-pin (3 × 3 × 0.6 mm) QFN (no E-Pad)	CY8C20246A-24LKXI	16 K	2 K	1	13	13	Yes	No	Yes
16-pin (3 × 3 × 0.6 mm) QFN (no E-Pad)	CY8C20246AS-24LKXI	16 K	2 K	1	13	13	Yes	No	Yes
16-pin (3 × 3 × 0.6 mm) QFN (no E-Pad) (Tape and Reel)	CY8C20246A-24LKXIT	16 K	2 K	1	13	13	Yes	No	Yes
16-pin (3 × 3 × 0.6 mm) QFN (no E-Pad) (Tape and Reel)	CY8C20246AS-24LKXIT	16 K	2 K	1	13	13	Yes	No	Yes
24-pin (4 × 4 × 0.6 mm) QFN	CY8C20336A-24LQXI	8 K	1 K	1	20	20	Yes	No	Yes
24-pin (4 × 4 × 0.6 mm) QFN (Tape and Reel)	CY8C20336A-24LQXIT	8 K	1 K	1	20	20	Yes	No	Yes
24-pin (4 × 4 × 0.6 mm) QFN	CY8C20346A-24LQXI	16 K	2 K	1	20	20	Yes	No	Yes
24-pin (4 × 4 × 0.6 mm) QFN	CY8C20346AS-24LQXI	16 K	2 K	1	20	20	Yes	No	Yes
24-pin (4 × 4 × 0.6 mm) QFN (Tape and Reel)	CY8C20346A-24LQXIT	16 K	2 K	1	20	20	Yes	No	Yes
24-pin (4 × 4 × 0.6 mm) QFN (Tape and Reel)	CY8C20346AS-24LQXIT	16 K	2 K	1	20	20	Yes	No	Yes
24-pin (4 × 4 × 0.6 mm) QFN	CY8C20396A-24LQXI	16 K	2 K	1	19	19	Yes	Yes	Yes
24-pin (4 × 4 × 0.6 mm) QFN (Tape and Reel)	CY8C20396A-24LQXIT	16 K	2 K	1	19	19	Yes	Yes	Yes
32-pin (5 × 5 × 0.6 mm) QFN	CY8C20436A-24LQXI	8 K	1 K	1	28	28	Yes	No	Yes
32-pin (5 × 5 × 0.6 mm) QFN (Tape and Reel)	CY8C20436A-24LQXIT	8 K	1 K	1	28	28	Yes	No	Yes
32-pin (5 × 5 × 0.6 mm) QFN	CY8C20446A-24LQXI	16 K	2 K	1	28	28	Yes	No	Yes
32-pin (5 × 5 × 0.6 mm) QFN	CY8C20446AS-24LQXI	16 K	2 K	1	28	28	Yes	No	Yes
32-pin (5 × 5 × 0.6 mm) QFN (Tape and Reel)	CY8C20446A-24LQXIT	16 K	2 K	1	28	28	Yes	No	Yes
32-pin (5 × 5 × 0.6 mm) QFN (Tape and Reel)	CY8C20446AS-24LQXIT	16 K	2 K	1	28	28	Yes	No	Yes
32-pin (5 × 5 × 0.6 mm) QFN	CY8C20466A-24LQXI	32 K	2 K	1	28	28	Yes	No	Yes
32-pin (5 × 5 × 0.6 mm) QFN	CY8C20466AS-24LQXI	32 K	2 K	1	28	28	Yes	No	Yes
32-pin (5 × 5 × 0.6 mm) QFN (Tape and Reel)	CY8C20466A-24LQXIT	32 K	2 K	1	28	28	Yes	No	Yes
32-pin (5 × 5 × 0.6 mm) QFN (Tape and Reel)	CY8C20466AS-24LQXIT	32 K	2 K	1	28	28	Yes	No	Yes
32-pin (5 × 5 × 0.6 mm) QFN	CY8C20496A-24LQXI	16 K	2 K	1	25	25	Yes	Yes	Yes
32-pin (5 × 5 × 0.6 mm) QFN (Tape and Reel)	CY8C20496A-24LQXIT	16 K	2 K	1	25	25	Yes	Yes	Yes

Notes
78. Dual-function Digital I/O Pins also connect to the common analog mux.
79. Not Recommended for New Designs.

Table 41. PSoC Device Key Features and Ordering Information *(continued)*

Package	Ordering Code	Flash (Bytes)	SRAM (Bytes)	CapSense Blocks	Digital I/O Pins	Analog Inputs [78]	XRES Pin	USB	ADC
48-pin SSOP [79]	CY8C20536A-24PVXI [79]	8 K	1 K	1	34	34	Yes	No	Yes
48-pin SSOP (Tape and Reel) [79]	CY8C20536A-24PVXIT [79]	8 K	1 K	1	34	34	Yes	No	Yes
48-pin SSOP [79]	CY8C20546A-24PVXI [79]	16 K	2 K	1	34	34	Yes	No	Yes
48-pin SSOP (Tape and Reel) [79]	CY8C20546A-24PVXIT [79]	16 K	2 K	1	34	34	Yes	No	Yes
48-pin SSOP [79]	CY8C20566A-24PVXI [79]	32 K	2 K	1	34	34	Yes	No	Yes
48-pin SSOP (Tape and Reel) [79]	CY8C20566A-24PVXIT [79]	32 K	2 K	1	34	34	Yes	No	Yes
48-pin (6 × 6 × 0.6 mm) QFN	CY8C20636A-24LQXI	8 K	1 K	1	36	36	Yes	No	Yes
48-pin (6 × 6 × 0.6 mm) QFN (Tape and Reel)	CY8C20636A-24LQXIT	8 K	1 K	1	36	36	Yes	No	Yes
48-pin (7 × 7 × 1.0 mm) QFN [79]	CY8C20636A-24LTXI [79]	8 K	1 K	1	36	36	Yes	No	Yes
48-pin (7 × 7 × 1.0 mm) QFN (Tape and Reel) [79]	CY8C20636A-24LTXIT [79]	8 K	1 K	1	36	36	Yes	No	Yes
48-pin (6 × 6 × 0.6 mm) QFN	CY8C20646A-24LQXI	16 K	2 K	1	36	36	Yes	Yes	Yes
48-pin (6 × 6 × 0.6 mm) QFN (Tape and Reel)	CY8C20646A-24LQXIT	16 K	2 K	1	36	36	Yes	Yes	Yes
48-pin (7 × 7 × 1.0 mm) QFN [79]	CY8C20646A-24LTXI [79]	16 K	2 K	1	36	36	Yes	Yes	Yes
48-pin (7 × 7 × 1.0 mm) QFN (Tape and Reel) [79]	CY8C20646A-24LTXIT [79]	16 K	2 K	1	36	36	Yes	Yes	Yes
48-pin (6 × 6 × 0.6 mm) QFN	CY8C20666A-24LQXI	32 K	2 K	1	36	36	Yes	Yes	Yes
48-pin (6 × 6 × 0.6 mm) QFN (Tape and Reel)	CY8C20666A-24LQXIT	32 K	2 K	1	36	36	Yes	Yes	Yes
48-pin (7 × 7 × 1.0 mm) QFN [79]	CY8C20666A-24LTXI [79]	32 K	2 K	1	36	36	Yes	Yes	Yes
48-pin (7 × 7 × 1.0 mm) QFN [79]	CY8C20666AS-24LTXI [79]	32 K	2 K	1	36	36	Yes	Yes	Yes
48-pin (7 × 7 × 1.0 mm) QFN (Tape and Reel) [79]	CY8C20666A-24LTXIT [79]	32 K	2 K	1	36	36	Yes	Yes	Yes
48-pin (7 × 7 × 1.0 mm) QFN (Tape and Reel) [79]	CY8C20666AS-24LTXIT [79]	32 K	2 K	1	36	36	Yes	Yes	Yes
48-pin (7 × 7 × 1.0 mm) QFN (OCD) [78]	CY8C20066A-24LTXI [78]	32 K	2 K	1	36	36	Yes	Yes	Yes
30-ball WLCSP	CY8C20746A-24FDXC	16 K	1 K	1	27	27	Yes	No	Yes
30-ball WLCSP (Tape and Reel)	CY8C20746A-24FDXCT	16 K	1 K	1	27	27	Yes	No	Yes
30-ball WLCSP	CY8C20766A-24FDXC	32 K	2 K	1	27	27	Yes	No	Yes
30-ball WLCSP (Tape and Reel)	CY8C20766A-24FDXCT	32 K	2 K	1	27	27	Yes	No	Yes
24-pin (4 × 4 × 0.6 mm) QFN	CY8C20336AN-24LQXI	8 K	1 K	1	20	20	Yes	No	No
24-pin (4 × 4 × 0.6 mm) QFN (Tape and Reel)	CY8C20336AN-24LQXIT	8 K	1 K	1	20	20	Yes	No	No
32-pin (5 × 5 × 0.6 mm) QFN	CY8C20436AN-24LQXI	8 K	1 K	1	28	28	Yes	No	No
32-pin (5 × 5 × 0.6 mm) QFN (Tape and Reel)	CY8C20436AN-24LQXIT	8 K	1 K	1	28	28	Yes	No	No
16-pin (3 × 3 × 0.6 mm) QFN (no E-Pad)	CY8C20246AS-24LKXI	16 K	2 K	1	13	13	Yes	No	Yes
16-pin (3 × 3 × 0.6 mm) QFN (no E-Pad, Tape and Reel)	CY8C20246AS-24LKXIT	16 K	2 K	1	13	13	Yes	No	Yes

Notes
78. Dual-function Digital I/O Pins also connect to the common analog mux.
79. Not Recommended for New Designs.

5. Missed Interrupt During Transition to Sleep

■ **Problem Definition**

If an interrupt is posted a short time (within 2.5 CPU cycles) before firmware commands the device to sleep, the interrupt will be missed.

■ **Parameters Affected**

No datasheet parameters are affected.

■ **Trigger Condition(S)**

Triggered by enabling sleep mode just prior to an interrupt.

■ **Scope of Impact**

The relevant interrupt service routine will not be run.

■ **Workaround**

None.

■ **Fix Status**

Will not be fixed

■ **Changes**

None

6. Wakeup from sleep with analog interrupt

■ **Problem Definition**

Device wakes up from sleep when an analog interrupt is trigger

■ **Parameters Affected**

No datasheet parameters are affected.

■ **Trigger Condition(S)**

Triggered by enabling analog interrupt during sleep mode when device operating temperature is 50 °C or above

■ **Scope of Impact**

Device unexpectedly wakes up from sleep

■ **Workaround**

Disable the analog interrupt before entering sleep and turn it back on upon wakeup.

■ **Fix Status**

Will not be fixed

■ **Changes**

None

Document History Page *(continued)*

Document Title: CY8C20XX6A/S, 1.8 V Programmable CapSense® Controller with SmartSense™ Auto-tuning 1–33 Buttons, 0–6 Sliders Document Number: 001-54459				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*P	3774062	UBU	10/11/2012	Updated Electrical Specifications: Updated AC Chip-Level Specifications: Updated Table 27: Changed minimum value of F_{32K1} parameter from 19 kHz to 15 kHz. Updated Packaging Information: spec 001-09116 – Changed revision from *F to *G. spec 001-13937 – Changed revision from *D to *E. spec 51-85061 – Changed revision from *E to *F. spec 001-13191 – Changed revision from *F to *G. spec 001-57280 – Changed revision from *C to *D.
*Q	3807186	PKS	15/11/2012	No content update; appended to EROS document.
*R	3836626	SRLI	01/03/2013	Updated Document Title to read as “CY8C20XX6A/S, 1.8 V Programmable CapSense® Controller with SmartSense™ Auto-tuning 1–33 Buttons, 0–6 Sliders”. Updated Features. Updated PSoC® Functional Overview: Replaced “CY8C20X36A/46A/66A/96A/46AS/66AS” with “CY8C20XX6A/S”. Updated Getting Started: Replaced “CY8C20X36A/46A/66A/96A/46AS/66AS” with “CY8C20XX6A/S”. Updated Pinouts: Updated 16-pin QFN (10 Sensing Inputs)[3, 4]: Replaced “12 Sensing Inputs” with “10 Sensing Inputs” in heading, added Note 3 only. Updated 24-pin QFN (17 Sensing Inputs) [8]: Replaced “12 Sensing Inputs” with “17 Sensing Inputs” in heading, added Note 8 only. Updated 24-pin QFN (15 Sensing Inputs (With USB)) [13]: Replaced “18 Sensing Inputs” with “15 Sensing Inputs” in heading, added Note 13 only. Updated 30-ball WLCSP (24 Sensing Inputs) [18]: Replaced “26 Sensing Inputs” with “24 Sensing Inputs” in heading, added Note 18 only. Updated 32-pin QFN (25 Sensing Inputs) [22]: Replaced “27 Sensing Inputs” with “25 Sensing Inputs” in heading, added Note 22 only. updated 32-pin QFN (22 Sensing Inputs (With USB)) [27]: Replaced “24 Sensing Inputs” with “22 Sensing Inputs” in heading, added Note 27 only. Updated 48-pin SSOP (31 Sensing Inputs) [32]: Replaced “33 Sensing Inputs” with “31 Sensing Inputs” in heading, added Note 32 only. Updated 48-pin QFN (33 Sensing Inputs) [36]: Replaced “35 Sensing Inputs” with “33 Sensing Inputs” in heading, added Note 36 only. Updated 48-pin QFN (33 Sensing Inputs (With USB)) [41]: Replaced “35 Sensing Inputs” with “33 Sensing Inputs” in heading, added Note 41 only. Updated 48-pin QFN (OCD) (33 Sensing Inputs) [46]: Added “33 Sensing Inputs” in heading, added Note 46 only. Updated Packaging Information: spec 001-42168 – Changed revision from *D to *E. spec 001-57280 – Changed revision from *D to *E.
*S	3997568	BVI	05/11/2013	Added Errata.
*T	4044148	BVI	06/28/2013	Added Errata Footnotes. Updated Packaging Information: spec 001-09116 – Changed revision from *G to *H. Updated to new template.

Document History Page *(continued)*

Document Title: CY8C20XX6A/S, 1.8 V Programmable CapSense® Controller with SmartSense™ Auto-tuning 1–33 Buttons, 0–6 Sliders Document Number: 001-54459				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
*U	4185313	BVI	11/07/2013	Updated Features. Updated Packaging Information: spec 001-09116 – Changed revision from *H to *I.
*V	4622119	SSHH	01/13/2015	Added More Information.
*W	4825924	SSHH	07/07/2015	Updated Pinouts: Updated 16-pin QFN (10 Sensing Inputs)[3, 4]: Updated Table 1: Added Note 7 and referred the same note in description of V_{SS} pin. Updated 24-pin QFN (17 Sensing Inputs) [8]: Updated Table 2: Added Note 12 and referred the same note in description of V_{SS} pin. Updated 24-pin QFN (15 Sensing Inputs (With USB)) [13]: Updated Table 3: Added Note 17 and referred the same note in description of V_{SS} pin. Updated 30-ball WLCSP (24 Sensing Inputs) [18]: Updated Table 4: Added Note 21 and referred the same note in description of V_{SS} pin. Updated 32-pin QFN (25 Sensing Inputs) [22]: Updated Table 5: Added Note 26 and referred the same note in description of V_{SS} pin. Updated 32-pin QFN (22 Sensing Inputs (With USB)) [27]: Updated Table 6: Added Note 31 and referred the same note in description of V_{SS} pin. Updated 48-pin SSOP (31 Sensing Inputs) [32]: Updated Table 7: Added Note 35 and referred the same note in description of V_{SS} pin. Updated 48-pin QFN (33 Sensing Inputs) [36]: Updated Table 8: Added Note 40 and referred the same note in description of V_{SS} pin. Updated 48-pin QFN (33 Sensing Inputs (With USB)) [41]: Updated Table 9: Added Note 45 and referred the same note in description of V_{SS} pin. Updated 48-pin QFN (OCD) (33 Sensing Inputs) [46]: Updated Table 10: Added Note 52 and referred the same note in description of V_{SS} pin. Updated Ordering Information: Removed prune part numbers (CY8C20636AN-24LTXI and CY8C20636AN-24LTXIT). Updated Packaging Information: spec 001-13937 – Changed revision from *E to *F. spec 001-13191 – Changed revision from *G to *H.
*X	5394582	SSHH	08/08/2016	Updated to new template. Completing Sunset Review.