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Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

Embedded - Microcontrollers - Application Specific represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	Capacitive Sensing
Core Processor	M8C
Program Memory Type	FLASH (32kB)
Controller Series	CY8C20xx6A
RAM Size	2K x 8
Interface	I²C, SPI, USB
Number of I/O	36
Voltage - Supply	1.71V ~ 5.5V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	48-UFQFN Exposed Pad
Supplier Device Package	48-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c20666as-24lqxit

More Information

Cypress provides a wealth of data at www.cypress.com to help you to select the right PSoC device for your design, and to help you to quickly and effectively integrate the device into your design. For a comprehensive list of resources, see the knowledge base article KBA92181, Resources Available for CapSense® Controllers. Following is an abbreviated list for CapSense devices:

- Overview: CapSense Portfolio, CapSense Roadmap
- Product Selectors: CapSense, CapSense Plus, CapSense Express, PSoC3 with CapSense, PSoC5 with CapSense, PSoC4. In addition, PSoC Designer offers a device selection tool at the time of creating a new project.
- Application notes: Cypress offers CapSense application notes covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with CapSense are:
  - AN64846: Getting Started With CapSense
  - AN73034: CY8C20xx6A/H/AS CapSense® Design Guide
  - AN2397: CapSense® Data Viewing Tools
- Technical Reference Manual (TRM):
  - PSoC® CY8C20xx6A/AS/L Family Technical Reference Manual
- Development Kits:
  - CY3280-20x66 Universal CapSense Controller Kit features a predefined control circuitry and plug-in hardware to make prototyping and debugging easy. Programming and I2C-to-USB Bridge hardware are included for tuning and data acquisition.
  - CY3280-BMM Matrix Button Module Kit consists of eight CapSense sensors organized in a 4x4 matrix format to form 16 physical buttons and eight LEDs. This module connects to any CY3280 Universal CapSense Controller Board, including CY3280-20x66 Universal CapSense Controller.
  - CY3280-BSM Simple Button Module Kit consists of ten CapSense buttons and ten LEDs. This module connects to any CY3280 Universal CapSense Controller Board, including CY3280-20x66 Universal CapSense Controller.

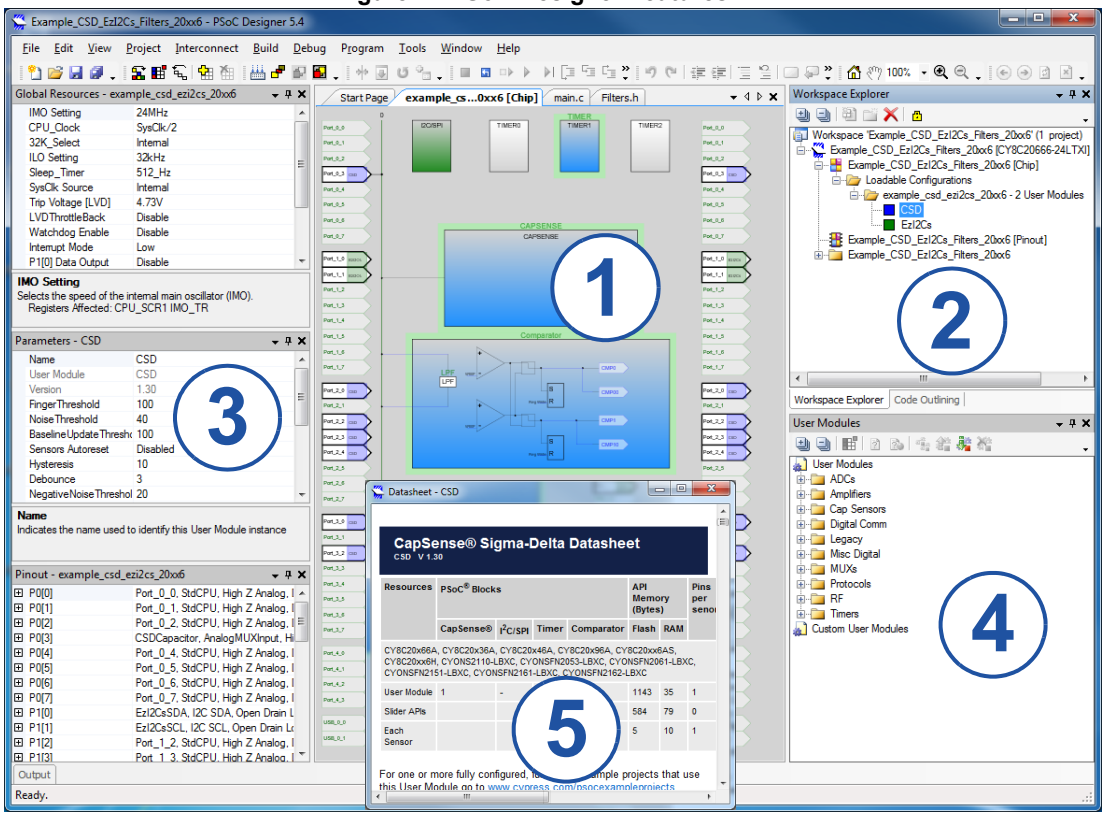
The CY3217-MiniProg1 and CY8CKIT-002 PSoC® MiniProg3 device provides an interface for flash programming.

PSoC Designer

PSoC Designer is a free Windows-based Integrated Design Environment (IDE). It enables concurrent hardware and firmware design of systems based on CapSense (see Figure 1). With PSoC Designer, you can:

1. Drag and drop User Modules to build your hardware system design in the main design workspace
2. Codesign your application firmware with the PSoC hardware, using the PSoC Designer IDE C compiler
3. Configure User Module
4. Explore the library of user modules
5. Review user module datasheets

Figure 1. PSoC Designer Features



PSoC® Functional Overview

The PSoC family consists of on-chip controller devices, which are designed to replace multiple traditional microcontroller unit (MCU)-based components with one, low cost single-chip programmable component. A PSoC device includes configurable analog and digital blocks, and programmable interconnect. This architecture allows the user to create customized peripheral configurations, to match the requirements of each individual application. Additionally, a fast CPU, Flash program memory, SRAM data memory, and configurable I/O are included in a range of convenient pinouts.

The architecture for this device family, as shown in the Logic Block Diagram on page 2, consists of three main areas:

- The Core
- CapSense Analog System
- System Resources (including a full-speed USB port).

A common, versatile bus allows connection between I/O and the analog system.

Each CY8C20XX6A/S PSoC device includes a dedicated CapSense block that provides sensing and scanning control circuitry for capacitive sensing applications. Depending on the PSoC package, up to 36 GPIO are also included. The GPIO provides access to the MCU and analog mux.

PSoC Core

The PSoC Core is a powerful engine that supports a rich instruction set. It encompasses SRAM for data storage, an interrupt controller, sleep and watchdog timers, and IMO and ILO. The CPU core, called the M8C, is a powerful processor with speeds up to 24 MHz. The M8C is a 4-MIPS, 8-bit Harvard-architecture microprocessor.

CapSense System

The analog system contains the capacitive sensing hardware. Several hardware algorithms are supported. This hardware performs capacitive sensing and scanning without requiring external components. The analog system is composed of the CapSense PSoC block and an internal 1 V or 1.2 V analog reference, which together support capacitive sensing of up to 33 inputs [2]. Capacitive sensing is configurable on each GPIO pin. Scanning of enabled CapSense pins are completed quickly and easily across multiple ports.

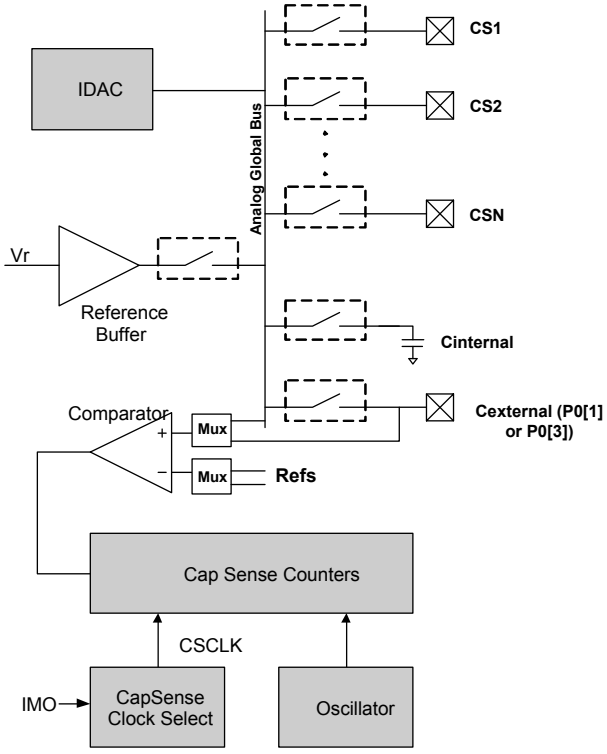
SmartSense

SmartSense is an innovative solution from Cypress that removes manual tuning of CapSense applications. This solution is easy to use and provides a robust noise immunity. It is the only auto-tuning solution that establishes, monitors, and maintains all required tuning parameters. SmartSense allows engineers to go from prototyping to mass production without re-tuning for manufacturing variations in PCB and/or overlay material properties.

SmartSense_EMC

In addition to the SmartSense auto tuning algorithm to remove manual tuning of CapSense applications, SmartSense_EMC user module incorporates a unique algorithm to improve robustness of capacitive sensing algorithm/circuit against high frequency conducted and radiated noise. Every electronic device must comply with specific limits for radiated and conducted external noise and these limits are specified by regulatory bodies (for example, FCC, CE, U/L and so on). A very good PCB layout design, power supply design and system design is a mandatory for a product to pass the conducted and radiated noise tests. An ideal PCB layout, power supply design or system design is not often possible because of cost and form factor limitations of the product. SmartSense_EMC with superior noise immunity is well suited and handy for such applications to pass radiated and conducted noise test.

Figure 2. CapSense System Block Diagram



Note
2. 36 GPIOs = 33 pins for capacitive sensing + 2 pins for I^2C + 1 pin for modulator capacitor.

Getting Started

The quickest way to understand PSoC silicon is to read this datasheet and then use the PSoC Designer Integrated Development Environment (IDE). This datasheet is an overview of the PSoC integrated circuit and presents specific pin, register, and electrical specifications.

For in depth information, along with detailed programming details, see the Technical Reference Manual for the CY8C20XX6A/S PSoC devices.

For up-to-date ordering, packaging, and electrical specification information, see the latest PSoC device datasheets on the web at www.cypress.com/psoc.

CapSense Design Guides

Design Guides are an excellent introduction to the wide variety of possible CapSense designs. They are located at www.cypress.com/go/CapSenseDesignGuides.

Refer Getting Started with CapSense design guide for information on CapSense design and CY8C20XX6A/H/AS CapSense® Design Guide for specific information on CY8C20XX6A/AS CapSense controllers.

Silicon Errata

Errata documents known issues with silicon including errata trigger conditions, scope of impact, available workarounds and silicon revision applicability. Refer to Silicon Errata for the PSoC® CY8C20x36A/46A/66A/96A/46AS/66AS/36H/46H families available at http://www.cypress.com/?rID=56239 for errata information on CY8C20xx6A/AS/H family of device. Compare errata document with datasheet for a complete functional description of device.

Development Kits

PSoC Development Kits are available online from and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

Training

Free PSoC technical training (on demand, webinars, and workshops), which is available online via www.cypress.com, covers a wide variety of topics and skill levels to assist you in your designs.

CYPros Consultants

Certified PSoC consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC consultant go to the CYPros Consultants web site.

Solutions Library

Visit our growing library of solution focused designs. Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

Technical Support

Technical support – including a searchable Knowledge Base articles and technical forums – is also available online. If you cannot find an answer to your question, call our Technical Support hotline at 1-800-541-4736.

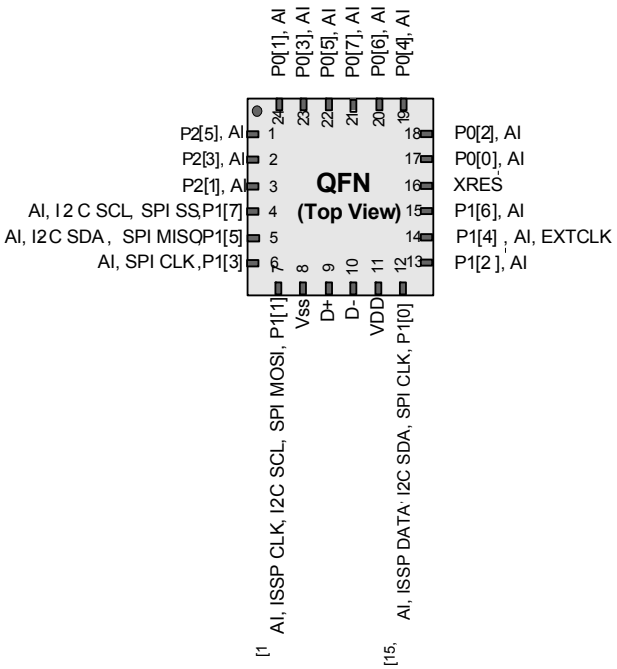
24-pin QFN (15 Sensing Inputs (With USB)) [13]

Table 3. Pin Definitions – CY8C20396A [14]

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I	P2[5]	
2	I/O	I	P2[3]	
3	I/O	I	P2[1]	
4	IOHR	I	P1[7]	I^2C SCL, SPI SS
5	IOHR	I	P1[5]	I^2C SDA, SPI MISO
6	IOHR	I	P1[3]	SPI CLK
7	IOHR	I	P1[1]	ISSP CLK[15], I^2C SCL, SPI MOSI
8	Power		V_{SS}	Ground[17]
9	I/O	I	D+	USB D+
10	I/O	I	D-	USB D-
11	Power		V_{DD}	Supply
12	IOHR	I	P1[0]	ISSP DATA[15], I^2C SDA, SPI CLK[16]
13	IOHR	I	P1[2]	
14	IOHR	I	P1[4]	Optional external clock input (EXTCLK)
15	IOHR	I	P1[6]	
16	RESET INPUT		XRES	Active high external reset with internal pull-down
17	IOH	I	P0[0]	
18	IOH	I	P0[2]	
19	IOH	I	P0[4]	
20	IOH	I	P0[6]	
21	IOH	I	P0[7]	
22	IOH	I	P0[5]	
23	IOH	I	P0[3]	Integrating input
24	IOH	I	P0[1]	Integrating input
CP	Power		V_{SS}	Center pad must be connected to Ground

LEGEND I = Input, O = Output, OH = 5 mA High Output Drive, R = Regulated Output

Figure 5. CY8C20396A



Notes
13. 20 GPIOs = 15 pins for capacitive sensing + 2 pins for I2C + 2 pins for USB + 1 pin for modulation capacitor.
14. The center pad (CP) on the QFN package must be connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it must be electrically floated and not connected to any other signal.
15. On power-up, the SDA(P1[0]) drives a strong high for 256 sleep clock cycles and drives resistive low for the next 256 sleep clock cycles. The SCL(P1[1]) line drives resistive low for 512 sleep clock cycles and both the pins transition to high impedance state. On reset, after XRES de-asserts, the SDA and the SCL lines drive resistive low for 8 sleep clock cycles and transition to high impedance state. Hence, during power-up or reset event, P1[1] and P1[0] may disturb the I2C bus. Use alternate pins if you encounter issues.
16. Alternate SPI clock.
17. All VSS pins should be brought out to one common GND plane.

DC Chip-Level Specifications

Table 13 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 13. DC Chip-Level Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{DD}[54, 55, 56, 57]	Supply voltage	No USB activity. Refer the table "DC POR and LVD Specifications" on page 26	1.71	–	5.50	V
V_{DDUSB}[54, 55, 56, 57]	Operating voltage	USB activity, USB regulator enabled	4.35	–	5.25	V
		USB activity, USB regulator bypassed	3.15	3.3	3.60	V
I_{DD24}	Supply current, IMO = 24 MHz	Conditions are $V_{DD} \leq 3.0$ V, $T_A = 25$ °C, CPU = 24 MHz. CapSense running at 12 MHz, no I/O sourcing current	–	2.88	4.00	mA
I_{DD12}	Supply current, IMO = 12 MHz	Conditions are $V_{DD} \leq 3.0$ V, $T_A = 25$ °C, CPU = 12 MHz. CapSense running at 12 MHz, no I/O sourcing current	–	1.71	2.60	mA
I_{DD6}	Supply current, IMO = 6 MHz	Conditions are $V_{DD} \leq 3.0$ V, $T_A = 25$ °C, CPU = 6 MHz. CapSense running at 6 MHz, no I/O sourcing current	–	1.16	1.80	mA
$I_{DDAVG10}$	Average supply current per sensor	One sensor scanned at 10 mS rate	–	250	–	µA
$I_{DDAVG100}$	Average supply current per sensor	One sensor scanned at 100 mS rate	–	25	–	µA
$I_{DDAVG500}$	Average supply current per sensor	One sensor scanned at 500 mS rate	–	7	–	µA
I_{SB0}[58, 59, 60, 61, 62, 63]	Deep sleep current	$V_{DD} \leq 3.0$ V, $T_A = 25$ °C, I/O regulator turned off	–	0.10	1.05	µA
I_{SB1}[58, 59, 60, 61, 62, 63]	Standby current with POR, LVD and sleep timer	$V_{DD} \leq 3.0$ V, $T_A = 25$ °C, I/O regulator turned off	–	1.07	1.50	µA
I_{SBI2C}[58, 59, 60, 61, 62, 63]	Standby current with I^2C enabled	Conditions are $V_{DD} = 3.3$ V, $T_A = 25$ °C and CPU = 24 MHz	–	1.64	–	µA

Notes

54. When V_{DD} remains in the range from 1.71 V to 1.9 V for more than 50 µs, the slew rate when moving from the 1.71 V to 1.9 V range to greater than 2 V must be slower than 1 V/500 µs to avoid triggering POR. The only other restriction on slew rates for any other voltage range or transition is the SR_{POWER_UP} parameter.
55. If powering down in standby sleep mode, to properly detect and recover from a V_{DD} brown out condition any of the following actions must be taken:
    a. Bring the device out of sleep before powering down.
    b. Assure that V_{DD} falls below 100 mV before powering back up.
    c. Set the No Buzz bit in the OSC_CR0 register to keep the voltage monitoring circuit powered during sleep.
    d. Increase the buzz rate to assure that the falling edge of V_{DD} is captured. The rate is configured through the PSSDC bits in the SLP_CFG register.
    For the referenced registers, refer to the *CY8C20X36 Technical Reference Manual*. In deep sleep mode, additional low power voltage monitoring circuitry allows V_{DD} brown out conditions to be detected for edge rates slower than 1V/ms.
56. For USB mode, the V_{DD} supply for bus-powered application should be limited to 4.35 V–5.35 V. For self-powered application, V_{DD} should be 3.15 V–3.45 V.
57. For proper CapSense block functionality, if the drop in V_{DD} exceeds 5% of the base V_{DD}, the rate at which V_{DD} drops should not exceed 200 mV/s. Base V_{DD} can be between 1.8 V and 5.5 V.
58. Errata: When the device is put to sleep in Standby or I2C_USB Mode and the bandgap circuit is refreshed less frequently than every 8 ms (default), the device may not come out of sleep when a sleep-ending input is received. For more information, see the "Errata" on page 46.
59. Errata: The I2C block exhibits occasional data and bus corruption errors when the I2C master initiates transactions while the device is in or out of transition of sleep mode. For more information, see the "Errata" on page 46.
60. Errata: When programmable timer 0 is used in "one-shot" mode by setting bit 1 of register 0,B0h (PT0_CFG), and the timer interrupt is used to wake the device from sleep, the interrupt service routine (ISR) may be executed twice. For more information, see the "Errata" on page 47.
61. Errata: When in sleep mode, if a GPIO interrupt happens simultaneously with a Timer0 or Sleep Timer interrupt, the GPIO interrupt may be missed, and the corresponding GPIO ISR not run. For more information, see the "Errata" on page 47.
62. Errata: If an interrupt is posted a short time (within 2.5 CPU cycles) before firmware commands the device to sleep, the interrupt will be missed. For more information, see the "Errata" on page 48.
63. Errata: Device wakes up from sleep when an analog interrupt is trigger. For more information, see the "Errata" on page 48.

DC GPIO Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 5.5 V and –40 °C ≤ T_A ≤ 85 °C, 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, or 1.71 V to 2.4 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 C and are for design guidance only.

Table 14. 3.0 V to 5.5 V DC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{PU}	Pull-up resistor	–	4	5.60	8	kΩ
V_{OH1}	High output voltage Port 2 or 3 or 4 pins	I_{OH} ≤ 10 µA, maximum of 10 mA source current in all I/Os	V_{DD} – 0.20	–	–	V
V_{OH2}	High output voltage Port 2 or 3 or 4 pins	I_{OH} = 1 mA, maximum of 20 mA source current in all I/Os	V_{DD} – 0.90	–	–	V
V_{OH3}	High output voltage Port 0 or 1 pins with LDO regulator Disabled for port 1	I_{OH} < 10 µA, maximum of 10 mA source current in all I/Os	V_{DD} – 0.20	–	–	V
V_{OH4}	High output voltage Port 0 or 1 pins with LDO regulator Disabled for port 1	I_{OH} = 5 mA, maximum of 20 mA source current in all I/Os	V_{DD} – 0.90	–	–	V
V_{OH5}	High output voltage Port 1 Pins with LDO Regulator Enabled for 3 V out	I_{OH} < 10 µA, V_{DD} > 3.1 V, maximum of 4 I/Os all sourcing 5 mA	2.85	3.00	3.30	V
V_{OH6}	High output voltage Port 1 pins with LDO regulator enabled for 3 V out	I_{OH} = 5 mA, V_{DD} > 3.1 V, maximum of 20 mA source current in all I/Os	2.20	–	–	V
V_{OH7}	High output voltage Port 1 pins with LDO enabled for 2.5 V out	I_{OH} < 10 µA, V_{DD} > 2.7 V, maximum of 20 mA source current in all I/Os	2.35	2.50	2.75	V
V_{OH8}	High output voltage Port 1 pins with LDO enabled for 2.5 V out	I_{OH} = 2 mA, V_{DD} > 2.7 V, maximum of 20 mA source current in all I/Os	1.90	–	–	V
V_{OH9}	High output voltage Port 1 pins with LDO enabled for 1.8 V out	I_{OH} < 10 µA, V_{DD} > 2.7 V, maximum of 20 mA source current in all I/Os	1.60	1.80	2.10	V
V_{OH10}	High output voltage Port 1 pins with LDO enabled for 1.8 V out	I_{OH} = 1 mA, V_{DD} > 2.7 V, maximum of 20 mA source current in all I/Os	1.20	–	–	V
V_{OL}	Low output voltage	I_{OL} = 25 mA, V_{DD} > 3.3 V, maximum of 60 mA sink current on even port pins (for example, P0[2] and P1[4]) and 60 mA sink current on odd port pins (for example, P0[3] and P1[5])	–	–	0.75	V
V_{IL}	Input low voltage	–	–	–	0.80	V
V_{IH}	Input high voltage	–	2.00	–	–	V
V_H	Input hysteresis voltage	–	–	80	–	mV
I_{IL}	Input leakage (Absolute Value)	–	–	0.001	1	µA
C_{PIN}	Pin capacitance	Package and pin dependent Temp = 25 °C	0.50	1.70	7	pF
$V_{ILLVT3.3}$	Input Low Voltage with low threshold enable set, Enable for Port1	Bit3 of IO_CFG1 set to enable low threshold voltage of Port1 input	0.8	V	–	–
$V_{IHLVT3.3}$	Input High Voltage with low threshold enable set, Enable for Port1	Bit3 of IO_CFG1 set to enable low threshold voltage of Port1 input	1.4	–	–	V
$V_{ILLVT5.5}$	Input Low Voltage with low threshold enable set, Enable for Port1	Bit3 of IO_CFG1 set to enable low threshold voltage of Port1 input	0.8	V	–	–
$V_{IHLVT5.5}$	Input High Voltage with low threshold enable set, Enable for Port1	Bit3 of IO_CFG1 set to enable low threshold voltage of Port1 input	1.7	–	–	V

Table 15. 2.4 V to 3.0 V DC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{PU}	Pull-up resistor	–	4	5.60	8	kΩ
V_{OH1}	High output voltage Port 2 or 3 or 4 pins	I_{OH} < 10 µA, maximum of 10 mA source current in all I/Os	V_{DD} – 0.20	–	–	V
V_{OH2}	High output voltage Port 2 or 3 or 4 pins	I_{OH} = 0.2 mA, maximum of 10 mA source current in all I/Os	V_{DD} – 0.40	–	–	V
V_{OH3}	High output voltage Port 0 or 1 pins with LDO regulator Disabled for port 1	I_{OH} < 10 µA, maximum of 10 mA source current in all I/Os	V_{DD} – 0.20	–	–	V
V_{OH4}	High output voltage Port 0 or 1 pins with LDO regulator Disabled for Port 1	I_{OH} = 2 mA, maximum of 10 mA source current in all I/Os	V_{DD} – 0.50	–	–	V
V_{OH5A}	High output voltage Port 1 pins with LDO enabled for 1.8 V out	I_{OH} < 10 µA, V_{DD} > 2.4 V, maximum of 20 mA source current in all I/Os	1.50	1.80	2.10	V
V_{OH6A}	High output voltage Port 1 pins with LDO enabled for 1.8 V out	I_{OH} = 1 mA, V_{DD} > 2.4 V, maximum of 20 mA source current in all I/Os	1.20	–	–	V
V_{OL}	Low output voltage	IOL = 10 mA, maximum of 30 mA sink current on even port pins (for example, P0[2] and P1[4]) and 30 mA sink current on odd port pins (for example, P0[3] and P1[5])	–	–	0.75	V
V_{IL}	Input low voltage	–	–	–	0.72	V
V_{IH}	Input high voltage	–	1.40	–		V
V_H	Input hysteresis voltage	–	–	80	–	mV
I_{IL}	Input leakage (absolute value)	–	–	1	1000	nA
C_{PIN}	Capacitive load on pins	Package and pin dependent Temp = 25 °C	0.50	1.70	7	pF
$V_{ILLVT2.5}$	Input Low Voltage with low threshold enable set, Enable for Port1	Bit3 of IO_CFG1 set to enable low threshold voltage of Port1 input	0.7	V	–	
$V_{IHLVT2.5}$	Input High Voltage with low threshold enable set, Enable for Port1	Bit3 of IO_CFG1 set to enable low threshold voltage of Port1 input	1.2		–	V

Table 16. 1.71 V to 2.4 V DC GPIO Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{PU}	Pull-up resistor	–	4	5.60	8	kΩ
V_{OH1}	High output voltage Port 2 or 3 or 4 pins	I_{OH} = 10 µA, maximum of 10 mA source current in all I/Os	V_{DD} – 0.20	–	–	V
V_{OH2}	High output voltage Port 2 or 3 or 4 pins	I_{OH} = 0.5 mA, maximum of 10 mA source current in all I/Os	V_{DD} – 0.50	–	–	V
V_{OH3}	High output voltage Port 0 or 1 pins with LDO regulator Disabled for Port 1	I_{OH} = 100 µA, maximum of 10 mA source current in all I/Os	V_{DD} – 0.20	–	–	V
V_{OH4}	High output voltage Port 0 or 1 Pins with LDO Regulator Disabled for Port 1	I_{OH} = 2 mA, maximum of 10 mA source current in all I/Os	V_{DD} – 0.50	–	–	V
V_{OL}	Low output voltage	I_{OL} = 5 mA, maximum of 20 mA sink current on even port pins (for example, P0[2] and P1[4]) and 30 mA sink current on odd port pins (for example, P0[3] and P1[5])	–	–	0.40	V
V_{IL}	Input low voltage	–	–	–	0.30 × V_{DD}	V

DC POR and LVD Specifications

Table 22 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 22. DC POR and LVD Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{POR0}	1.66 V selected in PSoC Designer	V_{DD} must be greater than or equal to 1.71 V during startup, reset from the XRES pin, or reset from watchdog.	1.61	1.66	1.71	V
V_{POR1}	2.36 V selected in PSoC Designer		–	2.36	2.41	V
V_{POR2}	2.60 V selected in PSoC Designer		–	2.60	2.66	V
V_{POR3}	2.82 V selected in PSoC Designer		–	2.82	2.95	V
V_{LVD0}	2.45 V selected in PSoC Designer	–	2.40	2.45	2.51	V
V_{LVD1}	2.71 V selected in PSoC Designer		2.64[64]	2.71	2.78	V
V_{LVD2}	2.92 V selected in PSoC Designer		2.85[65]	2.92	2.99	V
V_{LVD3}	3.02 V selected in PSoC Designer		2.95[66]	3.02	3.09	V
V_{LVD4}	3.13 V selected in PSoC Designer		3.06	3.13	3.20	V
V_{LVD5}	1.90 V selected in PSoC Designer		1.84	1.90	2.32	V
V_{LVD6}	1.80 V selected in PSoC Designer		1.75[67]	1.80	1.84	V
V_{LVD7}	4.73 V selected in PSoC Designer		4.62	4.73	4.83	V

DC Programming Specifications

Table 23 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 23. DC Programming Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
$V_{DDIWRITE}$	Supply voltage for flash write operations	–	1.71	–	5.25	V
I_{DDP}	Supply current during programming or verify	–	–	5	25	mA
V_{ILP}	Input low voltage during programming or verify	See the appropriate DC GPIO Specifications on page 22	–	–	V_{IL}	V
V_{IHP}	Input high voltage during programming or verify	See the appropriate "DC GPIO Specifications" on page 22	V_{IH}	–	–	V
I_{ILP}	Input current when Applying V_{ILP} to P1[0] or P1[1] during programming or verify	Driving internal pull-down resistor	–	–	0.2	mA
I_{IHP}	Input current when applying V_{IHP} to P1[0] or P1[1] during programming or verify	Driving internal pull-down resistor	–	–	1.5	mA
V_{OLP}	Output low voltage during programming or verify	–	–	–	V_{SS} + 0.75	V
V_{OHP}	Output high voltage during programming or verify	See appropriate DC GPIO Specifications on page 22. For V_{DD} > 3 V use V_{OH4} in Table 12 on page 20.	V_{OH}	–	V_{DD}	V
$Flash_{ENPB}$	Flash write endurance	Erase/write cycles per block	50,000	–	–	–
$Flash_{DR}$	Flash data retention	Following maximum Flash write cycles; ambient temperature of 55 °C	20	–	–	Years

Notes
64. Always greater than 50 mV above V_{PPOR1} voltage for falling supply.
65. Always greater than 50 mV above V_{PPOR2} voltage for falling supply.
66. Always greater than 50 mV above V_{PPOR3} voltage for falling supply.
67. Always greater than 50 mV above V_{PPOR0} voltage for falling supply.

DC I²C Specifications

Table 24 list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 5.5 V and –40 °C ≤ T_A ≤ 85 °C, 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, or 1.71 V to 2.4 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 24. DC I²C Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{ILI2C}	Input low level	3.1 V ≤ V_{DD} ≤ 5.5 V	–	–	0.25 × V_{DD}	V
		2.5 V ≤ V_{DD} ≤ 3.0 V	–	–	0.3 × V_{DD}	V
		1.71 V ≤ V_{DD} ≤ 2.4 V	–	–	0.3 × V_{DD}	V
V_{IHI2C}	Input high level	1.71 V ≤ V_{DD} ≤ 5.5 V	0.65 × V_{DD}	–	–	V

DC Reference Buffer Specifications

Table 25 list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 5.5 V and –40 °C ≤ T_A ≤ 85 °C, 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, or 1.71 V to 2.4 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 25. DC Reference Buffer Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{Ref}	Reference buffer output	1.7 V ≤ V_{DD} ≤ 5.5 V	1	–	1.05	V
V_{RefHi}	Reference buffer output	1.7 V ≤ V_{DD} ≤ 5.5 V	1.2	–	1.25	V

DC IDAC Specifications

Table 26 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 26. DC IDAC Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
IDAC_DNL	Differential nonlinearity	–4.5	–	+4.5	LSB	–
IDAC_INL	Integral nonlinearity	–5	–	+5	LSB	–
IDAC_Gain (Source)	Range = 0.5x	6.64	–	22.46	µA	DAC setting = 128 dec. Not recommended for CapSense applications.
	Range = 1x	14.5	–	47.8	µA	
	Range = 2x	42.7	–	92.3	µA	
	Range = 4x	91.1	–	170	µA	DAC setting = 128 dec
	Range = 8x	184.5	–	426.9	µA	DAC setting = 128 dec

AC Chip-Level Specifications

Table 27 lists guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 27. AC Chip-Level Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{IMO24}	IMO frequency at 24 MHz Setting	–	22.8	24	25.2	MHz
F_{IMO12}	IMO frequency at 12 MHz setting	–	11.4	12	12.6	MHz
F_{IMO6}	IMO frequency at 6 MHz setting	–	5.7	6.0	6.3	MHz
F_{CPU}	CPU frequency	–	0.75	–	25.20	MHz
F_{32K1}	ILO frequency	–	15	32	50	kHz
F_{32K_U}	ILO untrimmed frequency	–	13	32	82	kHz
DC_{IMO}	Duty cycle of IMO	–	40	50	60	%
DC_{ILO}	ILO duty cycle	–	40	50	60	%
SR_{POWER_UP}	Power supply slew rate	V_{DD} slew rate during power-up	–	–	250	V/ms
t_{XRST}	External reset pulse width at power-up	After supply voltage is valid	1	–	–	ms
t_{XRST2}	External reset pulse width after power-up[68]	Applies after part has booted	10	–	–	µs
t_{OS}	Startup time of ECO	–	–	1	–	s
t_{JIT_IMO}[69]	N=32	6 MHz IMO cycle-to-cycle jitter (RMS)	–	0.7	6.7	ns
		6 MHz IMO long term N (N = 32) cycle-to-cycle jitter (RMS)	–	4.3	29.3	ns
		6 MHz IMO period jitter (RMS)	–	0.7	3.3	ns
		12 MHz IMO cycle-to-cycle jitter (RMS)	–	0.5	5.2	ns
		12 MHz IMO long term N (N = 32) cycle-to-cycle jitter (RMS)	–	2.3	5.6	ns
		12 MHz IMO period jitter (RMS)	–	0.4	2.6	ns
		24 MHz IMO cycle-to-cycle jitter (RMS)	–	1.0	8.7	ns
		24 MHz IMO long term N (N = 32) cycle-to-cycle jitter (RMS)	–	1.4	6.0	ns
		24 MHz IMO period jitter (RMS)	–	0.6	4.0	ns

Notes

68. The minimum required XRES pulse length is longer when programming the device (see Table 33 on page 31).
69. Refer to Cypress Jitter Specifications application note, Understanding Datasheet Jitter Specifications for Cypress Timing Products – AN5054 for more information.

AC Programming Specifications

Figure 15. AC Waveform

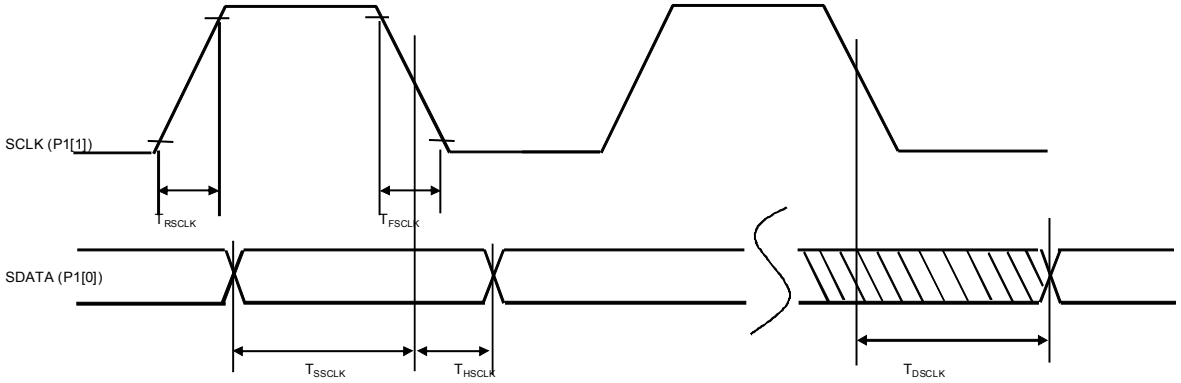


Table 33 lists the guaranteed maximum and minimum specifications for the entire voltage and temperature ranges.

Table 33. AC Programming Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
t_{RSCLK}	Rise time of SCLK	–	1	–	20	ns
t_{FSCLK}	Fall time of SCLK	–	1	–	20	ns
t_{SSCLK}	Data setup time to falling edge of SCLK	–	40	–	–	ns
t_{HSCLK}	Data hold time from falling edge of SCLK	–	40	–	–	ns
F_{SCLK}	Frequency of SCLK	–	0	–	8	MHz
t_{ERASEB}	Flash erase time (block)	–	–	–	18	ms
t_{WRITE}	Flash block write time	–	–	–	25	ms
t_{DSCLK}	Data out delay from falling edge of SCLK	$3.6 < V_{DD}$	–	–	60	ns
t_{DSCLK3}	Data out delay from falling edge of SCLK	$3.0 \le V_{DD} \le 3.6$	–	–	85	ns
t_{DSCLK2}	Data out delay from falling edge of SCLK	$1.71 \le V_{DD} \le 3.0$	–	–	130	ns
t_{XRST3}	External reset pulse width after power-up	Required to enter programming mode when coming out of sleep	300	–	–	µs
t_{XRES}	XRES pulse length	–	300	–	–	µs
$t_{VDDWAIT}$[71]	V_{DD} stable to wait-and-poll hold off	–	0.1	–	1	ms
$t_{VDDXRES}$[71]	V_{DD} stable to XRES assertion delay	–	14.27	–	–	ms
t_{POLL}	SDATA high pulse time	–	0.01	–	200	ms
t_{ACQ}[71]	“Key window” time after a V_{DD} ramp acquire event, based on 256 ILO clocks.	–	3.20	–	19.60	ms
$t_{XRESINI}$[71]	“Key window” time after an XRES event, based on 8 ILO clocks	–	98	–	615	µs

Note
71. Valid from 5 to 50 °C. See the spec, CY8C20X66, CY8C20X46, CY8C20X36, CY7C643XX, CY7C604XX, CY8CTST2XX, CY8CTMG2XX, CY8C20X67, CY8C20X47, CY8C20X37, Programming Spec for more details.

Table 35. SPI Master AC Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{SCLK}	SCLK clock frequency	$V_{DD} \geq 2.4$ V $V_{DD} < 2.4$ V	– –	– –	6 3	MHz MHz
DC	SCLK duty cycle	–	–	50	–	%
t_{SETUP}	MISO to SCLK setup time	$V_{DD} \geq 2.4$ V $V_{DD} < 2.4$ V	60 100	– –	– –	ns ns
t_{HOLD}	SCLK to MISO hold time	–	40	–	–	ns
t_{OUT_VAL}	SCLK to MOSI valid time	–	–	–	40	ns
t_{OUT_H}	MOSI high time	–	40	–	–	ns

Figure 17. SPI Master Mode 0 and 2

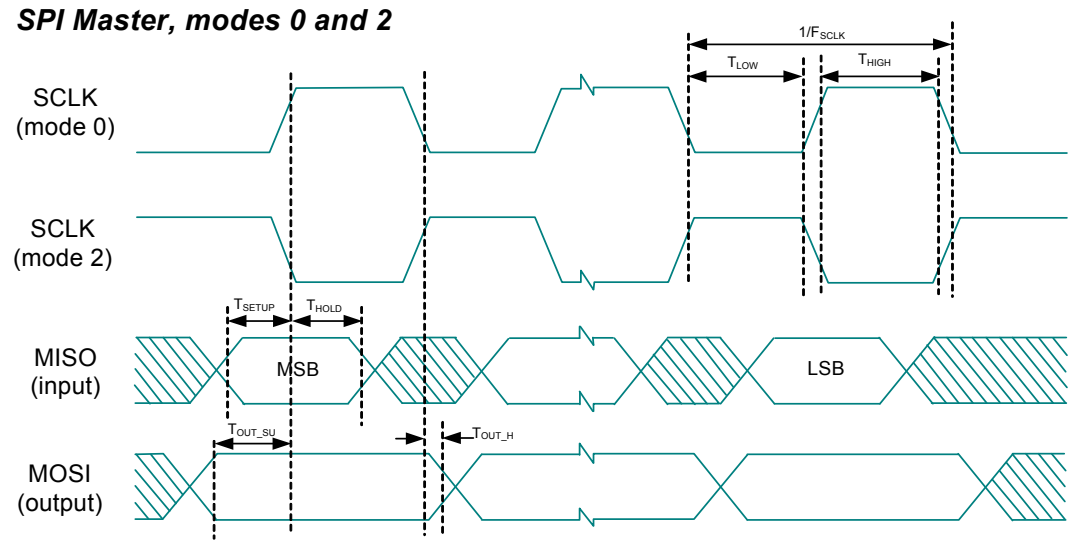


Figure 18. SPI Master Mode 1 and 3

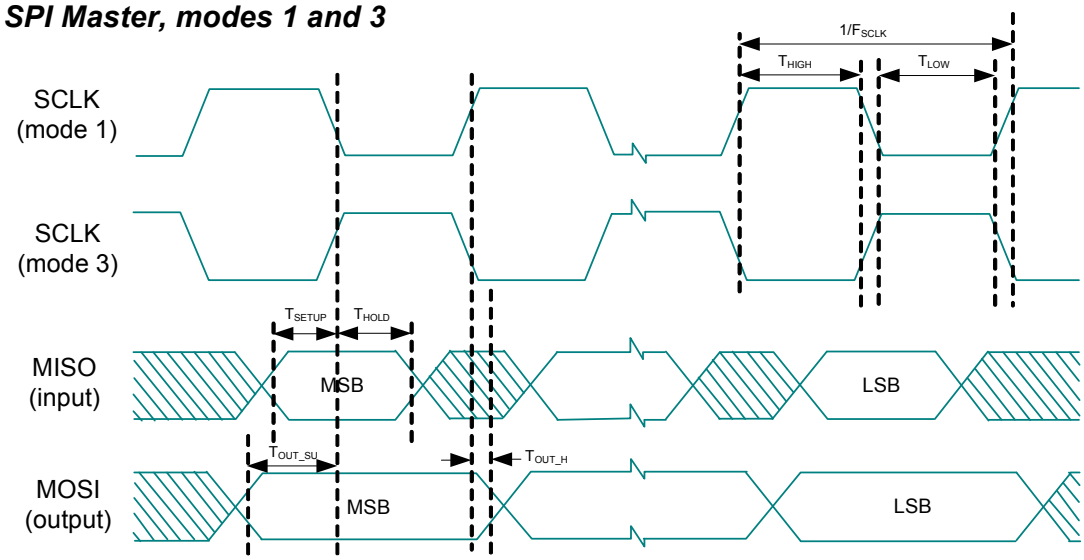


Table 36. SPI Slave AC Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{SCLK}	SCLK clock frequency	–	–	–	4	MHz
t_{LOW}	SCLK low time	–	42	–	–	ns
t_{HIGH}	SCLK high time	–	42	–	–	ns
t_{SETUP}	MOSI to SCLK setup time	–	30	–	–	ns
t_{HOLD}	SCLK to MOSI hold time	–	50	–	–	ns
t_{SS_MISO}	SS high to MISO valid	–	–	–	153	ns
t_{SCLK_MISO}	SCLK to MISO valid	–	–	–	125	ns
t_{SS_HIGH}	SS high time	–	50	–	–	ns
t_{SS_CLK}	Time from SS low to first SCLK	–	2/SCLK	–	–	ns
t_{CLK_SS}	Time from last SCLK to SS high	–	2/SCLK	–	–	ns

Figure 19. SPI Slave Mode 0 and 2

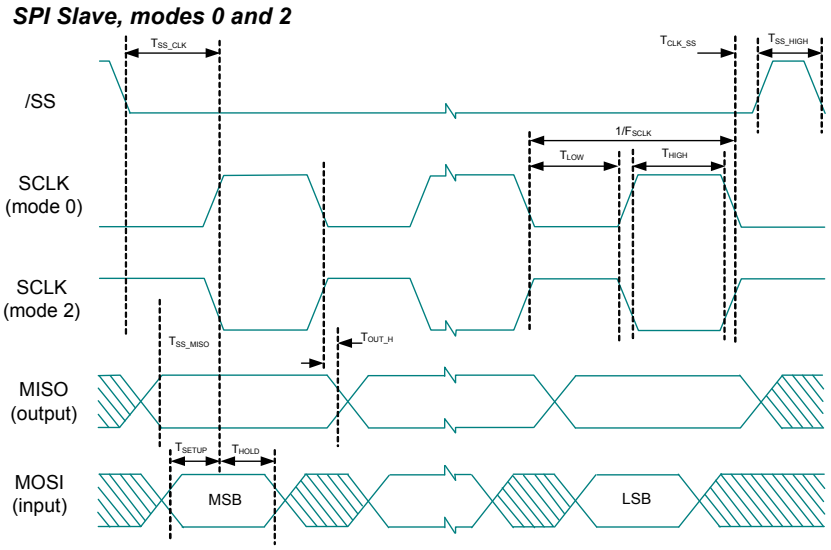


Figure 20. SPI Slave Mode 1 and 3

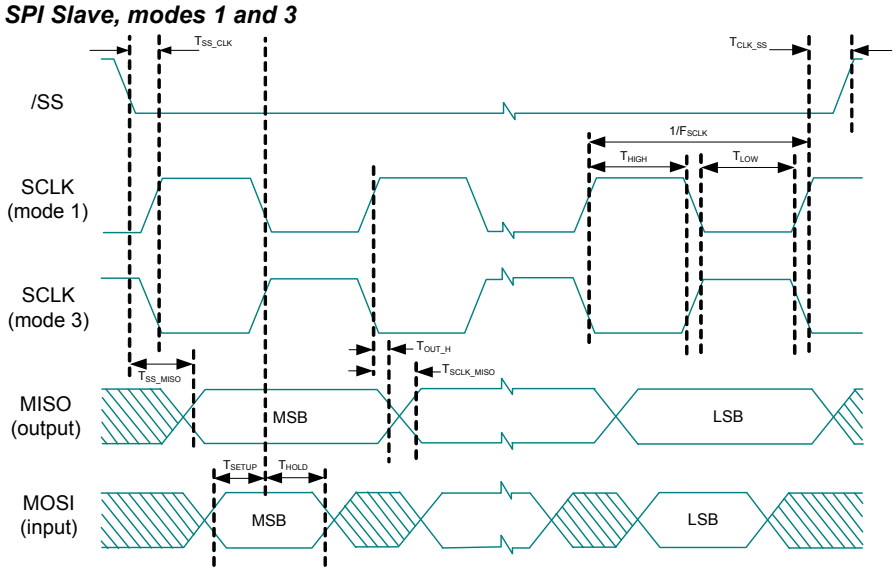


Figure 23. 32-pin QFN (5 × 5 × 0.55 mm) LQ32 3.5 × 3.5 E-Pad (Sawn) Package Outline, 001-42168

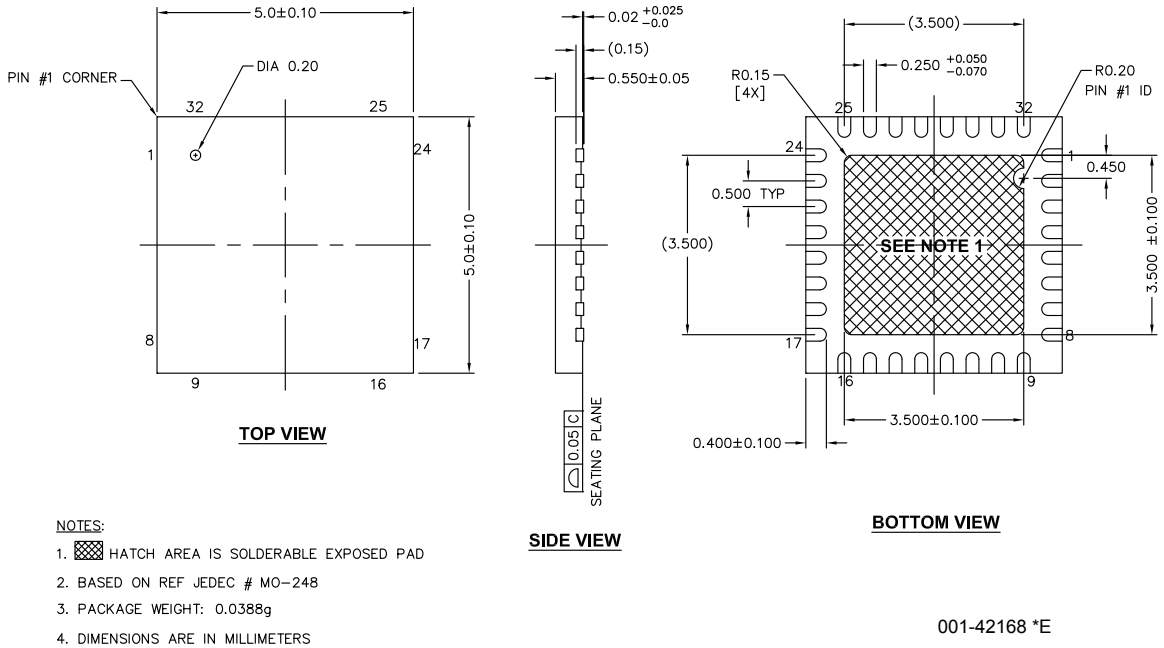
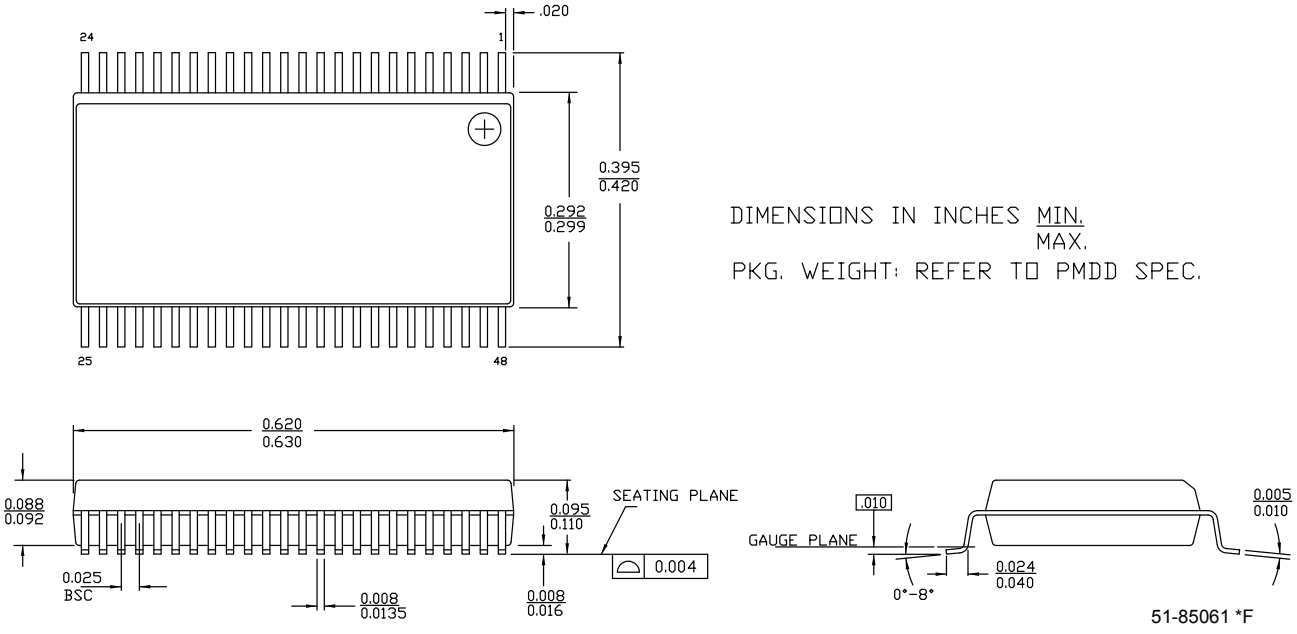


Figure 24. 48-pin SSOP (300 Mils) O483 Package Outline, 51-85061



Thermal Impedances

Table 37. Thermal Impedances per Package

Package	Typical θ_{JA} [73]	Typical θ_{JC}
16-pin QFN (No Center Pad)	33 °C/W	–
24-pin QFN [74]	21 °C/W	–
32-pin QFN [74]	20 °C/W	–
48-pin SSOP	69 °C/W	–
48-pin QFN (6 × 6 × 0.6 mm) [74]	25.20 °C/W	3.04 °C/W
48-pin QFN (7 × 7 × 1.0 mm) [74]	18 °C/W	–
30-ball WLCSP	54 °C/W	–

Capacitance on Crystal Pins

Table 38. Typical Package Capacitance on Crystal Pins

Package	Package Capacitance
32-pin QFN	3.2 pF
48-pin QFN	3.3 pF

Solder Reflow Specifications

Table 39 shows the solder reflow temperature limits that must not be exceeded.

Table 39. Solder Reflow Specifications

Package	Maximum Peak Temperature (T_C)	Maximum Time above T_C – 5 °C
16-pin QFN	260 °C	30 seconds
24-pin QFN	260 °C	30 seconds
32-pin QFN	260 °C	30 seconds
48-pin SSOP	260 °C	30 seconds
48-pin QFN (6 × 6 × 0.6 mm)	260 °C	30 seconds
48-pin QFN (7 × 7 × 1.0 mm)	260 °C	30 seconds
30-ball WLCSP	260 °C	30 seconds

Notes
73. $T_J = T_A + \text{Power} \times \theta_{JA}$.
74. To achieve the thermal impedance specified for the QFN package, the center thermal pad must be soldered to the PCB ground plane.

Ordering Information

Table 41 lists the CY8C20XX6A/S PSoC devices' key package features and ordering codes.

Table 41. PSoC Device Key Features and Ordering Information

Package	Ordering Code	Flash (Bytes)	SRAM (Bytes)	CapSense Blocks	Digital I/O Pins	Analog Inputs [78]	XRES Pin	USB	ADC
16-pin (3 × 3 × 0.6 mm) QFN (no E-Pad)	CY8C20236A-24LKXI	8 K	1 K	1	13	13	Yes	No	Yes
16-pin (3 × 3 × 0.6 mm) QFN (no E-Pad) (Tape and Reel)	CY8C20236A-24LKXIT	8 K	1 K	1	13	13	Yes	No	Yes
16-pin (3 × 3 × 0.6 mm) QFN (no E-Pad)	CY8C20246A-24LKXI	16 K	2 K	1	13	13	Yes	No	Yes
16-pin (3 × 3 × 0.6 mm) QFN (no E-Pad)	CY8C20246AS-24LKXI	16 K	2 K	1	13	13	Yes	No	Yes
16-pin (3 × 3 × 0.6 mm) QFN (no E-Pad) (Tape and Reel)	CY8C20246A-24LKXIT	16 K	2 K	1	13	13	Yes	No	Yes
16-pin (3 × 3 × 0.6 mm) QFN (no E-Pad) (Tape and Reel)	CY8C20246AS-24LKXIT	16 K	2 K	1	13	13	Yes	No	Yes
24-pin (4 × 4 × 0.6 mm) QFN	CY8C20336A-24LQXI	8 K	1 K	1	20	20	Yes	No	Yes
24-pin (4 × 4 × 0.6 mm) QFN (Tape and Reel)	CY8C20336A-24LQXIT	8 K	1 K	1	20	20	Yes	No	Yes
24-pin (4 × 4 × 0.6 mm) QFN	CY8C20346A-24LQXI	16 K	2 K	1	20	20	Yes	No	Yes
24-pin (4 × 4 × 0.6 mm) QFN	CY8C20346AS-24LQXI	16 K	2 K	1	20	20	Yes	No	Yes
24-pin (4 × 4 × 0.6 mm) QFN (Tape and Reel)	CY8C20346A-24LQXIT	16 K	2 K	1	20	20	Yes	No	Yes
24-pin (4 × 4 × 0.6 mm) QFN (Tape and Reel)	CY8C20346AS-24LQXIT	16 K	2 K	1	20	20	Yes	No	Yes
24-pin (4 × 4 × 0.6 mm) QFN	CY8C20396A-24LQXI	16 K	2 K	1	19	19	Yes	Yes	Yes
24-pin (4 × 4 × 0.6 mm) QFN (Tape and Reel)	CY8C20396A-24LQXIT	16 K	2 K	1	19	19	Yes	Yes	Yes
32-pin (5 × 5 × 0.6 mm) QFN	CY8C20436A-24LQXI	8 K	1 K	1	28	28	Yes	No	Yes
32-pin (5 × 5 × 0.6 mm) QFN (Tape and Reel)	CY8C20436A-24LQXIT	8 K	1 K	1	28	28	Yes	No	Yes
32-pin (5 × 5 × 0.6 mm) QFN	CY8C20446A-24LQXI	16 K	2 K	1	28	28	Yes	No	Yes
32-pin (5 × 5 × 0.6 mm) QFN	CY8C20446AS-24LQXI	16 K	2 K	1	28	28	Yes	No	Yes
32-pin (5 × 5 × 0.6 mm) QFN (Tape and Reel)	CY8C20446A-24LQXIT	16 K	2 K	1	28	28	Yes	No	Yes
32-pin (5 × 5 × 0.6 mm) QFN (Tape and Reel)	CY8C20446AS-24LQXIT	16 K	2 K	1	28	28	Yes	No	Yes
32-pin (5 × 5 × 0.6 mm) QFN	CY8C20466A-24LQXI	32 K	2 K	1	28	28	Yes	No	Yes
32-pin (5 × 5 × 0.6 mm) QFN	CY8C20466AS-24LQXI	32 K	2 K	1	28	28	Yes	No	Yes
32-pin (5 × 5 × 0.6 mm) QFN (Tape and Reel)	CY8C20466A-24LQXIT	32 K	2 K	1	28	28	Yes	No	Yes
32-pin (5 × 5 × 0.6 mm) QFN (Tape and Reel)	CY8C20466AS-24LQXIT	32 K	2 K	1	28	28	Yes	No	Yes
32-pin (5 × 5 × 0.6 mm) QFN	CY8C20496A-24LQXI	16 K	2 K	1	25	25	Yes	Yes	Yes
32-pin (5 × 5 × 0.6 mm) QFN (Tape and Reel)	CY8C20496A-24LQXIT	16 K	2 K	1	25	25	Yes	Yes	Yes

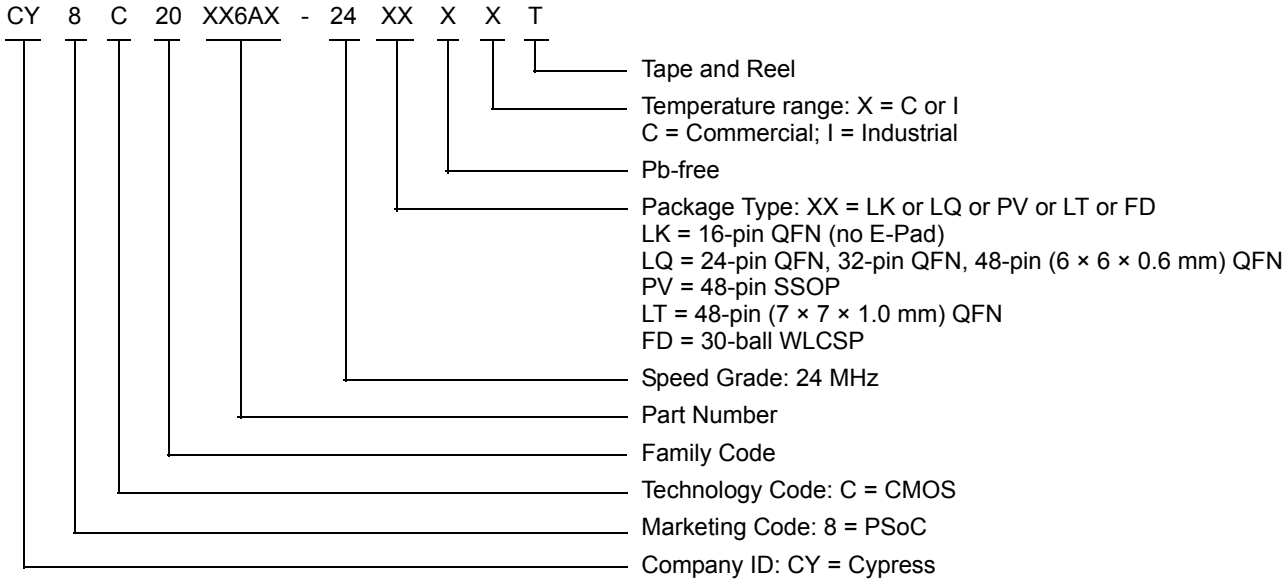
Notes
78. Dual-function Digital I/O Pins also connect to the common analog mux.
79. Not Recommended for New Designs.

Table 41. PSoC Device Key Features and Ordering Information *(continued)*

Package	Ordering Code	Flash (Bytes)	SRAM (Bytes)	CapSense Blocks	Digital I/O Pins	Analog Inputs [78]	XRES Pin	USB	ADC
24-pin (4 × 4 × 0.6 mm) QFN	CY8C20346AS-24LQXI	16 K	2 K	1	20	20	Yes	No	Yes
24-pin (4 × 4 × 0.6 mm) QFN (Tape and Reel)	CY8C20346AS-24LQXIT	16 K	2 K	1	20	20	Yes	No	Yes
32-pin (5 × 5 × 0.6 mm) QFN	CY8C20446AS-24LQXI	16 K	2 K	1	28	28	Yes	No	Yes
32-pin (5 × 5 × 0.6 mm) QFN (Tape and Reel)	CY8C20446AS-24LQXIT	16 K	2 K	1	28	28	Yes	No	Yes
32-pin (5 × 5 × 0.6 mm) QFN	CY8C20466AS-24LQXI	32 K	2 K	1	28	28	Yes	No	Yes
32-pin (5 × 5 × 0.6 mm) QFN (Tape and Reel)	CY8C20466AS-24LQXIT	32 K	2 K	1	28	28	Yes	No	Yes
48-pin (6 × 6 × 0.6 mm) QFN	CY8C20666AS-24LQXI	32 K	2 K	1	36	36	Yes	Yes	Yes
48-pin (6 × 6 × 0.6 mm) QFN (Tape and Reel)	CY8C20666AS-24LQXIT	32 K	2 K	1	36	36	Yes	Yes	Yes
48-pin (7 × 7 × 1.0 mm) QFN [79]	CY8C20666AS-24LTXI [79]	32 K	2 K	1	36	36	Yes	Yes	Yes
48-pin (7 × 7 × 1.0 mm) QFN (Tape and Reel) [79]	CY8C20666AS-24LTXIT [79]	32 K	2 K	1	36	36	Yes	Yes	Yes
48-pin (6 × 6 × 0.6 mm) QFN	CY8C20646AS-24LQXI	16 K	2 K	1	36	36	Yes	Yes	Yes
48-pin (6 × 6 × 0.6 mm) QFN (Tape and Reel)	CY8C20646AS-24LQXIT	16 K	2 K	1	36	36	Yes	Yes	Yes
48-pin (7 × 7 × 1.0 mm) QFN [79]	CY8C20646AS-24LTXI [79]	16 K	2 K	1	36	36	Yes	Yes	Yes
48-pin (7 × 7 × 1.0 mm) QFN (Tape and Reel) [79]	CY8C20646AS-24LTXIT [79]	16 K	2 K	1	36	36	Yes	Yes	Yes

Notes
78. Dual-function Digital I/O Pins also connect to the common analog mux.
79. Not Recommended for New Designs.

Ordering Code Definitions



Errata

This section describes the errata for the PSoC® CY8C20x36A/46A/66A/96A/46AS/66AS/36H/46H families. Details include errata trigger conditions, scope of impact, available workarounds, and silicon revision applicability. Contact your local Cypress Sales Representative if you have questions.

Qualification Status

Product Status: Production released.

Errata Summary

The following Errata items apply to CY8C20x36A/46A/66A/96A/46AS/66AS/36H/46H families.

1. Wakeup from sleep may intermittently fail

■ **Problem Definition**

When the device is put to sleep in Standby or I2C_USB Mode and the bandgap circuit is refreshed less frequently than every 8 ms (default), the device may not come out of sleep when a sleep-ending input is received.

■ **Parameters Affected**

None

■ **Trigger Condition(S)**

By default, when the device is in the Standby or I2C_USB sleep modes, the bandgap circuit is powered-up approximately every 8 ms to facilitate detection of POR or LVD events. This interval can be lengthened or the periodic power-up disabled to reduce sleep current by setting the ALT_BUZZ bits in the SLP_CFG2 register or the Disable Buzz bit in the OSC_CR0 register respectively. If the bandgap circuit refresh interval is set longer than the default 8 ms, the device may fail to wakeup from sleep and enter a locked up state that can only be recovered by Watchdog Reset, XRES, or POR.

■ **Scope of Impact**

The trigger conditions outlined above may cause the device to never wakeup.

■ **Workaround**

Prior to entering Standby or I2C_USB sleep modes, do not lengthen or disable the bandgap refresh interval by manipulating the ALT_BUZZ bits in the SLP_CFG2 register or the Disable Buzz bit in the OSC_CR0 register respectively.

■ **Fix Status**

This issue will not be corrected in the next silicon revision.

2. I^2C Errors

■ **Problem Definition**

The I^2C block exhibits occasional data and bus corruption errors when the I^2C master initiates transactions while the device is transitioning in to or out of sleep mode.

■ **Parameters Affected**

Affects reliability of I^2C communication to device, and between I^2C master and third party I^2C slaves.

■ **Trigger Condition(S)**

Triggered by transitions into and out of the device's sleep mode.

■ **Scope of Impact**

Data errors result in incorrect data reported to the I^2C master, or incorrect data received from the master by the device. Bus corruption errors can corrupt data in transactions between the I^2C master and third party I^2C slaves.

■ **Workaround**

Firmware workarounds are available in firmware. Generally the workaround consists of disconnecting the I^2C block from the bus prior to going to sleep modes. I^2C transactions during sleep are supported by a protocol in which the master wakes the device prior to the I^2C transaction.

■ **Fix Status**

To be fixed in future silicon.

■ **Changes**

None

5. Missed Interrupt During Transition to Sleep

■ **Problem Definition**

If an interrupt is posted a short time (within 2.5 CPU cycles) before firmware commands the device to sleep, the interrupt will be missed.

■ **Parameters Affected**

No datasheet parameters are affected.

■ **Trigger Condition(S)**

Triggered by enabling sleep mode just prior to an interrupt.

■ **Scope of Impact**

The relevant interrupt service routine will not be run.

■ **Workaround**

None.

■ **Fix Status**

Will not be fixed

■ **Changes**

None

6. Wakeup from sleep with analog interrupt

■ **Problem Definition**

Device wakes up from sleep when an analog interrupt is trigger

■ **Parameters Affected**

No datasheet parameters are affected.

■ **Trigger Condition(S)**

Triggered by enabling analog interrupt during sleep mode when device operating temperature is 50 °C or above

■ **Scope of Impact**

Device unexpectedly wakes up from sleep

■ **Workaround**

Disable the analog interrupt before entering sleep and turn it back on upon wakeup.

■ **Fix Status**

Will not be fixed

■ **Changes**

None

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