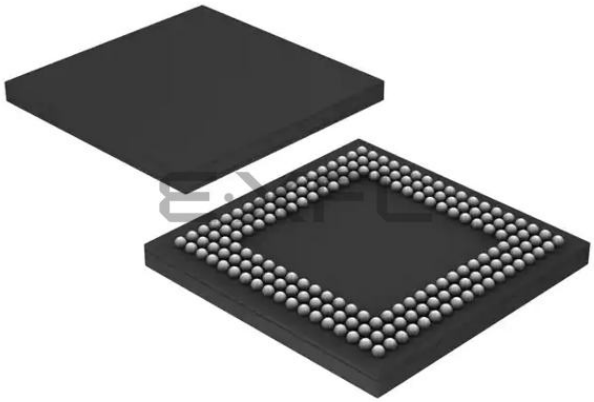

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	ARM926EJ-S
Core Size	16/32-Bit
Speed	180MHz
Connectivity	EBI/EMI, I²C, Memory Card, SPI, UART/USART, USB OTG
Peripherals	DMA, I²S, LCD, PWM, WDT
Number of I/O	-
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	96K x 8
Voltage - Supply (Vcc/Vdd)	1.1V ~ 3.6V
Data Converters	A/D 4x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	180-TFBGA
Supplier Device Package	180-TFBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc3130fet180-551

5. Pinning information

5.1 Pinning

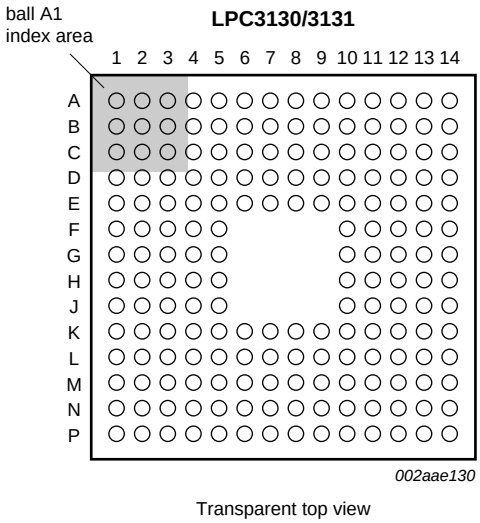


Fig 2. LPC3130/3131 pinning TFBGA180 package

Table 3. Pin allocation table

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
Row A							
1	EBI_D_10	2	EBI_A_1_CLE	3	EBI_D_9	4	mGPIO10
5	mGPIO7	6	mGPIO6	7	SPI_CS_OUT0	8	SPI_SCK
9	VDDI	10	FFAST_IN	11	VSSI	12	ADC10B_GNDA
13	ADC10B_VDDA33	14	ADC10B_GPA1	-	-	-	-
Row B							
1	EBI_D_8	2	VDDE_IOA	3	EBI_A_0_ALE	4	mNAND_RYBN2
5	mGPIO8	6	mGPIO5	7	SPI_MOSI	8	SPI_CS_IN
9	PWM_DATA	10	FFAST_OUT	11	GPIO3	12	VSSE_IOC
13	ADC10B_GPA2	14	ADC10B_GPA0	-	-	-	-
Row C							
1	EBI_D_7	2	EBI_D_11	3	VSSE_IOA	4	VSSE_IOA
5	mGPIO9	6	VDDI	7	VSSI	8	SPI_MISO
9	VDDI	10	I2C_SDA0	11	GPIO4	12	VDDI
13	VDDE_IOC	14	ADC10B_GPA3	-	-	-	-
Row D							
1	EBI_D_5	2	EBI_D_6	3	EBI_D_13	4	mNAND_RYBN3
5	VDDE_IOC	6	VSSE_IOC	7	VDDE_IOC	8	VSSE_IOC
9	VSSE_IOC	10	I2C_SCL0	11	VDDA12	12	VSSI
13	BUF_TCK	14	BUF_TMS	-	-	-	-

Table 3. Pin allocation table *…continued*

Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
Row E							
1	EBI_D_3	2	EBI_D_4	3	EBI_D_14	4	VSSE_IOA
5	VDDE_IOA	6	mNAND_RYBN0	7	mNAND_RYBN1	8	VDDE_IOC
9	VSSA12	10	VDDA12	11	ARM_TDO	12	I2C_SDA1
13	I2C_SCL1	14	I2STX_BCK1	-	-	-	-
Row F							
1	EBI_D_2	2	EBI_D_1	3	EBI_D_15	4	VSSE_IOA
5	VDDE_IOA	10	SCAN_TDO	11	BUF_TRST_N	12	I2STX_DATA1
13	I2SRX_WS1	14	I2SRX_BCK1	-	-	-	-
Row G							
1	EBI_NCAS_BLOUT_0	2	EBI_D_0	3	EBI_D_12	4	VSSI
5	VDDE_IOA	10	I2STX_WS1	11	VSSE_IOC	12	VDDE_IOC
13	SYSCLK_O	14	I2SRX_DATA1	-	-	-	-
Row H							
1	EBI_DQM_0_NOE	2	EBI_NRAS_BLOUT_1	3	VDDI	4	VSSE_IOA
5	VDDE_IOA	10	GPIO12	11	GPIO19	12	CLK_256FS_O
13	GPIO11	14	RSTIN_N	-	-	-	-
Row J							
1	NAND_NCS_0	2	EBI_NWE	3	NAND_NCS_1	4	CLOCK_OUT
5	USB_RREF	10	GPIO1	11	GPIO16	12	GPIO13
13	GPIO15	14	GPIO14	-	-	-	-
Row K							
1	NAND_NCS_2	2	NAND_NCS_3	3	VSSE_IOA	4	USB_VSSA_REF
5	mLCD_DB_12	6	mLCD_DB_6	7	mLCD_DB_10	8	mLCD_CSB
9	TDI	10	GPIO0	11	VDDE_IOC	12	GPIO17
13	GPIO20	14	GPIO18	-	-	-	-
Row L							
1	USB_VDDA12_PLL	2	USB_VBUS	3	USB_VSSA_TERM	4	VDDE_IOB
5	mLCD_DB_9	6	VSSI	7	VDDI	8	mLCD_E_RD
9	VSSE_IOC	10	VDDE_IOC	11	VSSI	12	VDDI
13	VSSE_IOC	14	GPIO2	-	-	-	-
Row M							
1	USB_ID	2	USB_VDDA33_DRV	3	VSSE_IOB	4	VSSE_IOB
5	VDDE_IOB	6	VSSE_IOB	7	VDDE_IOB	8	VSSE_IOB
9	VDDE_IOB	10	I2SRX_DATA0	11	mI2STX_WS0	12	mI2STX_BCK0
13	mI2STX_DATA0	14	TCK	-	-	-	-
Row N							
1	USB_GNDA	2	USB_DM	3	mLCD_DB_15	4	mLCD_DB_11
5	mLCD_DB_8	6	mLCD_DB_2	7	mLCD_DB_4	8	mLCD_DB_0
9	mLCD_RW_WR	10	I2SRX_BCK0	11	JTAGSEL	12	UART_TXD
13	mUART_CTS_N	14	mI2STX_CLK0	-	-	-	-

Table 4. Pin description

Pin names with prefix m are multiplexed pins. See Table 10 for pin function selection of multiplexed pins.

Pin name	BGA ball	Digital I/O level [1]	Application function	Pin state after reset[2]	Cell type [3]	Description
External Bus Interface (NAND flash controller)						
EBI_A_0_ALE[4]	B3	SUP4	DO	O	DIO4	EBI Address Latch Enable
EBI_A_1_CLE[4]	A2	SUP4	DO	O	DIO4	EBI Command Latch Enable
EBI_D_0[4]	G2	SUP4	DIO	I	DIO4	EBI Data I/O 0
EBI_D_1[4]	F2	SUP4	DIO	I	DIO4	EBI Data I/O 1
EBI_D_2[4]	F1	SUP4	DIO	I	DIO4	EBI Data I/O 2
EBI_D_3[4]	E1	SUP4	DIO	I	DIO4	EBI Data I/O 3
EBI_D_4[4]	E2	SUP4	DIO	I	DIO4	EBI Data I/O 4
EBI_D_5[4]	D1	SUP4	DIO	I	DIO4	EBI Data I/O 5
EBI_D_6[4]	D2	SUP4	DIO	I	DIO4	EBI Data I/O 6
EBI_D_7[4]	C1	SUP4	DIO	I	DIO4	EBI Data I/O 7
EBI_D_8[4]	B1	SUP4	DIO	I	DIO4	EBI Data I/O 8
EBI_D_9[4]	A3	SUP4	DIO	I	DIO4	EBI Data I/O 9
EBI_D_10[4]	A1	SUP4	DIO	I	DIO4	EBI Data I/O 10
EBI_D_11[4]	C2	SUP4	DIO	I	DIO4	EBI Data I/O 11
EBI_D_12[4]	G3	SUP4	DIO	I	DIO4	EBI Data I/O 12
EBI_D_13[4]	D3	SUP4	DIO	I	DIO4	EBI Data I/O 13
EBI_D_14[4]	E3	SUP4	DIO	I	DIO4	EBI Data I/O 14
EBI_D_15[4]	F3	SUP4	DIO	I	DIO4	EBI Data I/O 15
EBI_DQM_0_NOE[4]	H1	SUP4	DO	O	DIO4	NAND Read Enable (active LOW)
EBI_NWE[4]	J2	SUP4	DO	O	DIO4	NAND Write Enable (active LOW)
NAND_NCS_0[4]	J1	SUP4	DO	O	DIO4	NAND Chip Enable 0
NAND_NCS_1[4]	J3	SUP4	DO	O	DIO4	NAND Chip Enable 1
NAND_NCS_2[4]	K1	SUP4	DO	O	DIO4	NAND Chip Enable 2
NAND_NCS_3[4]	K2	SUP4	DO	O	DIO4	NAND Chip Enable 3
mNAND_RYBN0[4]	E6	SUP4	DI	I	DIO4	NAND Ready/Busy 0
mNAND_RYBN1[4]	E7	SUP4	DI	I	DIO4	NAND Ready/Busy 1
mNAND_RYBN2[4]	B4	SUP4	DI	I	DIO4	NAND Ready/Busy 2
mNAND_RYBN3[4]	D4	SUP4	DI	I	DIO4	NAND Ready/Busy 3
EBI_NCAS_BLOUT_0[4]	G1	SUP4	DO	O	DIO4	EBI Lower lane byte select (7:0)
EBI_NRAS_BLOUT_1[4]	H2	SUP4	DO	O	DIO4	EBI Upper lane byte select (15:8)
Pulse Width Modulation module						
PWM_DATA[4]	B9	SUP3	DO / GPIO	O	DIO1	PWM Output

[1] Digital I/O levels are explained in Table 5.

[2] I = input; I:PU = input with internal weak pull-up; I:PD = input with internal weak pull-down; O = output.

[3] Cell types are explained in Table 6.

[4] Pin can be configured as GPIO pin in the IOCONFIG block.

6. Functional description

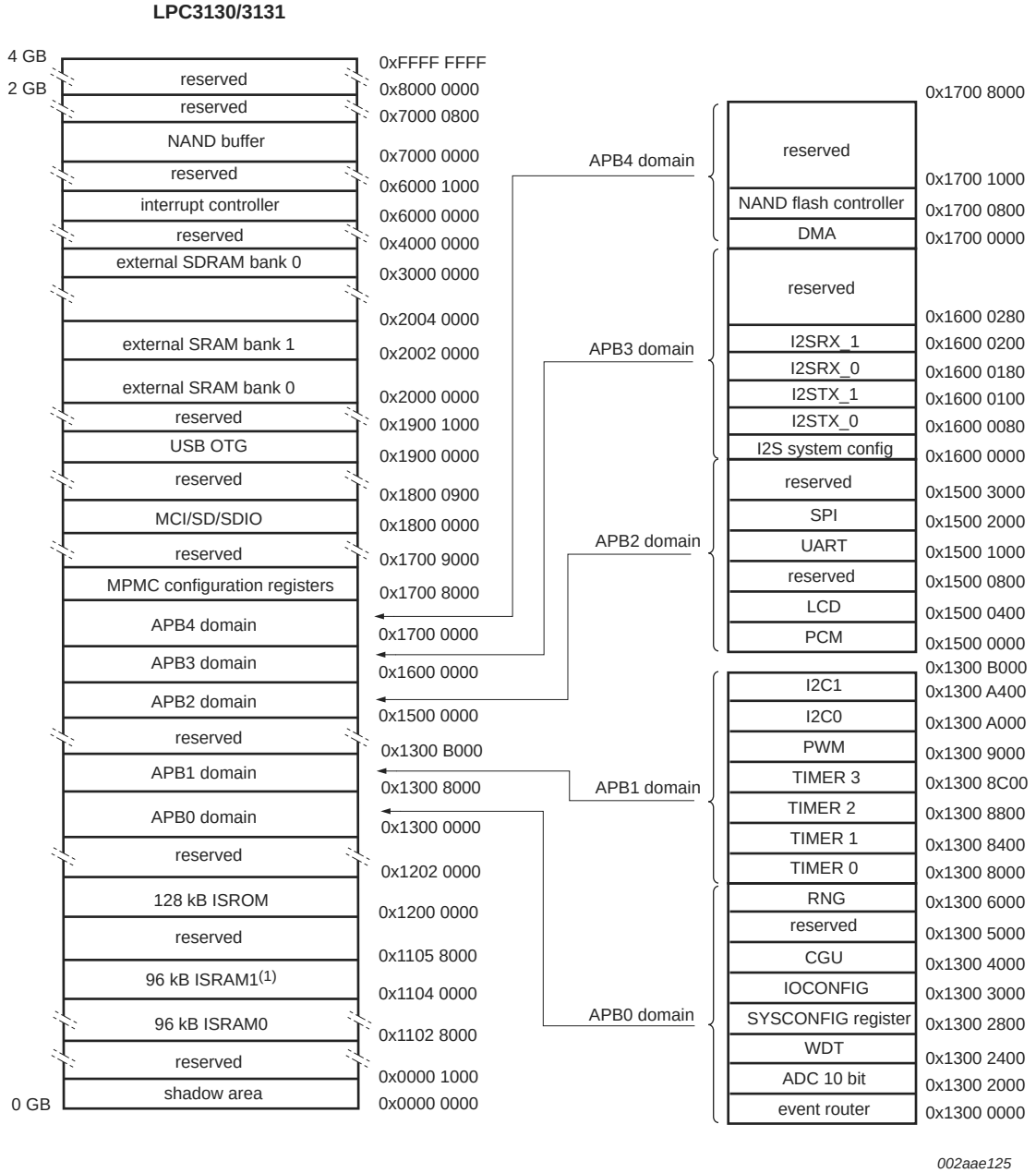
6.1 ARM926EJ-S

The processor embedded in the LPC3130/3131 is the ARM926EJ-S. It is a member of the ARM9 family of general-purpose microprocessors. The ARM926EJ-S is intended for multi-tasking applications where full memory management, high performance, and low power are important.

This module has the following features:

- ARM926EJ-S processor core which uses a five-stage pipeline consisting of fetch, decode, execute, memory, and write stages. The processor supports both the 32-bit ARM and 16-bit Thumb instruction sets, which allows a trade off between high performance and high code density. The ARM926EJ-S also executes an extended ARMv5TE instruction set which includes support for Java byte code execution.
- Contains an AMBA BIU for both data accesses and instruction fetches.
- Memory Management Unit (MMU).
- 16 kB instruction and 16 kB data separate cache memories with an 8 word line length. The caches are organized using Harvard architecture.
- Little Endian is supported.
- The ARM926EJ-S processor supports the ARM debug architecture and includes logic to assist in both hardware and software debugging.
- Supports dynamic clock gating for power reduction.
- The processor core clock can be set equal to the AHB bus clock or to an integer number times the AHB bus clock. The processor can be switched dynamically between these settings.
- ARM stall support.

6.2 Memory map



(1) LPC3131 only.

Fig 3. LPC3130/3131 memory map

- Supports 1/4-bit SD cards.
- Card detection and write protection.
- FIFO buffers of 16 bytes deep.
- Host pull-up control.
- SDIO suspend and resume.
- 1 to 65 535 bytes blocks.
- Suspend and resume operations.
- SDIO Read-wait.
- Maximum clock speed of 52 MHz (MMC 4.1).
- Supports CE-ATA 1.1.
- Supports 1-bit, 4-bit, and 8-bit MMC cards and CE-ATA devices.

6.10 High-speed Universal Serial Bus 2.0 On-The-Go (OTG)

The USB OTG module allows the LPC3130/3131 to connect directly to a USB host such as a PC (in device mode) or to a USB device in host mode. In addition, the LPC3130/3131 has a special, built-in mode in which it enumerates as a Device Firmware Upgrade (DFU) class, which allows for a (factory) download of the device firmware through USB.

This module has the following features:

- Complies with *Universal Serial Bus specification 2.0*.
- Complies with *USB On-The-Go supplement*.
- Complies with *Enhanced Host Controller Interface Specification*.
- Supports auto USB 2.0 mode discovery.
- Supports all high-speed USB-compliant peripherals.
- Supports all full-speed USB-compliant peripherals.
- Supports software Host Negotiation Protocol (HNP) and Session Request Protocol (SRP) for OTG peripherals.
- Contains UTMI+ compliant transceiver (PHY).
- Supports interrupts.
- This module has its own, integrated DMA engine.

USB-IF TestID for Hi-speed peripheral silicon: 40700062

USB-IF TestID for Hi-speed embedded host silicon: 120000182

6.11 DMA controller

The DMA Controller can perform DMA transfers on the AHB bus without using the CPU.

This module has the following features:

- Supported transfer types:

  Memory to memory:

- Visibility of the interrupt's request state before masking.
- Support for nesting of interrupt service routines.
- Interrupts routed to IRQ and to FIQ are vectored.
- Level interrupt support.

The following blocks can generate interrupts:

- NAND flash controller
- USB 2.0 high-speed OTG
- Event router
- 10-bit ADC
- UART
- LCD
- MCI
- SPI
- I2C0 and I2C1 controllers
- Timer0, Timer1, Timer2, and Timer3
- I^2S transmit: I2STX_0 and I2STX_1
- I^2S receive: I2SRX_0 and I2SRX_1
- DMA

6.13 Multi-layer AHB

The multi-layer AHB is an interconnection scheme based on the AHB protocol that enables parallel access paths between multiple masters and slaves in a system.

Multiple masters can have access to different slaves at the same time.

Figure 5 gives an overview of the multi-layer AHB configuration in the LPC3130/3131. AHB masters and slaves are numbered according to their AHB port number.

6.19 Event router

The event router extends the interrupt capability of the system by offering a flexible and versatile way of generating interrupts. Combined with the wake-up functionality of the CGU, it also offers a way to wake up the system from suspend mode (with all clocks deactivated).

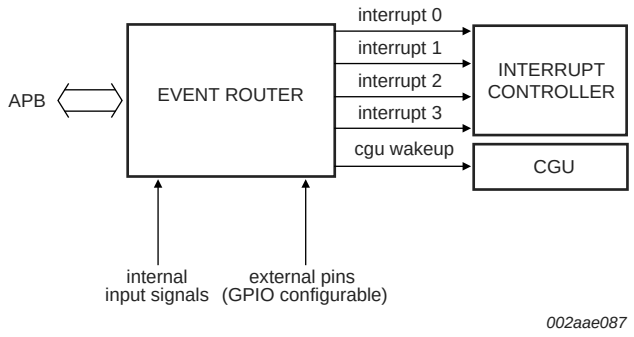


Fig 8. Event router block diagram

The event router has four interrupt outputs connected to the interrupt controller and one wake-up output connected to the CGU as shown in Figure 8. The output signals are activated when an event (for instance a rising edge) is detected on one of the input signals. The input signals of the event router are connected to relevant internal control signals in the system or to external signals through pins of the LPC3130/3131.

This module has the following features:

- Provides programmable routing of input events to multiple outputs for use as interrupts or wake up signals.
- Input events can come from internal signals or from the pins that can be used as GPIO.
- Inputs can be used either directly or latched (edge detected) as an event source.
- The active level (polarity) of the input signal for triggering events is programmable.
- Direct events will disappear when the input becomes inactive.
- Latched events will remain active until they are explicitly cleared.
- Each input can be masked globally for all inputs at once.
- Each input can be masked for each output individually.
- Event detect status can be read for each output separately.
- Event detection is fully asynchronous (no active clock required).
- Module can be used to generate a system wake-up from suspend mode.

Remark: All pins that can be used as GPIO are connected to the event router (see Figure 8). Note that they can be used to trigger events when in normal functional mode or in GPIO mode.

Table 10. Pin descriptions of multiplexed pins *…continued*

Pin Name	Default Signal	Alternate Signal	Description
mLCD_DB_15	LCD_DB_15	EBI_A_15	**LCD_DB_15 —** LCD bidirectional data line 15. **EBI_A_15 —** EBI address line 15.
Storage related pin multiplexing			
mGPIO5	GPIO5	MCI_CLK	**GPIO5 —** General Purpose I/O pin 5. **MCI_CLK —** MCI card clock.
mGPIO6	GPIO6	MCI_CMD	**GPIO_6 —** General Purpose I/O pin 6. **MCI_CMD —** MCI card command input/output.
mGPIO7	GPIO7	MCI_DAT_0	**GPIO7 —** General Purpose I/O pin 7. **MCI_DAT_0 —** MCI card data input/output line 0.
mGPIO8	GPIO8	MCI_DAT_1	**GPIO8 —** General Purpose I/O pin 8. **MCI_DAT_1 —** MCI card data input/output line 1.
mGPIO9	GPIO9	MCI_DAT_2	**GPIO9 —** General Purpose I/O pin 9. **MCI_DAT_2 —** MCI card data input/output line 2.
mGPIO10	GPIO10	MCI_DAT_3	**GPIO10 —** General Purpose I/O pin 10. **MCI_DAT_3 —** MCI card data input/output line 3.
NAND related pin multiplexing			
mNAND_RYBN0	NAND_RYBN0	MCI_DAT_4	**NAND_RYBN0 —** NAND flash controller Read/Not busy signal 0. **MCI_DAT_4 —** MCI card data input/output line 4.
mNAND_RYBN1	NAND_RYBN1	MCI_DAT_5	**NAND_RYBN1 —** NAND flash controller Read/Not busy signal 1. **MCI_DAT_5 —** MCI card data input/output line 5.
mNAND_RYBN2	NAND_RYBN2	MCI_DAT_6	**NAND_RYBN2 —** NAND flash controller Read/Not busy signal 2. **MCI_DAT_6 —** MCI card data input/output line 6.
mNAND_RYBN3	NAND_RYBN3	MCI_DAT7	**NAND_RYBN3 —** NAND flash controller Read/Not busy signal 3. **MCI_DAT7 —** MCI card data input/output line 7.
Audio related pin multiplexing			
mI2STX_DATA0	I2STX_DATA0	PCM_DA	**I2STX_DATA0 —** I^2S-bus interface 0 transmit data signal. **PCM_DA —** PCM serial data line A.
mI2STX_BCK0	I2STX_BCK0	PCM_FSC	**I2STX_BCK0 —** I^2S-bus interface 0 transmit bitclock signal. **PCM_FSC —** PCM frame synchronization signal.
mI2STX_WS0	I2STX_WS0	PCM_DCLK	**I2STX_WS0 —** I^2S-bus interface 0 transmit word select signal. **PCM_DCLK —** PCM data clock output.
mI2STX_CLK0	I2STX_CLK0	PCM_DB	**I2STX_CLK0 —** I^2S-bus interface 0 transmit clock signal. **PCM_DB —** PCM serial data line B.
UART related pin multiplexing			
mUART_CTS_N	UART_CTS_N	SPI_CS_OUT1	**UART_CTS_N —** UART modem control Clear-to-send signal. **SPI_CS_OUT1 —** SPI chip select out for slave 1 (used in master mode).
mUART_RTS_N	UART_RTS_N	SPI_CS_OUT2	**UART_RTS_N —** UART modem control Request-to-Send signal. **SPI_CS_OUT2 —** SPI chip select out for slave 2 (used in master mode).

8.1 Power consumption

Table 14. Power consumption

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Standby power mode[1]						
I_{DD}	Supply current	core; VDDI = 1.2 V	-	1.1	-	mA
		all other SUP1 supplies: VDDA12 = 1.2 V; USB_VDDA12_PL = 1.2 V	-	0.175	-	mA
		VDDE_IOA = 1.8 V	-	0.001	-	mA
		VDDE_IOB = 1.8 V	-	0.0008	-	mA
		VDDE_IOC = 3.3 v	-	0.065	-	mA
		ADC10B_VDDA33 = 3.3 V	-	0	-	mA
		USB_VDDA33 = 3.3 V	-	0	-	mA
		USB_VDDA_DRV = 3.3 V	-	0	-	mA
P	Power dissipation	Total for supply domains SUP1, SUP3, SUP4, SUP8	-	1.75	-	mW
External SDRAM based system (operating frequency 180 MHz (core)/ 90 MHz (bus)); heavy SDRAM load power; without dynamic clock scaling[2]						
I_{DD}	Supply current	core; VDDI = 1.2 V	-	67.2	-	mA
		all other SUP1 supplies: VDDA12 = 1.2 V; USB_VDDA12_PL = 1.2 V	-	0.93	-	mA
		VDDE_IOA = 1.8 V	-	11.54	-	mA
		VDDE_IOB = 1.8 V	-	6.64	-	mA
		VDDE_IOC = 3.3 V	-	0.08	-	mA
		ADC10B_VDDA33 = 3.3 V	-	0.0002	-	mA
		USB_VDDA33 = 3.3 V	-	1.63	-	mA
		USB_VDDA_DRV = 3.3 V	-	0.895	-	mA
P	Power dissipation	Total for supply domains SUP1, SUP3, SUP4, SUP8	-	123.1	-	mW
External SDRAM based system (operating frequency 180 MHz (core)/ 90 MHz (bus)); heavy SDRAM load power; with dynamic clock scaling[2][3]						
I_{DD}	Supply current	core; VDDI = 1.2 V	-	53.2	-	mA
		all other SUP1 supplies: VDDA12 = 1.2 V; USB_VDDA12_PL = 1.2 V	-	0.93	-	mA
		VDDE_IOA = 1.8 V	-	5	-	mA
		VDDE_IOB = 1.8 V	-	3.62	-	mA
		VDDE_IOC = 3.3 V	-	0.08	-	mA
		ADC10B_VDDA33 = 3.3 V	-	0.0002	-	mA
		USB_VDDA33 = 3.3 V	-	1.62	-	mA
		USB_VDDA_DRV = 3.3 V	-	0.895	-	mA
P	Power dissipation	Total for supply domains SUP1, SUP3, SUP4, SUP8	-	89	-	mW

9. Dynamic characteristics

9.1 LCD controller

9.1.1 Intel 8080 mode

Table 15. Dynamic characteristics: LCD controller in Intel 8080 mode

C_L = 25 pF, T_{amb} = −40 °C to +85 °C, unless otherwise specified; $V_{DD(IO)}$ = 1.8 V and 3.3 V (SUP8).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{su(A)}$	address set-up time		-	1 × LCDCLK	-	ns
$t_{h(A)}$	address hold time		-	2 × LCDCLK	-	ns
$t_{cy(a)}$	access cycle time	[1]	-	5 × LCDCLK	-	ns
$t_{w(en)W}$	write enable pulse width	[1]	-	2 × LCDCLK	-	ns
$t_{w(en)R}$	read enable pulse width	[1]	-	2 × LCDCLK	-	ns
t_r	rise time		2	-	5	ns
t_f	fall time		2	-	5	ns
$t_{d(QV)}$	data output valid delay time		-	−1 × LCDCLK	-	ns
$t_{dis(Q)}$	data output disable time		-	2 × LCDCLK	-	ns

[1] Timing is determined by the LCD Interface Control Register fields: INVERT_CS = 1; MI = 0; PS = 0; INVERT_E_RD = 0. See LPC3130/3131 *user manual*.

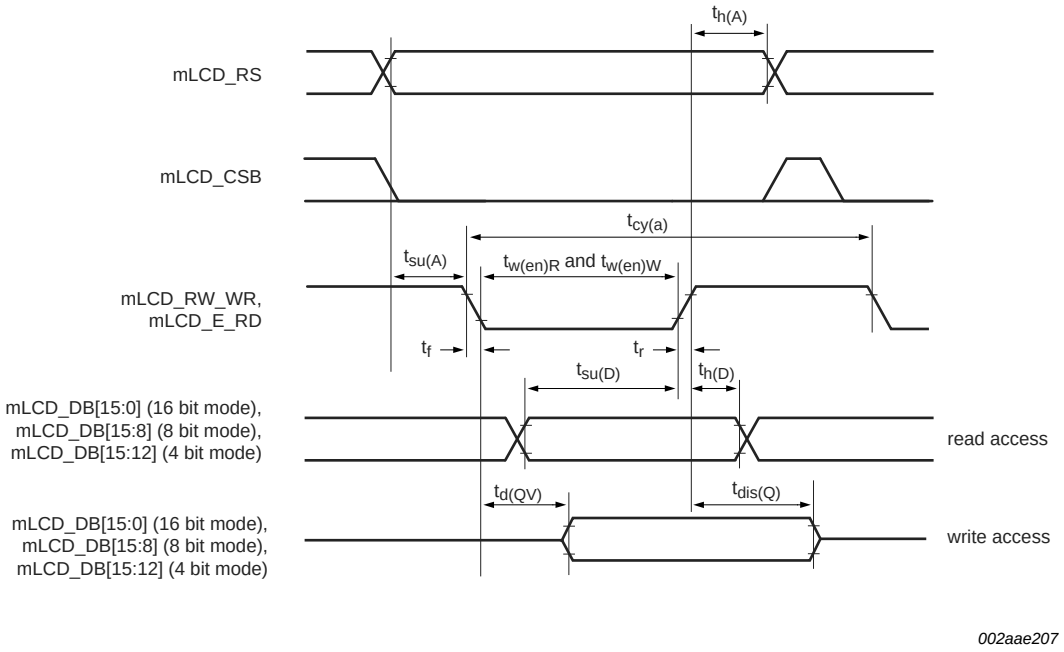


Fig 11. LCD timing (Intel 8080 mode)

[4] One HCLK cycle delay added when SYSCREG_MPMC_WAITREAD_DELAYx register bit 5 = 1.

[5] WAITRD must ≥ to WAITOEN for there to be any delay between $\overline{CS}$ active and $\overline{BLS}$ active. The maximum delay is limited to (WAITRD * HCLK).

[6] There is one less HCLK cycle when SYSCREG_MPMC_WAITREAD_DELAYx bit 5 = 1.

[7] The MPMC will ensure a minimum of one HCLK for this parameter.

[8] This formula applies when WAITWR is ≥ WAITWEN. One HCLK cycle minimum.

[9] This formula applies when WAITWR is ≥ WAITWEN.

[10] This formula applies when WAITWR is ≥ WAITWEN. Data valid minimum One HCLK cycle before $\overline{WE}$ goes active.

[11] This formula applies when WAITWR is ≥ WAITWEN. Three HCLK cycles minimum.

[12] Refer to the LPC3130/3131 *user manual* for the programming of WAITRD and HCLK.

[13] Refer to the LPC3130/3131 *user manual* for the programming of WAITWEN and HCLK.

[14] Refer to the LPC3130/3131 *user manual* for the programming of WAITWR and HCLK.

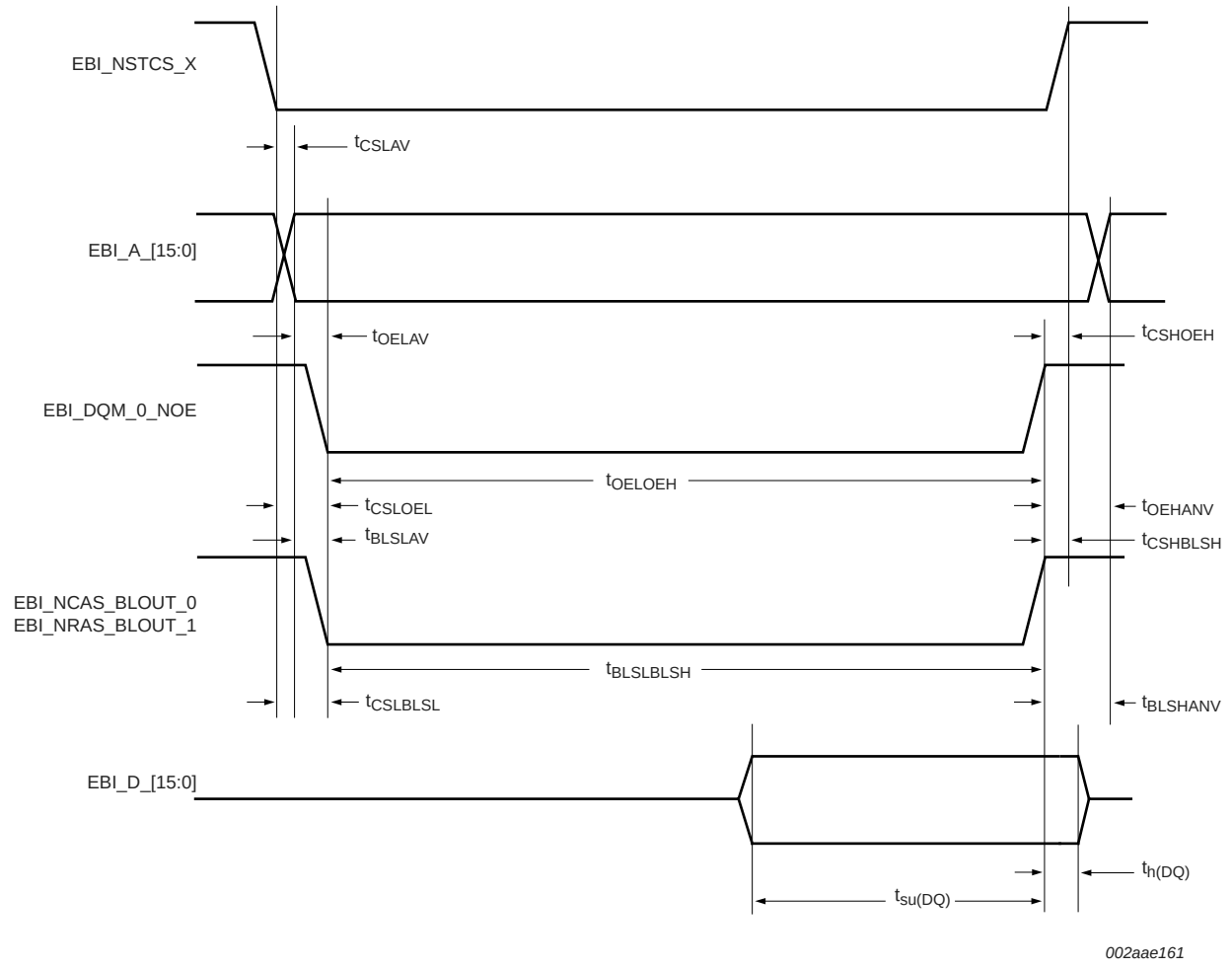
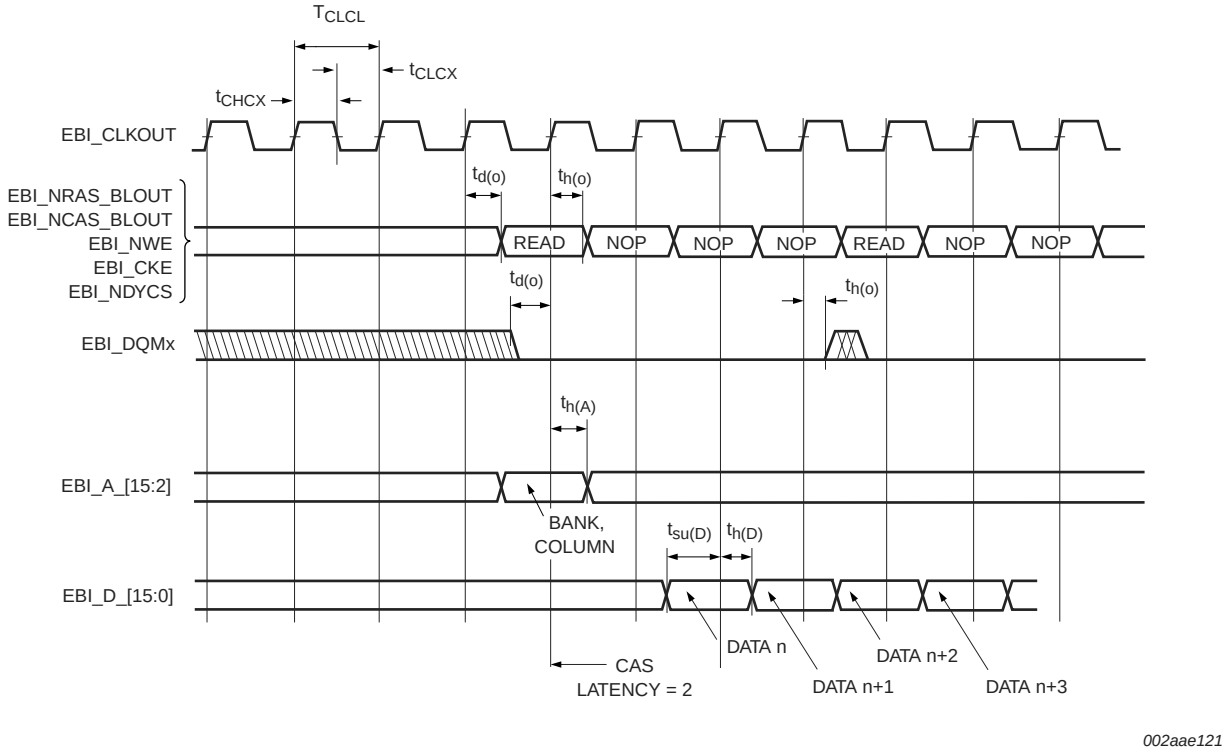


Fig 14. External memory read access to static memory



EBI_CKE is HIGH.

Fig 16. SDRAM burst read timing

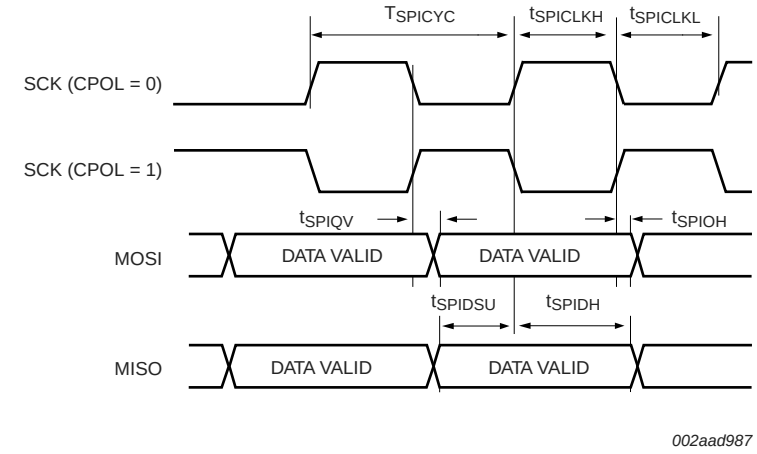


Fig 20. SPI master timing (CPHA = 0)

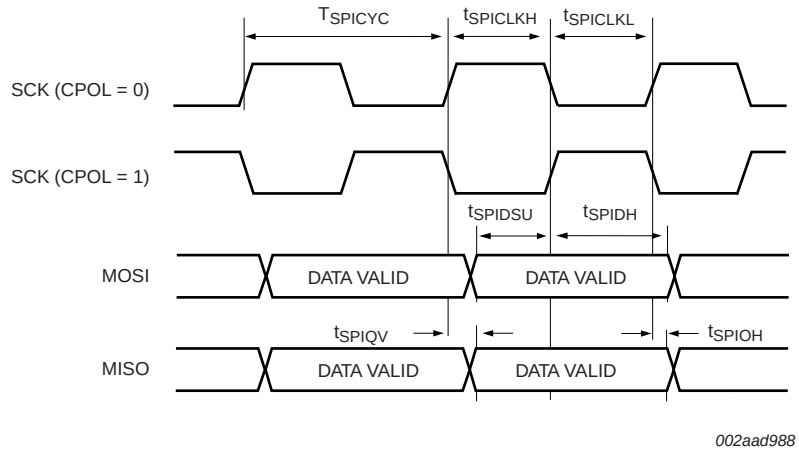


Fig 21. SPI slave timing (CPHA = 1)

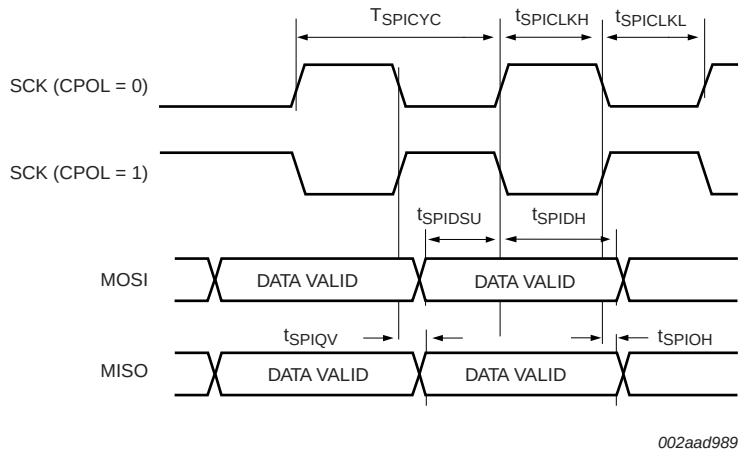


Fig 22. SPI slave timing (CPHA = 0)

9.6.1 Texas Instruments synchronous serial mode (SSI mode)

Table 23. Dynamic characteristic: SPI interface (SSI mode)
T_{amb} = −40 °C to +85 °C; $V_{DD(IO)}$ (SUP3) over specified ranges.[1]

Symbol	Parameter	Conditions	Min	Typ[2]	Max	Unit
$t_{su(SPI\_MISO)}$	SPI_MISO set-up time	T_{amb} = 25 °C; measured in SPI Master mode; see Figure 23	-	11	-	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

Remark: Note that the signal names SCK, MISO, and MOSI correspond to signals on pins SPI_SCK, SPI_MOSI, and SPI_MISO in the following SPI timing diagram.

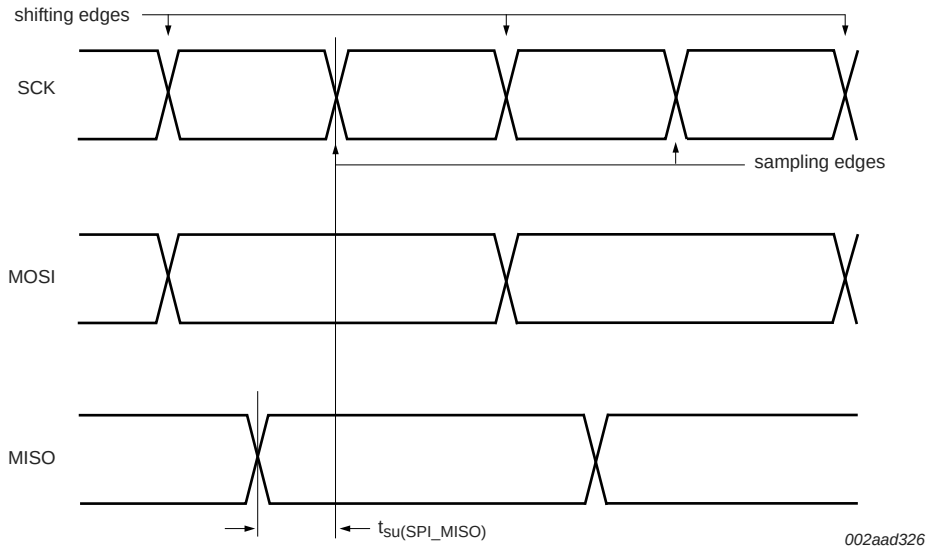


Fig 23. MISO line set-up time in SSI Master mode

9.7 10-bit ADC

Table 24: Dynamic characteristics: 10-bit ADC

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_s	sampling frequency	10 bit resolution	400	-	-	ksample/s
		2 bit resolution	-	-	1500	ksample/s
t_{conv}	conversion time	10 bit resolution	-	-	11	clock cycles
		2 bit resolution	3	-	-	clock cycles

11. Marking

Table 26. LPC3130/3131 Marking

Line	Marking	Description
A	LPC3130/3131	BASIC_TYPE

13. Abbreviations

Table 27. Abbreviations

Acronym	Description
A/D	Analog-to-Digital
ADC	Analog-to-Digital Converter
AHB	Advanced High-performance Bus
AMBA	Advanced Microcontroller Bus Architecture
APB	ARM Peripheral Bus
ATA	Advanced Transport Architecture
BIU	Bus Interface Unit
CE	Consumer Electronics
CGU	Clock Generation Unit
CRC	Cyclic Redundancy Check
DFU	Device Firmware Upgrade
DMA	Direct Memory Access
DRM	Digital Rights Management
DSP	Digital Signal Processing
EBI	External Bus Interface
ECC	Error Correction Code
EOP	End Of Packet
ESD	Electrostatic Discharge
FIFO	First In, First Out
FPGA	Field Programmable Gate Array
GF	Galois Field
INTC	Interrupt Controller
IOCONFIG	Input Output Configuration
IOM	ISDN Oriented Modular
IrDA	Infrared Data Association
IROM	Internal ROM
ISRAM	Internal Static RAM
ISROM	Internal Static ROM
JTAG	Joint Test Action Group
LSB	Least Significant Bit
MCI	Memory Card Interface
MCU	MicroController Unit
MMC	Multi-Media Card
MPMC	Multi-Port Memory Controller
OTG	On-The-Go
PCM	Pulse Code Modulation
PHY	Physical Layer
PLL	Phase Locked Loop
PWM	Pulse Width Modulation

15. Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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17. Contents

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