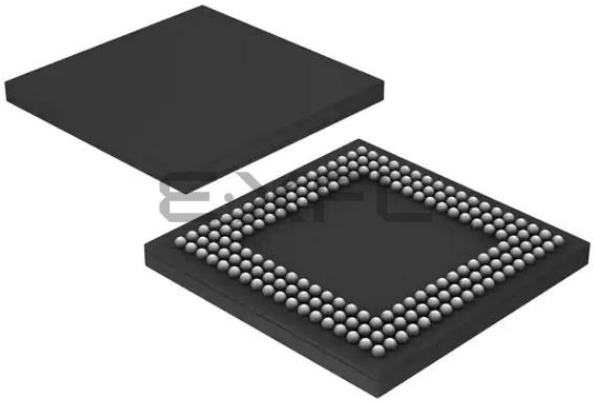

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	ARM926EJ-S
Core Size	16/32-Bit
Speed	180MHz
Connectivity	EBI/EMI, I²C, Memory Card, SPI, UART/USART, USB OTG
Peripherals	DMA, I²S, LCD, PWM, WDT
Number of I/O	-
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	192K x 8
Voltage - Supply (Vcc/Vdd)	1.1V ~ 3.6V
Data Converters	A/D 4x10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	180-TFBGA
Supplier Device Package	180-TFBGA (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc3131fet180-551

- Four 32-bit timers
- Watchdog timer
- PWM module
- Random Number Generator (RNG)
- General Purpose I/O (GPIO) pins
- Flexible and versatile interrupt structure
- JTAG interface with boundary scan and ARM debug access

- Operating voltage and temperature
  - Core voltage: 1.2 V
  - I/O voltage: 1.8 V, 3.3 V
  - Temperature: −40 °C to +85 °C
- TFBGA180 package: 12 × 12 mm^2, 0.8 mm pitch

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
LPC3130FET180	TFBGA180	plastic thin fine pitch ball grid array package, 180 balls, body 12 × 12 × 0.8 mm	SOT570-3
LPC3131FET180	TFBGA180	plastic thin fine pitch ball grid array package, 180 balls, body 12 × 12 × 0.8 mm	SOT570-3

Table 2. Ordering options for LPC3130/3131

Type number	Core/bus frequency	Total SRAM	High-speed USB	10-bit ADC channels	I^2S-bus/ I^2C-bus	MCI SDHC/ SDIO/ CE-ATA	Temperature range
LPC3130FET180	180 MHz/ 90 MHz	96 kB	Device/ Host/OTG	4	2 each	yes	−40 °C to +85 °C
LPC3131FET180	180 MHz/ 90 MHz	192 kB	Device/ Host/OTG	4	2 each	yes	−40 °C to +85 °C

Table 4. Pin description

Pin names with prefix m are multiplexed pins. See Table 10 for pin function selection of multiplexed pins.

Pin name	BGA ball	Digital I/O level [1]	Application function	Pin state after reset [2]	Cell type [3]	Description
Serial Peripheral Interface						
SPI_CS_OUT0 [4]	A7	SUP3	DO	O	DIO4	SPI Chip Select Output (Master)
SPI_SCK [4]	A8	SUP3	DIO	I	DIO4	SPI Clock Input (Slave) / Clock Output (Master)
SPI_MISO [4]	C8	SUP3	DIO	I	DIO4	SPI Data Input (Master) / Data Output (Slave)
SPI_MOSI [4]	B7	SUP3	DIO	I	DIO4	SPI Data Output (Master) / Data Input (Slave)
SPI_CS_IN [4]	B8	SUP3	DI	I	DIO4	SPI Chip Select Input (Slave)
Digital power supply						
VDDI	H3; L7; L12; C12; C6; A9; C9	SUP1	Supply	-	CS2	Digital Core Supply
VSSI	A11; C7; D12; G4; L6; L11		Ground	-	CG2	Digital Core Ground
Peripheral power supply						
VDDE_IOA	B2; E5; F5; G5; H5	SUP4	Supply	-	PS1	Peripheral supply for NAND flash interface
VDDE_IOB	L4; M5; M7; M9	SUP8	Supply	-	PS1	Peripheral supply for SDRAM/LCD
VDDE_IOC	C13; D5; D7; E8; G12; L10; K11	SUP3	Supply	-	PS1	Peripheral supply
VSSE_IOA	C3; C4; E4; F4; H4; K3		Ground	-	PG1	

Table 4. Pin description

Pin names with prefix m are multiplexed pins. See Table 10 for pin function selection of multiplexed pins.

Pin name	BGA ball	Digital I/O level [1]	Application function	Pin state after reset[2]	Cell type [3]	Description
VSSE_IOB	M3; M4; M6; M8		Ground	-	PG1	
VSSE_IOC	B12; D6; D8; D9; G11; L9; L13		Ground	-	PG1	
LCD Interface						
mLCD_CSB[4]	K8	SUP8	DO	O	DIO4	LCD Chip Select (active LOW)
mLCD_E_RD[4]	L8	SUP8	DO	O	DIO4	LCD, 6800 Enable, 8080 Read Enable (active HIGH)
mLCD_RS[4]	P8	SUP8	DO	O	DIO4	LCD, Instruction Register (LOW)/ Data Register (HIGH) select
mLCD_RW_WR[4]	N9	SUP8	DO	O	DIO4	LCD, 6800 Read/write Select, 8080 Write Enable (active HIGH)
mLCD_DB_0[4]	N8	SUP8	DIO	O	DIO4	LCD Data 0
mLCD_DB_1[4]	P9	SUP8	DIO	O	DIO4	LCD Data 1
mLCD_DB_2[4]	N6	SUP8	DIO	O	DIO4	LCD Data 2
mLCD_DB_3[4]	P6	SUP8	DIO	O	DIO4	LCD Data 3
mLCD_DB_4[4]	N7	SUP8	DIO	O	DIO4	LCD Data 4
mLCD_DB_5[4]	P7	SUP8	DIO	O	DIO4	LCD Data 5
mLCD_DB_6[4]	K6	SUP8	DIO	O	DIO4	LCD Data 6
mLCD_DB_7[4]	P5	SUP8	DIO	O	DIO4	LCD Data 7
mLCD_DB_8[4]	N5	SUP8	DIO	O	DIO4	LCD Data 8 / 8-bit Data 0
mLCD_DB_9[4]	L5	SUP8	DIO	O	DIO4	LCD Data 9 / 8-bit Data 1
mLCD_DB_10[4]	K7	SUP8	DIO	O	DIO4	LCD Data 10 / 8-bit Data 2
mLCD_DB_11[4]	N4	SUP8	DIO	O	DIO4	LCD Data 11 / 8-bit Data 3
mLCD_DB_12[4]	K5	SUP8	DIO	O	DIO4	LCD Data 12 / 8-bit Data 4 / 4-bit Data 0
mLCD_DB_13[4]	P4	SUP8	DIO	O	DIO4	LCD Data 13 / 8-bit Data 5 / 4-bit Data 1 / Serial Clock Output
mLCD_DB_14[4]	P3	SUP8	DIO	O	DIO4	LCD Data 14 / 8-bit Data 6 / 4-bit Data 2 / Serial Data Input
mLCD_DB_15[4]	N3	SUP8	DIO	O	DIO4	LCD Data 15 / 8-bit Data 7 / 4-bit Data 3 / Serial Data Output

Table 4. Pin description

Pin names with prefix m are multiplexed pins. See Table 10 for pin function selection of multiplexed pins.

Pin name	BGA ball	Digital I/O level [1]	Application function	Pin state after reset[2]	Cell type [3]	Description
External Bus Interface (NAND flash controller)						
EBI_A_0_ALE[4]	B3	SUP4	DO	O	DIO4	EBI Address Latch Enable
EBI_A_1_CLE[4]	A2	SUP4	DO	O	DIO4	EBI Command Latch Enable
EBI_D_0[4]	G2	SUP4	DIO	I	DIO4	EBI Data I/O 0
EBI_D_1[4]	F2	SUP4	DIO	I	DIO4	EBI Data I/O 1
EBI_D_2[4]	F1	SUP4	DIO	I	DIO4	EBI Data I/O 2
EBI_D_3[4]	E1	SUP4	DIO	I	DIO4	EBI Data I/O 3
EBI_D_4[4]	E2	SUP4	DIO	I	DIO4	EBI Data I/O 4
EBI_D_5[4]	D1	SUP4	DIO	I	DIO4	EBI Data I/O 5
EBI_D_6[4]	D2	SUP4	DIO	I	DIO4	EBI Data I/O 6
EBI_D_7[4]	C1	SUP4	DIO	I	DIO4	EBI Data I/O 7
EBI_D_8[4]	B1	SUP4	DIO	I	DIO4	EBI Data I/O 8
EBI_D_9[4]	A3	SUP4	DIO	I	DIO4	EBI Data I/O 9
EBI_D_10[4]	A1	SUP4	DIO	I	DIO4	EBI Data I/O 10
EBI_D_11[4]	C2	SUP4	DIO	I	DIO4	EBI Data I/O 11
EBI_D_12[4]	G3	SUP4	DIO	I	DIO4	EBI Data I/O 12
EBI_D_13[4]	D3	SUP4	DIO	I	DIO4	EBI Data I/O 13
EBI_D_14[4]	E3	SUP4	DIO	I	DIO4	EBI Data I/O 14
EBI_D_15[4]	F3	SUP4	DIO	I	DIO4	EBI Data I/O 15
EBI_DQM_0_NOE[4]	H1	SUP4	DO	O	DIO4	NAND Read Enable (active LOW)
EBI_NWE[4]	J2	SUP4	DO	O	DIO4	NAND Write Enable (active LOW)
NAND_NCS_0[4]	J1	SUP4	DO	O	DIO4	NAND Chip Enable 0
NAND_NCS_1[4]	J3	SUP4	DO	O	DIO4	NAND Chip Enable 1
NAND_NCS_2[4]	K1	SUP4	DO	O	DIO4	NAND Chip Enable 2
NAND_NCS_3[4]	K2	SUP4	DO	O	DIO4	NAND Chip Enable 3
mNAND_RYBN0[4]	E6	SUP4	DI	I	DIO4	NAND Ready/Busy 0
mNAND_RYBN1[4]	E7	SUP4	DI	I	DIO4	NAND Ready/Busy 1
mNAND_RYBN2[4]	B4	SUP4	DI	I	DIO4	NAND Ready/Busy 2
mNAND_RYBN3[4]	D4	SUP4	DI	I	DIO4	NAND Ready/Busy 3
EBI_NCAS_BLOUT_0[4]	G1	SUP4	DO	O	DIO4	EBI Lower lane byte select (7:0)
EBI_NRAS_BLOUT_1[4]	H2	SUP4	DO	O	DIO4	EBI Upper lane byte select (15:8)
Pulse Width Modulation module						
PWM_DATA[4]	B9	SUP3	DO / GPIO	O	DIO1	PWM Output

[1] Digital I/O levels are explained in Table 5.

[2] I = input; I:PU = input with internal weak pull-up; I:PD = input with internal weak pull-down; O = output.

[3] Cell types are explained in Table 6.

[4] Pin can be configured as GPIO pin in the IOCONFIG block.

6. Functional description

6.1 ARM926EJ-S

The processor embedded in the LPC3130/3131 is the ARM926EJ-S. It is a member of the ARM9 family of general-purpose microprocessors. The ARM926EJ-S is intended for multi-tasking applications where full memory management, high performance, and low power are important.

This module has the following features:

- ARM926EJ-S processor core which uses a five-stage pipeline consisting of fetch, decode, execute, memory, and write stages. The processor supports both the 32-bit ARM and 16-bit Thumb instruction sets, which allows a trade off between high performance and high code density. The ARM926EJ-S also executes an extended ARMv5TE instruction set which includes support for Java byte code execution.
- Contains an AMBA BIU for both data accesses and instruction fetches.
- Memory Management Unit (MMU).
- 16 kB instruction and 16 kB data separate cache memories with an 8 word line length. The caches are organized using Harvard architecture.
- Little Endian is supported.
- The ARM926EJ-S processor supports the ARM debug architecture and includes logic to assist in both hardware and software debugging.
- Supports dynamic clock gating for power reduction.
- The processor core clock can be set equal to the AHB bus clock or to an integer number times the AHB bus clock. The processor can be switched dynamically between these settings.
- ARM stall support.

Table 8. LPC3130/3131 boot modes

Boot mode	GPIO0	GPIO1	GPIO2	Description
NAND	0	0	0	Boots from NAND flash. If proper image is not found, boot ROM will switch to DFU boot mode.
SPI	0	0	1	Boot from SPI NOR flash connected to SPI_CS_OUT0. If proper image is not found, boot ROM will switch to DFU boot mode.
DFU	0	1	0	Device boots via USB using DFU class specification.
SD/MMC	0	1	1	Boot ROM searches all the partitions on the SD/MMC/SDHC/MMC+/eMMC/eSD card for boot image. If partition table is missing, it will start searching from sector 0. A valid image is said to be found if a valid image header is found, followed by a valid image. If a proper image is not found, boot ROM will switch to DFU boot mode.
Reserved 0	1	0	0	Reserved for testing.
NOR flash	1	0	1	Boot from parallel NOR flash connected to EBI_NSTCS_1.
UART	1	1	0	Boot ROM tries to download boot image from UART ((115200 – 8 – n -1) assuming 12 MHz FFAST clock).
Test	1	1	1	Boot ROM is testing ISRAM using memory pattern test. After test switches to UART boot mode.

6.8 Internal RAM memory

The ISRAM (Internal Static RAM Memory) controller module is used as controller between the AHB bus and the internal RAM memory. The internal RAM memory can be used as working memory for the ARM processor and as temporary storage to execute the code that is loaded by boot ROM from external devices such as SPI-flash, NAND flash, and SD/MMC cards.

This module has the following features:

- Capacity of 96 kB (LPC3130) or 192 kB (LPC3131)
- On LPC3131 implemented as two independent 96 kB memory banks

6.9 Memory Card Interface (MCI)

The MCI controller interface can be used to access memory cards according to the Secure Digital (SD) and Multi-Media Card (MMC) standards. The host controller can be used to interface to small form factor expansion cards compliant to the SDIO card standard as well. Finally, the MCI supports CE-ATA 1.1 compliant hard disk drives.

This module has the following features:

- One 8-bit wide interface.
- Supports high-speed SD, versions 1.01, 1.10 and 2.0.
- Supports SDIO version 1.10.
- Supports MMCplus, MMCmobile and MMCmicro cards based on MMC 4.1.
- Supports SDHC memory cards.
- CRC generation and checking.

- Supports 1/4-bit SD cards.
- Card detection and write protection.
- FIFO buffers of 16 bytes deep.
- Host pull-up control.
- SDIO suspend and resume.
- 1 to 65 535 bytes blocks.
- Suspend and resume operations.
- SDIO Read-wait.
- Maximum clock speed of 52 MHz (MMC 4.1).
- Supports CE-ATA 1.1.
- Supports 1-bit, 4-bit, and 8-bit MMC cards and CE-ATA devices.

6.10 High-speed Universal Serial Bus 2.0 On-The-Go (OTG)

The USB OTG module allows the LPC3130/3131 to connect directly to a USB host such as a PC (in device mode) or to a USB device in host mode. In addition, the LPC3130/3131 has a special, built-in mode in which it enumerates as a Device Firmware Upgrade (DFU) class, which allows for a (factory) download of the device firmware through USB.

This module has the following features:

- Complies with *Universal Serial Bus specification 2.0*.
- Complies with *USB On-The-Go supplement*.
- Complies with *Enhanced Host Controller Interface Specification*.
- Supports auto USB 2.0 mode discovery.
- Supports all high-speed USB-compliant peripherals.
- Supports all full-speed USB-compliant peripherals.
- Supports software Host Negotiation Protocol (HNP) and Session Request Protocol (SRP) for OTG peripherals.
- Contains UTMI+ compliant transceiver (PHY).
- Supports interrupts.
- This module has its own, integrated DMA engine.

USB-IF TestID for Hi-speed peripheral silicon: 40700062

USB-IF TestID for Hi-speed embedded host silicon: 120000182

6.11 DMA controller

The DMA Controller can perform DMA transfers on the AHB bus without using the CPU.

This module has the following features:

- Supported transfer types:

  Memory to memory:

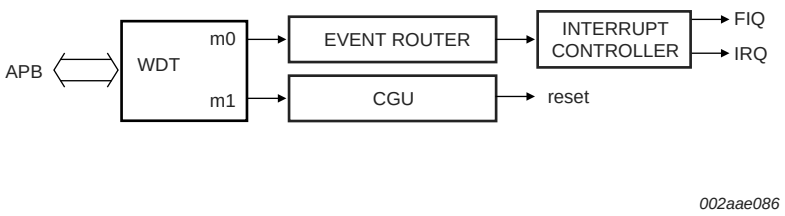


Fig 7. Block diagram of the Watchdog timer

6.17 Input/Output configuration module (IOCONFIG)

The General Purpose Input/Output (GPIO) pins can be controlled through the register interface provided in the IOCONFIG module. Next to several dedicated GPIO pins, most digital I/O pins can also be used as GPIO if they are not required for their normal, dedicated function.

This module has the following features:

- Provides control for the digital pins that can double as GPIO (next to their normal function). The pinning list in Table 4 indicates which pins can double as GPIO.
- Each pin controlled by the IOCONFIG can be configured for four operational modes:
  - Normal operation (i.e. controlled by a function block).
  - Driven LOW.
  - Driven HIGH.
  - High impedance/input.
- The GPIO pins can be observed (read) in any mode.
- The register interface provides set and clear access methods for choosing the operational mode.

6.18 10-bit Analog-to-Digital Converter (ADC10B)

This module is a 10-bit successive approximation Analog-to-Digital Converter (ADC) with an input multiplexer to allow for multiple analog signals on its input. A common use of this module is to read out multiple keys on one input from a resistor network.

This module has the following features:

- Four analog input channels, selected by an analog multiplexer.
- Programmable ADC resolution from 2 bit to 10 bit.
- The maximum conversion rate is 400 ksample/s for 10 bit resolution and 1500 ksample/s for 2 bit resolution.
- Single A/D conversion scan mode and continuous A/D conversion scan mode.
- Power-down mode.

6.26.1 Pin connections

Table 10. Pin descriptions of multiplexed pins

Pin Name	Default Signal	Alternate Signal	Description
Video related pin multiplexing			
mLCD_CSB	LCD_CSB	EBI_NSTCS_0	**LCD_CSB —** LCD chip select for external LCD controller. **EBI_NSTCS_0 —** EBI static memory chip select 0.
mLCD_DB_1	LCD_DB_1	EBI_NSTCS_1	**LCD_DB_1 —** LCD bidirectional data line 1. **EBI_NSTCS_1 —** EBI static memory chip select 1.
mLCD_DB_0	LCD_DB_0	EBI_CLKOUT	**LCD_DB_0 —** LCD bidirectional data line 0. **EBI_CLKOUT —** EBI SDRAM clock signal.
mLCD_E_RD	LCD_E_RD	EBI_CKE	**LCD_E_RD —** LCD enable/read signal. **EBI_CKE —** EBI SDRAM clock enable.
mLCD_RS	LCD_RS	EBI_NDYCS	**LCD_RS —** LCD register select signal. **EBI_NDYCS —** EBI SDRAM chip select.
mLCD_RW_WR	LCD_RW_WR	EBI_DQM_1	**LCD_RW_WR —** LCD read write/write signal. **EBI_DQM_1 —** EBI SDRAM data mask output 1.
mLCD_DB_2	LCD_DB_2	EBI_A_2	**LCD_DB_2 —** LCD bidirectional data line 2. **EBI_A_2 —** EBI address line 2.
mLCD_DB_3	LCD_DB_3	EBI_A_3	**LCD_DB_3 —** LCD bidirectional data line 3. **EBI_A_3 —** EBI address line 3.
mLCD_DB_4	LCD_DB_4	EBI_A_4	**LCD_DB_4 —** LCD bidirectional data line 4. **EBI_A_4 —** EBI address line 4.
mLCD_DB_5	LCD_DB_5	EBI_A_5	**LCD_DB_5 —** LCD bidirectional data line 5. **EBI_A_5 —** EBI address line 5.
mLCD_DB_6	LCD_DB_6	EBI_A_6	**LCD_DB_6 —** LCD bidirectional data line 6. **EBI_A_6 —** EBI address line 6.
mLCD_DB_7	LCD_DB_7	EBI_A_7	**LCD_DB_7 —** LCD bidirectional data line 7. **EBI_A_7 —** EBI address line 7.
mLCD_DB_8	LCD_DB_8	EBI_A_8	**LCD_DB_8 —** LCD bidirectional data line 8. **EBI_A_8 —** EBI address line 8.
mLCD_DB_9	LCD_DB_9	EBI_A_9	**LCD_DB_9 —** LCD bidirectional data line 9. **EBI_A_9 —** EBI address line 9.
mLCD_DB_10	LCD_DB_10	EBI_A_10	**LCD_DB_10 —** LCD bidirectional data line 10. **EBI_A_10 —** EBI address line 10.
mLCD_DB_11	LCD_DB_11	EBI_A_11	**LCD_DB_11 —** LCD bidirectional data line 11. **EBI_A_11 —** EBI address line 11.
mLCD_DB_12	LCD_DB_12	EBI_A_12	**LCD_DB_12 —** LCD bidirectional data line 12. **EBI_A_12 —** EBI address line 12.
mLCD_DB_13	LCD_DB_13	EBI_A_13	**LCD_DB_13 —** LCD bidirectional data line 13. **EBI_A_13 —** EBI address line 13.
mLCD_DB_14	LCD_DB_14	EBI_A_14	**LCD_DB_14 —** LCD bidirectional data line 14. **EBI_A_14 —** EBI address line 14.

Table 10. Pin descriptions of multiplexed pins *…continued*

Pin Name	Default Signal	Alternate Signal	Description
mLCD_DB_15	LCD_DB_15	EBI_A_15	**LCD_DB_15 —** LCD bidirectional data line 15. **EBI_A_15 —** EBI address line 15.
Storage related pin multiplexing			
mGPIO5	GPIO5	MCI_CLK	**GPIO5 —** General Purpose I/O pin 5. **MCI_CLK —** MCI card clock.
mGPIO6	GPIO6	MCI_CMD	**GPIO_6 —** General Purpose I/O pin 6. **MCI_CMD —** MCI card command input/output.
mGPIO7	GPIO7	MCI_DAT_0	**GPIO7 —** General Purpose I/O pin 7. **MCI_DAT_0 —** MCI card data input/output line 0.
mGPIO8	GPIO8	MCI_DAT_1	**GPIO8 —** General Purpose I/O pin 8. **MCI_DAT_1 —** MCI card data input/output line 1.
mGPIO9	GPIO9	MCI_DAT_2	**GPIO9 —** General Purpose I/O pin 9. **MCI_DAT_2 —** MCI card data input/output line 2.
mGPIO10	GPIO10	MCI_DAT_3	**GPIO10 —** General Purpose I/O pin 10. **MCI_DAT_3 —** MCI card data input/output line 3.
NAND related pin multiplexing			
mNAND_RYBN0	NAND_RYBN0	MCI_DAT_4	**NAND_RYBN0 —** NAND flash controller Read/Not busy signal 0. **MCI_DAT_4 —** MCI card data input/output line 4.
mNAND_RYBN1	NAND_RYBN1	MCI_DAT_5	**NAND_RYBN1 —** NAND flash controller Read/Not busy signal 1. **MCI_DAT_5 —** MCI card data input/output line 5.
mNAND_RYBN2	NAND_RYBN2	MCI_DAT_6	**NAND_RYBN2 —** NAND flash controller Read/Not busy signal 2. **MCI_DAT_6 —** MCI card data input/output line 6.
mNAND_RYBN3	NAND_RYBN3	MCI_DAT7	**NAND_RYBN3 —** NAND flash controller Read/Not busy signal 3. **MCI_DAT7 —** MCI card data input/output line 7.
Audio related pin multiplexing			
mI2STX_DATA0	I2STX_DATA0	PCM_DA	**I2STX_DATA0 —** I^2S-bus interface 0 transmit data signal. **PCM_DA —** PCM serial data line A.
mI2STX_BCK0	I2STX_BCK0	PCM_FSC	**I2STX_BCK0 —** I^2S-bus interface 0 transmit bitclock signal. **PCM_FSC —** PCM frame synchronization signal.
mI2STX_WS0	I2STX_WS0	PCM_DCLK	**I2STX_WS0 —** I^2S-bus interface 0 transmit word select signal. **PCM_DCLK —** PCM data clock output.
mI2STX_CLK0	I2STX_CLK0	PCM_DB	**I2STX_CLK0 —** I^2S-bus interface 0 transmit clock signal. **PCM_DB —** PCM serial data line B.
UART related pin multiplexing			
mUART_CTS_N	UART_CTS_N	SPI_CS_OUT1	**UART_CTS_N —** UART modem control Clear-to-send signal. **SPI_CS_OUT1 —** SPI chip select out for slave 1 (used in master mode).
mUART_RTS_N	UART_RTS_N	SPI_CS_OUT2	**UART_RTS_N —** UART modem control Request-to-Send signal. **SPI_CS_OUT2 —** SPI chip select out for slave 2 (used in master mode).

6.29 System control registers

The System Control Registers (SysCReg) module provides a register interface for some of the high-level settings in the system such as multiplexers and mode settings. This is an auxiliary module included in this overview for the sake of completeness.

6.30 I2S0/1 interfaces

The I2S0/1 receive and I2S0/1 transmit modules have the following features:

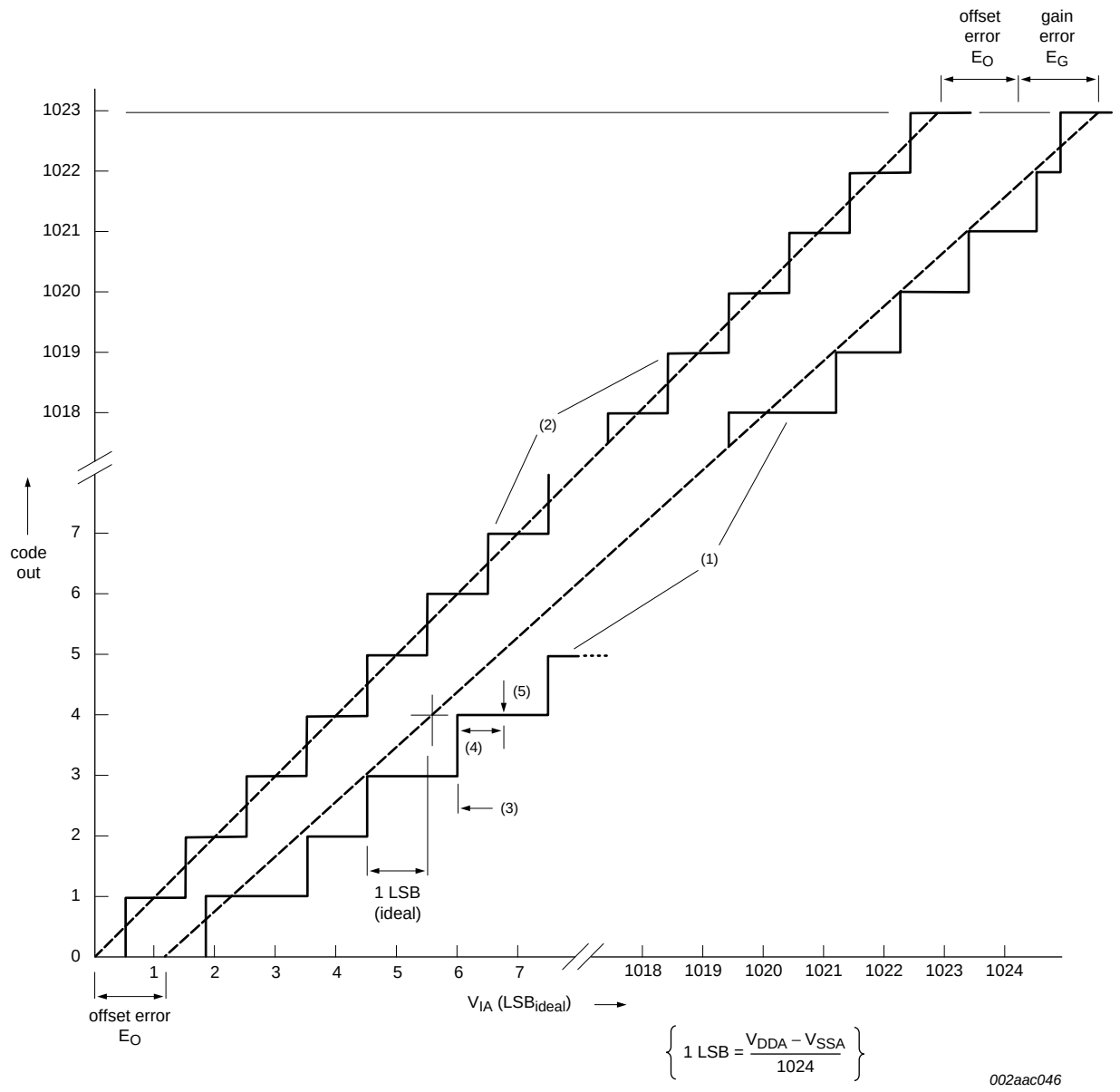
- Audio interface compatible with the I^2S standard.
- I2S0/1 receive supports master mode and slave mode.
- I2S0/1 transmit supports master mode.
- Supports LSB justified words of 16, 18, 20 and 24 bits.
- Supports a configurable number of bit clock periods per Word Select period (up to 128 bit clock periods).
- Supports DMA transfers.
- Transmit FIFO (I^2S transmit) or receive FIFO (I^2S receive) of 4 stereo samples.
- Supports single 16 bit transfers to/from the left or right FIFO.
- Supports single 24 bit transfers to/from the left or right FIFO.
- Supports 32-bit interleaved transfers, with the lower 16 bits representing the left audio sample, and the higher 16 bits representing the right audio sample.
- Supports two 16-bit audio samples combined in a 32-bit word (2 left or 2 right samples) to reduce bus load.
- Provides maskable interrupts for audio status: FIFO underrun/overrun/full/ half_full/not empty for left and right channel separately.

8. Static characteristics

Table 12: Static characteristics

T_{amb} = −40 °C to +85 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply pins						
$V_{DD(IO)}$	input/output supply voltage	NAND flash controller pads (SUP4) and LCD interface (SUP8); 1.8 V mode	1.65	1.8	1.95	V
		NAND flash controller pads (SUP4) and LCD interface (SUP8); 3.3 V mode	2.5	3.3	3.6	V
		other peripherals (SUP 3)	2.7	3.3	3.6	V
$V_{DD(CORE)}$	core supply voltage	(SUP1)	1.1	1.2	1.3	V
$V_{DD(OSC\_PLL)}$	oscillator and PLL supply voltage	on pin VDDA12; for 12 MHz oscillator (SUP1)	1.0	1.2	1.3	V
$V_{DD(ADC)}$	ADC supply voltage	on pin ADC10B_VDDA33; for 10-bit ADC (SUP 3)	2.7	3.3	3.6	V
V_{BUS}	bus supply voltage	on pin USB_VBUS (SUP5)	-	5.0	-	V
$V_{DDA(USB)(3V3)}$	USB analog supply voltage (3.3 V)	on pin USB_VDDA33 (SUP 3)	3.0	3.3	3.6	V
		on pin USB_VDDA33_DRV (SUP 3); driver	2.7	3.3	3.6	V
$V_{DDA(PLL)(1V2)}$	PLL analog supply voltage (1.2 V)	on pin USB_VDDA12_PLL (SUP1)	1.1	1.2	1.3	V
Input pins and I/O pins configured as input						
V_I	input voltage		0	-	VDDE_IOC	V
V_{IH}	HIGH-level input voltage	SUP3; SUP4; SUP8	0.7VDDE_IOx (x = A, B, C)	-	-	V
V_{IL}	LOW-level input voltage	SUP3; SUP4; SUP8	-	-	0.3VDDE_IOx (x = A, B, C)	V
V_{hys}	hysteresis voltage	SUP4; SUP8				V
		1.8 V mode	400	-	600	mV
		3.3 V mode	550	-	850	mV
		SUP3	0.1VDDE_IOC	-	-	V
I_{IL}	LOW-level input current	V_I = 0 V; no pull-up	-	-	2.1	μA
I_{IH}	HIGH-level input current	$V_I = V_{DD(IO)}$; no pull-down	-	-	3.9	μA
I_{latch}	I/O latch-up current	$-(1.5V_{DD(IO)}) < V_I < (1.5V_{DD(IO)})$ [1]	-	-	100	mA



(1) Example of an actual transfer curve.

(2) The ideal transfer curve.

(3) Differential linearity error (E_D).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

Fig 10. ADC characteristics

[4] One HCLK cycle delay added when SYSCREG_MPMC_WAITREAD_DELAYx register bit 5 = 1.

[5] WAITRD must ≥ to WAITOEN for there to be any delay between $\overline{CS}$ active and $\overline{BLS}$ active. The maximum delay is limited to (WAITRD * HCLK).

[6] There is one less HCLK cycle when SYSCREG_MPMC_WAITREAD_DELAYx bit 5 = 1.

[7] The MPMC will ensure a minimum of one HCLK for this parameter.

[8] This formula applies when WAITWR is ≥ WAITWEN. One HCLK cycle minimum.

[9] This formula applies when WAITWR is ≥ WAITWEN.

[10] This formula applies when WAITWR is ≥ WAITWEN. Data valid minimum One HCLK cycle before $\overline{WE}$ goes active.

[11] This formula applies when WAITWR is ≥ WAITWEN. Three HCLK cycles minimum.

[12] Refer to the LPC3130/3131 *user manual* for the programming of WAITRD and HCLK.

[13] Refer to the LPC3130/3131 *user manual* for the programming of WAITWEN and HCLK.

[14] Refer to the LPC3130/3131 *user manual* for the programming of WAITWR and HCLK.

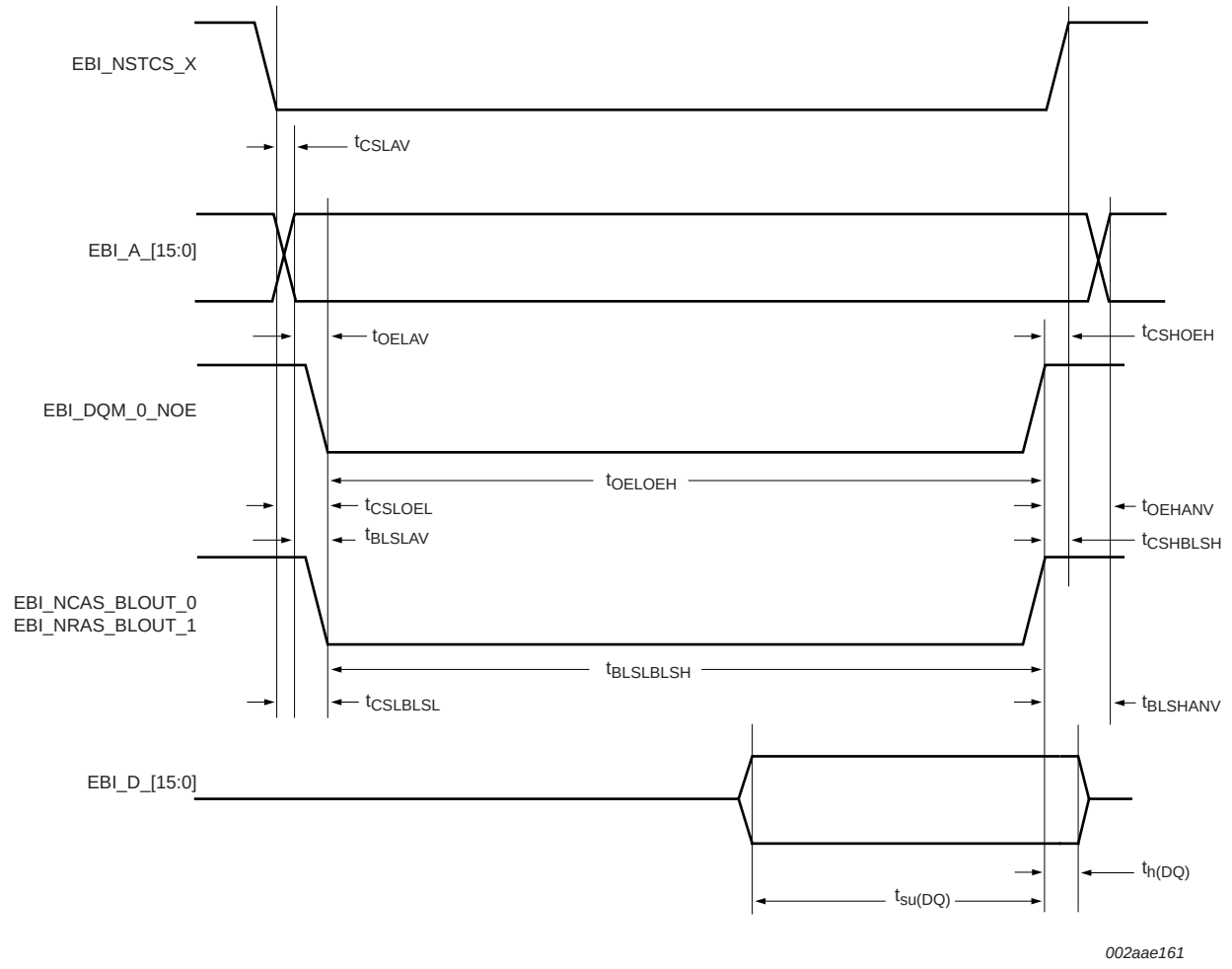


Fig 14. External memory read access to static memory

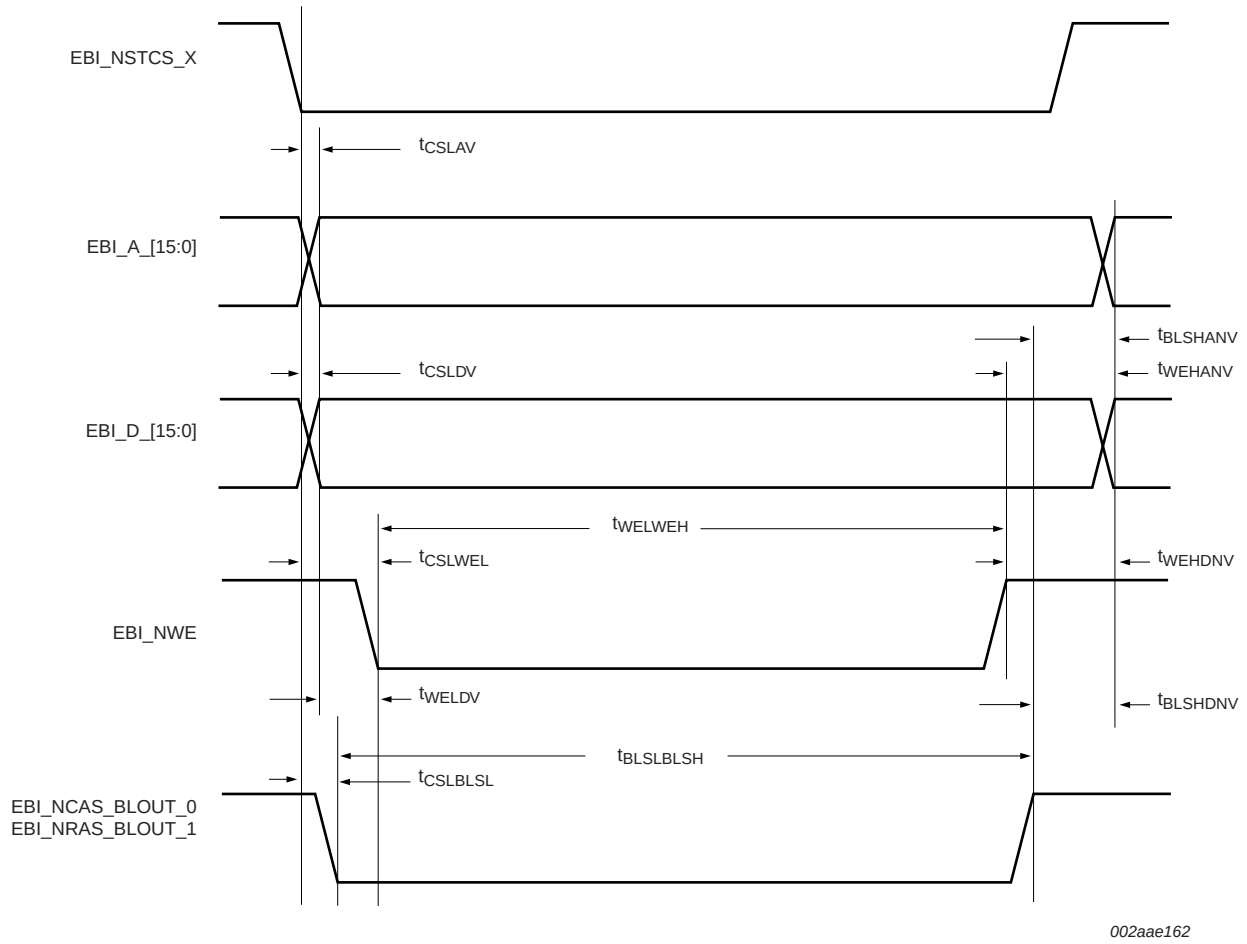


Fig 15. External memory write access to static memory

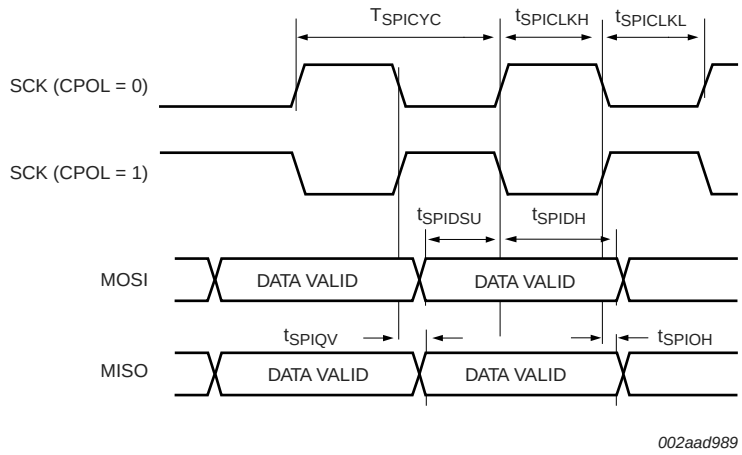


Fig 22. SPI slave timing (CPHA = 0)

10. Application information

Table 25. LCD panel connections

TFBGA pin #	Pin name	Reset function (default)	LCD mode					
			Parallel					Serial
			LCD panel data mapping			Control function		
			16 bit	8 bit	4 bit	6800	8080	
K8	mLCD_CSB/EBI_NSTCS_0	LCD_CSB	-	-	-	LCD_CSB	LCD_CSB	LCD_CSB
L8	mLCD_E_RD/EBI_CKE	LCD_E_RD	-	-	-	LCD_E	LCD_RD	-
P8	mLCD_RS/EBI_NDYCS	LCD_RS	-	-	-	LCD_RS	LCD_RS	LCD_RS
N9	mLCD_RW_WR/EBI_DQM_1	LCD_RW_WR	-	-	-	LCD_RW	LCD_WR	-
N8	mLCD_DB_0/EBI_CLKOUT	LCD_DB_0	LCD_DB_0	-	-	-	-	-
P9	mLCD_DB_1/EBI_NSTCS_1	LCD_DB_1	LCD_DB_1	-	-	-	-	-
N6	mLCD_DB_2/EBI_A_2	LCD_DB_2	LCD_DB_2	-	-	-	-	-
P6	mLCD_DB_3/EBI_A_3	LCD_DB_3	LCD_DB_3	-	-	-	-	-
N7	mLCD_DB_4/EBI_A_4	LCD_DB_4	LCD_DB_4	-	-	-	-	-
P7	mLCD_DB_5/EBI_A_5	LCD_DB_5	LCD_DB_5	-	-	-	-	-
K6	mLCD_DB_6/EBI_A_6	LCD_DB_6	LCD_DB_6	-	-	-	-	-
P5	mLCD_DB_7/EBI_A_7	LCD_DB_7	LCD_DB_7	-	-	-	-	-
N5	mLCD_DB_8/EBI_A_8	LCD_DB_8	LCD_DB_8	LCD_DB_0	-	-	-	-
L5	mLCD_DB_9/EBI_A_9	LCD_DB_9	LCD_DB_9	LCD_DB_1	-	-	-	-
K7	mLCD_DB_10/EBI_A_10	LCD_DB_10	LCD_DB_10	LCD_DB_2	-	-	-	-
N4	mLCD_DB_11/EBI_A_11	LCD_DB_11	LCD_DB_11	LCD_DB_3	-	-	-	-
K5	mLCD_DB_12/EBI_A_12	LCD_DB_12	LCD_DB_12	LCD_DB_4	LCD_DB_0	-	-	-
P4	mLCD_DB_13/EBI_A_13	LCD_DB_13	LCD_DB_13	LCD_DB_5	LCD_DB_1	-	-	SER_CLK
P3	mLCD_DB_14/EBI_A_14	LCD_DB_14	LCD_DB_14	LCD_DB_6	LCD_DB_2	-	-	SER_DAT_IN
N3	mLCD_DB_15/EBI_A_15	LCD_DB_15	LCD_DB_15	LCD_DB_7	LCD_DB_3	-	-	SER_DAT_OUT

Table 27. Abbreviations *…continued*

Acronym	Description
RNG	Random Number Generator
ROM	Read-Only Memory
SD	Secure Digital
SDHC	Secure Digital High Capacity
SDIO	Secure Digital Input Output
SDR	Single Data Rate
SE0	Single Ended Zero
SIR	Serial IrDA
SPI	Serial Peripheral Interface
SSI	Serial Synchronous Interface
SysCReg	System Control Registers
TAP	Test Access Port
TDO	Test Data Out
UART	Universal Asynchronous Receiver Transmitter
USB	Universal Serial Bus
UTMI	USB 2.0 Transceiver Macrocell Interface
WDT	WatchDog Timer

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